

# 8-Bit Buffers with Schmitt Trigger Inputs

SN54/74LS310 SN54/74S310  
 SN54/74LS340 SN54/74S340  
 SN54/74LS341 SN54/74S341  
 SN54/74LS344 SN54/74S344

## Features

- Schmitt-trigger inputs guarantee high noise margin
- Three-state outputs drive bus lines
- Typical input and output capacitance  $\leq 10$  pf
- Low-current PNP inputs reduce loading
- 20-pin SKINNYDIP® saves space
- 8-bit data path matches byte boundaries
- Ideal for microprocessor interface
- Complementary-enable '310 and '341 types combine multiplexer and driver functions
- Pin-compatible with SN54/74S210/240/1/4 and SN54/74LS210/240/1/4; can be direct replacement in systems with noise problems

## Description

In addition to the standard Schottky and low-power Schottky 8-bit buffers, Monolithic Memories provides full hysteresis with a "true" Schmitt-trigger circuit. The improved performance characteristics are designed (1) for the low-power Schottky buffers, to be consistent with the SN54/74LS14 hex Schmitt-trigger inverter, and to guarantee a full 400 mV noise immunity; (2) for the Schottky buffers, to have low propagation delays, and to guarantee a full 500 mV noise immunity. The Schmitt-trigger operation makes these L/S buffers ideal for bus receivers in a noisy environment.

These 8-bit buffers provide high-speed and high-current interface capability for bus-organized digital systems. The three-state drivers will source a termination to ground (up to 133Ω) or sink a pull-up to  $V_{CC}$  as in the popular 220Ω/330Ω computer

## Ordering Information

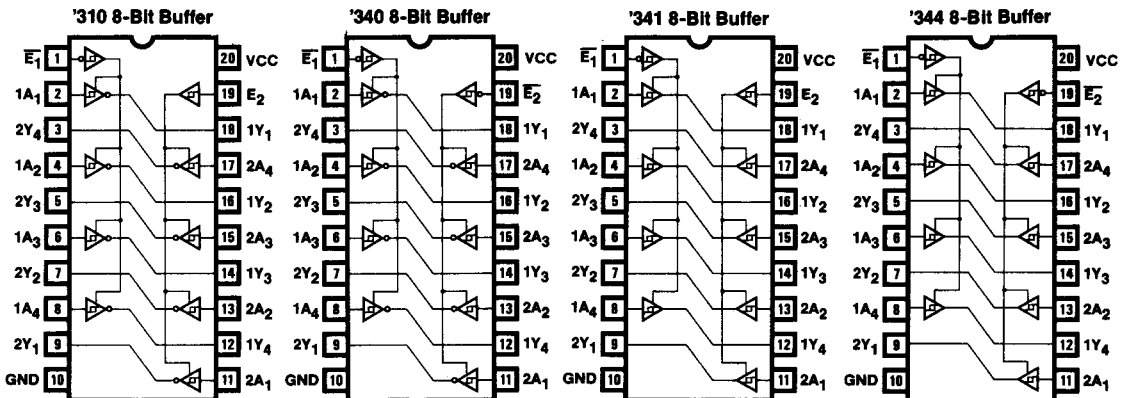
PART NUMBER	PKG*	TEMP	ENABLE	POLARITY	POWER
SN54LS310	J,F	mil	High-Low	Invert	LS
SN74LS310	N,J	com	Low		
SN54LS340	J,F	mil	High-Low		
SN74LS340	N,J	com	Low		
SN54LS341	J,F	mil	High-Low	Non-Invert	S
SN74LS341	N,J	com	Low		
SN54LS344	J,F	mil	High-Low	Non-Invert	S
SN74LS344	N,J	com	Low		
SN54S310	J,F	mil	High-Low		
SN74S310	N,J	com	Low		
SN54S340	J,F	mil	High-Low	Non-Invert	S
SN74S340	N,J	com	Low		
SN54S341	J,F	mil	High-Low	Non-Invert	S
SN74S341	N,J	com	Low		
SN54S344	J,F	mil	High-Low		
SN74S344	N,J	com	Low		

peripheral termination. The PNP inputs provide improved fan-in with 0.25 mA  $I_{IL}$  for the low-power Schottky buffers and 0.25 mA  $I_{IL}$  for the Schottky buffers.

The '340 and '344 provide inverting and non-inverting outputs respectively, with assertive-low enables. The '310 and '341 also provide inverting and non-inverting outputs respectively, but with complementary (both assertive-low and assertive-high) enables, to allow transceiver or multiplexer operation.

All of the 8-bit devices are packaged in the popular 20-pin SKINNYDIP®.

## Logic Symbols



\*For other package types, please contact your local sales representative.

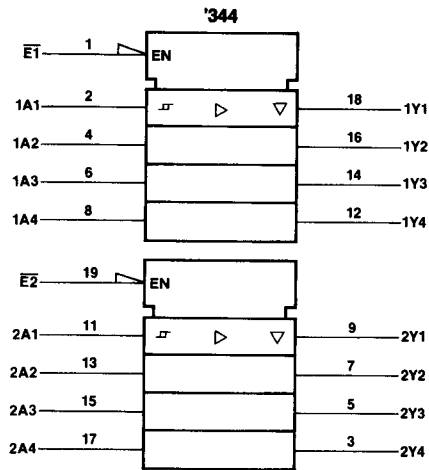
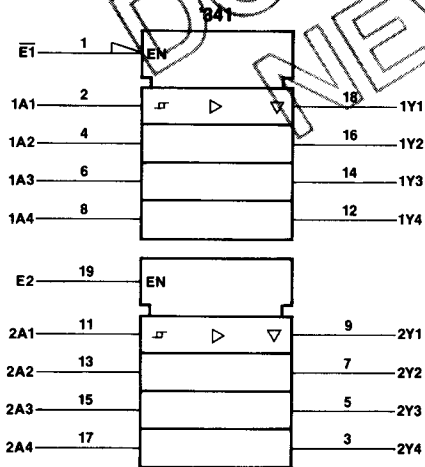
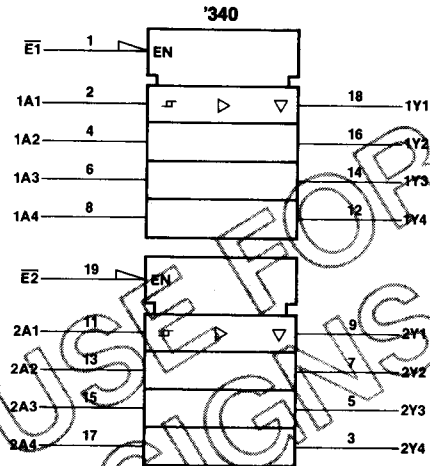
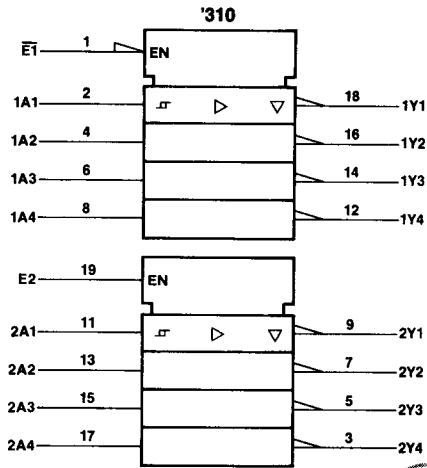
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2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374

TWX: 910-338-2376

**Monolithic Memories**

IEEE Symbols



**Absolute Maximum Ratings**

Supply voltage $V_{CC}$ .....	7 V
Input voltage .....	7 V
Off-state output voltage .....	5.5 V
Storage temperature .....	-65° to +150°C

**Operating Conditions**

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
$T_A$	Operating free-air temperature	-55		125	0		75	°C

**Electrical Characteristics Over Operating Conditions**

SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{T+}$	Positive threshold voltage	Any A*	1.5	1.7	2.0	1.5	1.7	2.0	V
$V_{T-}$	Negative threshold voltage	Any A*	0.6	0.9	1.1	0.6	0.9	1.1	V
$V_{IC}$	Input clamp voltage	$V_{CC} = \text{MIN}$ $I_I = -18 \text{ mA}$			1.5			-1.5	V
$\Delta V_T$	Hysteresis ( $V_{T+} - V_{T-}$ )	Any A*	0.4	0.5		0.4	0.8		V
$\Delta V_{DB}$	Dead band voltage	Any A*	0.4			0.4			V
$V_{IL}$	Input low voltage	Any E*			0.8			0.8	V
$V_{IH}$	Input high voltage	Any E*	2.0			2.0			V
$I_{IL}$	Low-level input current	$V_{CC} = \text{MAX}$ $V_I = 0.4 \text{ V}$			-0.2			-0.2	mA
$I_{IH}$	High-level input current	$V_{CC} = \text{MAX}$ $V_I = 2.7 \text{ V}$			20			20	$\mu\text{A}$
$I_I$	Maximum input current	$V_{CC} = \text{MAX}$ $V_I = 7 \text{ V}$			0.1			0.1	mA
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}$ $V_{T+} = 2 \text{ V}$ $V_{T-} = 0.6 \text{ V}$ $I_{OL} = 12 \text{ mA}$			0.4			0.4	V
		$I_{OL} = 24 \text{ mA}$					0.5		
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}$ $V_{T+} = 2 \text{ V}$ $V_{T-} = 0.6 \text{ V}$ $I_{OH} = -3 \text{ mA}$	2.4	3.4		2.4	3.4		V
		$I_{OH} = -12 \text{ mA}$	2						
		$I_{OH} = -15 \text{ mA}$				2			
$I_{OZL}$	Off-state output current	$V_{CC} = \text{MAX}$ $V_{T+} = 2 \text{ V}$ $V_{T-} = 0.6 \text{ V}$ $V_O = 0.4 \text{ V}$			-20			-20	$\mu\text{A}$
$I_{OZH}$		$V_O = 2.7 \text{ V}$			20			20	$\mu\text{A}$
$I_{OS}$	Output short-circuit current**	$V_{CC} = \text{MAX}$	-40	-225		-40	-225		mA
$I_{CC}$	Supply Current	Outputs High Outputs Low Outputs Disabled	$V_{CC} = \text{MAX}$ Outputs open	'LS310,'LS340	17	27	17	27	mA
				'LS341,'LS344	18	35	18	35	
				'LS310,'LS340	26	44	26	44	
				'LS341,'LS344	32	46	32	46	
				'LS310,'LS340	29	50	29	50	
				'LS341,'LS344	34	54	34	54	

\*\* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

\* "A" indicates data input, "E" indicates enable input.

**Switching Characteristics**  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	'LS310, 'LS340		'LS341, 'LS344		UNIT
			MIN	TYP	MAX	MIN	
$t_{PLH}$	Data to Output delay	$C_L = 45\text{ pF}$ $R_L = 667\ \Omega$	19	25	19	25	ns
$t_{PHL}$			19	25	19	25	ns
$t_{PZL}$	Output Enable delay		32	40	25	40	ns
$t_{PZH}$			23	35	24	35	ns
$t_{PLZ}$	Output Disable delay	$C_L = 5\text{ pF}$ $R_L = 667\ \Omega$	18	30	21	30	ns
$t_{PHZ}$			18	25	18	25	ns

DO NOT USE FOR NEW DESIGNS

**Absolute Maximum Ratings**

Supply voltage $V_{CC}$ .....	7.0 V
Input voltage .....	5.5 V
Off-state output voltage .....	5.5 V
Storage temperature .....	-65° to +150°C

**Operating Conditions**

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
$T_A$	Operating free-air temperature	-55		125	0		75	°C

**Electrical Characteristics Over Operating Conditions**

SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY			COMMERCIAL			UNIT	
			MIN	TYP	MAX	MIN	TYP	MAX		
$V_{T+}$	Positive threshold voltage	Any A*	1.5	1.8	2.05	1.6	1.8	2.0	V	
$V_{T-}$	Negative threshold voltage	Any A*	0.8	1.1	1.35	0.8	1.1	1.3	V	
$V_{IC}$	Input clamp voltage	$V_{CC} = \text{MIN}$ $I_I = -18 \text{ mA}$			-1.2			-1.2	V	
$\Delta V_T$	Hysteresis ( $V_{T+} - V_{T-}$ )	Any A*	0.5	0.7		0.5	0.7		V	
$\Delta V_{DB}$	Dead band voltage	Any A*	0.5			0.3			V	
$V_{IL}$	Input low voltage	Any E*			0.8			0.8	V	
$V_{IH}$	Input high voltage	Any E*			2.0			2.0	V	
$I_{IL}$	Low-level input current	$V_{CC} = \text{MAX}$ $V_I = 0.5 \text{ V}$			-0.25			-0.25	mA	
$I_{IH}$	High-level input current	$V_{CC} = \text{MAX}$ $V_I = 2.7 \text{ V}$			50			50	$\mu\text{A}$	
$I_I$	Maximum input current	$V_{CC} = \text{MAX}$ $V_I = 5.5 \text{ V}$			1			1	mA	
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}$ $V_T = 2 \text{ V}$ $I_{OL} = 48 \text{ mA}$			0.55				V	
		$V_T = 0.8 \text{ V}$ $I_{OL} = 64 \text{ mA}$						0.55	V	
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}$ $I_{OH} = -1 \text{ mA}$						2.7	V	
		$I_{OH} = -3 \text{ mA}$	2.4	3.4			2.4	3.4		
		$V_{T+} = 2 \text{ V}$ $I_{OH} = -12 \text{ mA}$	2							
		$V_{T-} = 0.8 \text{ V}$ $I_{OH} = -15 \text{ mA}$					2			
$I_{OZL}$	Off-state output current	$V_{CC} = \text{MAX}$ $V_O = 0.5 \text{ V}$			-50			-50	$\mu\text{A}$	
		$V_{IH} = 2.0 \text{ V}$ $V_{IL} = 0.8 \text{ V}$ $V_O = 2.7 \text{ V}$			50			50	$\mu\text{A}$	
$I_{OS}$	Output short-circuit current**	$V_{CC} = \text{MAX}$			-50	-225		-50	-225	mA
$I_{CC}$	Supply Current	$V_{CC} = \text{MAX}$ Outputs open		'S310, 'S340	50	80		50	80	mA
				'S341, 'S344	80	130		80	130	
				'S310, 'S340	110	155		100	155	
				'S341, 'S344	130	180		130	185	
				'S310, 'S340	135	180		135	180	
				'S341, 'S344	155	180		150	200	

\*\* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

\* "A" indicates data input, "E" indicates enable input.

**Switching Characteristics**  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	'S310, 'S340			'S341, 'S344			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$t_{PLH}$	Data to Output delay	$C_L = 50\text{ pF}$ $R_L = 90\Omega$	11	15	16	22	ns		
$t_{PHL}$			16	22	10	15	ns		
$t_{PZL}$	Output Enable delay		8	15	10	15	ns		
$t_{PZH}$			6	12	7	12	ns		
$t_{PLZ}$	Output Disable delay	$C_L = 5\text{ pF}$ $R_L = 90\Omega$	10	15	10	15	ns		
$t_{PHZ}$			7	12	7	12	ns		

DO NOT USE FOR NEW DESIGNS

Function Tables

'310

$\overline{E}_1$	$E_2$	1Y OUTPUTS	2Y OUTPUTS
H	H	Z	Enabled (Inverting)
H	L	Z	Z
L	H	Enabled (Inverting)	Enabled (Inverting)
L	L	Enabled (Inverting)	Z

'340

$\overline{E}_1$	$\overline{E}_2$	1Y OUTPUTS	2Y OUTPUTS
H	H	Z	Z
H	L	Z	Enabled (Inverting)
L	H	Enabled (Inverting)	Z
L	L	Enabled (Inverting)	Enabled (Inverting)

'341

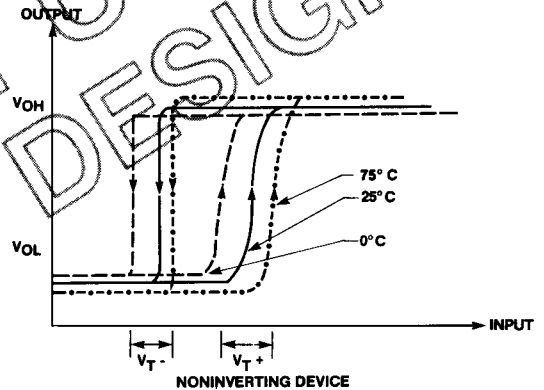
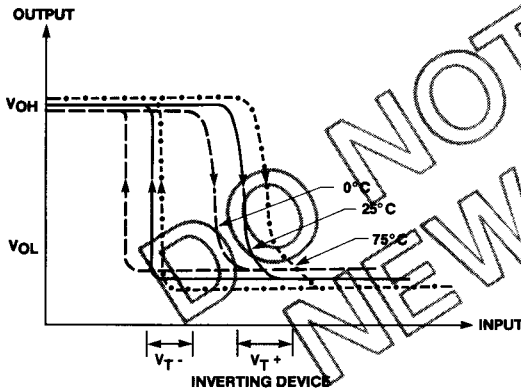
$\overline{E}_1$	$E_2$	1Y OUTPUTS	2Y OUTPUTS
H	H	Z	Enabled
H	L	Z	Z
L	H	Enabled	Enabled
L	L	Enabled	Z

'344

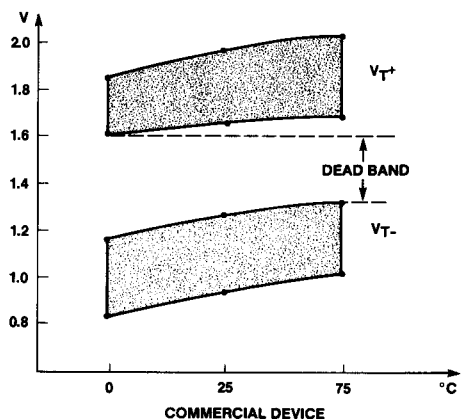
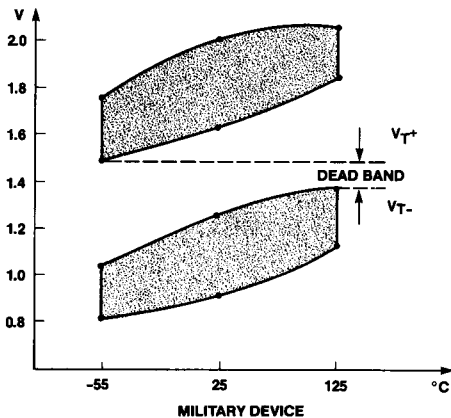
$\overline{E}_1$	$\overline{E}_2$	1Y OUTPUTS	2Y OUTPUTS
H	H	Z	Z
H	L	Z	Enabled
L	H	Enabled	Enabled
L	L	Enabled	Enabled

Z = High impedance (output off).

INPUT VS OUTPUT VOLTAGE TRANSFER CHARACTERISTIC

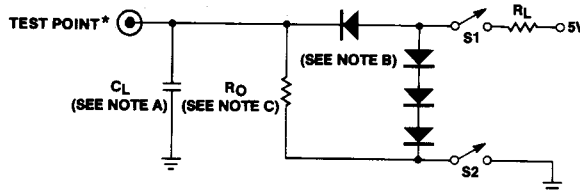


THRESHOLD VOLTAGE VS OPERATING TEMPERATURE



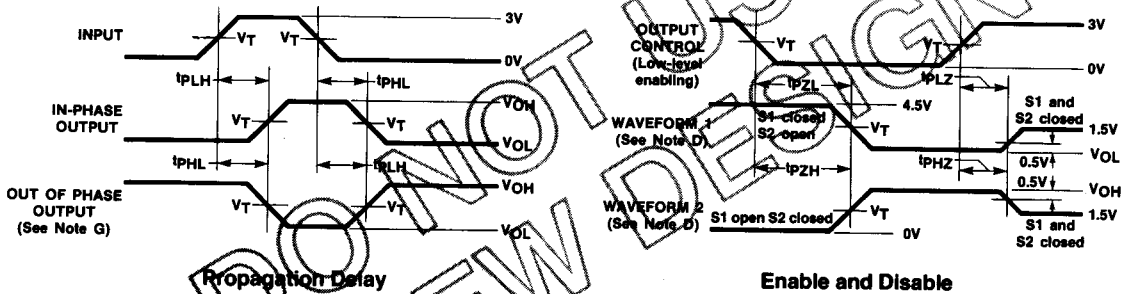
\* Dead Band: The hysteresis is guaranteed at any operating temperature and voltage.

Test Load



\* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Test Waveforms



DO NOT USE FOR NEW DESIGNS

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. All diodes are 1N916 or 1N3064.
  - C. For Series 54/74S310/340/341/344  $R_O = 5K$ ,  $V_T = V_{T+} = 1.8 V$  for low-to-high input transition.  
For Series 54/74S310/340/341/344  $R_O = 5K$ ,  $V_T = V_{T-} = 1.1 V$  for high-to-low input transition.  
For Series 54/74LS310/340/341/344  $R_O = 5K$ ,  $V_T = V_{T+} = 1.7 V$  for low-to-high input transition.  
For Series 54/74LS310/340/341/344  $R_O = 5K$ ,  $V_T = V_{T-} = 0.9 V$  for high-to-low input transition.
  - D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.  
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
  - F. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_{OUT} = 50\Omega$  and:  
For Series 54/74S,  $t_R \leq 2.5 \text{ ns}$ ,  $t_F \leq 2.5 \text{ ns}$ .  
For Series 54/74LS and PALs,  $t_R \leq 15 \text{ ns}$ ,  $t_F \leq 6 \text{ ns}$ .
  - G. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed. (Propagation delays are measured from the inputs crossing  $V_{T+}$ ,  $V_{T-}$  to the outputs crossing  $V_T$ .)