TBB1002

Twin Build in Biasing Circuit MOS FET IC
VHF/UHF RF Amplifier

HITACHI

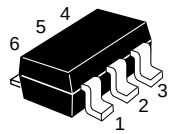
ADE-208-987F (Z)
7th. Edition
Dec. 2000

Features

- Small SMD package CMPAK-6 built in twin BBFET; To reduce using parts cost & PC board space.
- Suitable for World Standard Tuner RF amplifier.
- Very useful for total tuner cost reduction.
- Withstanding to ESD; Build in ESD absorbing diode. Withstand up to 200 V at C = 200 pF, Rs = 0 conditions.
- Provide mini mold packages; CMPAK-6

Outline

CMPAK-6



1. Gate-1(1)
2. Source
3. Drain(1)
4. Drain(2)
5. Gate-2
6. Gate-1(2)

Notes: 1. Marking is “BM”.
2. TBB1002 is individual type number of HITACHI TWIN BBFET.

Hitachi semiconductor

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DS}	6	V
Gate1 to source voltage	V_{G1S}	+6 -0	V
Gate2 to source voltage	V_{G2S}	+6 -0	V
Drain current	I_D	30	mA
Channel power dissipation	Pch[*3]	250	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 3. Value on the glass epoxy board (49mm × 38mm × 1mm).

Electrical Characteristics (Ta = 25°C)

The below specification are applicable for UHF unit (FET1)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	6	—	—	V	I_D = 200µA, V_{G1S} = V_{G2S} = 0
Gate1 to source breakdown voltage	$V_{(BR)G1SS}$	+6	—	—	V	I_{G1} = +10µA, V_{G2S} = V_{DS} = 0
Gate2 to source breakdown voltage	$V_{(BR)G2SS}$	+6	—	—	V	I_{G2} = +10µA, V_{G1S} = V_{DS} = 0
Gate1 to source cutoff current	I_{G1SS}	—	—	+100	nA	V_{G1S} = +5V, V_{G2S} = V_{DS} = 0
Gate2 to source cutoff current	I_{G2SS}	—	—	+100	nA	V_{G2S} = +5V, V_{G1S} = V_{DS} = 0
Gate1 to source cutoff voltage	$V_{G1S(off)}$	0.5	0.75	1.0	V	V_{DS} = 5V, V_{G2S} = 4V, I_D = 100µA
Gate2 to source cutoff voltage	$V_{G2S(off)}$	0.5	0.75	1.0	V	V_{DS} = 5V, V_{G1S} = 5V, I_D = 100µA
Drain current	$I_{D(op)}$	13	17	21	mA	V_{DS} = 5V, V_{G1} = 5V V_{G2S} = 4V, R_G = 100kΩ
Forward transfer admittance	$\|y_{fs}\|$	21	26	31	mS	V_{DS} = 5V, V_{G1} = 5V, V_{G2S} =4V R_G = 100kΩ, f = 1kHz
Input capacitance	c_{iss}	1.4	1.8	2.2	pF	V_{DS} = 5V, V_{G1} = 5V
Output capacitance	c_{oss}	1.0	1.4	1.8	pF	V_{G2S} =4V, R_G = 100kΩ
Reverse transfer capacitance	c_{rss}	—	0.02	0.04	pF	f = 1MHz
Power gain	PG	16	21	—	dB	V_{DS} = V_{G1} = 5V, V_{G2S} = 4V R_G = 100kΩ, f = 900MHz Zi=S11*, Zo=S22*(:PG)
Noise figure	NF	—	1.7	2.5	dB	Zi=S11opt (:NF)

Electrical Characteristics (Ta = 25°C)

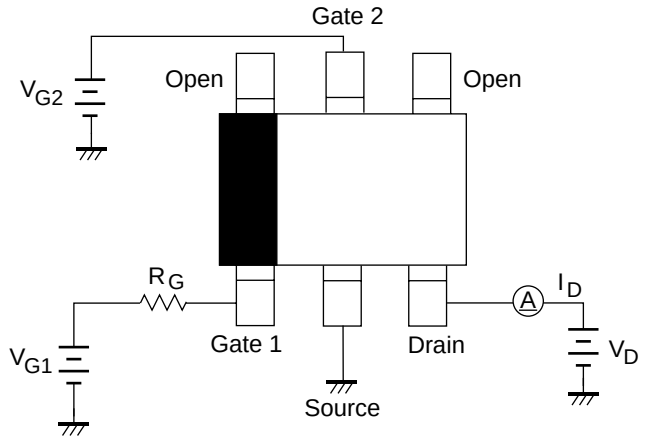
The below specification are applicable for VHF unit (FET2)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	6	—	—	V	I_D = 200µA, V_{G1S} = V_{G2S} = 0
Gate1 to source breakdown voltage	$V_{(BR)G1SS}$	+6	—	—	V	I_{G1} = +10µA, V_{G2S} = V_{DS} = 0
Gate2 to source breakdown voltage	$V_{(BR)G2SS}$	+6	—	—	V	I_{G2} = +10µA, V_{G1S} = V_{DS} = 0
Gate1 to source cutoff current	I_{G1SS}	—	—	+100	nA	V_{G1S} = +5V, V_{G2S} = V_{DS} = 0
Gate2 to source cutoff current	I_{G2SS}	—	—	+100	nA	V_{G2S} = +5V, V_{G1S} = V_{DS} = 0
Gate1 to source cutoff voltage	$V_{G1S(off)}$	0.5	0.75	1.0	V	V_{DS} = 5V, V_{G2S} = 4V, I_D = 100µA
Gate2 to source cutoff voltage	$V_{G2S(off)}$	0.5	0.75	1.0	V	V_{DS} = 5V, V_{G1S} = 5V, I_D = 100µA
Drain current	$I_{D(op)}$	14	18	22	mA	V_{DS} = 5V, V_{G1} = 5V, V_{G2S} = 4V, R_G = 82kΩ
Forward transfer admittance	$\|y_{fs}\|$	20	25	30	mS	V_{DS} = 5V, V_{G1} = 5V, V_{G2S} =4V, R_G = 82kΩ, f = 1kHz
Input capacitance	c_{iss}	2.2	2.6	3.0	pF	V_{DS} = 5V, V_{G1} = 5V
Output capacitance	c_{oss}	1.2	1.6	2.0	pF	V_{G2S} =4V, R_G = 82kΩ
Reverse transfer capacitance	c_{rss}	—	0.03	0.05	pF	f = 1MHz
Power gain	PG	22	27	—	dB	V_{DS} = V_{G1} = 5V, V_{G2S} = 4V
Noise figure	NF	—	1.2	1.7	dB	R_G = 82kΩ, f = 200MHz

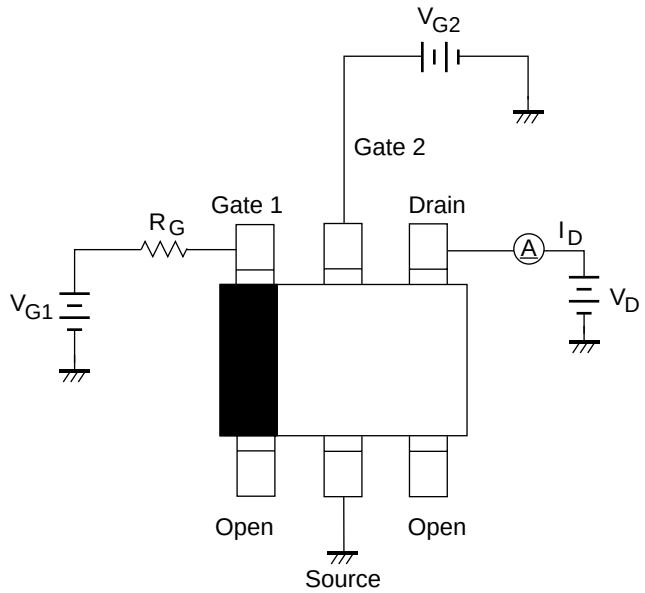
Test Circuits

- **DC Biasing Circuit for Operating Characteristic Items** ($I_{D(op)}$, |yfs|, Ciss, Coss, Crss, NF, PG)

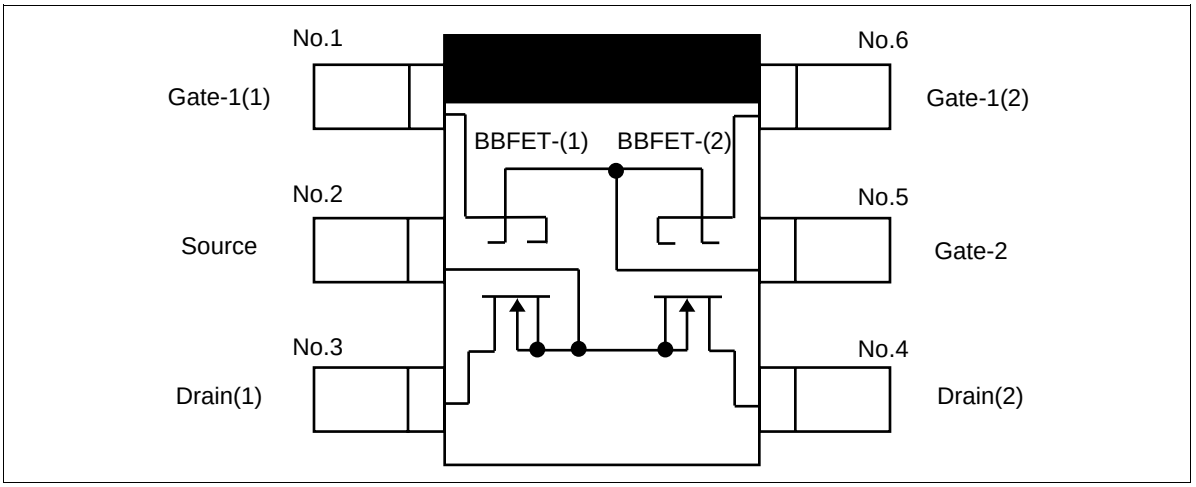
Measurment of FET1



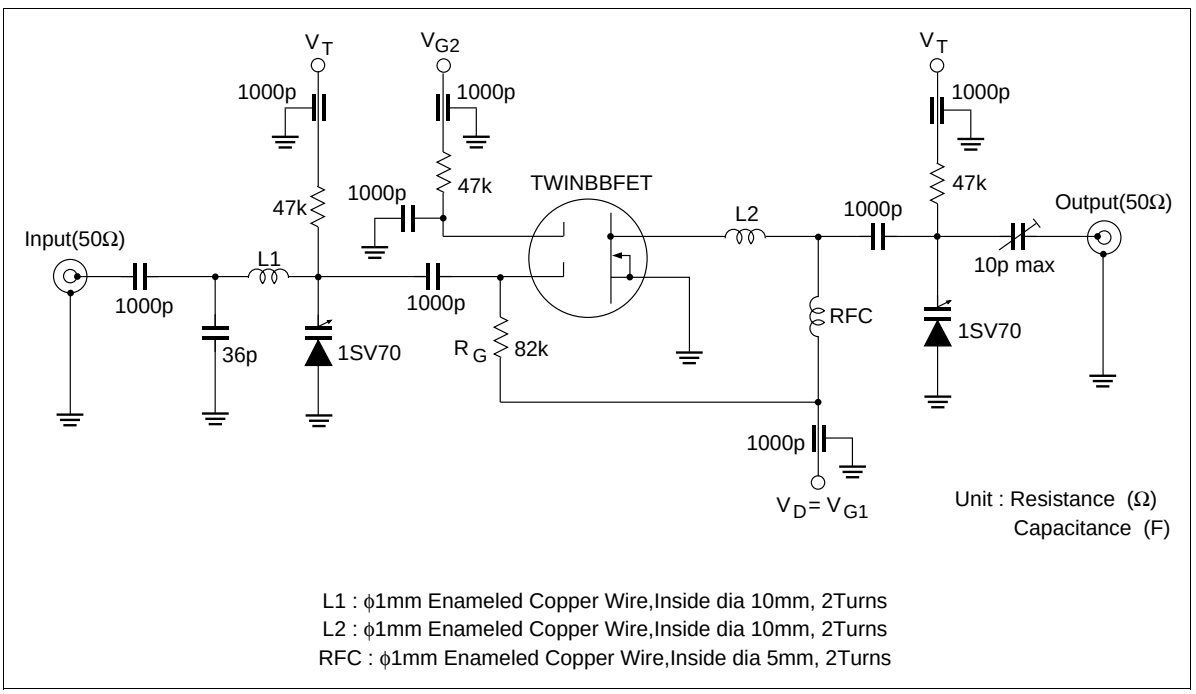
Measurment of FET2



- **Equivalent Circuit**

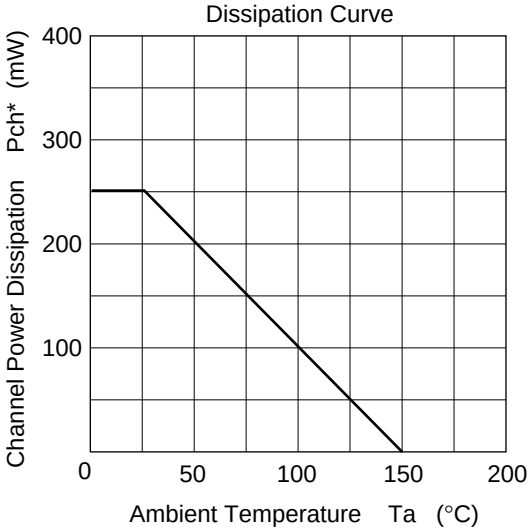


- **200 MHz Power Gain, Noise Figure Test Circuit**



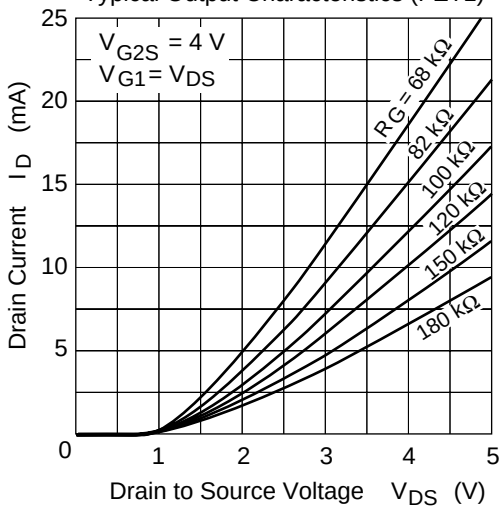
L1 : ϕ1mm Enameled Copper Wire,Inside dia 10mm, 2Turns
L2 : ϕ1mm Enameled Copper Wire,Inside dia 10mm, 2Turns
RFC : ϕ1mm Enameled Copper Wire,Inside dia 5mm, 2Turns

Maximum Channel Power Dissipation Curve

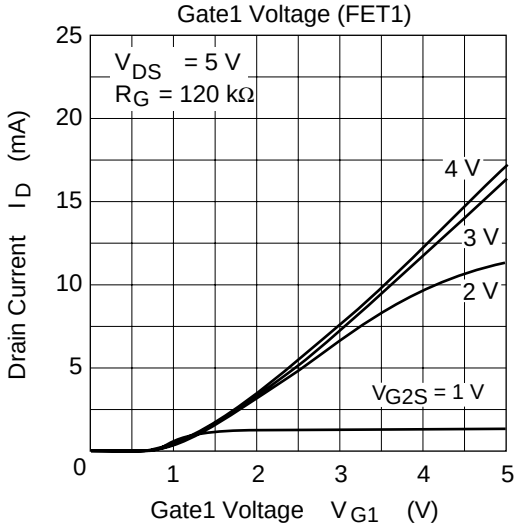


* Value on the glass epoxy board (49mm × 38mm × 1mm)

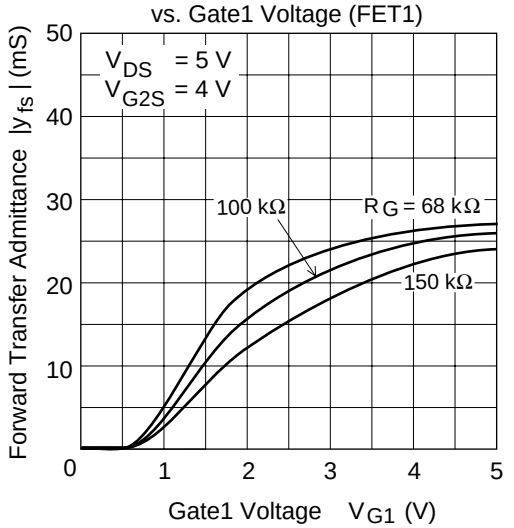
Typical Output Characteristics (FET1)



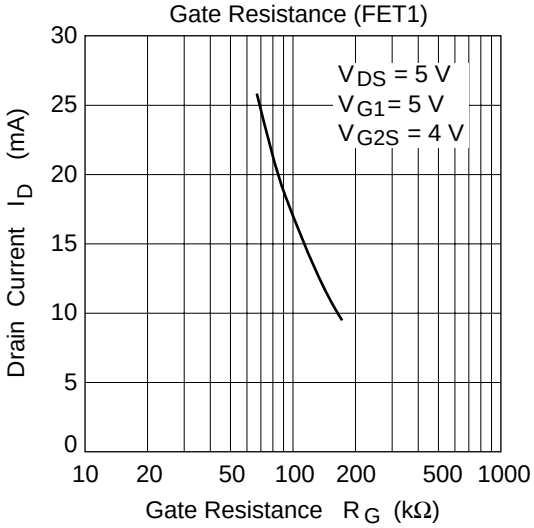
Drain Current vs. Gate1 Voltage (FET1)



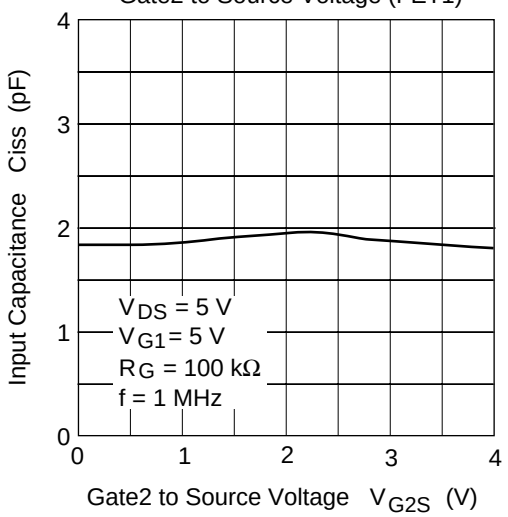
Forward Transfer Admittance vs. Gate1 Voltage (FET1)



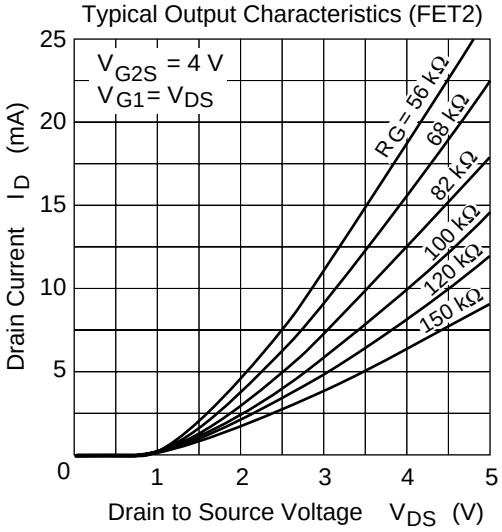
Drain Current vs.
Gate Resistance (FET1)



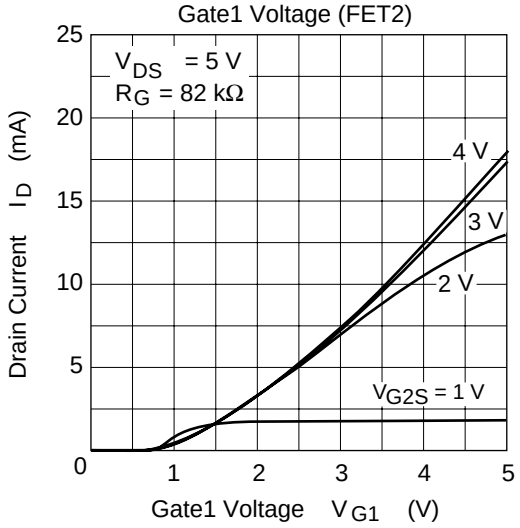
Input Capacitance vs.
Gate2 to Source Voltage (FET1)



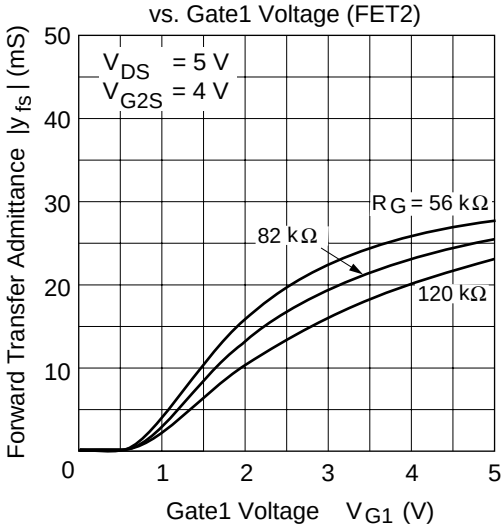
Typical Output Characteristics (FET2)



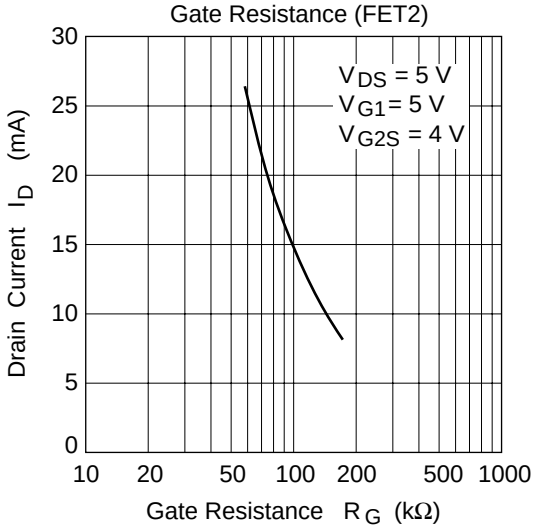
Drain Current vs.
Gate1 Voltage (FET2)



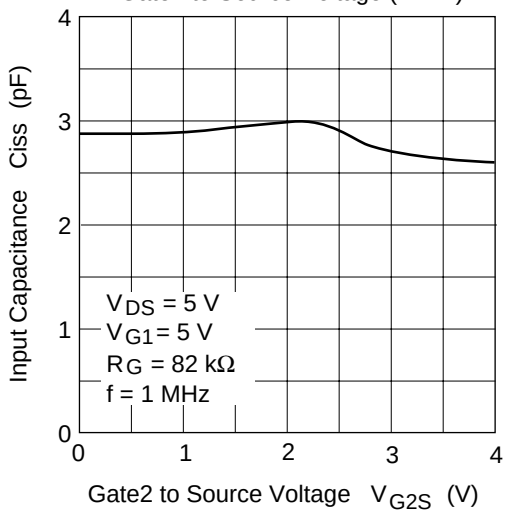
Forward Transfer Admittance vs. Gate1 Voltage (FET2)



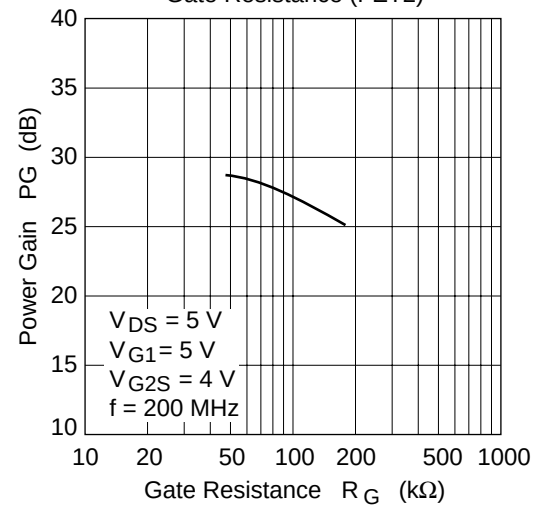
Drain Current vs. Gate Resistance (FET2)



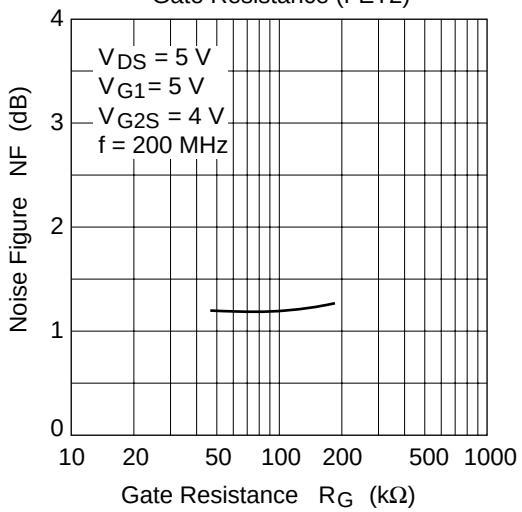
Input Capacitance vs. Gate2 to Source Voltage (FET2)



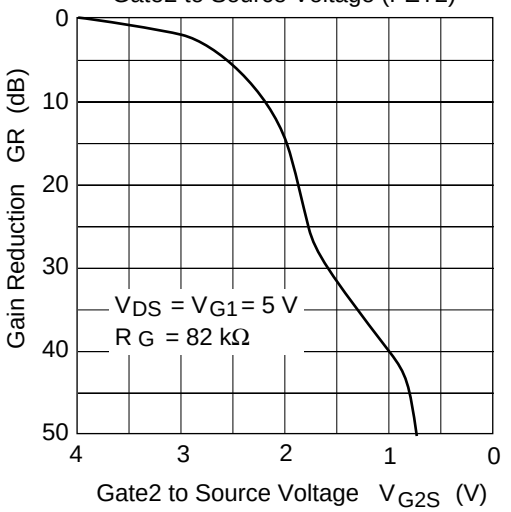
Power Gain vs. Gate Resistance (FET2)



Noise Figure vs.
Gate Resistance (FET2)

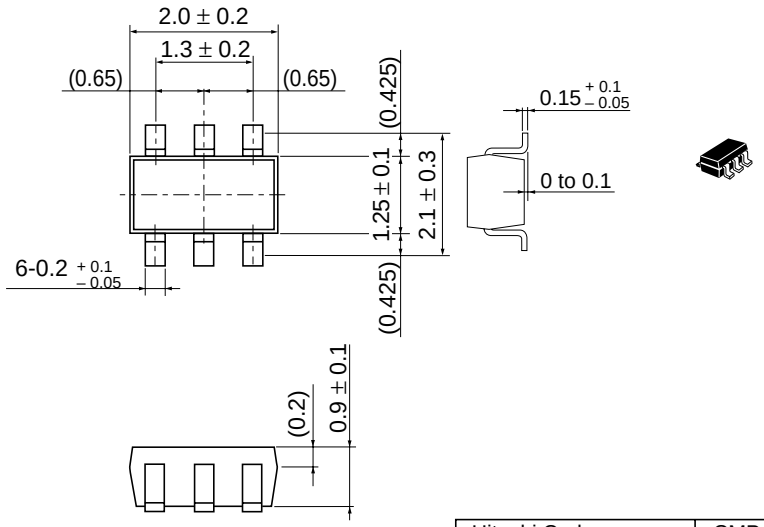


Gain Reduction vs.
Gate2 to Source Voltage (FET2)



Package Dimensions

As of January, 2001
Unit: mm



Hitachi Code	CMPAK-6
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.006 g

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