

2N5196/5197/5198/5199

Monolithic N-Channel JFET Duals

Product Summary

Part Number	$V_{GS(off)}$ (V)	$V_{(BR)GSS}$ Min (V)	g_{fs} Min (mS)	I_G Max (pA)	$ V_{GS1} - V_{GS2} $ Max (mV)
2N5196	-0.7 to -4	-50	1	-15	5
2N5197	-0.7 to -4	-50	1	-15	5
2N5198	-0.7 to -4	-50	1	-15	10
2N5199	-0.7 to -4	-50	1	-15	15

Features

- Monolithic Design
- High Slew Rate
- Low Offset/Drift Voltage
- Low Gate Leakage: 5 pA
- Low Noise
- High CMRR: 100 dB

Benefits

- Tight Differential Match vs. Current
- Improved Op Amp Speed, Settling Time Accuracy
- Minimum Input Error/Trimming Requirement
- Insignificant Signal Loss/Error Voltage
- High System Sensitivity
- Minimum Error with Large Input Signal

Applications

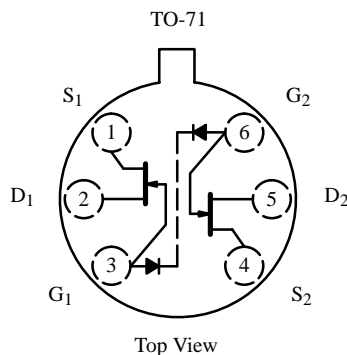
- Wideband Differential Amps
- High-Speed, Temp-Compensated, Single-Ended Input Amps
- High Speed Comparators
- Impedance Converters

Description

The 2N5196/5197/5198/5199 JFET duals are designed for high-performance differential amplification for a wide range of precision test instrumentation applications. This series features tightly matched specs, low gate leakage for accuracy, and wide dynamic range with I_G guaranteed at $V_{DG} = 20$ V.

The hermetically-sealed TO-71 package is available with full military processing (see Military Information and the 2N5545/5546/5547JANTX/JANTXV data sheet).

For similar products see the low-noise U/SST401 series, the high-gain 2N5911/5912, and the low-leakage U421/423 data sheets.



Absolute Maximum Ratings

Gate-Drain, Gate-Source Voltage -50 V
 Gate Current 50 mA
 Lead Temperature ($1/16''$ from case for 10 sec.) 300 °C
 Storage Temperature -65 to 200 °C
 Operating Junction Temperature -55 to 150 °C

Power Dissipation : Per Side^a 250 mW
 Total^b 500 mW

Notes

- Derate 2 mW/°C above 85 °C
- Derate 4 mW/°C above 85 °C

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70252.

2N5196/5197/5198/5199

Specifications^a for 2N5196 and 2N5197

Parameter	Symbol	Test Conditions	Typ ^b	Limits				Unit
				2N5196		2N5197		
				Min	Max	Min	Max	
Static								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	$I_G = -1 \mu A, V_{DS} = 0 V$	-57	-50		-50		V
Gate-Source Cutoff Voltage	$V_{GS(off)}$	$V_{DS} = 20 V, I_D = 1 nA$	-2	-0.7	-4	-0.7	-4	
Saturation Drain Current ^c	I_{DSS}	$V_{DS} = 20 V, V_{GS} = 0 V$	3	0.7	7	0.7	7	mA
Gate Reverse Current	I_{GSS}	$V_{GS} = -30 V, V_{DS} = 0 V$	-10		-25		-25	pA
		$T_A = 150^\circ C$	-20		-50		-50	nA
Gate Operating Current	I_G	$V_{DG} = 20 V, I_D = 200 \mu A$	-5		-15		-15	pA
		$T_A = 125^\circ C$	-0.8		-15		-15	nA
Gate-Source Voltage	V_{GS}	$V_{DG} = 20 V, I_D = 200 \mu A$	-1.5	-0.2	-3.8	-0.2	-3.8	V
Dynamic								
Common-Source Forward Transconductance	g_{fs}	$V_{DS} = 20 V, V_{GS} = 0 V$ $f = 1 kHz$	2.5	1	4	1	4	mS
Common-Source Output Conductance	g_{os}		2		50		50	μS
Common-Source Forward Transconductance	g_{fs}	$V_{DS} = 20 V, I_D = 200 \mu A$ $f = 1 kHz$	0.8	0.7	1.6	0.7	1.6	mS
Common-Source Output Conductance	g_{os}		1		4		4	μS
Common-Source Input Capacitance	C_{iss}	$V_{DS} = 20 V, V_{GS} = 0 V$ $f = 1 MHz$	3		6		6	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1		2		2	
Equivalent Input Noise Voltage	\bar{e}_n	$V_{DS} = 20 V, V_{GS} = 0 V, f = 1 kHz$	9		20		20	$\frac{nV}{\sqrt{Hz}}$
Noise Figure	NF	$V_{DS} = 20 V, V_{GS} = 0 V$ $f = 100 Hz, R_G = 10 M\Omega$			0.5		0.5	dB
Matching								
Differential Gate-Source Voltage	$ V_{GS1} - V_{GS2} $	$V_{DG} = 20 V, I_D = 200 \mu A$			5		5	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta V_{GS1} - V_{GS2} }{\Delta T}$	$V_{DG} = 20 V, I_D = 200 \mu A$ $T_A = -55 \text{ to } 125^\circ C$			5		10	$\frac{\mu V}{^\circ C}$
Saturation Drain Current Ratio	$\frac{I_{DSS1}}{I_{DSS2}}$	$V_{DS} = 20 V, V_{GS} = 0 V$	0.98	0.95	1	0.95	1	
Transconductance Ratio	$\frac{g_{fs1}}{g_{fs2}}$	$V_{DS} = 20 V, I_D = 200 \mu A$ $f = 1 kHz$	0.99	0.97	1	0.97	1	
Differential Output Conductance	$ g_{os1} - g_{os2} $		0.1		1		1	μS
Differential Gate Current	$ I_{G1} - I_{G2} $	$V_{DG} = 20 V, I_D = 200 \mu A$ $T_A = 125^\circ C$	0.1		5		5	nA
Common Mode Rejection Ratio ^d	CMRR	$V_{DG} = 10 \text{ to } 20 V, I_D = 200 \mu A$	100					dB

2N5196/5197/5198/5199

Specifications^a for 2N5198 and 2N5199

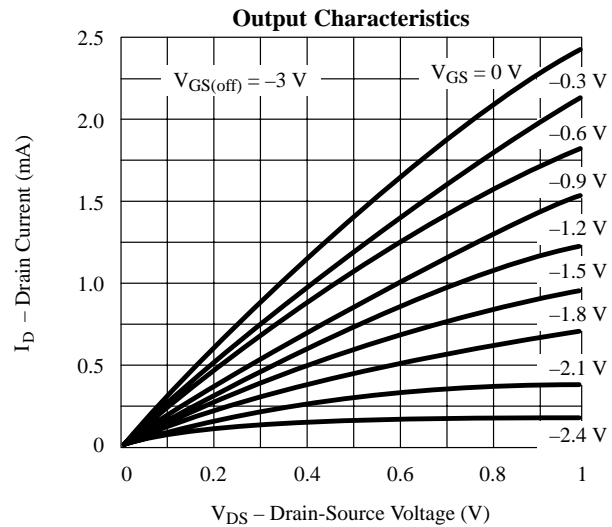
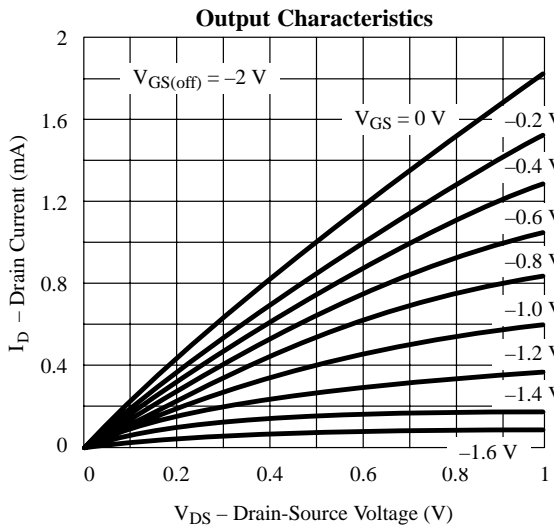
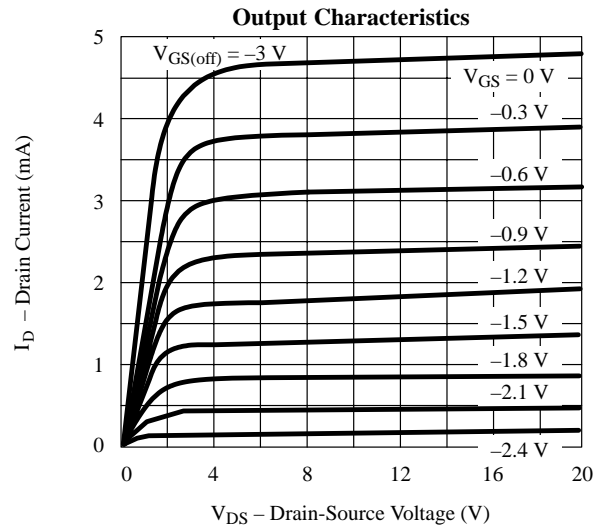
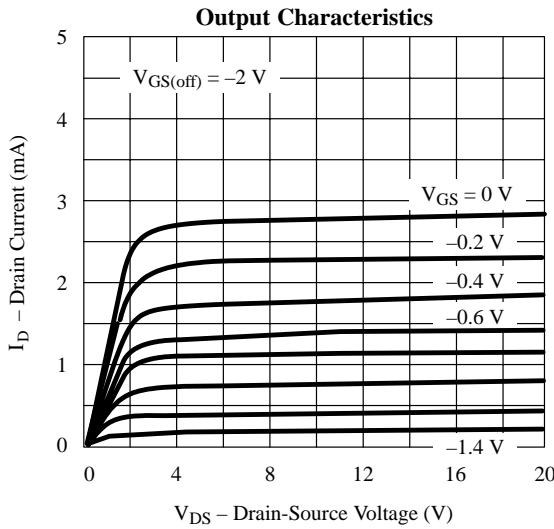
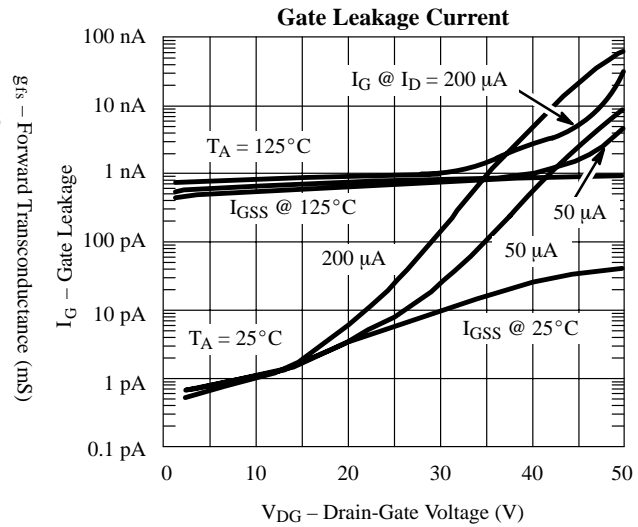
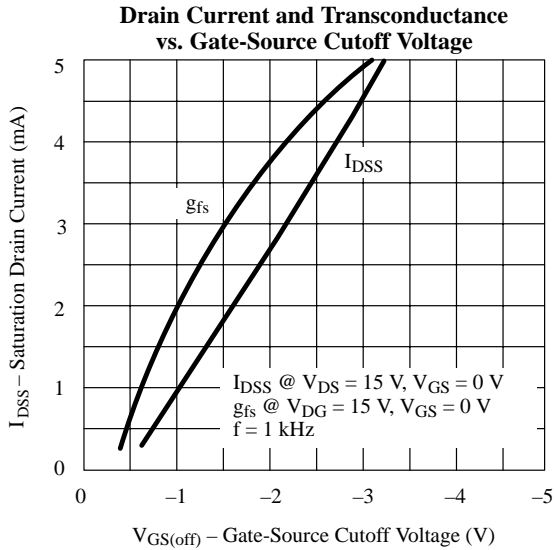
Parameter	Symbol	Test Conditions	Typ ^b	Limits				Unit
				2N5198		2N5199		
				Min	Max	Min	Max	
Static								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	$I_G = -1 \mu A, V_{DS} = 0 V$	-57	-50		-50		V
Gate-Source Cutoff Voltage	$V_{GS(off)}$	$V_{DS} = 20 V, I_D = 1 nA$	-2	-0.7	-4	-0.7	-4	
Saturation Drain Current ^c	I_{DSS}	$V_{DS} = 20 V, V_{GS} = 0 V$	3	0.7	7	0.7	7	mA
Gate Reverse Current	I_{GSS}	$V_{GS} = -30 V, V_{DS} = 0 V$	-10		-25		-25	pA
		$T_A = 150^\circ C$	-20		-50		-50	nA
Gate Operating Current	I_G	$V_{DG} = 20 V, I_D = 200 \mu A$	-5		-15		-15	pA
		$T_A = 125^\circ C$	-0.8		-15		-15	nA
Gate-Source Voltage	V_{GS}	$V_{DG} = 20 V, I_D = 200 \mu A$	-1.5	-0.2	-3.8	-0.2	-3.8	V
Dynamic								
Common-Source Forward Transconductance	g_{fs}	$V_{DS} = 20 V, V_{GS} = 0 V, f = 1 kHz$	2.5	1	4	1	4	mS
Common-Source Output Conductance	g_{os}		2		50		50	μS
Common-Source Forward Transconductance	g_{fs}	$V_{DS} = 20 V, I_D = 200 \mu A, f = 1 kHz$	0.8	0.7	1.6	0.7	1.6	mS
Common-Source Output Conductance	g_{os}		1		4		4	μS
Common-Source Input Capacitance	C_{iss}	$V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz$	3		6		6	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1		2		2	
Equivalent Input Noise Voltage	\bar{e}_n	$V_{DS} = 20 V, V_{GS} = 0 V, f = 1 kHz$	9		20		20	nV/\sqrt{Hz}
Noise Figure	NF	$V_{DS} = 20 V, V_{GS} = 0 V, f = 100 Hz, R_G = 10 M\Omega$			0.5		0.5	dB
Matching								
Differential Gate-Source Voltage	$ V_{GS1} - V_{GS2} $	$V_{DG} = 20 V, I_D = 200 \mu A$			10		15	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta V_{GS1} - V_{GS2} }{\Delta T}$	$V_{DG} = 20 V, I_D = 200 \mu A, T_A = -55 \text{ to } 125^\circ C$			20		40	$\mu V/^\circ C$
Saturation Drain Current Ratio	$\frac{I_{DSS1}}{I_{DSS2}}$	$V_{DS} = 20 V, V_{GS} = 0 V$	0.97	0.95	1	0.95	1	
Transconductance Ratio	$\frac{g_{fs1}}{g_{fs2}}$	$V_{DS} = 20 V, I_D = 200 \mu A, f = 1 kHz$	0.97	0.95	1	0.95	1	
Differential Output Conductance	$ g_{os1} - g_{os2} $		0.2		1		1	μS
Differential Gate Current	$ I_{G1} - I_{G2} $	$V_{DG} = 20 V, I_D = 200 \mu A, T_A = 125^\circ C$	0.1		5		5	nA
Common Mode Rejection Ratio ^d	CMRR	$V_{DG} = 10 \text{ to } 20 V, I_D = 200 \mu A$	97					dB

Notes

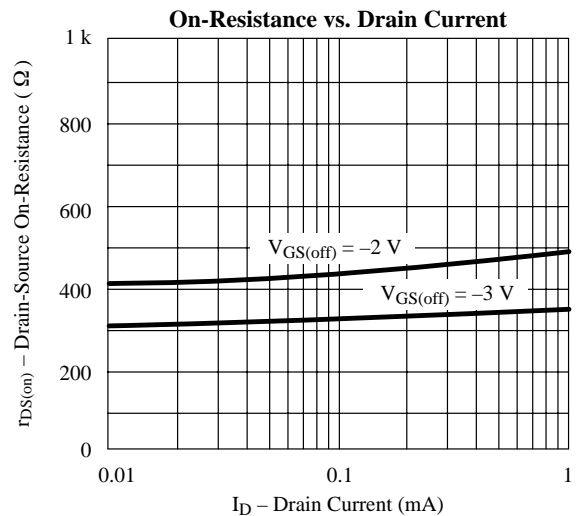
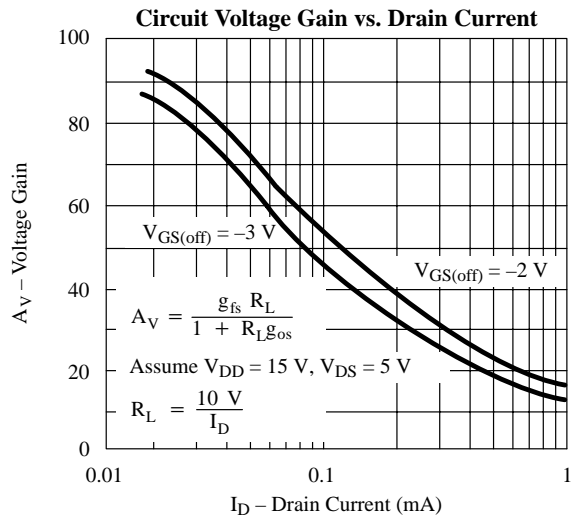
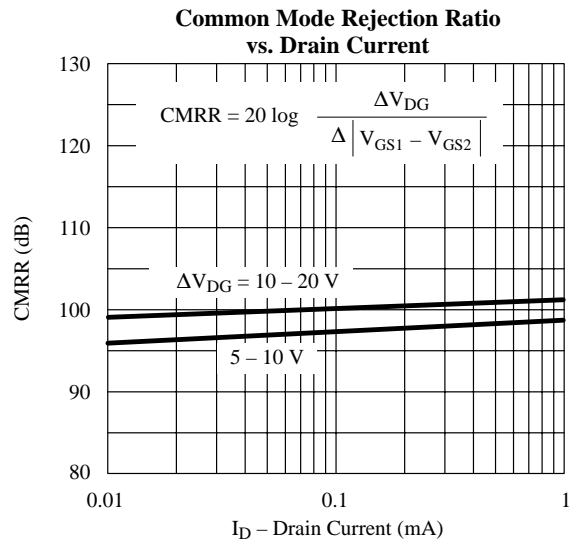
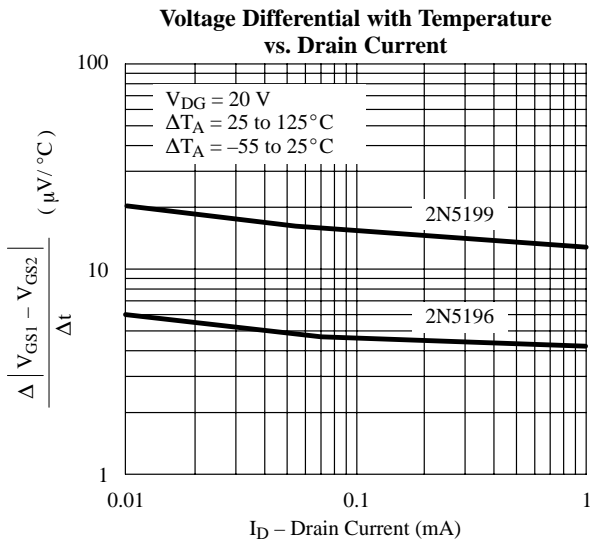
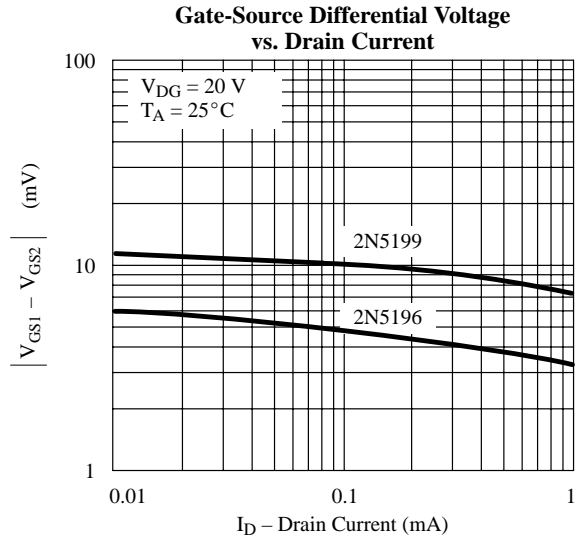
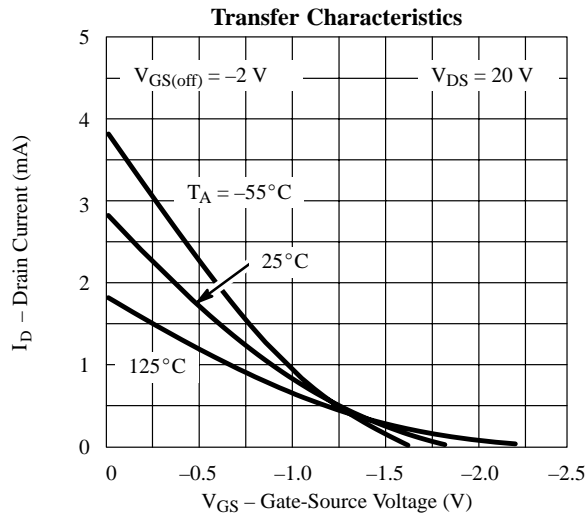
- $T_A = 25^\circ C$ unless otherwise noted.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- Pulse test: $PW \leq 300 \mu s$ duty cycle $\leq 3\%$.
- This parameter not registered with JEDEC.

NQP

Typical Characteristics



Typical Characteristics (Cont'd)



Typical Characteristics (Cont'd)

