

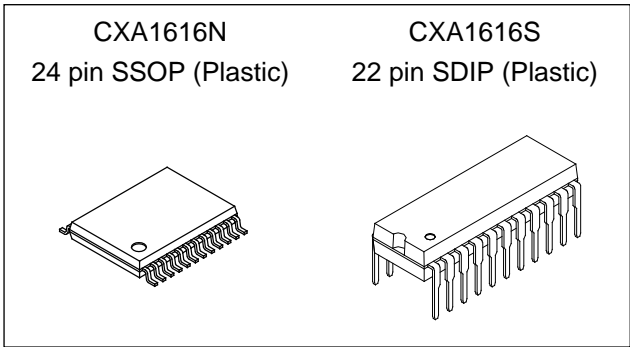
## Sync Discriminator for CRT Displays

**Description**

The CXA1616N/S automatically selects one of three types of sync signals – separate sync, composite sync, or sync-on video – to shape the waveform. It is ideally suited as a synchronous signal processor for auto tracking type displays.

**Features**

- Output of synchronous signal polarity information is obtainable
- Supported polarities and amplitudes of input signals are as follows:
  - V. separate sync  
(positive/negative polarity, 1 to 5Vp-p  
For capacitor input 1.5 to 5Vp-p)
  - H. separate sync  
(positive/negative polarity, 1 to 5Vp-p)
  - Composite sync  
(positive/negative polarity, 1 to 5Vp-p)
  - Sync-on video  
(negative polarity sync level: 0.2 to 0.6Vp-p,  
picture level: 0 to 2.1Vp-p)



**Absolute Maximum Ratings** (Ta = 25°C)

- Supply voltage Vcc 14 V
- Operating temperature Topr -20 to +75 °C
- Storage temperature Tstg -65 to +150 °C
- Allowable power dissipation PD 900 mW

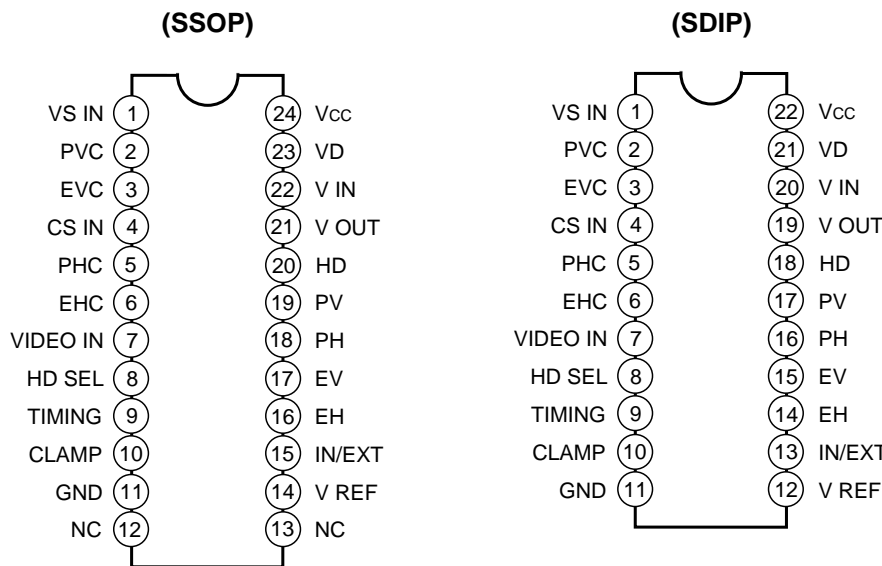
**Operating Condition**

- Supply voltage Vcc 12 ± 0.5 V

**Applications**

CRT display monitors

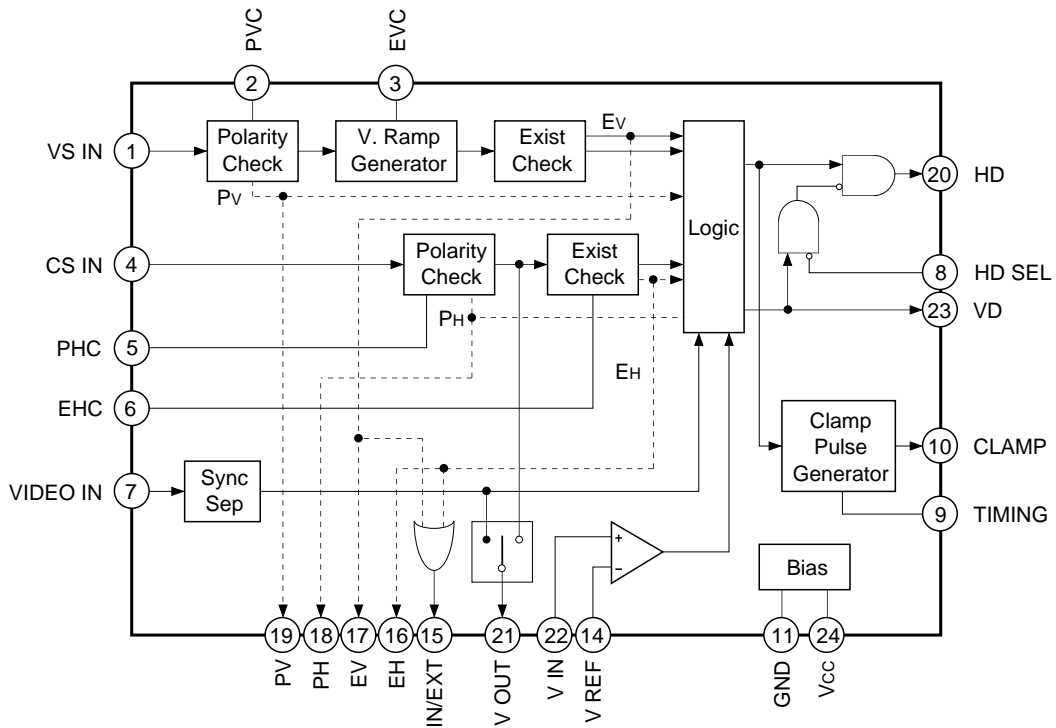
**Pin Configuration (Top View)**



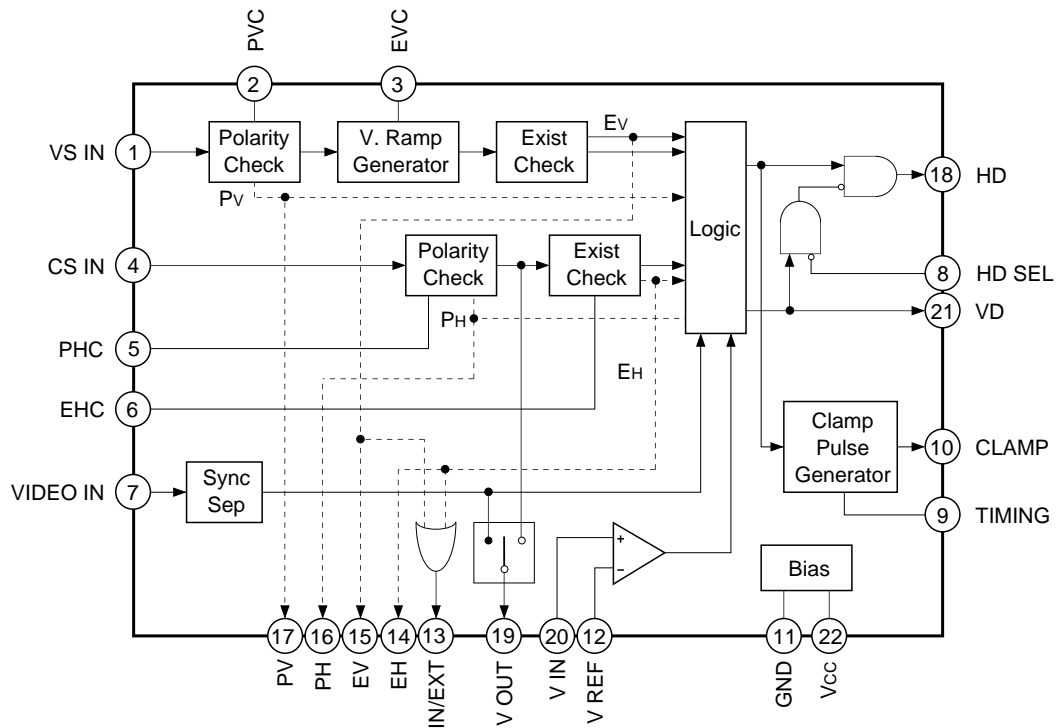
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Block Diagram

(SSOP)



(SDIP)



Pin Description

(Ta = 25°C, Vcc = 12V)

Pin No.		Symbol	Pin voltage	Equivalent circuit	Description
SDIP	SSOP				
1	1	VS IN	—		<p>Inputs the vertical separate sync. Inputs at TTL level and polarity is positive/negative.</p> <p><math>V_{Low} \leq 0.5V</math>  <math>V_{High} \geq 4.5V</math></p> <p>Connect a pull-down resistance of 470kΩ or less to GND.</p>
2	2	PVC	0.3, 3.4V		<p>Connection pin of an integral capacitor for the polarity discriminator circuit (Polarity Check); connects a 0.22μF capacitor to GND.</p> <p>When the capacitor is connected at positive polarity: 3.4V; negative polarity: 0.3V. No input : 3.7V.</p>
5	5	PHC			
3	3	EVC	4.3 to 7.9V		<p>Vertical ramp waveform generator. Generates a ramp waveform synchronized to the input separate sync frequency. Connects a 0.68μF capacitor to GND.</p> <p>The charging time constant (rising edge) of ramp waveform is determined by the 2kΩ resistance and the external 0.68μF capacitor, and the discharging time constant (falling edge) by the external 0.68μF capacitor and the internal 17μA current.</p> <p>When there is a vertical separate sync, the voltage at Pin 3 rises between 5.5 and 7.9V, existence discrimination (Exist Check) is performed, and an input signal is judged to exist.</p> <p>The voltage is 4.3V when no input signal exists.</p>
4	4	CS IN	4.2V		<p>Inputs the composite and horizontal separate sync (positive/negative polarity). Amplitude is 1 to 5Vp-p. Input through a capacitor.</p>

Pin No.		Symbol	Pin voltage	Equivalent circuit	Description
SDIP	SSOP				
6	6	EHC	3.0, 4.8V		<p>Connects a quasi-peak hold circuit with a 33kΩ resistance and 0.22μF capacitor to discriminate input signal existence during composite sync input. When there is a composite sync, the voltage is held by the quasi-peak hold circuit at 4.2 to 4.8V. This voltage is then compared to a 3.8V reference voltage, and an input signal is judged to exist.</p> <p>The voltage is 3.0V when no input signal exists.</p>
7	7	VIDEO IN	4.5V		<p>Inputs the sync-on video (sync is negative polarity). Connect a 0.47μF capacitor and a 270Ω resistance in series between the pin and its signal source.</p> <p>The slice level is determined by the relationship between the sync frequency and Pulse width and the sum of the 200Ω internal resistance and the 270Ω external resistance multiplied by the 29μA current.</p> $\Delta V \approx 29\mu A \times (T_2/T_1) \times (200 + 270)$
8	8	HD SEL	—		<p>Selects whether or not to output the VD interval portion of HD (H Drive Pulse).</p> <p>Input is at TTL level.</p> <p><math>V_{Low} \leq 0.5V</math></p> <p><math>V_{High} \geq 2.0V</math></p> <p>Low level: The VD interval HD is not output.</p> <p>High level or open: The VD interval HD is output as is.</p>
9	9	TIMING	10.5V		<p>Connect a desired capacitor and a 12kΩ resistance in parallel to GND. This capacitor changes the output pulse width of clamp pulse. (See Fig. 1)</p>

Pin No.		Symbol	Pin voltage	Equivalent circuit	Description
SDIP	SSOP				
10	10	CLAMP	0.15V		Clamp pulse output. This is an open collector at positive polarity.
11	11	GND	0V	—	GND
12	14	V REF	—		Reference for the vertical sync separator circuit. Connect an external resistance between Vcc and GND to apply the reference voltage. Based on 4.4V. (See Fig. 2)
13 14 15 16 17	15 16 17 18 19	IN/EXT EH EV PH PV	0.12, 4.5V		Outputs the polarity and existence information of a sync signal. See "Description of Operation" for their I/O matrix.
18	20	HD	0.15V		HD (H Drive Pulse) output. This is an open collector at positive polarity.
19	21	V OUT	2.3V		Outputs the sync signal separated from the composite sync or sync-on video for the vertical sync separator. Positive polarity output at an amplitude of 2.3 to 6.0V.

Pin No.		Symbol	Pin voltage	Equivalent circuit	Description
SDIP	SSOP				
20	22	V IN	—		<p>Input for vertical sync separation comparator. Connect an integrator with a 3.9kΩ resistance and a 3300pF capacitor between Pins 19 and 20. The comparator operates when the voltage of the integrated sync signal at the vertical interval becomes higher than the voltage which lowers by <math>V_{BE}</math> (approximately 0.7V) from the voltage at Pin 12.</p>
21	23	VD	0.15V		<p>VD (V Drive Pulse) output. This is an open collector at positive polarity.</p>
22	24	Vcc	12V	—	Power supply.

## Electrical Characteristics

(Ta = 25°C, Vcc = 12V, See the Electrical Characteristics Test Circuit)

No.	Item	Symbol	Measurement description	Measurement point	Min.	Typ.	Max.	Unit
1	VD output voltage	E <sub>VD</sub>	Measures the height of the VD output wave for VS (vertical separate sync) input. Input signal A (tw = 12.5μs). 5V output power supply, R <sub>L</sub> = 2.2kΩ.	VD ( Pin 21 ) ( Pin 23 )	(H level) 4.85 (L level) 0	5.0 0.15	5.0 0.4	V V
2	VD output pulse width 1	t <sub>v1</sub>	Measures the width of the VD output pulse for VS (vertical separate sync) input. Input signal A (tw = 12.5μs).	VD ( Pin 21 ) ( Pin 23 )	11.5	12.5	13.5	μs
3	VD output pulse width 2	t <sub>v2</sub>	Measures the width of the VD output pulse for CS (composite sync) input. Input signal B (tw = 12.5μs)	VD ( Pin 21 ) ( Pin 23 )	6.5	10	12.5	μs
4	VD output pulse width 3	t <sub>v3</sub>	Measures the width of the VD output pulse for VIDEO IN (sync-on video) input. Input signal C (tw = 12.5μs).	VD ( Pin 21 ) ( Pin 23 )	6.5	10	12.5	μs
5	HD output voltage	E <sub>HD</sub>	Measures the height of the HD output wave for CS (composite sync) input. Input signal D (tw = 0.65μs). 5V output power supply, R <sub>4</sub> = 2.2kΩ.	HD ( Pin 18 ) ( Pin 20 )	(H level) 4.85 (L level) 0	5.0 0.15	5.0 0.4	V V
6	HD output pulse width 1	th <sub>1</sub>	Measures the width of the HD output pulse for CS (composite sync) input. Input signal B (tw = 0.65μs).	HD ( Pin 18 ) ( Pin 20 )	0.5	0.65	0.8	μs
7	HD output pulse width 2	th <sub>2</sub>	Measures the width of the HD output pulse for VIDEO IN (sync-on video) input. Input signal C (tw = 0.65μs).	HD ( Pin 18 ) ( Pin 20 )	0.5	0.65	0.8	μs
8	Clamp pulse output voltage	E <sub>CP</sub>	Measures the height of the clamp pulse output wave for CS (composite sync) input. Input signal B (tw = 0.65μs). 5V output power supply, R <sub>15</sub> = 2.2kΩ.	CLAMP ( Pin 10 )	(H level) 4.85 (L level) 0	5.0 0.15	5.0 0.4	V V
9	Clamp pulse output pulse width 1	t <sub>c1</sub>	Measures the width of the clamp pulse output pulse for CS (composite sync) input. Input signal B. Connects Pin 9 to GND through a 560pF capacitor and a 12kΩ resistance in parallel.	CLAMP ( Pin 10 )	—	0.25	—	μs
10	Clamp pulse output pulse width 2	t <sub>c2</sub>	Measures the width of the clamp pulse output pulse for VIDEO IN (sync-on video) input. Input signal C. Connects Pin 9 to GND through a 10nF capacitor and a 12kΩ resistance in parallel.	CLAMP ( Pin 10 )	3.7	4.1	4.5	μs

(Ta = 25°C, Vcc = 12V, See the Electrical Characteristics Test Circuit)

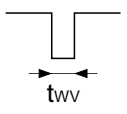
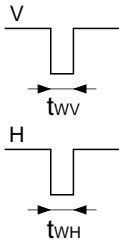
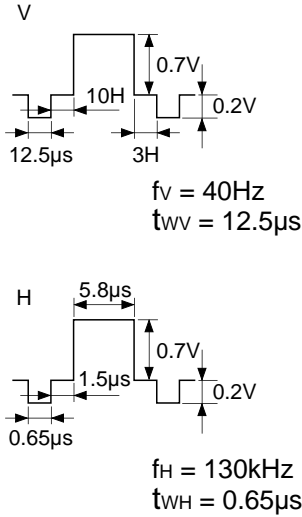
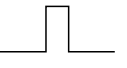
No.	Item	Symbol	Measurement description	Measurement point	Min.	Typ.	Max.	Unit
11	PVC voltage 1	V <sub>PV1</sub>	The voltage integral of the vertical polarity discrimination circuit for VS (vertical separate sync) input. Input signal F (negative logic).	PVC (Pin 2)	—	0.3	—	V
12	PVC voltage 2	V <sub>PV2</sub>	The voltage integral of the vertical polarity discrimination circuit for VS (vertical separate sync) input. Input signal G (positive logic).	PVC (Pin 2)	—	3.4	—	V
13	PHC voltage 1	V <sub>PH1</sub>	The voltage integral of the vertical polarity discrimination circuit for CS (composite sync) input. Input signal H (negative logic).	PHC (Pin 5)	—	0.4	—	V
14	PHC voltage 2	V <sub>PH2</sub>	The voltage integral of the vertical polarity discrimination circuit for CS (composite sync) input. Input signal I (positive logic).	PHC (Pin 5)	—	3.4	—	V
15	EVC voltage 1	V <sub>EV1</sub>	Measures the voltage of the vertical ramp waveform generator for VS (vertical separate sync) input. Input signal A.	EVC (Pin 3)	—	7.9	—	V
16	EVC voltage 2	V <sub>EV2</sub>	Measures the voltage of the vertical ramp waveform generator for VS (vertical separate sync) input. No input signal.	EVC (Pin 3)	—	4.3	—	V
17	EHC voltage 1	V <sub>EH1</sub>	Measures the sync existence discrimination voltage for CS (composite sync) input. Input signal J.	EHC (Pin 6)	—	4.8	—	V
18	EHC voltage 2	V <sub>EH2</sub>	Measures the sync existence discrimination voltage for CS (composite sync) input. No input signal.	EHC (Pin 6)	—	3.0	—	V
19	HD delay 1	td <sub>1</sub>	Measures the delay difference between CS and HD for CS (composite sync) input. The time from the CS (negative polarity) fall time (50%) to the HD output rise time (50%). Input signal B.	HD (Pin 18) (Pin 20)	120	190	250	ns
20	HD delay 2	td <sub>2</sub>	Measures the delay difference between CS and HD for CS (composite sync) input. The time from the CS (positive polarity) rise time (50%) to the HD output rise time (50%). Input signal D.	HD (Pin 18) (Pin 20)	120	205	260	ns



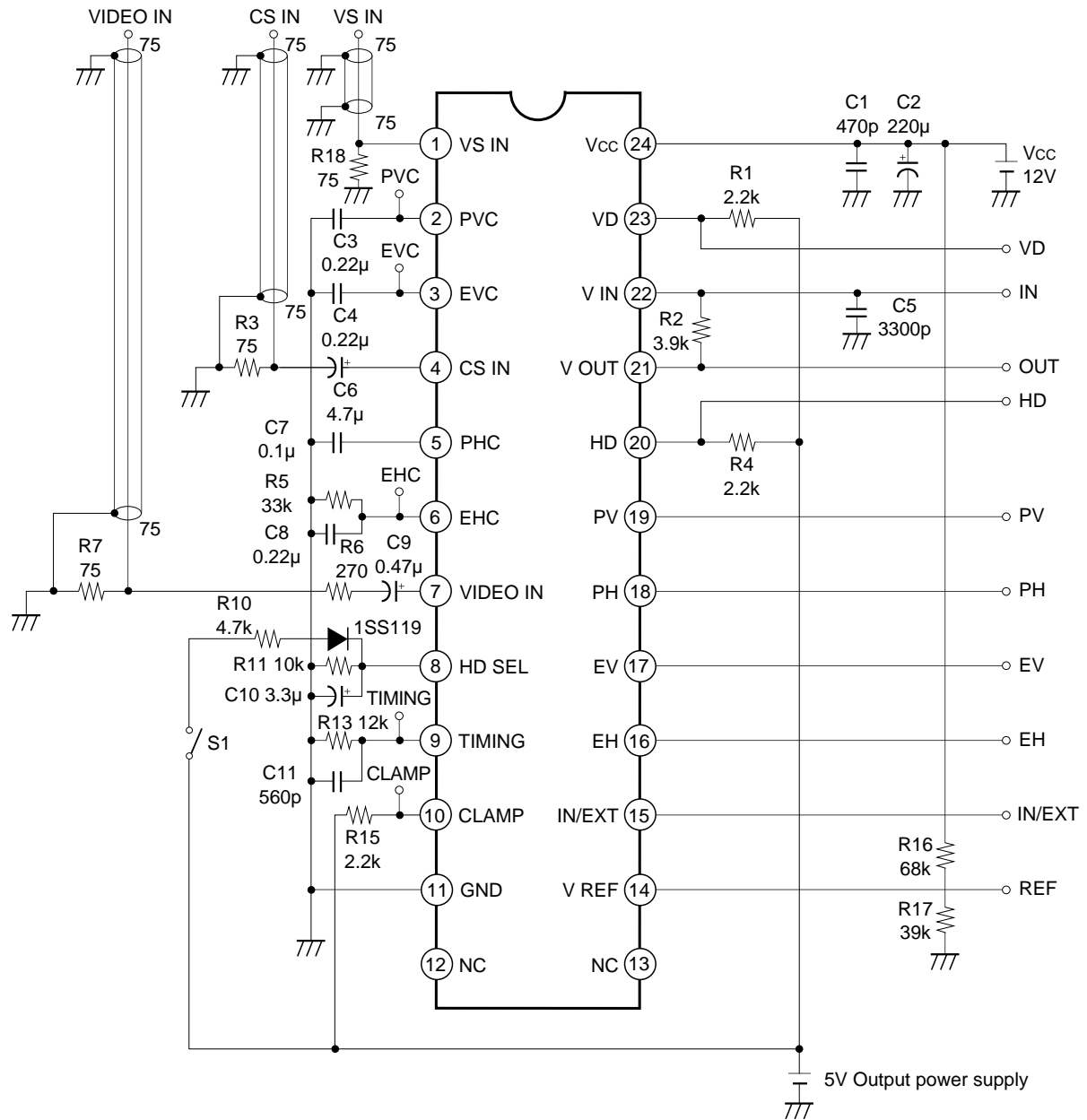
(Ta = 25°C, Vcc = 12V, See the Electrical Characteristics Test Circuit)

No.	Item	Symbol	Measurement description	Measurement point	Min.	Typ.	Max.	Unit
21	HD delay 3	td <sub>3</sub>	Measures the delay difference between the input signal sync and HD for VIDEO IN (sync-on video) input. The time from the input sync fall time (50%) to the HD output rise time (50%). Input signal C.	HD (Pin 18) (Pin 20)	110	180	240	ns
22	HD delay difference	thd	Compares the delay differences from both the VIDEO IN (sync-on video) input and the CS (composite sync) input to the HD output. (Compares Measurement No. 19 to 21).	HD (Pin 18) (Pin 20)	—	25	40	ns
23	Clamp pulse delay 1	tcd <sub>1</sub>	Measures the delay difference between HD and the clamp pulse for CS (composite sync) input. The time from the HD output fall time (50%) to the clamp pulse output rise time (50%). Input signal B.	CLAMP (Pin 10)	110	140	180	ns
24	Clamp pulse delay 2	tcd <sub>2</sub>	Measures the delay difference between HD and the clamp pulse for CS (composite sync) input. The time from the HD output fall time (50%) to the clamp pulse output rise time (50%). Input signal D.	CLAMP (Pin 10)	110	140	180	ns
25	Clamp pulse delay 3	tcd <sub>3</sub>	Measures the delay difference between HD and the clamp pulse for VIDEO IN (sync-on video) input. The time from the HD output fall time (50%) to the clamp pulse output rise time (50%). Input signal C.	CLAMP (Pin 10)	90	130	170	ns
26	Logic output voltage High	Q <sub>H</sub>	Polarity and existence information output of the sync signal. Measures the High level voltage under no load condition.	Q <sub>1</sub> to Q <sub>4</sub> (Pin 13 to 17) (Pin 15 to 19)	3.5	4.5	5.0	V
27	Logic output voltage Low	Q <sub>L</sub>	Polarity and existence information output of the sync signal. Measures the Low level voltage under no load condition.	Q <sub>1</sub> to Q <sub>4</sub> (Pin 13 to 17) (Pin 15 to 19)	0	0.12	0.4	V
28	Current consumption	I <sub>cc</sub>	Vcc = 12V, measures the current consumption for no input signal.	V <sub>cc</sub> (Pin 22) (Pin 24)	18	27	35	mA

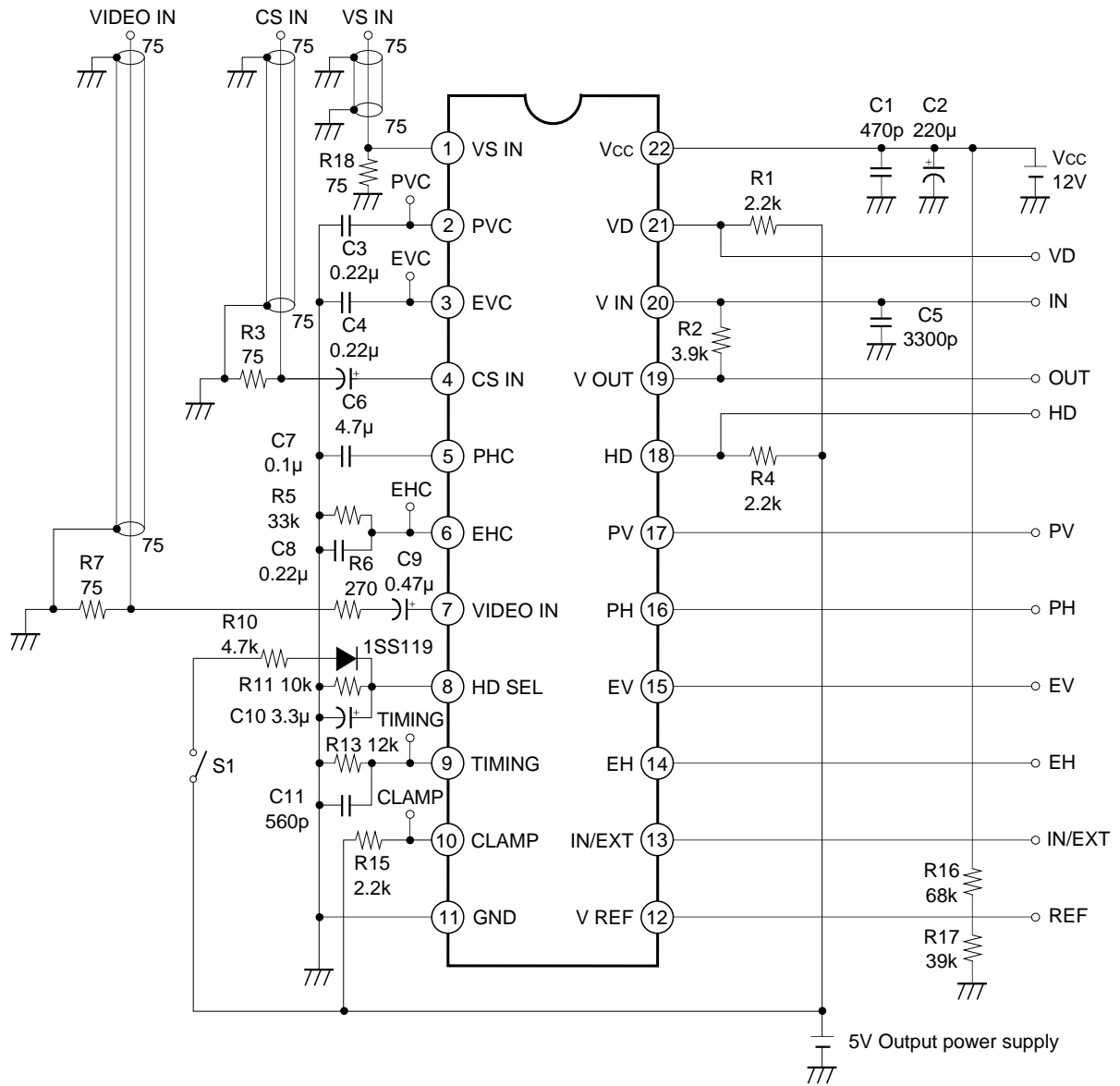
Signal Source Types

Signal	Item	V. SYNC IN (Pin 1)	Composite SYNC IN (Pin 4)	VIDEO IN (Pin 7)
A	1, 2, 15	 <p><math>f_v = 40\text{Hz}</math>  <math>t_{wv} = 12.5\mu\text{s}</math>                      Negative logic                      1Vp-p</p>		
B	3, 6, 8, 9, 19, 23		 <p><math>f_v = 40\text{Hz}</math>  <math>t_{wv} = 12.5\mu\text{s}</math>                      Negative logic                      1Vp-p</p> <p><math>f_H = 130\text{kHz}</math>  <math>t_{wH} = 0.65\mu\text{s}</math>                      Negative logic                      1Vp-p</p>	
C	4, 7, 10, 21, 25			 <p><math>f_v = 40\text{Hz}</math>  <math>t_{wv} = 12.5\mu\text{s}</math></p> <p><math>f_H = 130\text{kHz}</math>  <math>t_{wH} = 0.65\mu\text{s}</math></p>
D	5, 20, 24		<p><math>f_H = 130\text{kHz}</math>  <math>t_{wH} = 0.65\mu\text{s}</math>                      Positive logic 1Vp-p</p>	
F	11	<p><math>f_v = 200\text{Hz}</math>  <math>t_{wv} = 0.3\text{ms}</math>                      Negative logic 5Vp-p</p>		
G	12	 <p><math>f_v = 200\text{Hz}</math>  <math>t_{wv} = 0.3\text{ms}</math>                      Positive logic                      5Vp-p</p>		
H	13		<p><math>f_H = 130\text{kHz}</math>  <math>t_{wv} = 0.65\mu\text{s}</math>                      Negative logic 5Vp-p</p>	
I	14		<p><math>f_H = 130\text{kHz}</math>  <math>t_{wv} = 0.65\mu\text{s}</math>                      Positive logic 5Vp-p</p>	
J	17		<p><math>f_H = 15\text{kHz}</math>  <math>t_{wv} = 3.3\mu\text{s}</math>                      Negative logic 1Vp-p</p>	

Electrical Characteristics Test Circuit (SSOP)



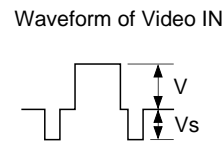
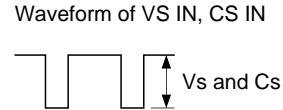
Electrical Characteristics Test Circuit (SDIP)



**Description of Operation**

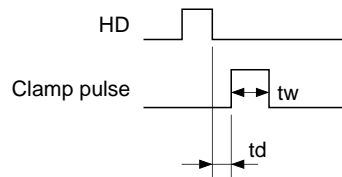
**Input Signals**

- VS IN (Pin 1)  
 fv: 40 to 200Hz  
 Vs: 1 to 5Vp-p (positive/negative polarity)  
 1.5 to 5Vp-p (positive/negative polarity, for capacitor input)
- CS IN (Pin 4)  
 fh: 15k to 130kHz  
 Vs: 1 to 5Vp-p (positive/negative polarity)
- Video IN (Pin 7)  
 fh: 15k to 130kHz  
 fv: 40 to 200Hz  
 V: 0 to 2.1Vp-p  
 Vs: 0.2 to 0.6Vp-p



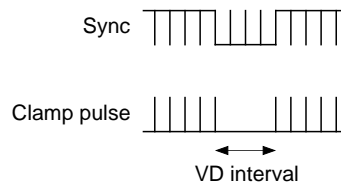
**Clamp Pulse Output**

- The clamp pulse (Pin 10) is output under the conditions described in 1 and 2 below.  
 When output with Pin 10 operating as an open collector, its polarity is positive.  
 td: 130 to 140ns delay to HD output  
 tw: Clamp pulse width is variable from 200ns to 3µs depending on the capacitor value connected to Pin 9.



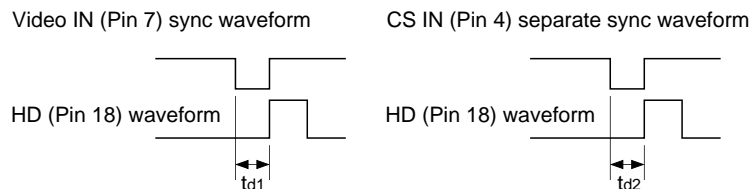
<Conditions>

- 1) Clamp pulse is not output during the VD interval for CS IN or Video IN.



- 2) Clamp pulse is output during the VD interval for HS and VS separate sync.

**I/O Delay Time Difference**



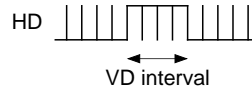
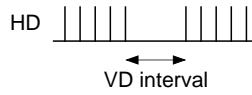
- td<sub>1</sub>: Delay time between Video IN (Pin 7) input and HD (Pin 18) output
- td<sub>2</sub>: Delay time between CS IN (Pin 4) input and HD (Pin 18) output
- td<sub>1</sub>, td<sub>2</sub> = 200 to 260ns
- | td<sub>1</sub> - td<sub>2</sub> | = to 30ns to

**HD Selection Function**

HD SEL

Low: The VD interval HD is not output.

High: The VD interval HD is output as is.



**Mode Matrix of Sync Polarity Discrimination Signal**

CS IN (Pin 4)	VS IN (Pin 1)	EH out (Pin 14)	EV out (Pin 15)	PH out (Pin 16)	PV out (Pin 17)	Sync IN/EXT (Pin 13)
HD, COMP (positive polarity)	No signal	H	L	L	L	H
	VD (positive)	H	H	L	L	H
	VD (negative)	H	H	L	H	H
HD, COMP (negative polarity)	No signal	H	L	H	L	H
	VD (positive)	H	H	H	L	H
	VD (negative)	H	H	H	H	H
No signal	No signal	L	L	L	L	L
	VD (positive)	L	H	L	L	H
	VD (negative)	L	H	L	H	H

Low level: 0 to 0.2V, High level: 4.5 to 4.7V

**I/O Matrix**

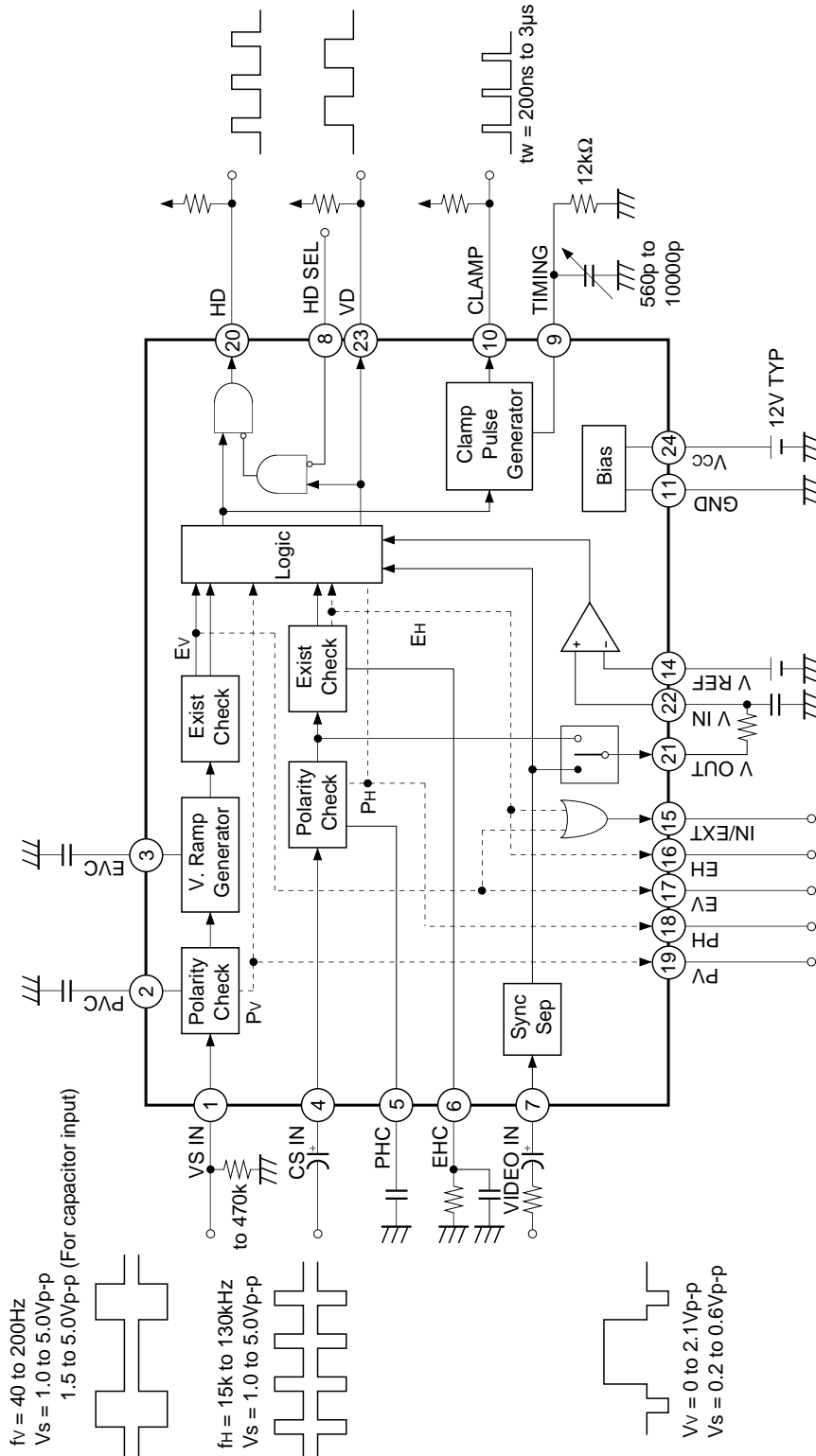
VS IN	CS IN	VIDEO IN	VD OUT	HD OUT
O	O	*	VS	CS
—	O	*	CS	CS
—	—	O	VIDEO	VIDEO
—	—	—	(VIDEO)	(VIDEO)

O: signal input

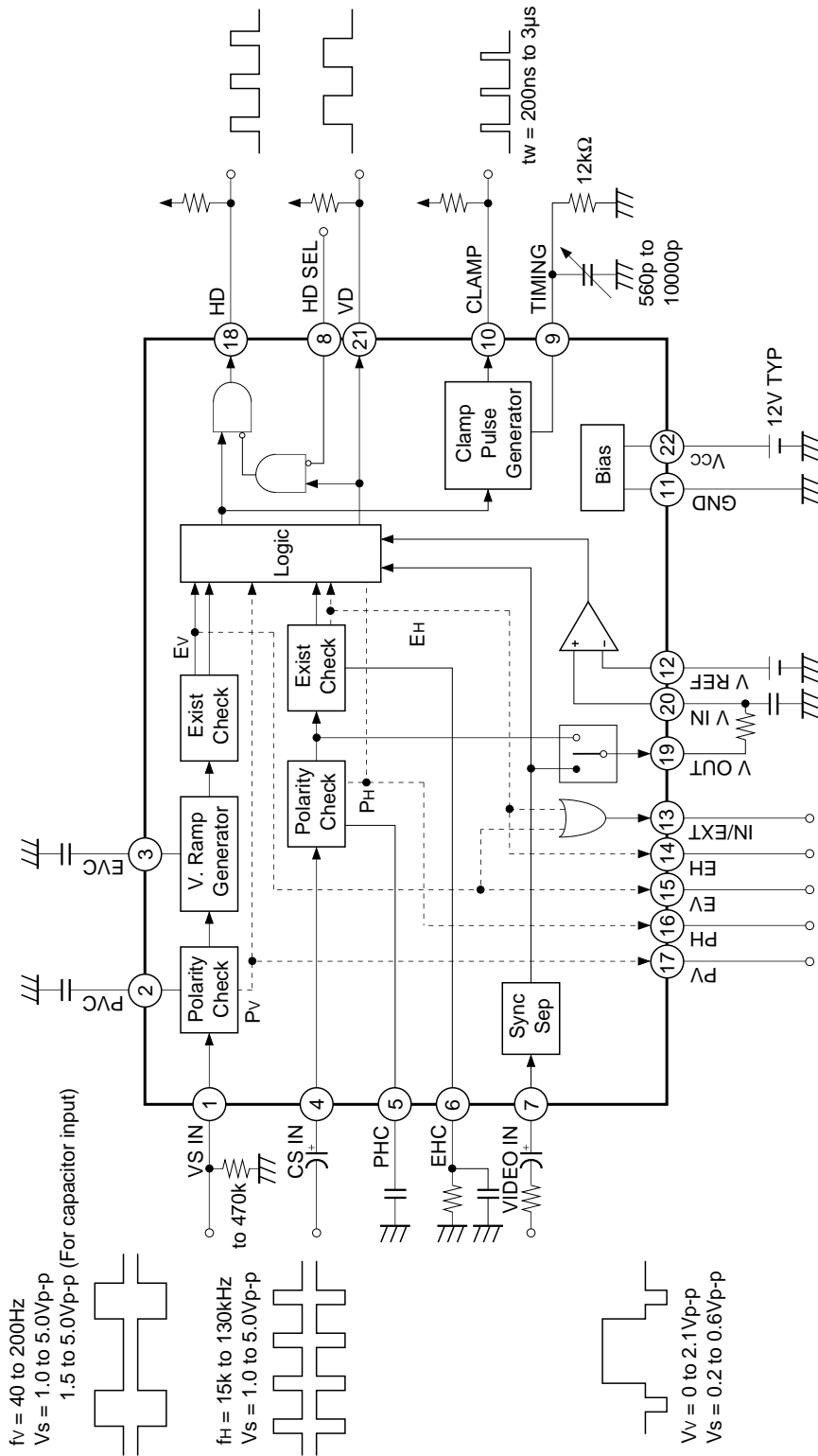
—: no signal

\* : unrelated to input signal

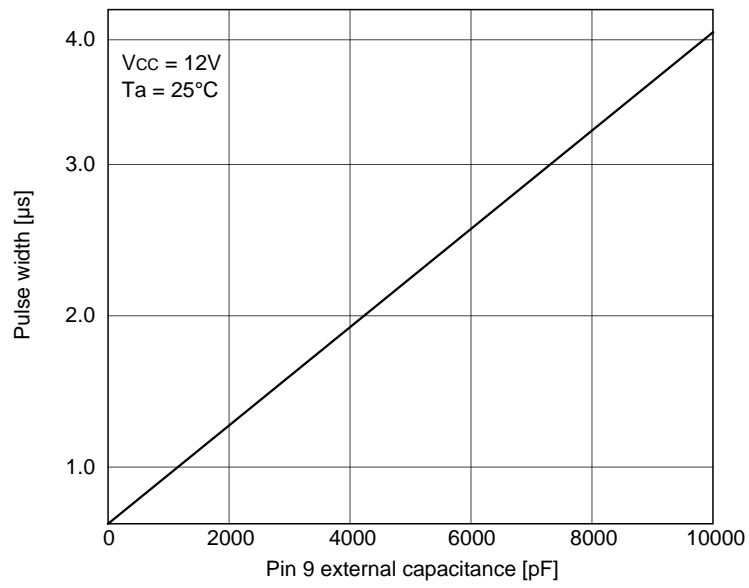
Operation and Waveforms (SSOP)



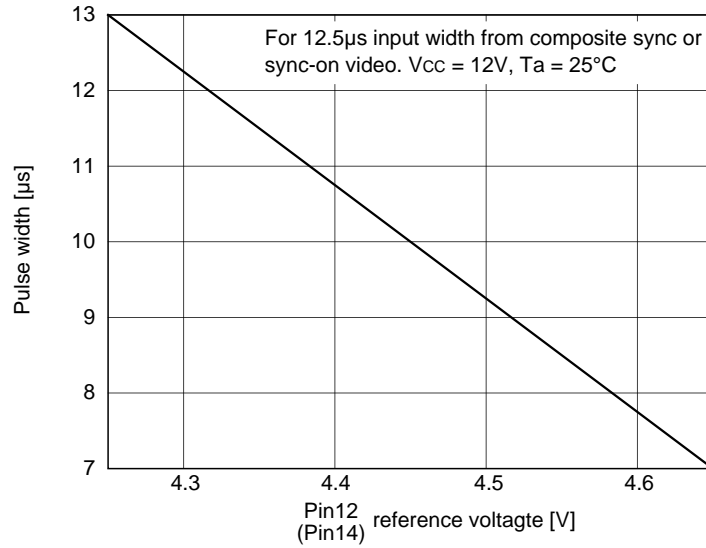
Operation and Waveforms (SDIP)





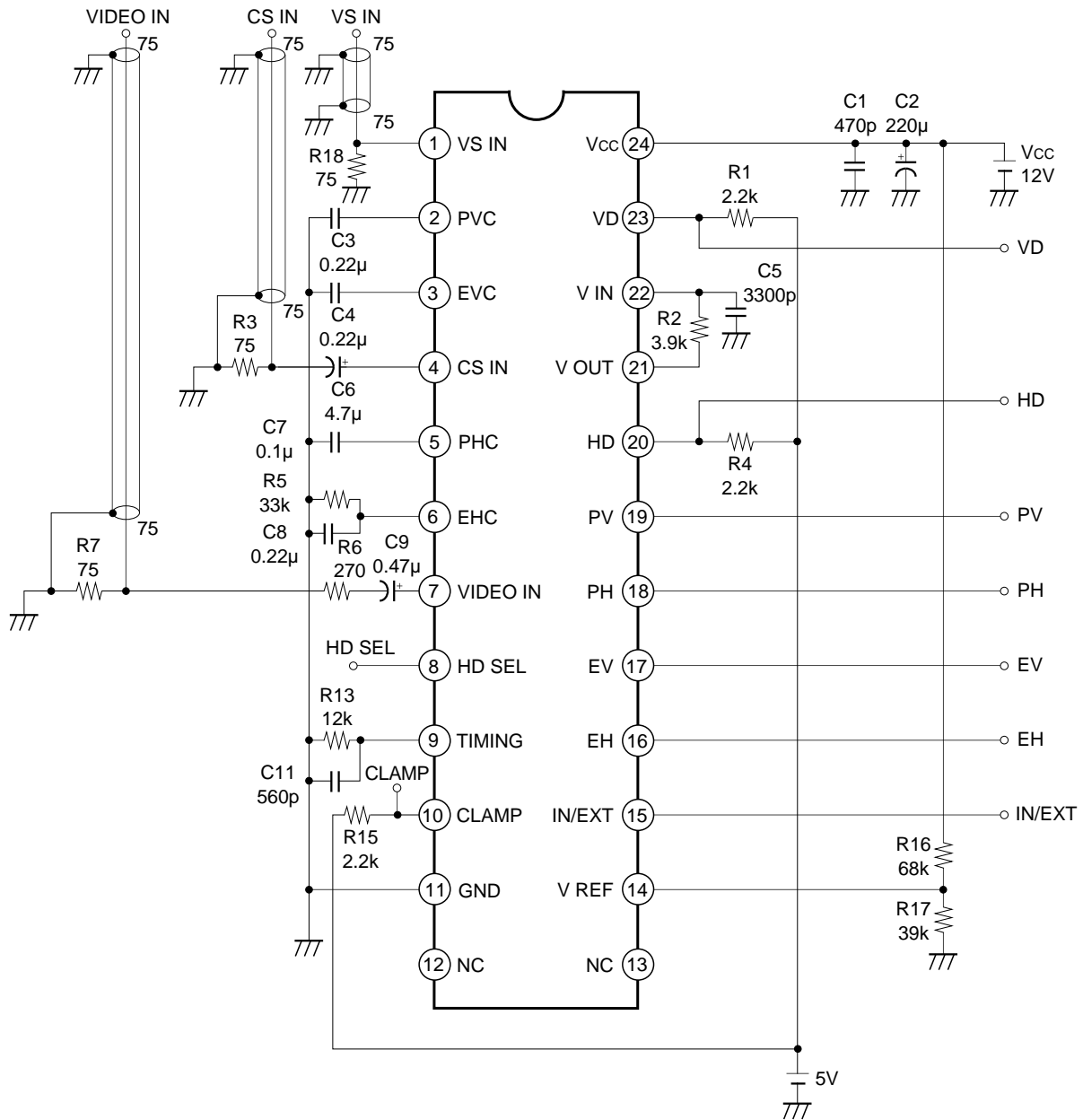


**Fig. 1. Clamp pulse output pulse width characteristics**

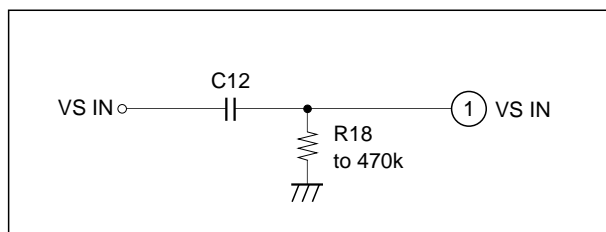


**Fig. 2. VD output pulse width characteristics**

Application Circuit (SSOP)



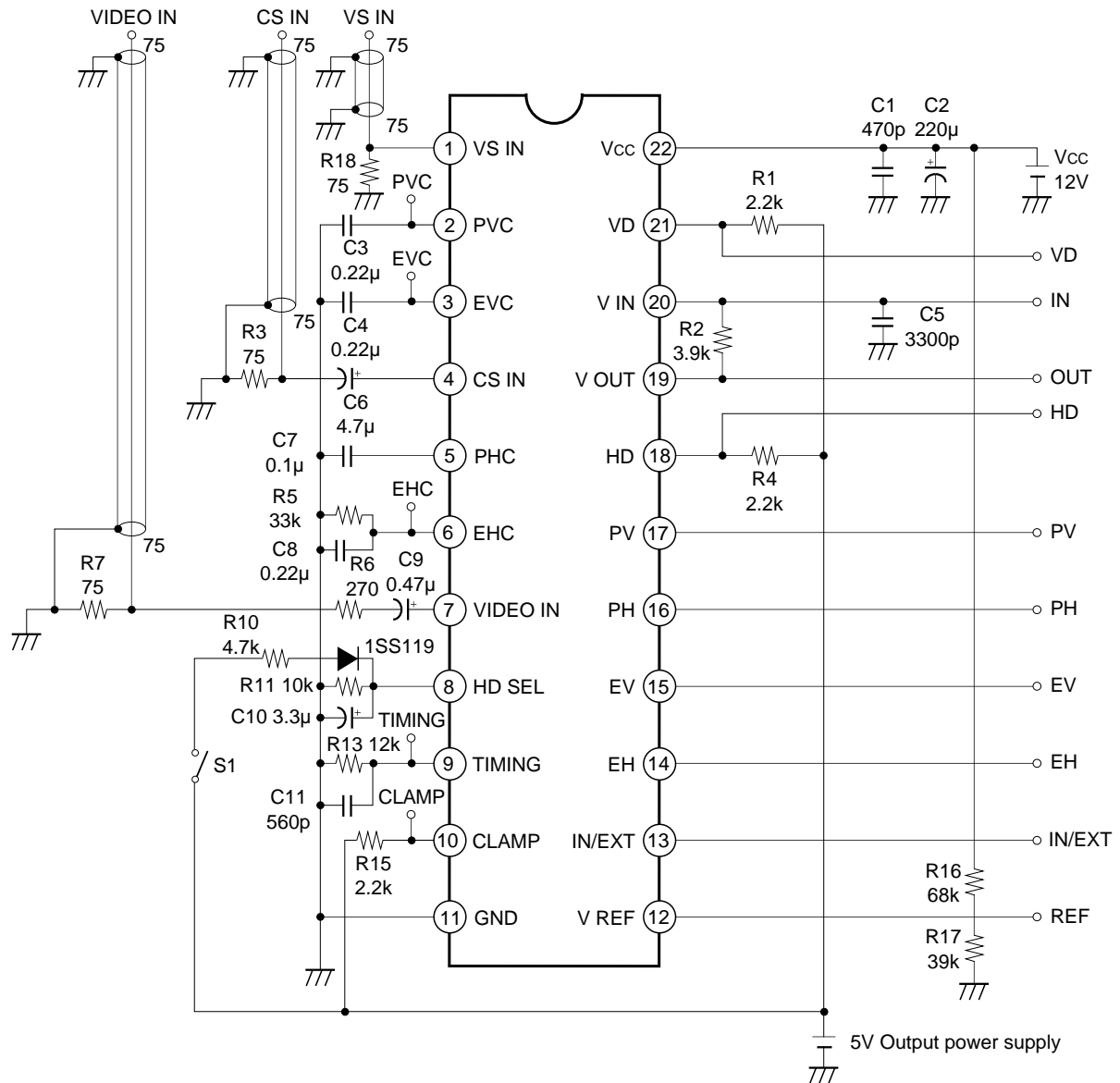
**Note)** Connect a resistance of 470kΩ or less between Pin 1 and GND when inputting to VS IN (Pin 1) through a capacitor. Consider sags in determining the constant setting. Make input signal amplitude 1.5 to 5.0Vp-p for capacitor input.



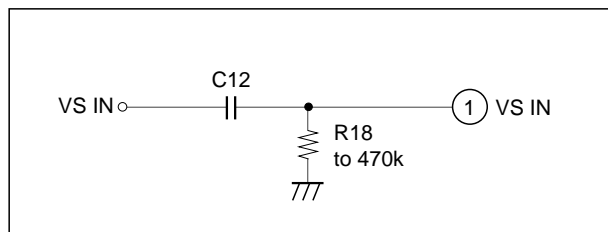
Application circuit with VS IN (Pin 1) capacitor input

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Application Circuit (SDIP)



**Note)** Connect a resistance of 470kΩ or less between Pin 1 and GND when inputting to VS IN (Pin 1) through a capacitor. Consider sags in determining the constant setting. Make input signal amplitude 1.5 to 5.0Vp-p for capacitor input.



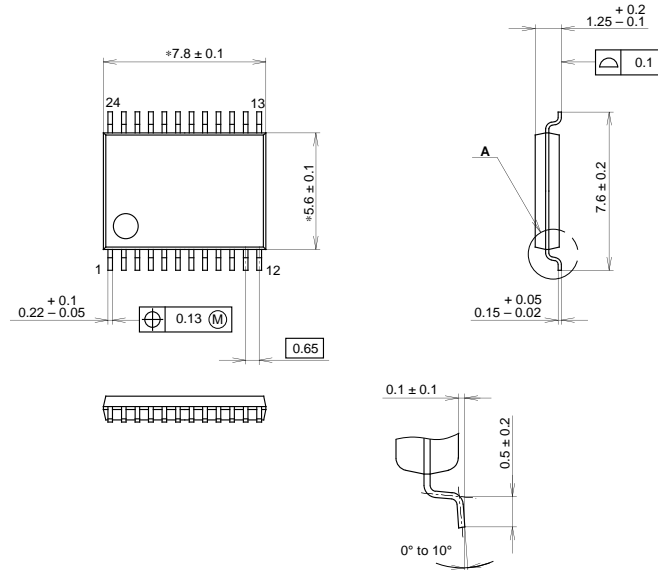
Application circuit with VS IN (Pin 1) capacitor input

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Package Outline Unit: mm

CXA1616N

24PIN SSOP(PLASTIC)



NOTE: Dimensions "\*" does not include mold protrusion.

DETAIL A

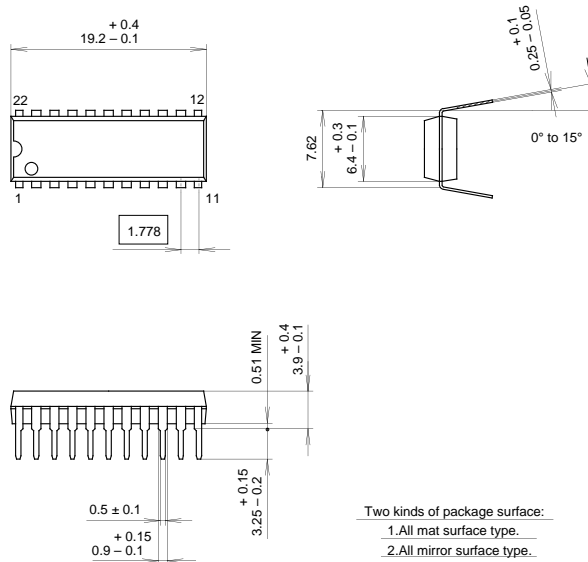
PACKAGE STRUCTURE

SONY CODE	SSOP-24P-L01
EIAJ CODE	SSOP024-P-0056
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.1g

CXA1616S

22PIN SDIP (PLASTIC)



Two kinds of package surface:  
 1. All mat surface type.  
 2. All mirror surface type.

PACKAGE STRUCTURE

SONY CODE	SDIP-22P-01
EIAJ CODE	SDIP022-P-0300
JEDEC CODE	

MOLDING COMPOUND	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.95g