PRELIMINARY

Integrated Circuit Systems, Inc.

ICS843404

LVCMOS/CRYSTAL-TO-3.3V LVPECL AND LVDS CLOCK GENERATOR

GENERAL DESCRIPTION

The ICS843404 is a low phase noise Fibre Channel Clock Generator and is a member of the HiPerClockS™ family of high performance clock solutions from ICS. The device provides two banks of 1 LVPECL output per bank and one bank of 2 LVDS outputs. Each bank can be independently set by using their respective frequency select pins for the following output frequencies: 318.75MHz, 212.5MHz, 159.375MHz or 106.25MHz, using a 25.5MHz 18pF parallel resonant crystal. The ICS843404 can also be driven from a 25.5MHz single-ended reference clock. For system debug or test purposes, the PLL can be bypassed using the VCO_SEL pin.

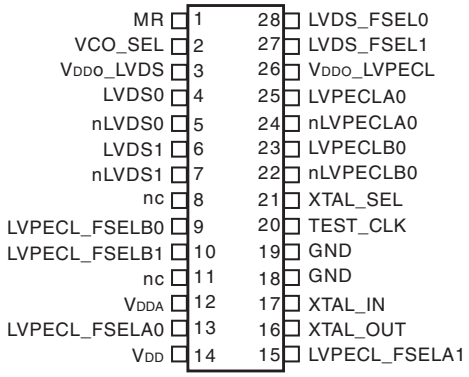
FEATURES

- Three banks of outputs: 1 bank of 2 LVDS outputs and 2 banks of 1 LVPECL output
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended reference clock input
- 4 independently selectable output frequency on each bank: 318.7MHz, 212.5MHz, 159.375MHz and 106.25MHz
- Maximum output frequency: 318.75MHz
- Crystal input frequency: 25.5MHz
- V_{DDO}_LVPECL can be set for 3.3V or 2.5V, allowing the device to generate 3.3V or 2.5V LVPECL levels
- RMS phase jitter at 106.25MHz, using a 25.5MHz crystal (637KHz to 10Mhz intergration): 4.82ps (typical)
- Phase noise @ 106.25MHz

Offset	Noise Power
100Hz	-84.6 dBc/Hz
1KHz	-105.7 dBc/Hz
10KHz	-122.3 dBc/Hz
100KHz	-125.9 dBc/Hz

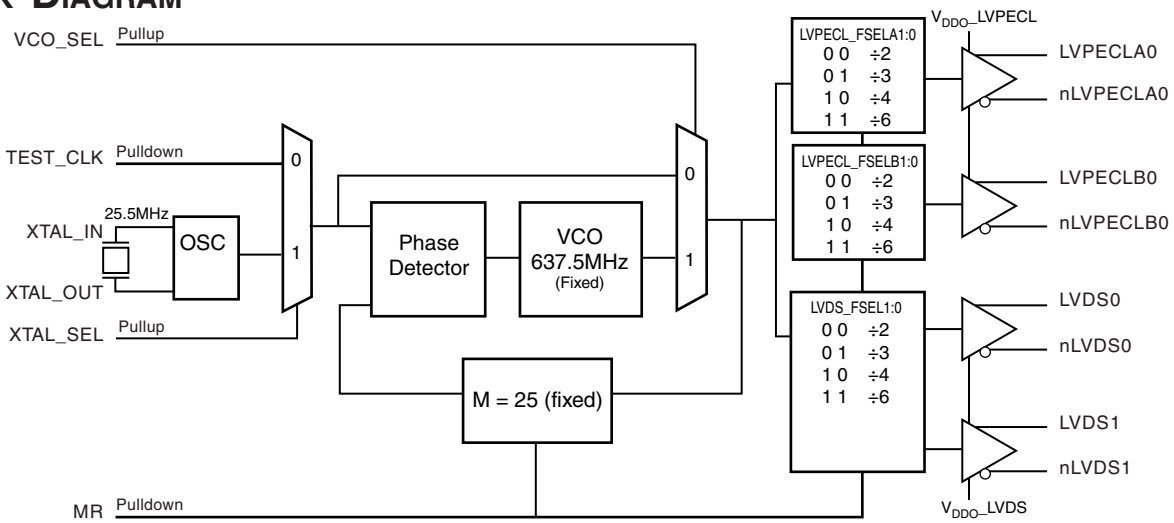
- Supply voltage modes:
  - $V_{DD} = V_{DDA} = 3.3V$
  - $V_{DDO_}$LVPECL = 3.3V or 2.5V
  - $V_{DDO_}$LVDS = 3.3V
- 0°C to 70°C ambient operating temperature
- Lead-Free package available
- Industrial termperature information available upon request

PIN ASSIGNMENT



ICS843404
28-Lead TSSOP, 173-MIL
4.4mm x 9.7mm x 0.92mm
body package
G Package
Top View

BLOCK DIAGRAM



The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs LVPECLx/LVDSx to go low and the inverted outputs nLVPECLx/nLVDSx to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
2	VCO_SEL	Input	Pullup	VCO select pin. When HIGH, PLL is enabled. When LOW, PLL is in Bypass mode. LVCMOS/LVTTL interface levels.
3	V_{DDO}_LVDS	Power		Output supply pin for LVDS outputs.
4, 5	LVDS0, nLVDS0	Output		Differential output pair. LVDS interface levels.
6, 7	LVDS1, nLVDS1	Output		Differential output pair. LVDS interface levels.
8, 11	nc	Unused		No connect.
9	LVPECL_FSELB0	Input	Pulldown	Frequency select pin for LVPECLB outputs. See Table 3B. LVCMOS/LVTTL interface levels.
10	LVPECL_FSELB1	Input	Pullup	Frequency select pin for LVPECLB outputs. See Table 3B. LVCMOS/LVTTL interface levels.
12	V_{DDA}	Power		Analog supply pin.
13	LVPECL_FSELA0	Input	Pulldown	Frequency select pin for LVPECLA outputs. See Table 3B. LVCMOS/LVTTL interface levels.
14	V_{DD}	Power		Core supply pin.
15	LVPECL_FSELA1	Input	Pullup	Frequency select pin for LVPECLA outputs. See Table 3B. LVCMOS/LVTTL interface levels.
16, 17	XTAL_OUT, XTAL_IN	Input		Parallel resonant crystal interface. XTAL_IN is the input, XTAL_OUT is the output.
18, 19	GND	Power		Negative supply pin.
20	TEST_CLK	Input	Pulldown	LVCMOS/LVTTL clock input.
21	XTAL_SEL	Input	Pullup	Selects between crystal or TEST_CLK inputs as the the PLL Reference source. Selects XTAL inputs when HIGH. Selects TEST_CLK when LOW. LVCMOS/LVTTL interface levels.
22, 23	nLVPECLB0, LVPECLB0	Output		Differential output pair. LVPECL interface levels.
24, 25	nLVPECLA0, LVPECLA0	Ouput		Differential output pair. LVPECL interface levels.
26	V_{DDO}_LVPECL	Power		Output supply pin for LVPECL outputs.
27, 28	LVDS_FSEL1, LVDS_FSEL0	Input	Pulldown	Frequency select pins for LVDS outputs. See Table 3A. LVCMOS/LVTTL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ

TABLE 3A. LVDS FREQUENCY SELECT FUNCTION TABLE

Inputs			LVDS Output Frequency (MHz) (25.5MHz Crystal)
LVDS_FSEL1	LVDS_FSEL0	LVDS Output Divider	
0	0	2	318.75 (default)
0	1	3	212.5
1	0	4	159.375
1	1	6	106.25

TABLE 3B. LVPECLA0 FREQUENCY SELECT FUNCTION TABLE

Inputs			LVPECLA0 Output Frequency (MHz) (25.5MHz Crystal)
LVPECL_FSELA1	LVPECL_FSELA0	LVPECLA0 Output Divider	
0	0	2	318.75
0	1	3	212.5
1	0	4	159.375 (default)
1	1	6	106.25

TABLE 3C. LVPECLB0 FREQUENCY SELECT FUNCTION TABLE

Inputs			LVPECLB0 Output Frequency (MHz) (25.5MHz Crystal)
LVPECL_FSELB1	LVPECL_FSELB0	LVPECLB0 Output Divider	
0	0	2	318.75
0	1	3	212.5
1	0	4	159.375 (default)
1	1	6	106.25

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O (LVPECL Outputs)	
Continuous Current	50mA
Surge Current	100mA
Outputs, I_O (LVDS Outputs)	
Continuous Current	10mA
Surge Current	15mA
Package Thermal Impedance, θ_{JA}	49.8°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. LVPECL POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDO}$ = 3.3V±5%, V_{DDA} = 2.9V TO 3.465V, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		2.9	3.3	3.465	V
V_{DDO_LVPECL}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			TBD		mA
I_{DDA}	Analog Supply Current			TBD		mA
I_{DDO_LVPECL}	Output Supply Current			TBD		mA

TABLE 4B. LVPECL POWER SUPPLY DC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDA} = 2.9V TO 3.465V, V_{DDO} = 2.5V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		2.9	3.3	3.465	V
V_{DDO_LVPECL}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current			TBD		mA
I_{DDA}	Analog Supply Current			TBD		mA
I_{DDO_LVPECL}	Output Supply Current			TBD		mA

TABLE 4C. LVDS POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDO}$ = 3.3V±5%, V_{DDA} = 2.9V TO 3.465V, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		2.9	3.3	3.465	V
V_{DDO_LVDS}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			TBD		mA
I_{DDA}	Analog Supply Current			TBD		mA
I_{DDO_LVDS}	Output Supply Current			TBD		mA

TABLE 4D. LVCMOS / LVTTL DC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 3.3V±5% OR 2.5V±5%, V_{DDA} = 2.9V TO 3.465V, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	VCO_SEL, XTAL_SEL, LVPECL_FSELA0:F_SELA1, LVPECL_FSELB0:F_SELB1 LVDS_FSEL0:F_SEL1, MR		-0.3		0.8	V
		TEST_CLK		-0.3		1.3	V
I_{IH}	Input High Current	TEST_CLK, MR, LVPECL_FSELA0, LVPECL_FSELB0, LVDS_FSEL0, LVDS_FSEL1	V_{DD} = V_{IN} = 3.465V,			150	µA
		LVPECL_FSELA1, LVPECL_FSELB1, VCO_SEL, XTAL_SEL	V_{DD} = V_{IN} = 3.465V,	5			µA
I_{IL}	Input Low Current	TEST_CLK, MR, LVPECL_FSELA0, LVPECL_FSELB0, LVDS_FSEL0, LVDS_FSEL1	V_{DD} = 3.465V, V_{IN} = 0V,	-5			µA
		LVPECL_FSELA1, LVPECL_FSELB1, VCO_SEL, XTAL_SEL	V_{DD} = 3.465V, V_{IN} = 0V,	-150			µA

TABLE 4E. LVPECL DC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 3.3V±5% OR 2.5V±5%, V_{DDA} = 2.9V TO 3.465V, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{DDO} - 1.4		V_{DDO} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{DDO} - 2.0		V_{DDO} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		0.9	V

NOTE 1: Outputs terminated with 50Ω to V_{DDO} - 2V.

TABLE 4F. LVDS DC CHARACTERISTICS, V_{DD} = V_{DDO} = 3.3V±5%, V_{DDA} = 2.9V TO 3.465V, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			350		mV
ΔV_{OD}	V_{OD} Magnitude Change			4		mV
V_{OS}	Offset Voltage			1.35		V
ΔV_{OS}	V_{OS} Magnitude Change			5		mV

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25.5		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

NOTE: Characterized using an 18pf parallel resonant crystal.

TABLE 6A. LVPECL AC CHARACTERISTICS, $V_{DD} = V_{DDO}$ = 3.3V±5%, V_{DDA} = 2.9V TO 3.465V, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				318.75	MHz
*t*sk(b)	Bank Skew; NOTE 1			15		ps
*t*sk(o)	Output Skew; NOTE 2, 3			TBA		ps
*t*jit(Ø)	RMS Phase Jitter, (Random); NOTE 4	318.75MHz (12KHz - 20MHz)		5.64		ps
		212.5MHz (1.274MHz - 20MHz)		2.82		ps
		159.375MHz (12k - 20MHz)		5.77		ps
		106.25MHz (637KHz - 10MHz)		4.82		ps
t_L	PLL Lock Time			1		ms
t_R / t_F	Output Rise/Fall Time	20% to 80%		400		ps
odc	Output Duty Cycle			50		%

NOTE 1: Defined as skew within a bank of ourputs at the same voltages and with equal load conditions.
NOTE 2: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at the differential cross point.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Please refer to the Phase Noise Plots.

TABLE 6B. LVPECL AC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDA} = 2.9V TO 3.465V, V_{DDO} = 2.5V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				318.75	MHz
*t*sk(b)	Bank Skew; NOTE 1			15		ps
*t*sk(o)	Output Skew; NOTE 2, 3			TBA		ps
*t*jit(Ø)	RMS Phase Jitter, (Random); NOTE 4	318.75MHz (12KHz - 20MHz)		5.03		ps
		212.5MHz (1.274MHz - 20MHz)		2.73		ps
		159.375MHz(12k - 20MHz)		4.60		ps
		106.25MHz (637KHz - 10MHz)		3.96		ps
t_L	PLL Lock Time			1		ms
t_R / t_F	Output Rise/Fall Time	20% to 80%		400		ps
odc	Output Duty Cycle			50		%

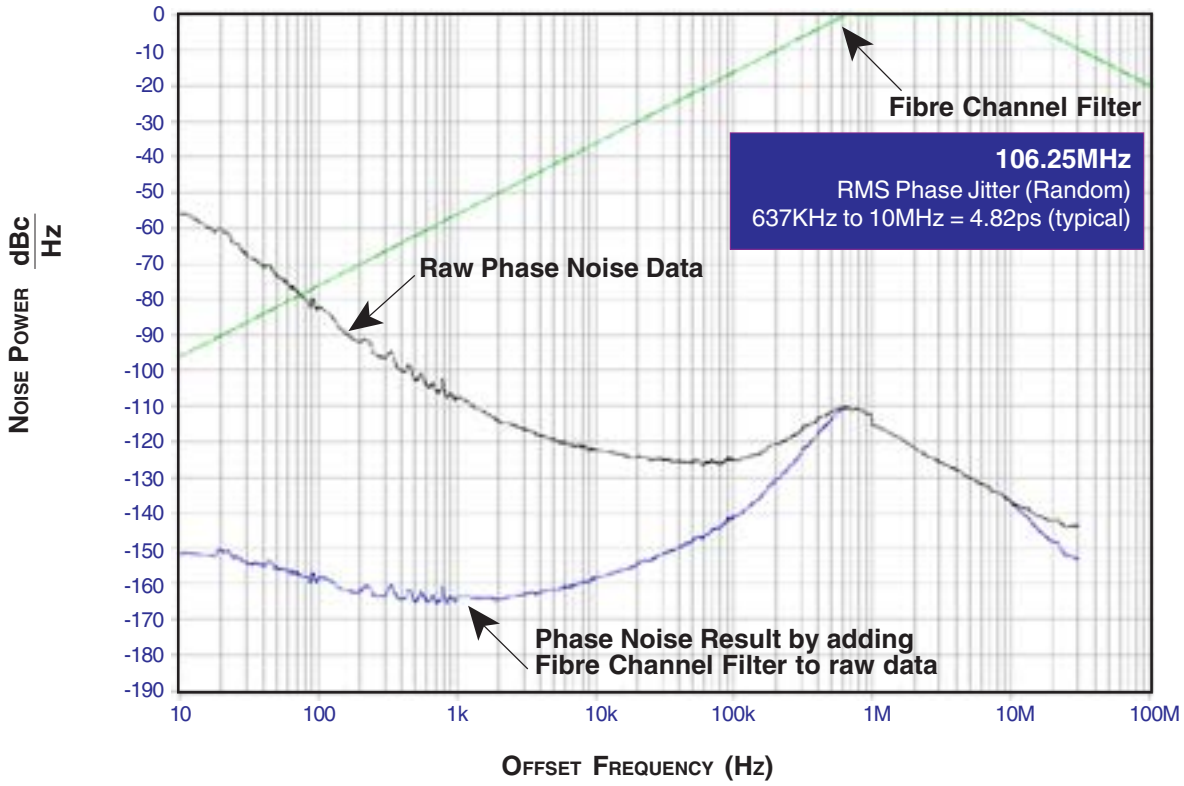
See NOTES 1 through 4 above.

TABLE 6C. LVDS AC CHARACTERISTICS, $V_{DD} = V_{DDO}$ = 3.3V±5%, V_{DDA} = 2.9V TO 3.465V, TA = 0°C TO 70°C

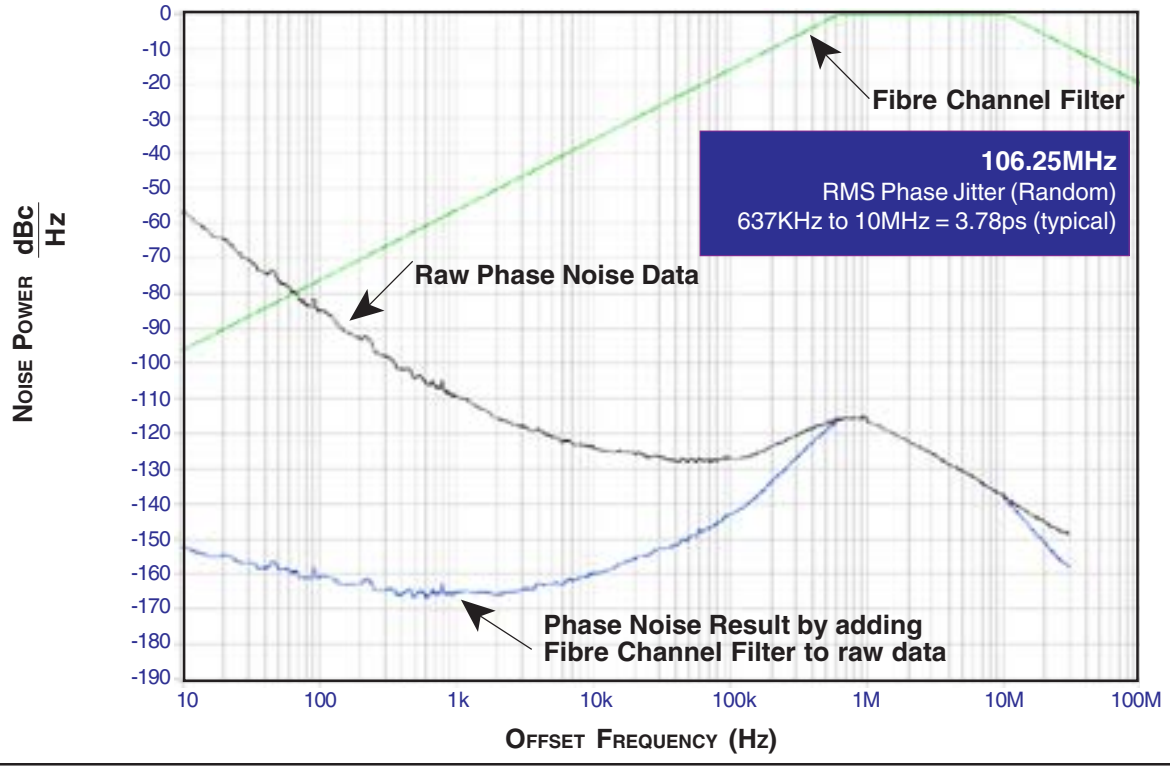
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				318.75	MHz
*t*sk(b)	Bank Skew; NOTE 1			15		ps
*t*sk(o)	Output Skew; NOTE 2, 3			TBA		ps
*t*jit(Ø)	RMS Phase Jitter, (Random); NOTE 4	318.75MHz (12KHz - 20MHz)		4.25		ps
		212.5MHz (1.274MHz - 20MHz)		4.19		ps
		159.375MHz(12k - 20MHz)		4.30		ps
		106.25MHz (637KHz - 10MHz)		3.78		ps
t_L	PLL Lock Time			1		ms
t_R / t_F	Output Rise/Fall Time	20% to 80%		350		ps
odc	Output Duty Cycle			50		%

See NOTES 1 through 4 above.

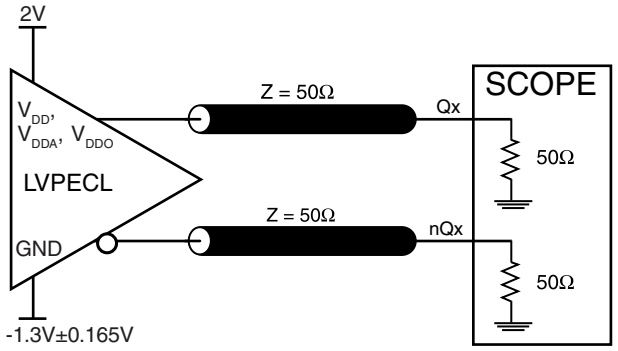
TYPICAL PHASE NOISE AT 106.25MHZ FOR LVPECL



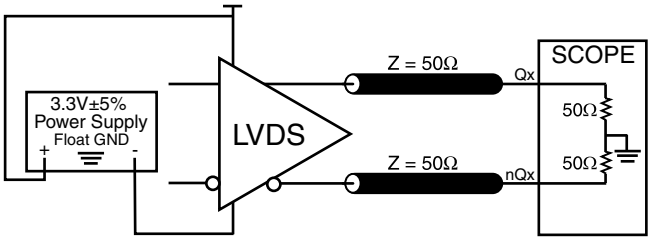
TYPICAL PHASE NOISE AT 106.25MHZ FOR LVDS



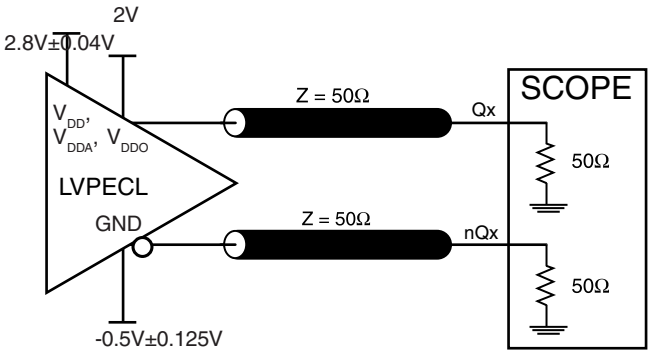
PARAMETER MEASUREMENT INFORMATION



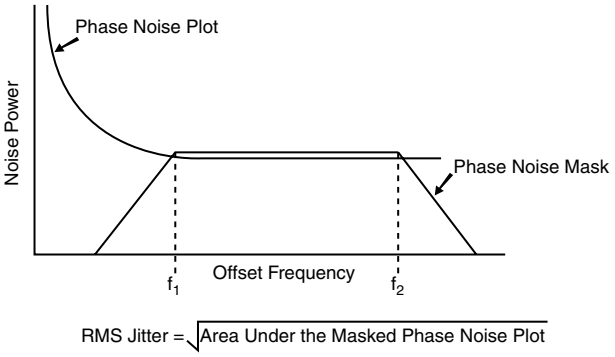
LVPECL 3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



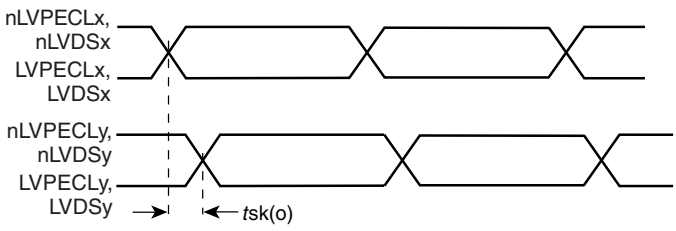
LVDS 3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



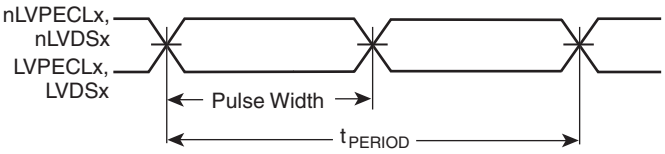
LVPECL 3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



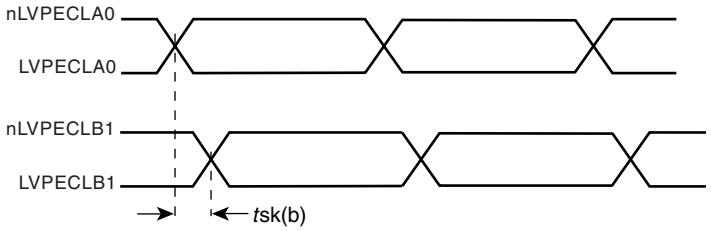
RMS PHASE JITTER



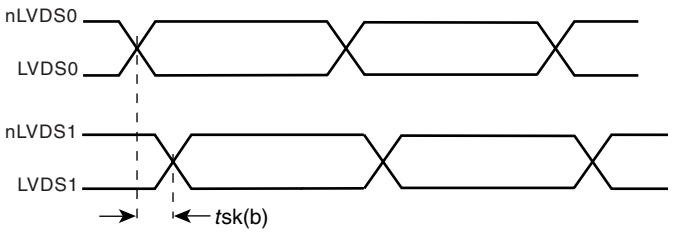
OUTPUT SKEW



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

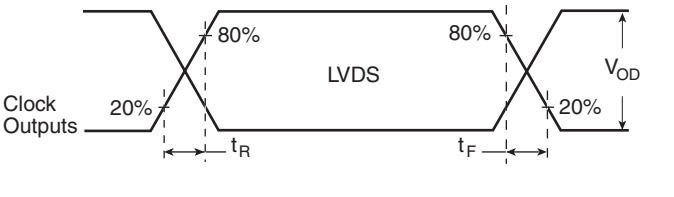


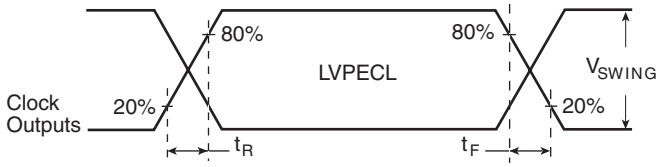
LVPECL BANK SKEW



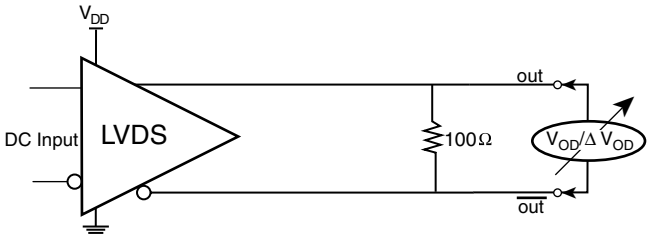
LVDS BANK SKEW

BANK SKEW (MAXIMUM VALUE)

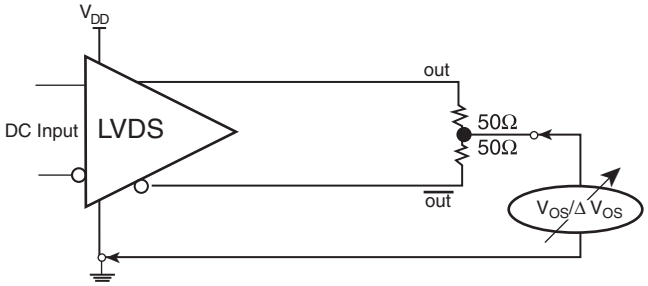




OUTPUT RISE/FALL TIME



DIFFERENTIAL OUTPUT VOLTAGE SETUP



OFFSET VOLTAGE SETUP

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS843404 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, and V_{DDO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 24Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA}.

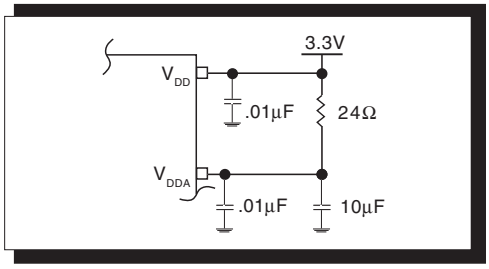


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS843404 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 25.5MHz 18pF parallel resonant crystal and were chosen to minimize the ppm error.

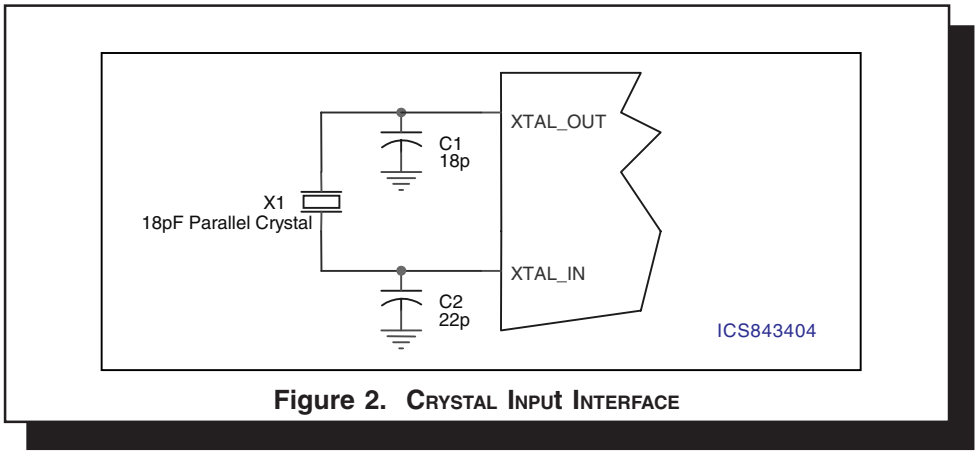


Figure 2. CRYSTAL INPUT INTERFACE

LVDS DRIVER TERMINATION

A general LVDS interface is shown in *Figure 3.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the un-used outputs.

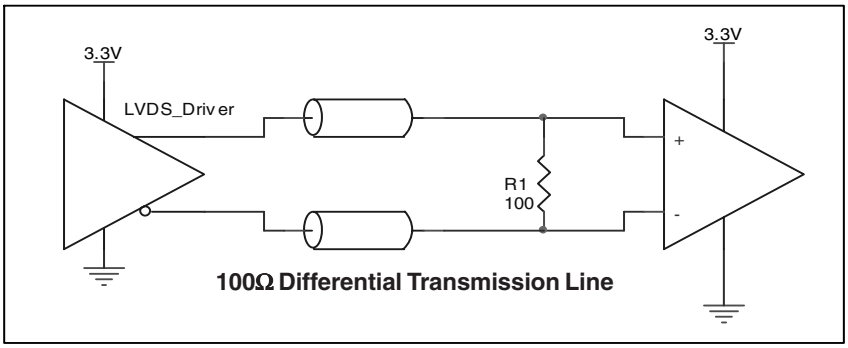


FIGURE 3. TYPICAL LVDS DRIVER TERMINATION

TERMINATION FOR 3.3V LVPECL OUTPUT

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

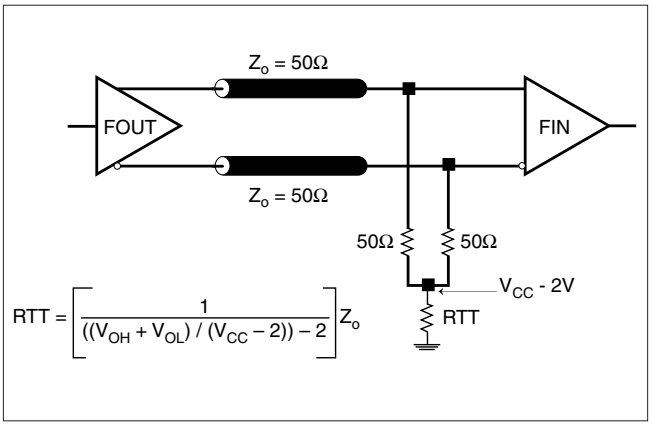


FIGURE 4A. LVPECL OUTPUT TERMINATION

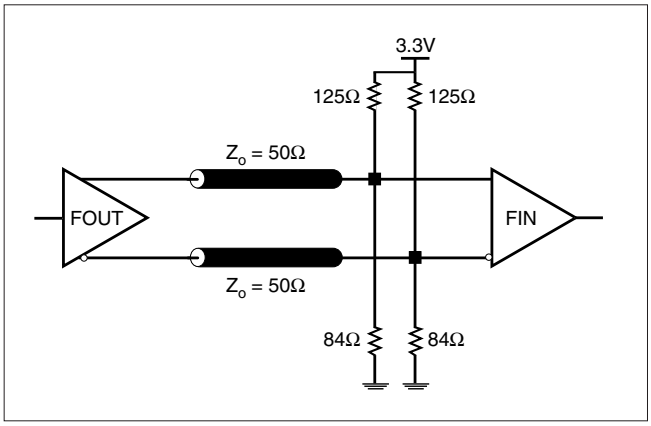


FIGURE 4B. LVPECL OUTPUT TERMINATION

TERMINATION FOR 2.5V LVPECL OUTPUT

Figure 5A and *Figure 5B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{DD} - 2V. For V_{DDO} = 2.5V, the V_{DDO} - 2V is very close to ground level. The R3 in Figure 5B can be eliminated and the termination is shown in *Figure 5C*.

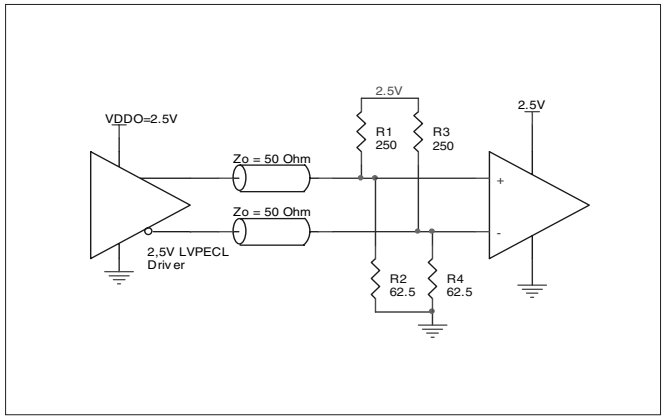


FIGURE 5A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

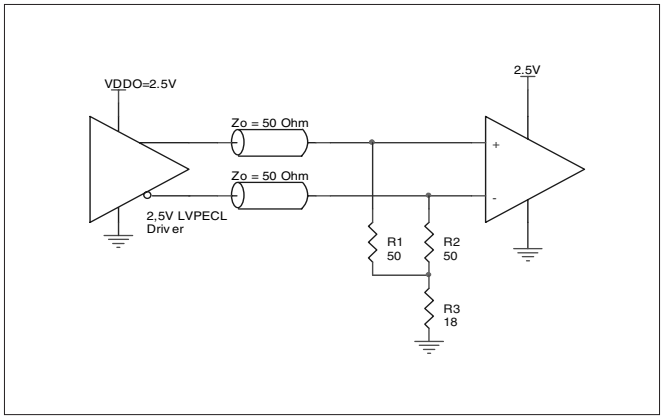


FIGURE 5B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

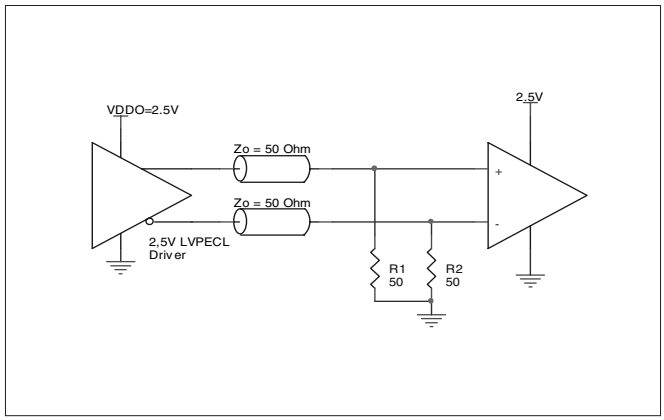


FIGURE 5C. 2.5V LVPECL TERMINATION EXAMPLE

LAYOUT GUIDELINE

Figure 6 shows a schematic example of the ICS843404. An example of LVEPCL termination is shown in this schematic. Additional LVPECL termination approaches are shown in the LVPECL Termination Application Note. In this example, an 18pF parallel resonant 25.5MHz crystal is used. The C1=27pF and C2=33pF are recommended for frequency accuracy. For different board layout, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy.

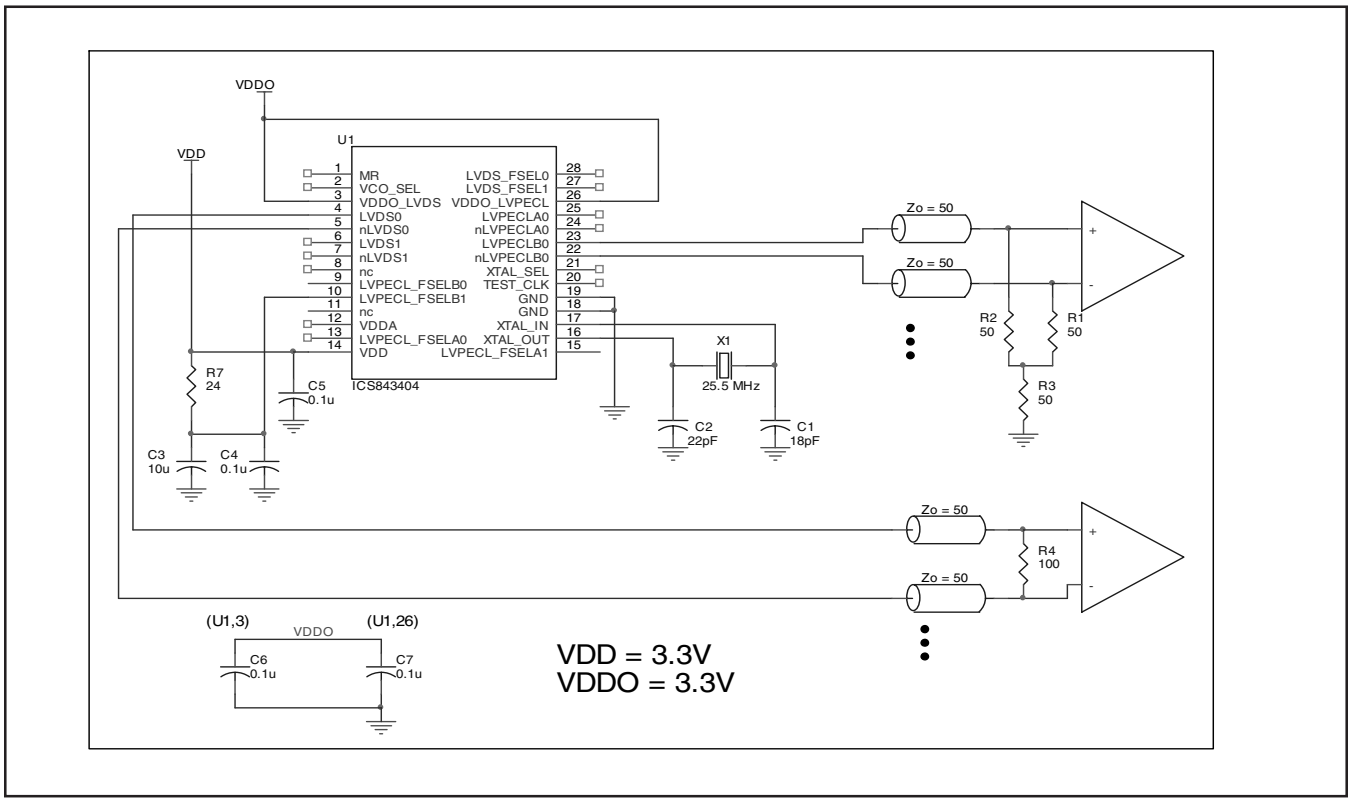


FIGURE 6. ICS843404 SCHEMATIC EXAMPLE

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 28 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	82.9°C/W	68.7°C/W	60.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	49.8°C/W	43.9°C/W	41.2°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS843404 is: 2314

PACKAGE OUTLINE - G SUFFIX FOR 28 LEAD TSSOP

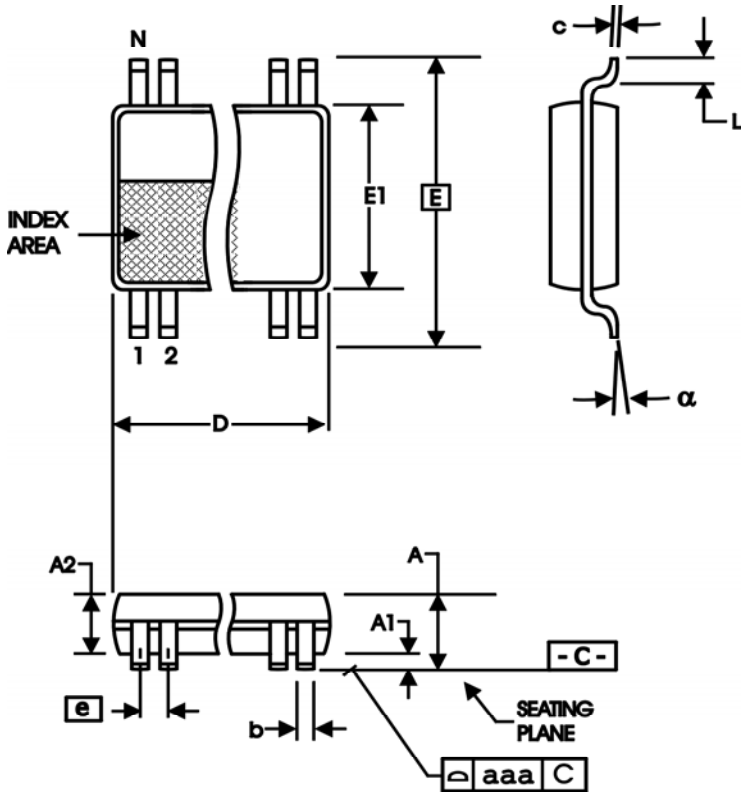


TABLE 8. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	28	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	9.60	9.80
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS843404AG	ICS843404AG	28 Lead TSSOP	48 per tube	0°C to 70°C
ICS843404AGT	ICS843404AG	28 Lead TSSOP on Tape and Reel	1000	0°C to 70°C
ICS843404AGLF	ICS843404AGLF	28 Lead "Lead Free" TSSOP	48 per tube	0°C to 70°C
ICS843404AGLFT	ICS843404AGLF	28 Lead "Lead Free" TSSOP on Tape and Reel	1000	0°C to 70°C