Ordering number: EN*4300

CMOS IC

LC86E6032

8-Bit Single-Chip Microcontroller

Preliminary

Overview

The LC86E6032 microcontroller is a CMOS 8-bit single chip microcontroller with UVEPROM for LC866000A series.
This microcontroller has the same functions and pin assignment as for the LC866000A series mask ROM version, and a 32K-byte EPROM.
Program data is rewritable. It is suitable for program developments.

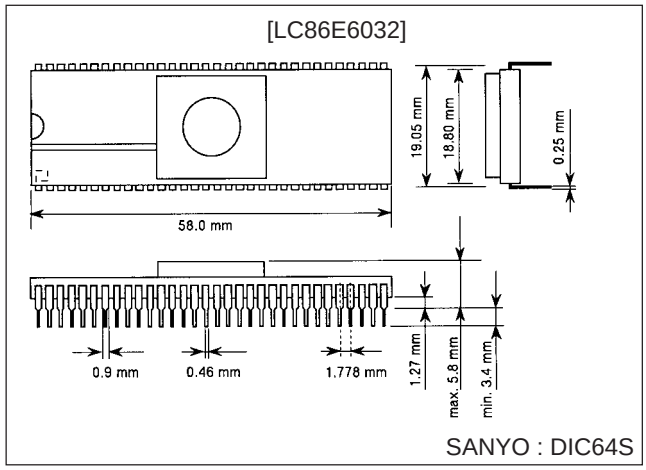
Features

(1) Option switching using EPROM data
The optional functions of the LC866000A series can be specified using EPROM data.
LC86E6032 can be checked the functions of trial piece using the mass production board.
(2) Internal 32K-byte UVEPROM
32K-byte UVEPROM (ultraviolet erasable and programmable ROM) is built in. This corresponds to LC866032B/28B/24B/20A/16A/12A/08A.
(3) The pin compatible with mask ROM version
(4) Factory shipment
DIC-64S
QFC-64E (Under development)

Package Dimensions

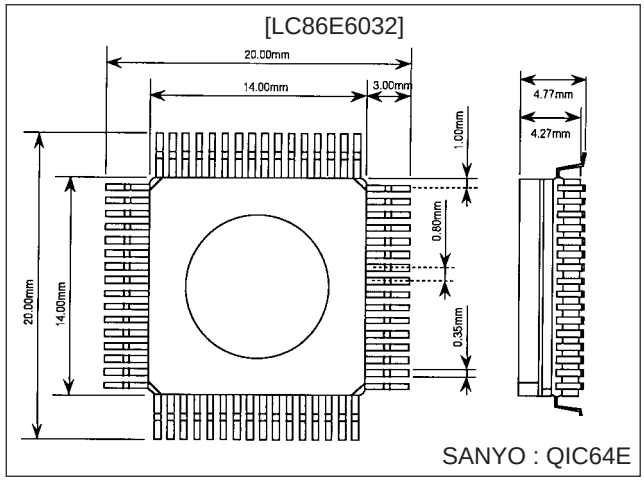
unit : mm

3126-DIC64S



unit : mm

3152-QFC64E



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Notice for Use

LC86E6032 is provided for the program development and checking the function of LC866000A series.
At using, take notice of the followings.

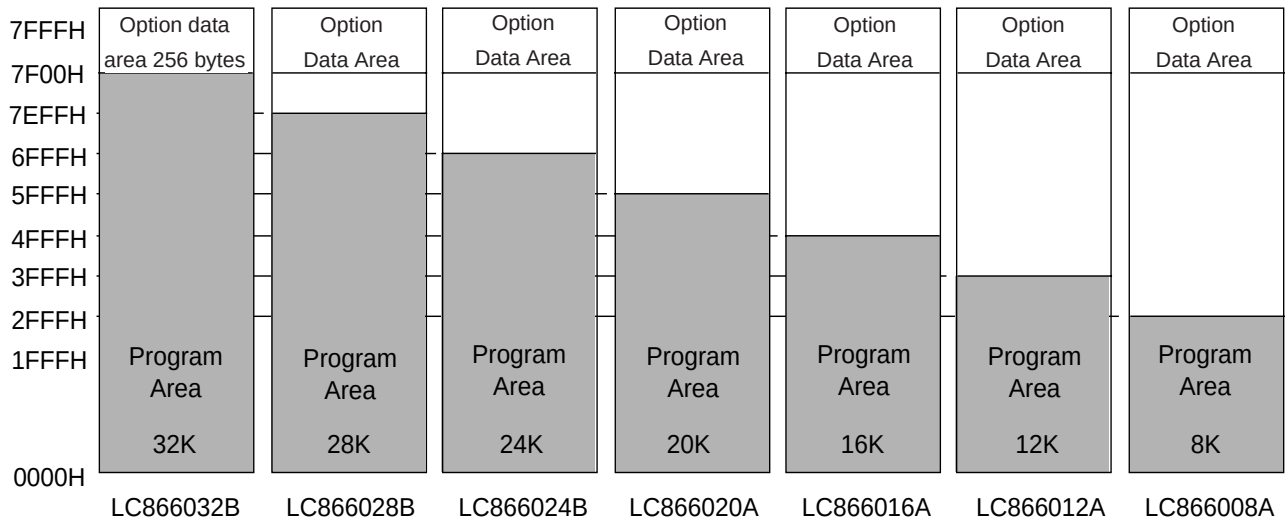
(1) Reset

It is necessary to be sure to go into 'L' level and hold for 200 μs to reset terminal ($\overline{RES}$) after power supplied voltage has been over inferior limit of supply voltage.
The option is specified until 3ms after going into 'H' level to reset terminal by degrees.
The program is executed from 00H of program counter. The output form of all ports are N-channel open-drain while 'L' level to reset terminal.

(2) Option

The LC86E6032 uses 256 bytes addressed 7F00H to 7FFFH in program memory as option data area.
This area does not affect the execution of program but means that the LC866032A program memory is 32512 bytes addressed 0000H to 7EFFH.
The option data is specified by the option-setting program "SU866000.EXE". The specified option data is linked to the program area by linkage editor "L866000.EXE".

(3) ROM space



(4) Points of difference LC86E6032 and LC866000A series (mask ROM version)

Item	LC86E6032	LC866032B/28B/24B/20A/16A/12A/08A
Operating temperature range (Topr)	+10°C to +40°C	–30°C to +70°C
Output form of port at reset	Open-drain output	Output form specified by option data
Output form of segment S0/T0 to S6/T6 S7/T7 to S15/T15 S16 to S23 S24 to S29	Pulldown resistance Not provided Provided (fixed) Provided (fixed) Not provided	Pulldown resistance: Provided/ Not provided Specified by option Provided (fixed) Specified by option Specified by option
Operating supply voltage range (V_{DD})	4.5 to 6.0V	2.5 to 6.0V

Option

A kind of option corresponding LC86E6032

Option types	Pins, Circuits	Contents of option
Input/output form of input/output ports	Port 0 (specified in a bit)	1. Input :No Pullup MOS Transistor Output :N-channel open-drain 2. Input :Pullup MOS Transistor Output :CMOS
	Port 1 (specified in a bit)	1. Input :Programmable pullup MOS Transistor Output :N-channel open-drain 2. Input :Programmable pullup MOS Transistor Output :CMOS
Pullup MOS Transistor of input port	Port 7 (specified in a bit)	1. No Pullup MOS Transistor 2. Pullup MOS Transistor

A kind of option not corresponding LC86E6032

Option types	Pins,Circuits	Contents of option
Pulldown resistance of high voltage withstand output terminal	S0/T0 to S6/T6 S16 to S29 (specified in a bit)	1. Pulldown resistance 2. No Pulldown resistance

How to Use

(1) Specification of options
LC86E6032 must be programmed after specifying option data. The option is specified by “SU866000.EXE”. The specified option file and the file created by our macro assembler “M866000.EXE” are linked by our linkage loader “L866000.EXE” which creates .HEX file, then the option code is put in the option specifed area (7F00H to 7FFFH) of its .HEX file.

(2) How to write data to EPROM
When writing data that was created by the linker to the LC86E6032, a general-purpose EPROM programmer can be used by using special write conversion boards (W86EP6032D, W86EP6032Q).

- Recommended EPROM programmers

Supplier	EPROM programmer
Advantest	R4945, R4944, R4943
Andou	AF-9704
AVAL	PKW-1100, PKW-3000
Minato Electronics	MODEL 1890A

- “27512 (Vp-p = 12.5 V) Intel high-speed programming” mode should be used. The address must be set to "0000H to 7FFFH" and the jumper (DASEC) must be set 'OFF' at programming.

(3) How to use the data security function
"Data security" is a function to prevent the EPROM data from being read.
Instructions on using the data security function:

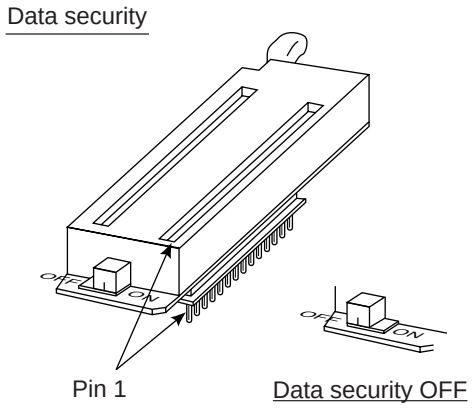
1. Set the jumper (DASEC) of the attachment 'ON'.
2. Attempt to program the EPROM.
   The EPROM programmer displays an error. The error is a result of normal activity of the data security feature, and does not indicate a problem with the programmer or the LSI.

Notes

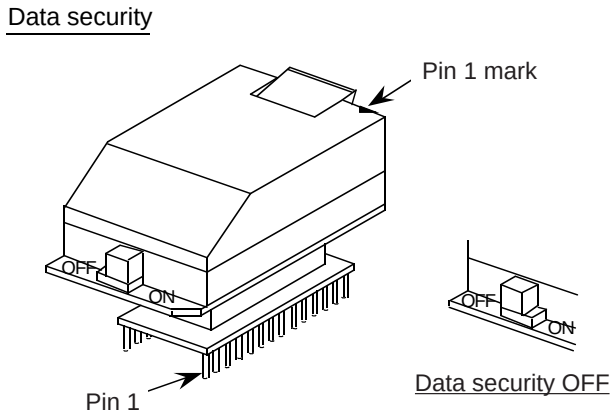
- The data security function is not carried out when the data of all address contain 'FF' at step 2 above.
- Data security cannot be executed when the sequential writing operation of programming "BLANK=>PROGRAM=>VERIFY" is used at step 2 above.
- Set the jumper 'OFF' after the execution of data security.

(4) Erasing data
Use a general-purpose EPROM eraser to erase the written data.

(5) Shielding
The UVEPROM (ultraviolet erasable programmable ROM) is incorporated in the IC. Cover the window of the IC with a seal in use.

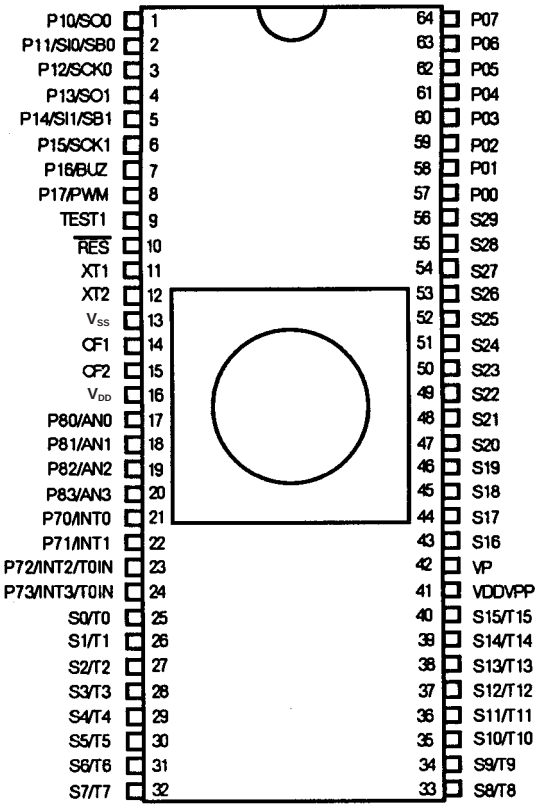


W86EP6032D



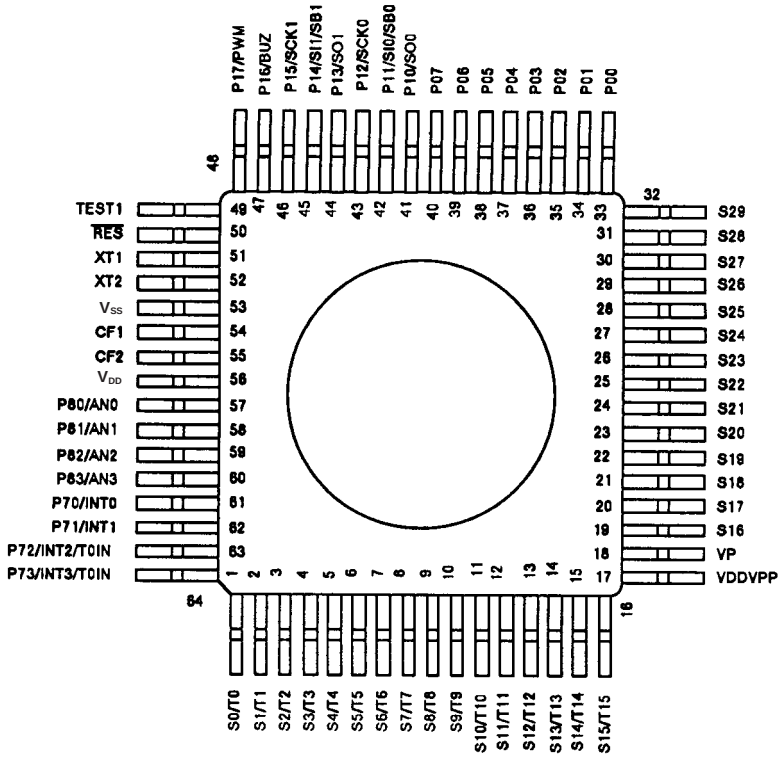
W86EP6032Q

Pin Assignment



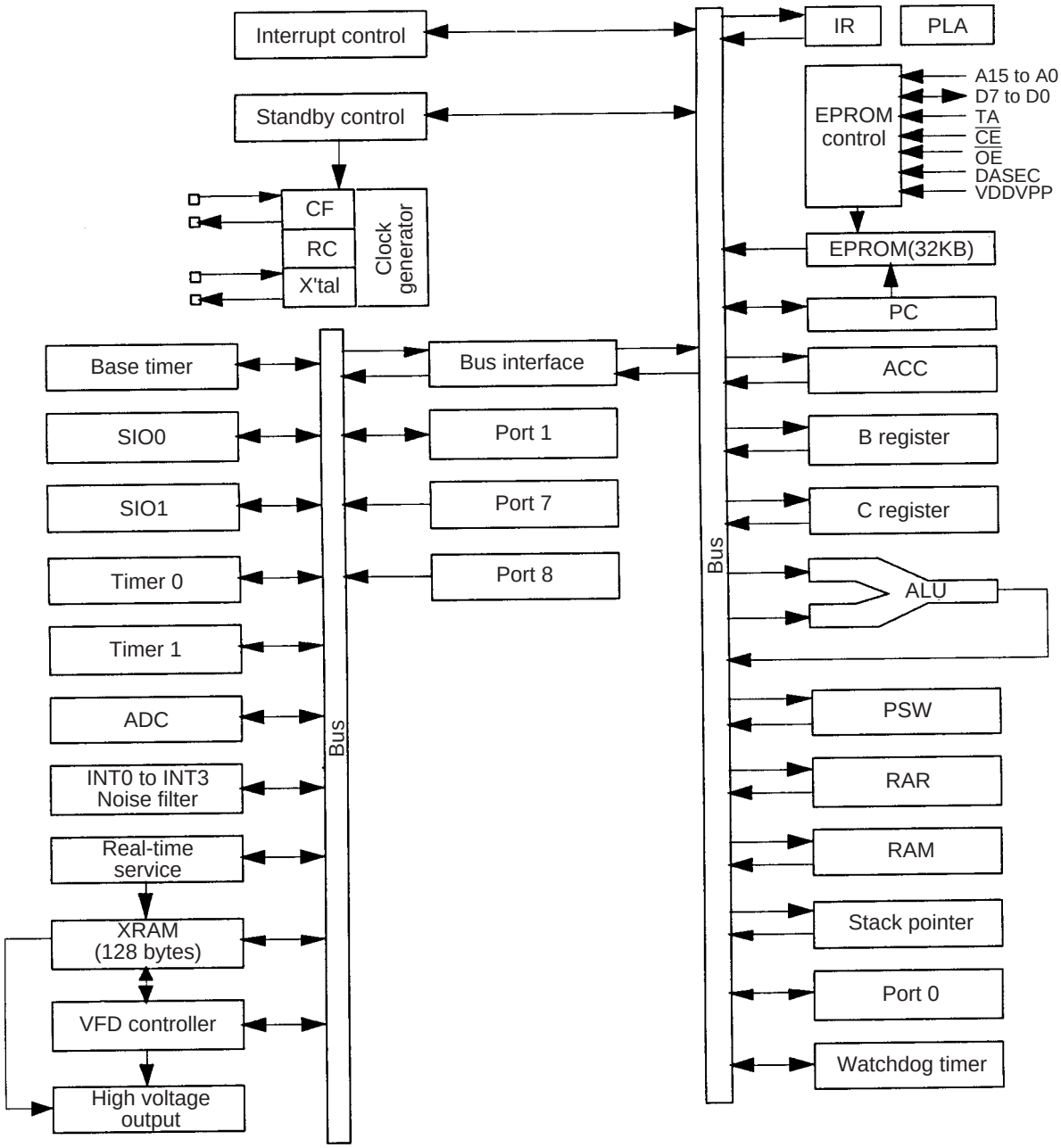
Top view

Pin Assignment



Top view

System Block Diagram



Pin Description

<table>
<tr><th>Pin name</th><th>I/O</th><th>Function description</th><th>Option</th><th>Function in PROM mode</th></tr>
<tr><td>V_{SS}</td><td>—</td><td>Power supply pin (–)</td><td></td><td></td></tr>
<tr><td>V_{DD}</td><td>—</td><td>Power supply pin (+)</td><td></td><td></td></tr>
<tr><td>VP</td><td>—</td><td>Power supply pin (–)
(Power supply for VFD display drive output)
(Power supply for pull-down resistor)</td><td></td><td></td></tr>
<tr><td>VDDVPP</td><td>—</td><td>Power supply pin (+)</td><td></td><td>Power for programming</td></tr>
<tr><td>PORT0
P00 to P07</td><td>I/O</td><td>• 8-bit input/output port
• Input/output specification can be made for 4-bit unit.
• Input for HOLD release
• Input for port 0 interrupt</td><td>• Pull-up resistor : Provided/Not provided
• Output form : CMOS/ N-channel open-drain.</td><td></td></tr>
<tr><td>PORT1
P10 to P17</td><td>I/O</td><td>• 8-bit input/output port
• Data direction can be specified for each bit.
• Other pin functions
P10 : SIO0 data output
P11 : SIO0 data input/ bus input/output
P12 : SIO0 clock input/output
P13 : SIO1 data output
P14 : SIO1 data input/ bus input/output
P15 : SIO1 clock input/output
P16 : Buzzer output
P17 : Timer 1 output (PWM output)</td><td>Output form : CMOS/ N-channel open-drain</td><td>Data input/output
• D0 to D7</td></tr>
<tr><td>PORT7

P70

P71 to P73</td><td>

I/O

I</td><td>• 4-bit input port
• Other pin functions
P70 : INT0 input/HOLD release/N-channel transistor output for watchdog timer.
P71 : INT 1 input/HOLD release.
P72 : INT 2 input/timer 0 event input.
P73 : INT 3 input with noise filter/timer 0 event input.
• Interrupt received format, vector address.
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & falling</th><th>High level</th><th>Low level</th><th>Vector</th></tr>
<tr><td>INT0</td><td>Enable</td><td>Enable</td><td>Disable</td><td>Enable</td><td>Enable</td><td>03H</td></tr>
<tr><td>INT1</td><td>Enable</td><td>Enable</td><td>Disable</td><td>Enable</td><td>Enable</td><td>0BH</td></tr>
<tr><td>INT2</td><td>Enable</td><td>Enable</td><td>Enable</td><td>Disable</td><td>Disable</td><td>13H</td></tr>
<tr><td>INT3</td><td>Enable</td><td>Enable</td><td>Enable</td><td>Disable</td><td>Disable</td><td>1BH</td></tr>
</table></td><td>• Pull-up resistor : Provided/Not provided</td><td>Input of PROM control signal

• DASEC (*1)
• $\overline{OE}$ (*2)
• $\overline{CE}$ (*3)</td></tr>
<tr><td>PORT8
P80 to P83</td><td>I</td><td>• 4-bit input port
• Other functions
AD input port (4 port pins)</td><td></td><td></td></tr>
<tr><td>S0/T0 to S6/T6</td><td>O</td><td>Output for VFD display controller
Segment/timing common output</td><td></td><td></td></tr>
<tr><td>S7/T7 to S15/T15</td><td>O</td><td>Output for VFD display controller
Segment/timing common output
Output with built-in pull-down resistor</td><td></td><td>•S14/T14 : TA (*4)
•S15/T15 : A14 (*5)</td></tr>
</table>

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Pin name	I/O	Function description	Option	Function in PROM mode
S16 to S23	O	Output for VFD display controller Segment output Output with built-in pull-down resistor		Address input •A13 to A0
S24 to S29	O	Output for VFD display controller Segment output		
$\overline{RES}$	I	Reset pin		
TEST1	O	Test pin Should be left open.		
XT1	I	Input pin for 32.768 kHz crystal oscillation When not used, connect to V_{DD}.		
XT2	O	Output pin for 32.768 kHz crystal oscillation When not used, should be left open.		
CF1	I	Input pin for ceramic resonator oscillation		
CF2	O	Output pin for ceramic resonator oscillation		

*1 Memory select input for data security
*2 Output enable input
*3 Chip enable input
*4 TA → PROM control signal input
*5 A14 → Address input

* All of port options can be specified in bit unit.
* A state of pins at reset.

Pin name	Input/output mode	A state of pullup resistor specified at pullup option
Ports 0,7	Input	Fixd pullup resistor exsists
Port 1	Input	Programmable pullup resistor OFF

Pin name	A state of P-channel transistor
S0/T0 to S15/T15	P-channel transistor OFF
S16 to S29	P-channel transistor OFF

Specification

1. Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter		Symbol	Pins	Conditions		Ratings			Unit
					V_{DD}[V]	min	typ	max	
Maximum supply voltage		V_{DD} max	V_{DD},VDDVPP	V_{DD} = VDDVPP		–0.3		+7.0	V
Input voltage		V_I(1)	• P 71, 72, 73 • Port 8 • RES			–0.3		V_{DD}+0.3	
		V_I(2)	VP			V_{DD}–45		V_{DD}+0.3	
Output voltage		V_O	• S0/T0 to S15/T15 • S16 to S29			V_{DD}–45		V_{DD}+0.3	
Input/output voltage		V_{IO}	Ports 0, 1,P 70			–0.3		V_{DD}+0.3	
High-level output current	Peak output current	I_{OPH}(1)	Ports 0, 1	• CMOS output • At each pin		–4			mA
		I_{OPH}(2)	S0/T0 to S15/T15	At each pin		–30			
		I_{OPH}(3)	S16 to S29	At each pin		–15			
	Total output current	$\sum I_{OAH}$(1)	Port 0	Total of all pins		–10			
		$\sum I_{OAH}$(2)	Port 1	Total of all pins		–10			
		$\sum I_{OAH}$(3)	• S0/T0 to S15/T15 • S16 to S29	Total of all pins		–130			
Low-level output current	Peak output current	I_{OPL}(1)	Ports 0, 1	At each pin				20	
		I_{OPL}(2)	P70	At each pin				15	
	Total output current	$\sum I_{OAL}$(1)	Port 0	Total of all pins				–30	
		$\sum I_{OAL}$(2)	Port 1,P70	Total of all pins				40	
Allowable power dissipation		Pd max(1)	DIC64S	Ta = +10°C to +40°C				760	mW
		Pd max(2)	QFC64E	Ta = +10°C to +40°C		To be determined after evaluation			
Operating temperature range		Topr				+10		+40	°C
Storage temperature range		Tstg				–65		150	

2. Allowable Operating Conditions at Ta = +10°C to +40°C, V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions	V_{DD}[V]	Ratings min	Ratings typ	Ratings max	Unit
Operating supply voltage range	V_{DD}	V_{DD}	0.98 µs ≤ tCYC tCYC ≤ 400 µs		4.5		6.0	V
HOLD voltage	V_{HD}	V_{DD}	• When in HOLD mode • RAM and registers retain previous data.		2.0		6.0	
Pulldown supply voltage	VP	VP		4.5 to 6.0	–35		V_{DD}	
Input high-level voltage	V_{IH}(1)	Port 0 (Schmitt)	Output disable	4.5 to 6.0	0.4V_{DD} +0.9		V_{DD}	
	V_{IH}(2)	• Port 1 • P72, 73 (Schmitt)	Output disable	4.5 to 6.0	0.75V_{DD}		V_{DD}	
	V_{IH}(3)	• P70 Port input/interrupt. • P71 • $\overline{RES}$ (Schmitt)	Output N-channel transistor OFF	4.5 to 6.0	0.75V_{DD}		V_{DD}	
	V_{IH}(4)	P70 Watchdog timer	Output N-channel transistor OFF	4.5 to 6.0	0.9V_{DD}		V_{DD}	
	V_{IH}(5)	• Port 8		4.5 to 6.0	0.75V_{DD}		V_{DD}	
Input low-level voltage	V_{IL}(1)	Port 0 (Schmitt)	Output disable	4.5 to 6.0	V_{SS}		0.2V_{DD}	
	V_{IL}(2)	• Port 1 • P72, 73(Schmitt)	Output disable	4.5 to 6.0	V_{SS}		0.25V_{DD}	
	V_{IL}(3)	• P70 Port input/interrupt. • P71 • $\overline{RES}$ (Schmitt)	N-channel transistor OFF	4.5 to 6.0	V_{SS}		0.25V_{DD}	
	V_{IL}(4)	P70 Watchdog timer	N-channel transistor OFF	4.5 to 6.0	V_{SS}		0.8V_{DD} –1.0	
	V_{IL}(5)	• Port 8		4.5 to 6.0	V_{SS}		0.25V_{DD}	
Operation cycle time	tCYC			4.5 to 6.0	0.98		400	µs
Oscillation frequency range (Note 1)	FmCF(1)	CF1, CF2	• 12 MHz (ceramic resonator oscillation). • Refer to Figure 1.	4.5 to 6.0	11.76	12	12.24	MHz
	FmCF(2)	CF1, CF2	• 3 MHz (ceramic resonator oscillation). • Refer to Figure 1.	4.5 to 6.0	2.94	3	3.06	
	FmRC		RC oscillation	4.5 to 6.0	0.4	0.8	2.0	
	FsXtal	XT1, XT2	• 32.768 kHz (crystal oscillation). • Refer to Figure 2.	4.5 to 6.0		32.768		kHz
Oscillation stable time period (Note 1)	tmsCF(1)	CF1, CF2	• 12 MHz (ceramic resonator oscillation). • Refer to Figure 3.	4.5 to 6.0		0.02	0.2	ms
	tmsCF(2)	CF1, CF2	• 3 MHz (ceramic resonator oscillation). • Refer to Figure 3.	4.5 to 6.0		0.1	1	
	tssXtal	XT1, XT2	• 32.768 kHz (crystal oscillation). • Refer to Figure 3.	4.5 to 6.0		1	1.5	s

(Note 1) Refer to Table 1 and Table 2 for the oscillation constants.

3. Electrical Characteristics at Ta= +10°C to +40°C , V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions	Ratings				Unit
				V_{DD} [V]	min	typ	max	
Input high-level current	I_{IH}(1)	• Port 1 • Port 0 without pull-up MOS transistor	• Output disable • Pull-up MOS transistor OFF. • V_{IN} = V_{DD} (including off-state leak current of output transistor)	4.5 to 6.0			1	µA
	I_{IH}(2)	• Port 7 without pull-up MOS transistor • Port 8	V_{IN}= V_{DD}	4.5 to 6.0			1	
	I_{IH}(3)	• $\overline{RES}$	V_{IN} = V_{DD}	4.5 to 6.0			1	
Input low-level current	I_{IL}(1)	• Port 1 • Port 0 without pull-up MOS transistor	• Output disable • Pull-up MOS transistor OFF. • V_{IN} = V_{SS} (including off-state leak current of output transistor)	4.5 to 6.0	–1			
	I_{IL}(2)	• Port 7 without pull-up MOS transistor • Port 8	V_{IN} = V_{SS}	4.5 to 6.0	–1			
	I_{IL}(3)	• $\overline{RES}$	V_{IN} = V_{SS}	4.5 to 6.0	–1			
Output high-level voltage	V_{OH}(1)	• Ports 0, 1 at CMOS output	I_{OH} = –1.0 mA	4.5 to 6.0	V_{DD}–1			V
	V_{OH}(2)		I_{OH} = –0.1 mA	4.5 to 6.0	V_{DD}–0.5			
	V_{OH}(3)	S0/T0 to S15/T15	I_{OH} = –20 mA	4.5 to 6.0	V_{DD}–1.8			
	V_{OH}(4)		• I_{OH}= –1.0 mA • The current of any unmeasurement pin is not over 1 mA.	4.5 to 6.0	V_{DD}–1			
	V_{OH}(5)	S16 to S29	I_{OH} = –5 mA	4.5 to 6.0	V_{DD}–1.8			
	V_{OH}(6)		• I_{OH}= –1.0 mA • The current of any unmeasurement pin is not over 1 mA.	4.5 to 6.0	V_{DD}–1			
Output low-level voltage	V_{OL}(1)	Ports 0,1	I_{OL} = 10 mA	4.5 to 6.0			1.5	
	V_{OL}(2)		• I_{OL} = 1.6 mA • The total current of the Ports 0,1 is not over 40 mA	4.5 to 6.0			0.4	
	V_{OL}(3)	P70	I_{OL} = 1 mA	4.5 to 6.0			0.4	
Pull-up MOS transistor resistor	Rpu	• Ports 0, 1 • Port 7	V_{OH} = 0.9 V_{DD}	4.5 to 6.0	15	40	70	kΩ
Output off-state leak current	I_{OFF}(1)	• S0/T0 to S6/T6 • S24 to S29 (Without pulldown resistor)	• Output P-channel transistor OFF. • V_{OUT}= Vss	4.5 to 6.0	–1			µA
	I_{OFF}(2)		• Output P-channel transistor OFF. • V_{OUT}= V_{DD}–40V	4.5 to 6.0	–30			

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Parameter	Symbol	Pins	Conditions	Ratings				Unit
				V_{DD} [V]	min	typ	max	
Pulldown resistor	R_{pd}	• S7/T7 to S15T15 • S16 to S23 (With pulldown resistor)	• Output P-channel transistor OFF. • V_{OUT}= 3V • VP= –30V	5.0	60	100	200	kΩ
Hysteresis voltage	V_{HIS}	• Ports 0,1 • Port 7 • $\overline{RES}$	• Output disable	4.5 to 6.0		0.1V_{DD}		V
Pin capacitance	CP	All pins	• f=1MHz • Unmeasurement terminals for input are set to V_{SS} level. • Ta= 25°C	4.5 to 6.0		10		pF

4. Serial Input/Output Characteristics at Ta = +10°C to +40°C , V_{SS} = 0 V

Parameter			Symbol	Pins	Conditions	Ratings				Unit
						V_{DD} [V]	min	typ	max	
Serial clock	Input clock	Cycle	tCKCY(1)	SCK0, SCK1	Refer to Figure 5.	4.5 to 6.0	2			tCYC
		Low-level pulse width	tCKL(1)			4.5 to 6.0	1			
		High-level pulse width	tCKH(1)			4.5 to 6.0	1			
	Output clock	Cycle	tCKCY(2)	SCK0, SCK1	• Use pull-up resistor (1 kΩ) when set to open-drain output. • Refer to Figure 5.	4.5 to 6.0	2			
		Low-level pulse width	tCKL(2)			4.5 to 6.0		1/2tCKCY		
		High-level pulse width	tCKH(2)			4.5 to 6.0		1/2tCKCY		
Serial input	Data set-up time		tICK	• SI0, SI1 • SB0, SB1	• Data set-up to SCK0, 1 • Refer to Figure 5.	4.5 to 6.0	0.1			µs
	Data hold time		tCKI			4.5 to 6.0	0.1			
Serial output	Output delay time (Serial clock is extrnal clock.)		tCKO(1)	• SO0, SO1 • SB0, SB1	• Data hold from SCK0, 1 • Use pull-up resistor (1 kΩ) when set to open-drain output. • Refer to Figure 5.	4.5 to 6.0			7/12tCYC +0.2	
	Output delay time (Serial clock is internal clock.)		tCKO(2)	• SO0, SO1 • SB0, SB1	• Data hold from SCK0, 1 • Use pull-up resistor (1 kΩ) when set to open-drain output. • Refer to Figure 5.	4.5 to 6.0			1/3tCYC +0.2	

5. Pulse Input Conditions at Ta = +10°C to +40°C, V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions	Ratings			Unit
			V_{DD} [V]	min	typ	max	
High/low-level pulse width	tPIH(1) tPIL(1)	• INT0, INT1 • INT2/T0IN	• Interrupt acceptable • Timer 0 pulse countable	4.5 to 6.0	1		tCYC
	tPIH(2) tPIL(2)	INT3/T0IN (The noise rejection clock selected to 1/1.)	• Interrupt acceptable • Timer 0 pulse countable	4.5 to 6.0	2		
	tPIH(3) tPIL(3)	INT3/T0IN (The noise rejection clock selected to 1/64.)	• Interrupt acceptable • Timer 0 pulse countable	4.5 to 6.0	128		
	tPIL(4)	$\overline{RES}$	Reset acceptable	4.5 to 6.0	200		µs

6. A/D Converter Characteristics at Ta = +10°C to +40°C, V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions	Ratings			Unit
			V_{DD} [V]	min	typ	max	
Resolution	N		4.5 to 6.0		8		bit
Absolute precision	ET		(Note 2)			±1.5	LSB
Conversion time	tCAD		A/D conversion time = 16 x tCYC (ADCR2 = 0) (Note 3)	15.68 (tCYC = 0.98 µs)		65.28 (tCYC = 4.08 µs)	µs
			A/D conversion time = 32 x tCYC (ADCR2 = 1) (Note 3)	31.36 (tCYC = 0.98 µs)		130.56 (tCYC = 4.08 µs)	
Analog input voltage range	V_{AIN}	AN0 to AN3		V_{SS}		V_{DD}	V
Analog port input current	I_{AINH}		V_{AIN} = V_{DD}			1	µA
	I_{AINL}		V_{AIN} = V_{SS}	–1			

(Note 2) Absolute precision excepts quantizing error (±1/2 LSB).
(Note 3) The conversion time is the time from execution of the instruction to start conversion to the completion of shifting the A/D converted value to the register.

7. Current Drain Characteristics at Ta = +10°C to +40°C , V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions	Ratings				Unit
				V_{DD} [V]	min	typ	max	
Current drain during basic operation (Note 4)	I_{DDOP}(1)	V_{DD}	• FmCF = 12 MHz for ceramic resonator oscillation. • FsXtal = 32.768 kHz for crystal oscillator. • System clock : 12 MHz side • Internal RC oscillator stopped.	4.5 to 6.0		13	26	mA
	I_{DDOP}(2)		• FmCF = 3 MHz for ceramic resonator oscillation. • FsXtal = 32.768 kHz for crystal oscillator. • System clock : 3 MHz side • Internal RC oscillator stopped.	4.5 to 6.0		6.5	14	
	I_{DDOP}(3)		• FmCF = 0 Hz (when oscillator stops). • FsXtal = 32.768 kHz for crystal oscillator. • System clock : RC oscillator.	4.5 to 6.0		4	10	
	I_{DDOP}(4)		• FmCF = 0 Hz (when oscillator stops). • FsXtal = 32.768 kHz for crystal oscillator. • System clock : 32.768 kHz side • Internal RC oscillator stopped.	4.5 to 6.0		3.5	9	

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Parameter	Symbol	Pins	Conditions	Ratings				Unit
				V_{DD} [V]	min	typ	max	
Current drain at HALT mode (Note 4)	$I_{DDHALT}(1)$	V_{DD}	• HALT mode • FmCF = 12 MHz for ceramic resonator oscillation. • FsXtal = 32.768 kHz for crystal oscillator. • System clock : 12 MHz side • Internal RC oscillator stopped.	4.5 to 6.0		5	10	mA
	$I_{DDHALT}(2)$		• HALT mode • FmCF = 3 MHz for ceramic resonator oscillation. • FsXtal = 32.768 kHz for crystal oscillator. • System clock : 3 MHz side • Internal RC oscillator stopped.	4.5 to 6.0		1.8	4.6	
	$I_{DDHALT}(3)$		• HALT mode • FmCF = 0 Hz (when oscillator stops). • FsXtal = 32.768 kHz for crystal oscillator. • System clock : RC oscillator	4.5 to 6.0		400	800	µA
	$I_{DDHALT}(4)$		• HALT mode • FmCF = 0 Hz (when oscillator stops). • FsXtal = 32.768 kHz for crystal oscillator. • System clock : 32.768 kHz side • Internal RC oscillator stopped.	4.5 to 6.0		20	60	
Current drain at HOLD mode (Note 4)	$I_{DDHOLD}(1)$	V_{DD}	HOLD mode	4.5 to 6.0		0.05	30	
	$I_{DDHOLD}(2)$			2.5 to 4.5		0.02	20	

(Note 4) The currents of output transistors and pull-up MOS transistors are ignored.

Oscillation type	Supplier	Oscillator	C1	C2
12 MHz ceramic resonator oscillation	Murata	CSA12.0MTZ	33 pF	33 pF
		CSA12.0MT	33 pF	33 pF
		CST12.0MTW	on chip	
	Kyocera	KBR–12.0M	33 pF	33 pF
3 MHz ceramic resonator oscillation	Murata	CSA3.00MG	33pF	33 pF
		CST3.00MGW	on chip	
	Kyocera	KBR–3.0MS	47 pF	47 pF

* Both C1 and C2 must use K rank (±10%) and SL characteristics.

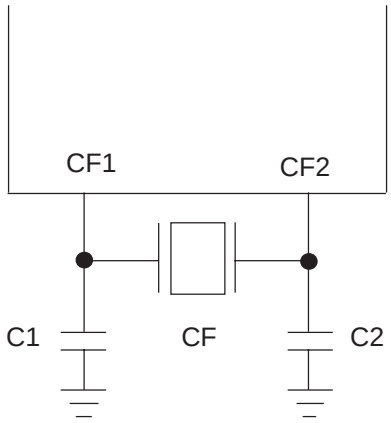
Table 1. Ceramic Resonator Oscillation Guaranteed Constants (Main-clock)

Oscillation type	Supplier	Oscillator	C3	C4
32.768 kHz crystal oscillation	Dai Sinku	DT-38(1TA252E00)	18 pF	18 pF
	Kyocera	KF-38G-13P0200	18 pF	18 pF

* Both C3 and C4 must use J rank (±5%) and CH characteristics.
(If high precision is unnecessary, use K rank (±10%) and SL characteristics.)

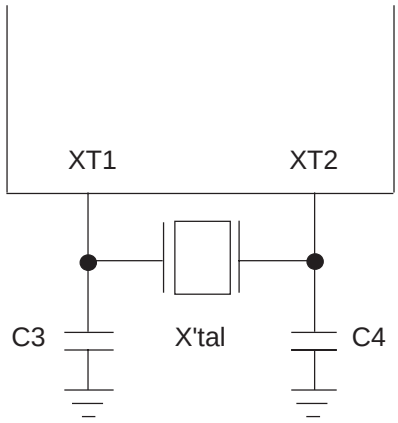
Table 2. Crystal Oscillation Guaranteed Constants (Sub-clock)

Notes • Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest pattern length.
• If you use other oscillators herein, we provide no guarantee for the characteristics.



Main-clock circuit

Figure 1 Ceramic Resonator Oscillation



Sub-clock circuit

Figure 2 Crystal Oscillation

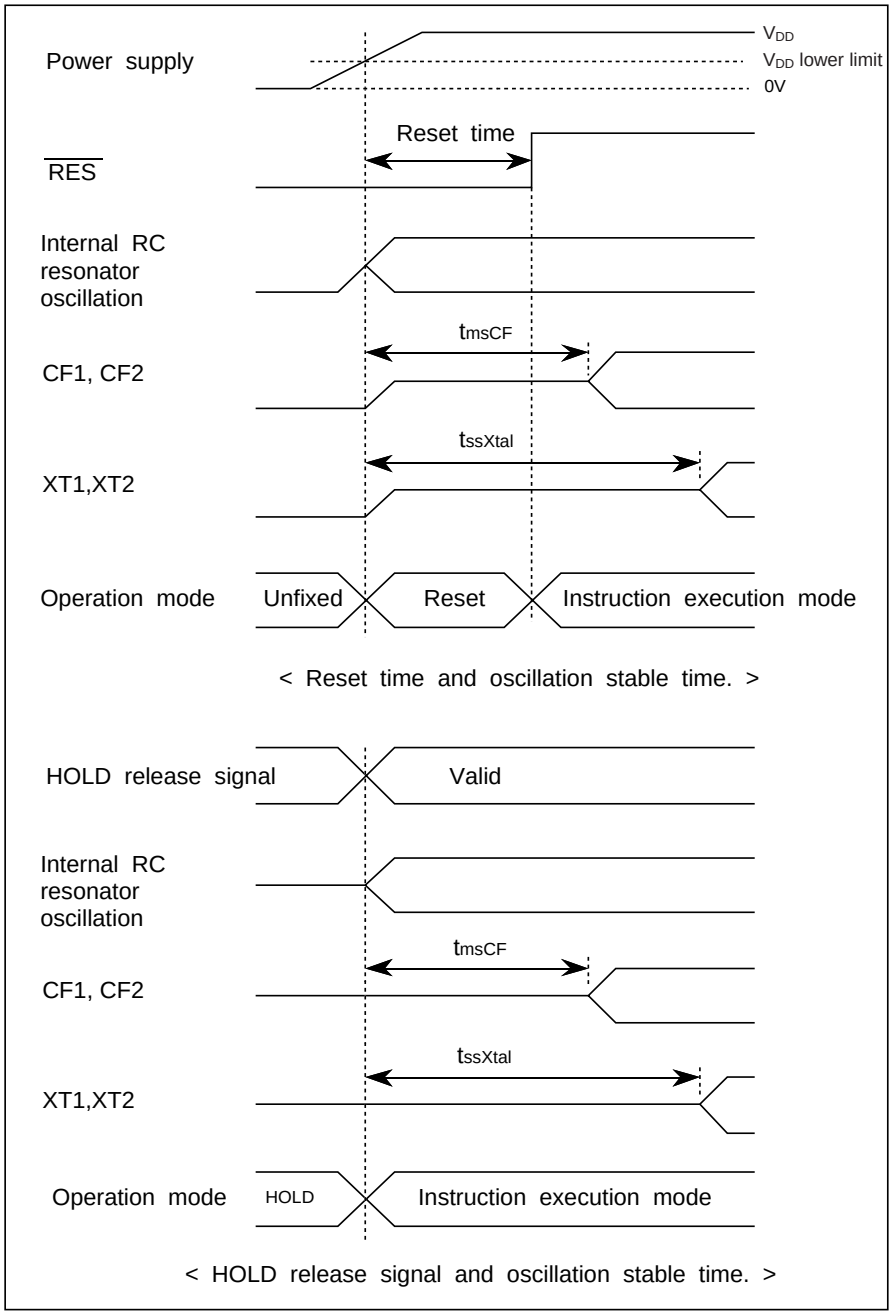
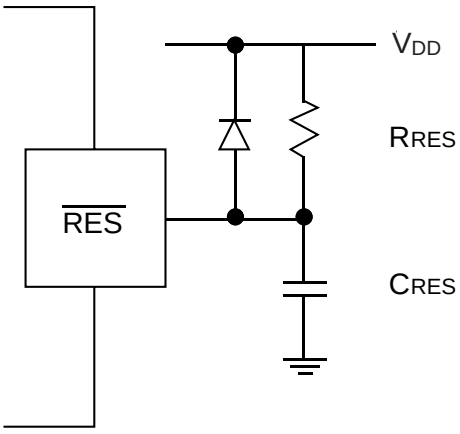
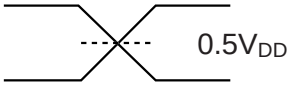


Figure 3 Oscillation Stable Time

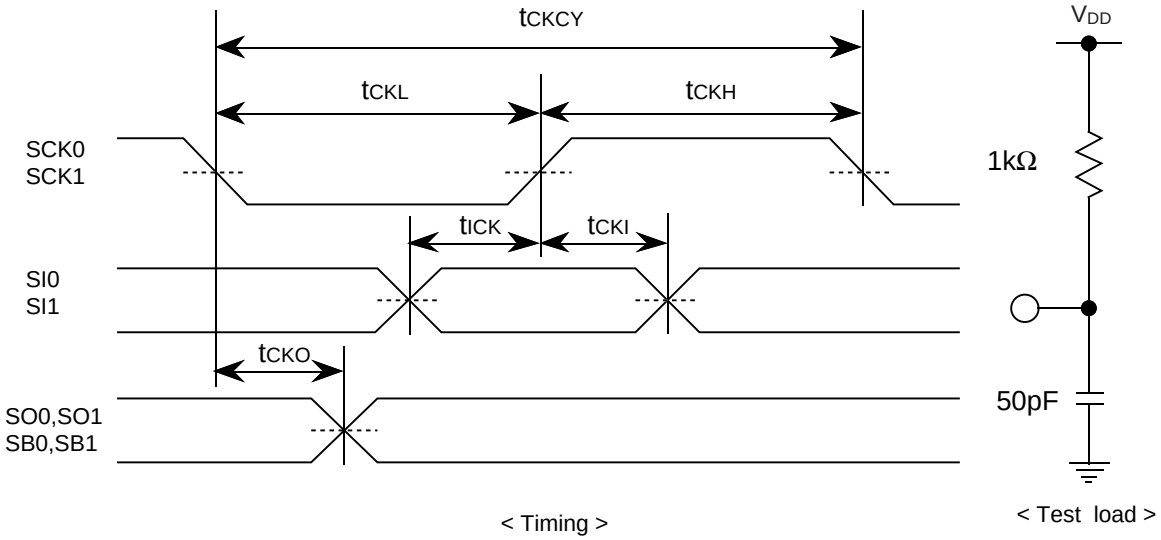


(Note)
The values of C_{RES} and R_{RES} should be determined such that reset time is at least 200 µs, measured from the moment the power exceeds the V_{DD} lower limit.

Figure 4 Reset Circuit



< AC timing point >



< Timing >

< Test load >

Figure 5 Serial Input/Output Test Conditions

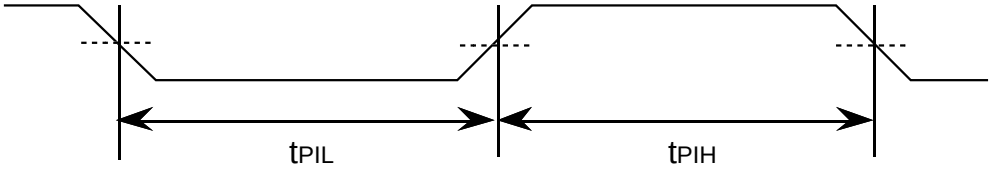


Figure 6 Pulse Input Timing Conditions