PNP
MJ11017
MJ11021*
NPN
MJ11018*
MJ11022

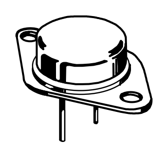
*Motorola Preferred Device

Complementary Darlington Silicon Power Transistors

. . . designed for use as general purpose amplifiers, low frequency switching and motor control applications.

- High dc Current Gain @ 10 Adc — h_{FE} = 400 Min (All Types)
- Collector–Emitter Sustaining Voltage
  $V_{CEO(sus)}$ = 150 Vdc (Min) – MJ11018, 17
  = 250 Vdc (Min) – MJ11022, 21
- Low Collector–Emitter Saturation
  $V_{CE(sat)}$ = 1.0 V (Typ) @ I_C = 5.0 A
  = 1.8 V (Typ) @ I_C = 10 A
- Monolithic Construction
- 100% SOA Tested @ V_{CE} = 44 V, I_C = 4.0 A, t = 250 ms.

30 AMPERE DARLINGTON POWER TRANSISTORS COMPLEMENTARY SILICON 60–120 VOLTS 200 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	MJ11018 MJ11017	MJ11022 MJ11021	Unit
Collector–Emitter Voltage	V_{CEO}	150	250	Vdc
Collector–Base Voltage	V_{CB}	150	250	Vdc
Emitter–Base Voltage	V_{EB}	50		Vdc
Collector Current — Continuous Peak	I_C	15 30		Adc
Base Current	I_B	0.5		Adc
Total Device Dissipation @ T_C = 25°C Derate Above 25°C	P_D	175 1.16		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +175 –65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.86	°C/W

(1) Pulse Test: Pulse Width 5.0 ms, Duty Cycle ≤ 10%.

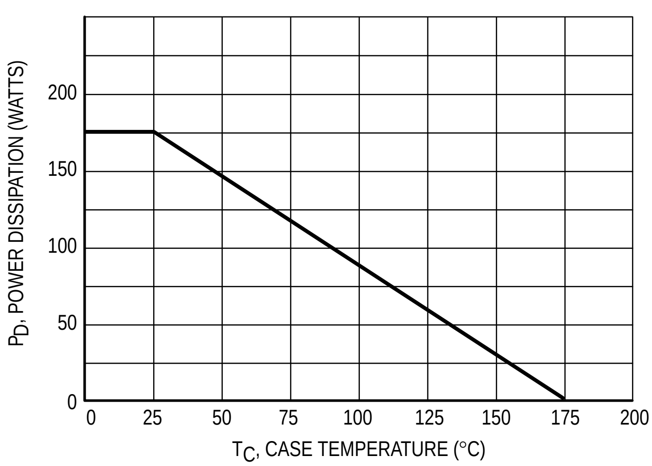


Figure 1. Power Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

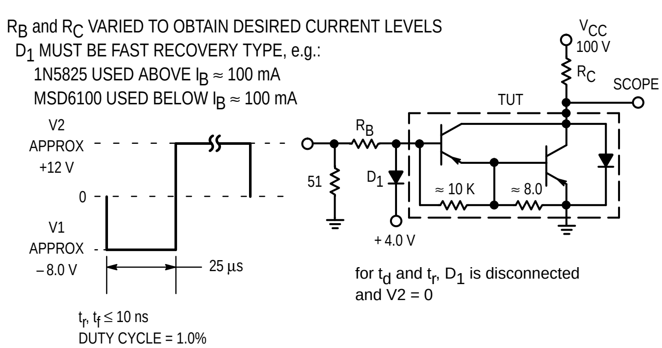
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 0. 1 Adc, I_B = 0)	MJ11017, MJ11018 MJ11021, MJ11022	$V_{CEO(sus)}$	150 250	— —	Vdc
Collector Cutoff Current (V_{CE} = 75, I_B = 0) (V_{CE} = 125, I_B = 0)	MJ11017, MJ11018 MJ11021, MJ11022	I_{CEO}	— —	1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_J = 150°C)		I_{CEV}	— —	0.5 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 10 Adc, V_{CE} = 5.0 Vdc) (I_C = 15 Adc, V_{CE} = 5.0 Vdc)		h_{FE}	400 100	15,000 —	—
Collector–Emitter Saturation Voltage (I_C = 10 Adc, I_B = 100 mA) (I_C = 15 Adc, I_B = 150 mA)		$V_{CE(sat)}$	— —	2.0 3.4	Vdc
Base–Emitter On Voltage I_C = 10 A, V_{CE} = 5.0 Vdc)		$V_{BE(on)}$	—	2.8	Vdc
Base–Emitter Saturation Voltage (I_C = 15 Adc, I_B = 150 mA)		$V_{BE(sat)}$	—	3.8	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain Bandwidth Product (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		$[h_{fe}]$	3.0	—	Mhz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	MJ11018, MJ11022 MJ11017, MJ11021	C_{ob}	— —	400 600	pF
Small–Signal Current Gain (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz)		h_{fe}	75	—	—

SWITCHING CHARACTERISTICS

Characteristic		Symbol	Typical NPN	Typical PNP	Unit
Delay Time	(V_{CC} = 100 V, I_C = 10 A, I_B = 100 mA $V_{BE(off)}$ = 50 V) (See Figure 2.)	t_d	150	75	ns
Rise Time		t_r	1.2	0.5	µs
Storage Time		t_s	4.4	2.7	µs
Fall Time		t_f	10.0	2.5	µs

(1) Pulsed Test: Pulse Width = 300 µs, Duty Cycle ≤ 2%.



For NPN test circuit reverse diode and voltage polarities.

Figure 2. Switching Times Test Circuit

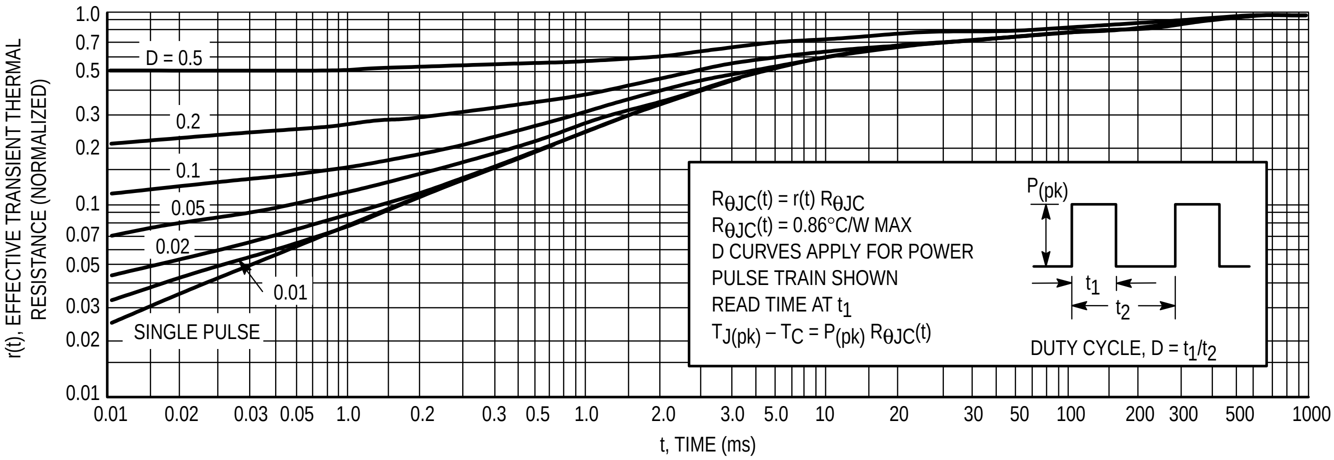


Figure 3. Thermal Response

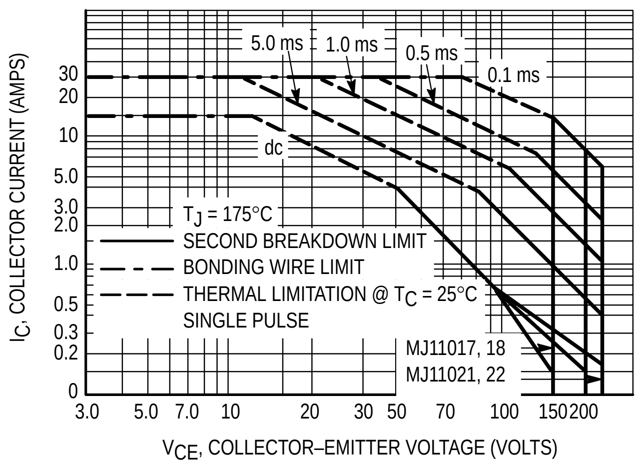


Figure 4. Maximum Rated Forward Bias Safe Operating Area (FBSOA)

FORWARD BIAS

There are two limitations on the power handling ability of a transistor average junction temperature and second breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 4 is based on $T_{J(pk)}$ = 175°C, T_C is variable dependIng on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 175°C. $T_{J(pk)}$ may be calculated from the data in Figure 3. At high case temperatures thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

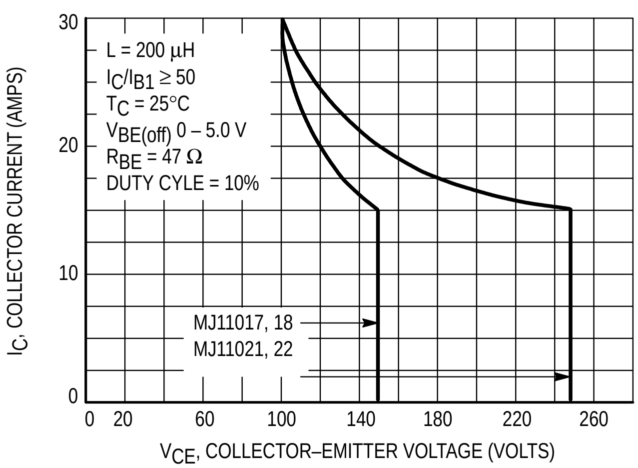


Figure 5. Maximum RBSOA, Reverse Bias Safe Operating Area

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be hold to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage–current conditions during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 5 gives ROSOA characteristics.

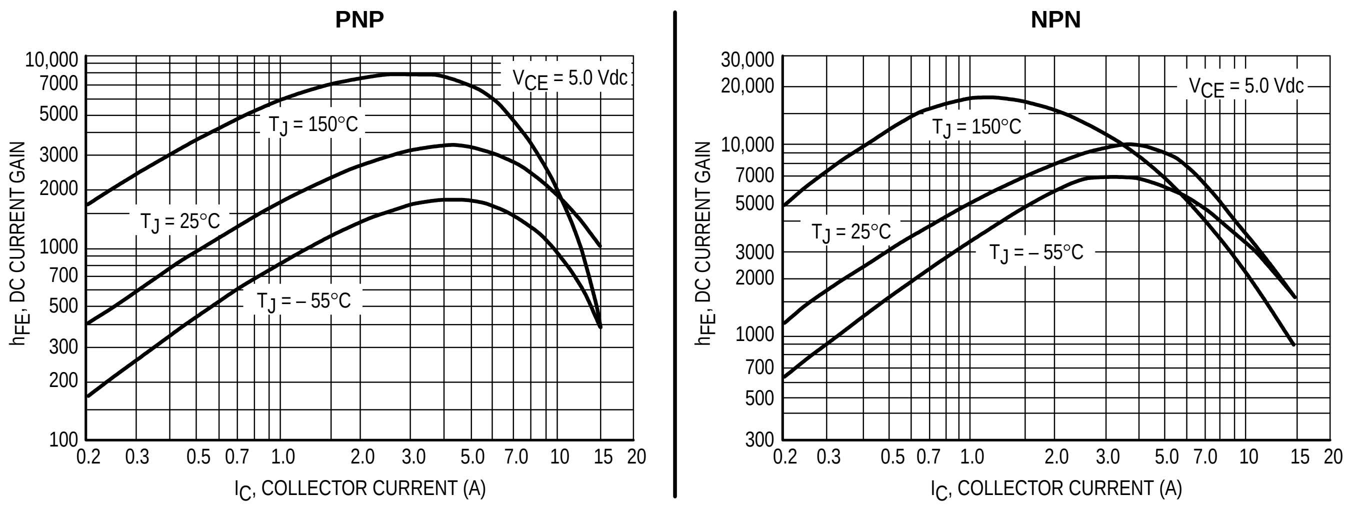


Figure 6. DC Current Gain

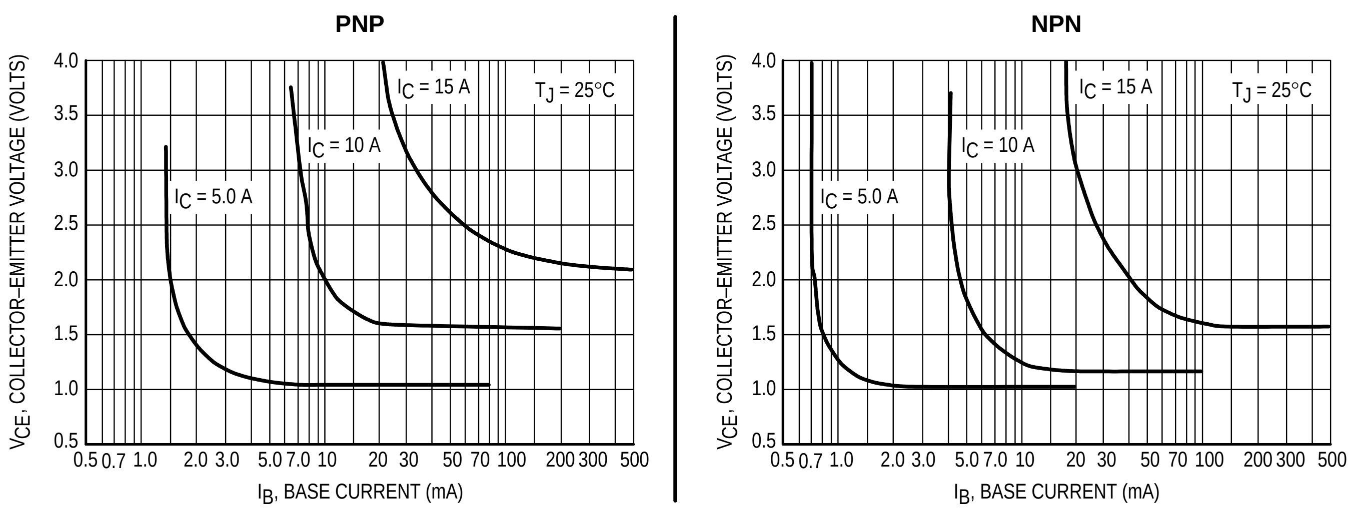


Figure 7. Collector Saturation Region

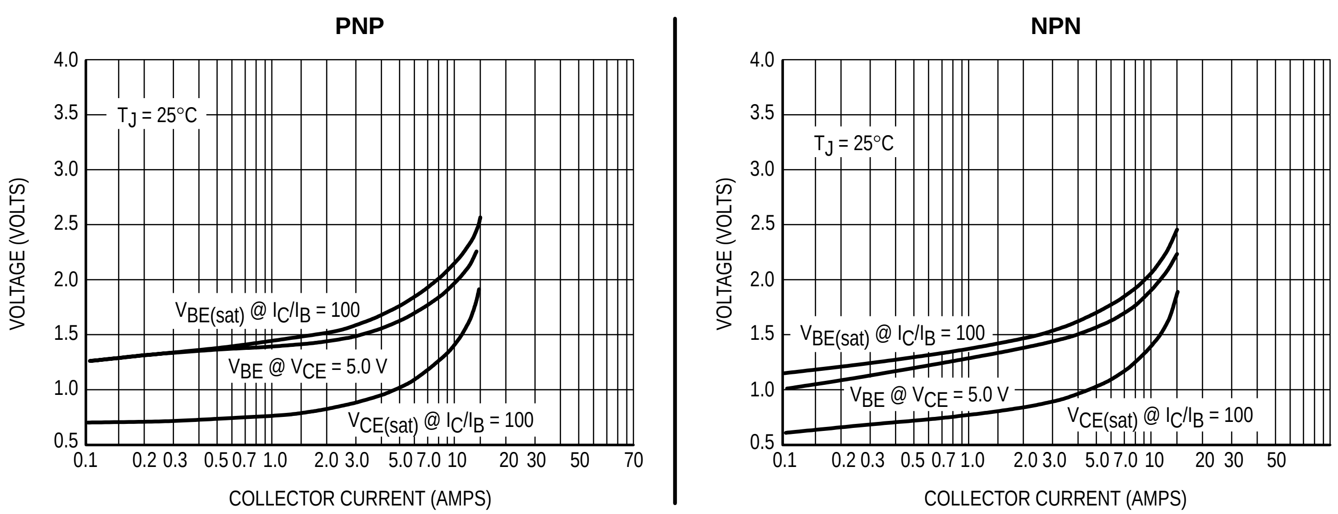
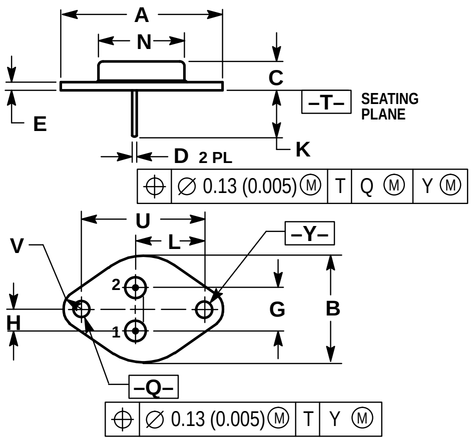


Figure 8. “On” Voltages

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO–204AA OUTLINE SHALL APPLY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.550 REF		39.37 REF	
B	—	1.050	—	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	—	0.830	—	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

CASE 1–07
TO–204AA (TO–3)
ISSUE Z

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