MK1449B
Sound/SCSI+Fast Ethernet Clock

Description

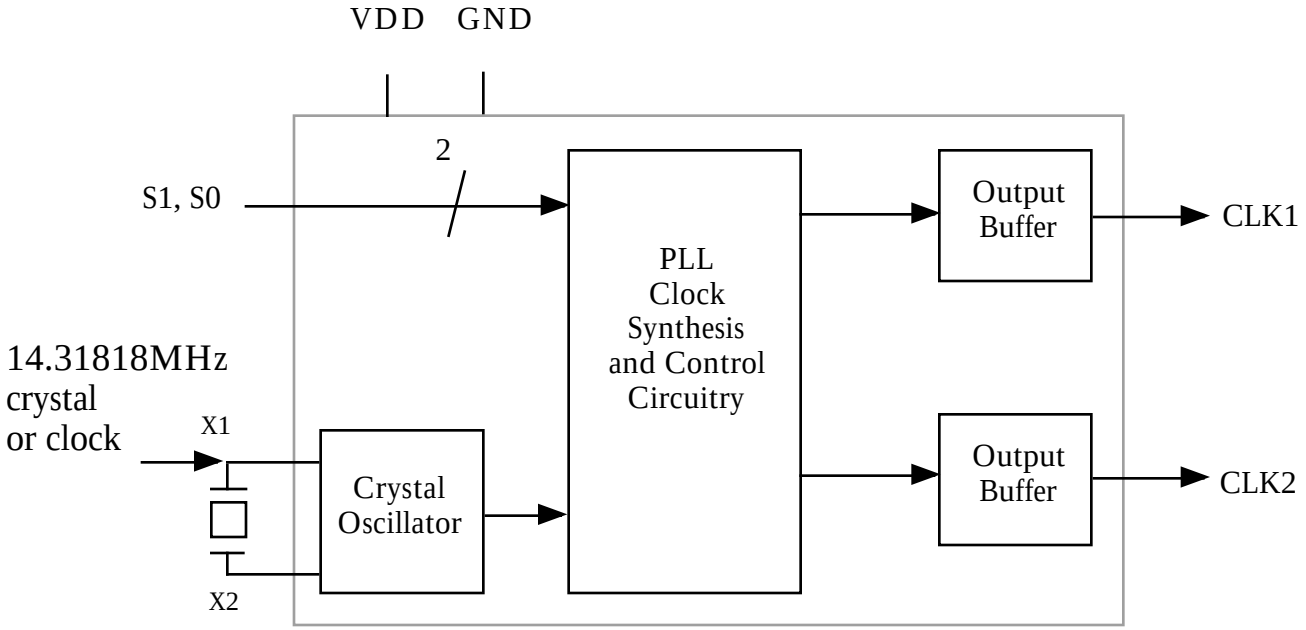
The MK1449B is the most cost effective way to generate high quality, high frequency clock outputs for SCSI plus Fast Ethernet devices, or AC97 sound chips. Using Phase-Locked-Loop (PLL) techniques, the device uses a standard fundamental mode, inexpensive 14.31818 MHz crystal or clock to produce two output clocks.

The device can accept either a crystal or clock input. Also on the chip is the ability to generate a 1.25x clock of the reference plus the reference, making it possible to generate 20 and 25 MHz clocks from a 20 MHz crystal.

Features

- Packaged as 8 pin SOIC
- For Fast Ethernet plus SCSI on computer motherboards
- For AC97 sound on computer motherboards
- Less than 1 ppm synthesis error
- Input crystal frequency of 14.31818 MHz
- Operating voltages of 3.0 to 5.5V
- Available in industrial temperature
- Full CMOS level outputs with 25mA drive capability at TTL levels
- Ideal for oscillator replacement
- Advanced, low power CMOS process

Block Diagram



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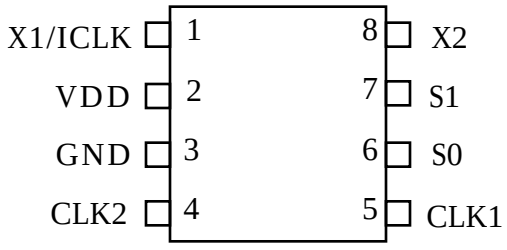
Pin Assignment



Clock Decoding Table (MHz)

S1	S0	CLK1	CLK2
0	0	test	test
0	1	40	25
1	0	49.152	12.288
1	1	x1.25	Reference

0 = connect directly to ground.
1 = connect directly to VDD.
In the 1,1 mode, crystals or clocks from 5 to 27 MHz can be used as an input.

Pin Descriptions

Number	Name	Type	Description
1	X1/ICLK	I	Crystal connection or clock input. Connect to a 14.31818MHz parallel resonant crystal.
2	VDD	P	Connect to +3.3V or +5V.
3	GND	P	Connect to ground.
4	CLK2	O	Clock 2 output per Table above.
5	CLK1	O	Clock 1 output per Table above.
6	S0	I	Select 0 for output clocks. Connect to GND or VDD. See table above.
7	S1	I	Select 1 for output clocks. Connect to GND or VDD. See table above.
8	X2	O	Crystal connection to a 14.31818 MHz crystal. Leave unconnected for clock input.

Key: I = Input, O = output, P = power supply connection

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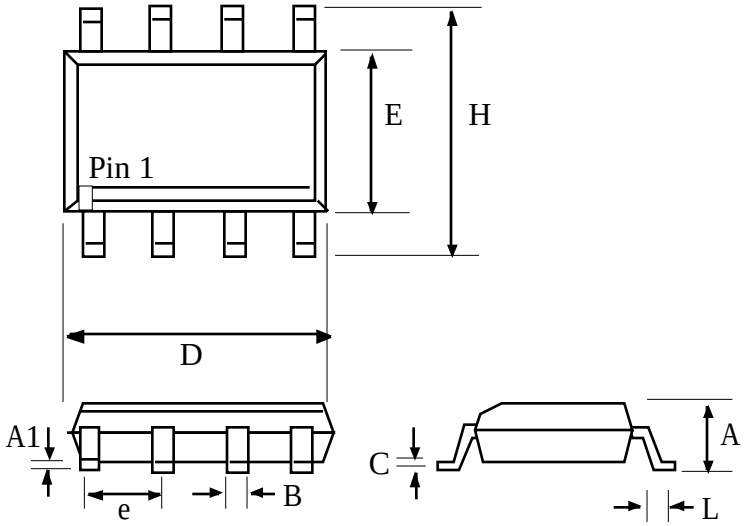
Electrical Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Units
ABSOLUTE MAXIMUM RATINGS (stresses beyond these can permanently damage the device)					
Supply Voltage, VDD	Referenced to GND			7	V
Inputs	Referenced to GND	-0.5		VDD+0.5	V
Clock Output	Referenced to GND	-0.5		VDD+0.5	V
Ambient Operating Temperature		0		70	°C
	Industrial temperature	-40		85	°C
Soldering Temperature	Max of 10 seconds			260	°C
Storage temperature		-65		150	°C
DC CHARACTERISTICS (VDD = 3.3V unless otherwise noted)					
Operating Voltage, VDD		3		5.5	V
Input High Voltage, VIH, ICLK only	ICLK (Pin 1)	(VDD/2)+1	VDD/2		V
Input Low Voltage, VIL, ICLK only	ICLK (Pin 1)		VDD/2	(VDD/2)-1	V
Input High Voltage, VIH	S0, S1	VDD-0.5			V
Input Low Voltage, VIL	S0, S1			0.5	V
Output High Voltage, VOH	IOH=-25mA	2.4			V
Output Low Voltage, VOL	IOL=25mA			0.4	V
IDD Operating Supply Current, 5V	No Load, 25, 40MHz		18		mA
IDD Operating Supply Current, 3.3V	No Load, 25, 40MHz		10		mA
Short Circuit Current	CLK output		±70		mA
On-Chip Pull-up Resistor	Pin 7		270		kΩ
Input Capacitance, S1, S0	Pins 6, 7		4		pF
AC CHARACTERISTICS (VDD = 3.3V unless otherwise noted)					
Input Frequency, crystal input		10	14.31818	27	MHz
Input Frequency, clock input		10	14.31818	50	MHz
Output Frequency	VDD = 3.0 to 5.5V	10		75	MHz
Output Clock Rise Time	0.8 to 2.0V		1		ns
Output Clock Fall Time	2.0 to 0.8V		1		ns
Output Clock Duty Cycle	at VDD/2	40	49 to 51	60	%
Synthesis error, 25, 40 MHz				1	ppm
Synthesis error, 12.288, 49.152 MHz				1	ppm
Absolute Clock Period Jitter, 20 pF load	Deviation from mean		±240		ps
One Sigma Clock Period Jitter, 20 pF load			100		ps

External Components / Crystal Selection

The MK1449B requires a 0.01µF decoupling capacitor to be connected between VDD and GND. It must be connected close to the MK1449B to minimize lead inductance. No external power supply filtering is required for this device. 33Ω terminating resistors can be used next to the CLK pins. The total on-chip capacitance is approximately 13 pF, so a parallel resonant, fundamental mode crystal should be used. For crystals with a specified load capacitance greater than 13 pF, crystal capacitors should be connected from each of the pins X1 and X2 to ground. The value (in pF) of these crystal caps should be = $(C_L-13)*2$, where C_L is the crystal load capacitance in pF. These external capacitors are only required for applications where the exact frequency is critical. For a clock input, connect to X1 and leave X2 unconnected (no capacitors on either).

Package Outline and Package Dimensions (For current dimensional specifications, see JEDEC pub. no. 95)



8 pin SOIC

	Inches		Millimeters	
Symbol	Min	Max	Min	Max
A	0.053	0.069	1.35	1.75
A1	0.004	0.0098	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.0075	0.0098	0.19	0.25
D	0.189	0.197	4.80	5.00
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
e	.050 BSC		1.27 BSC	
L	0.016	0.05	0.41	1.27

Ordering Information

Part/Order Number	Marking	Package	Temperature
MK1449S	MK1449S	8 pin SOIC	0 to 70 °C
MK1449STR	MK1449S	8 pin SOIC on tape and reel	0 to 70 °C
MK1449SI	MK1449SI	8 pin SOIC	-40 to 85 °C
MK1449SITR	MK1449SI	8 pin SOIC on tape and reel	-40 to 85 °C