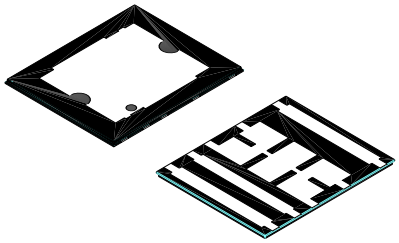
STK850

N-CHANNEL 30V - 0.0024 Ω - 30A - PolarPAK™ STripFET™ Power MOSFET

General features

Type	V_{DSS}	$R_{DS(on)}$	$R_{DS(on)}*Q_g$	P_{TOT}
STK850	30V	<0.0029Ω	58.8 nC*mΩ	5.2W

- ULTRA LOW TOP AND BOTTOM JUNCTION TO CASE THERMAL RESISTANCE
- VERY LOW CAPACITANCES
- 100% R_g TESTED
- FULLY INCAPSULATED DIE
- IN COMPLIANCE WITH THE 2002/95/EC EUROPEAN DIRECTIVE

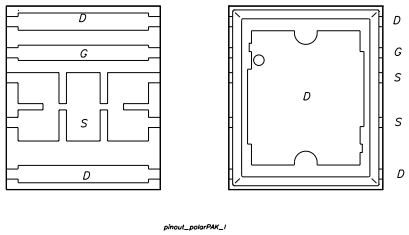


PolarPAK™

Description

This MOSFET is the latest development of STMicroelectronics unique “Single Feature Size™” strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, moreover the double sides cooling package with ultra low junction to case thermal resistance allows to handle higher levels of current.

Internal schematic diagram



Bottom View Top View

Applications

- HIGH CURRENT VRM
- SINCHRONOUS RECTIFICATION
- DC-DC CONVERTERS FOR TELECOM

Order codes

Sales Type	Marking	Package	Packaging
STK850	K850	PolarPAK™	TAPE & REEL

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage (V_{GS} = 0)	30	V
V_{GS}	Gate-Source Voltage	± 16	V
I_D *Note* 2	Drain Current (continuous) at T_C = 25°C	30	A
I_D	Drain Current (continuous) at T_C = 100°C	18.75	A
I_{DM} *Note* 1	Drain Current (pulsed)	120	A
P_{TOT} *Note* 2	Total Dissipation at T_C = 25°C	5.2	W
	Derating Factor	0.0416	W/°C
T_j T_{stg}	Operating Junction Temperature Storage Temperature	-55 to 150	°C

Table 2. Thermal data

		Typ.	Max	Unit
Rthj-amb *Note* 2	Thermal Resistance Junction-amb	20	24	°C/W
Rthj-c *Note* 3	Thermal Resistance Junction-case (Top Drain)	0.8	1	°C/W
Rthj-c *Note* 4	Thermal Resistance Junction-case (Source)	2.2	2.7	°C/W

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	I_D = 250µA, V_{GS}= 0	30			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating, V_{DS} = Max Rating,Tc=125°C			1 10	µA µA
I_{GSS}	Gate Body Leakage Current (V_{DS} = 0)	V_{GS} = ±16V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}= V_{GS}, I_D = 250µA	1		2.5	V
$R_{DS(on)}$	Static Drain-Source On Resistance	V_{GS}= 10V, I_D= 15A V_{GS}= 4.5V, I_D= 15A		0.0024 0.0029	0.0029 0.0035	Ω Ω

Table 4. Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} *Note* 5	Forward Transconductance	V_{DS} =10V, I_D = 15A		48		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} =25V, f=1 MHz, V_{GS}=0		3150 940 90		pF pF pF
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD}=15V, I_D = 30A V_{GS} =4.5V (see Figure 14)		24.5 8 8.2	32.5	nC nC nC

Table 5. Switching times

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD}= 15V, I_D= 15A, R_G=4.7Ω, V_{GS}=4.5V (see Figure 15)		20 57		ns ns
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	V_{DD}=15V, I_D= 15A, R_G=4.7Ω, V_{GS}=4.5V (see Figure 15)		31 13		ns ns

Table 6. Source drain diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} *Note* 1	Source-drain Current Source-drain Current (pulsed)				30 120	A A
V_{SD} *Note* 5	Forward on Voltage	I_{SD}= 15A, V_{GS}=0			1.2	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD}= 30A, di/dt = 100A/µs, V_{DD}=20V, Tj=150°C (see Figure 15)		39 39.8 2		ns nC A

(1)Pulse width limited by package

(2) When mounted on FR-4 board of 1inch^2 , 2 oz Cu and ≤ 10sec

(3) Steady State

(4) Measured at Source pin when the device is mounted on FR-4 board in steady state

(5) Pulsed: pulse duration = 300µs, duty cycle 1.5%

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2.1 Electrical characteristics (curves)

Figure 1. Safe Operating Area

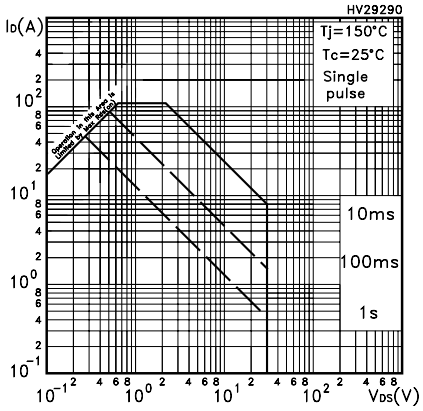


Figure 2. Thermal Impedance

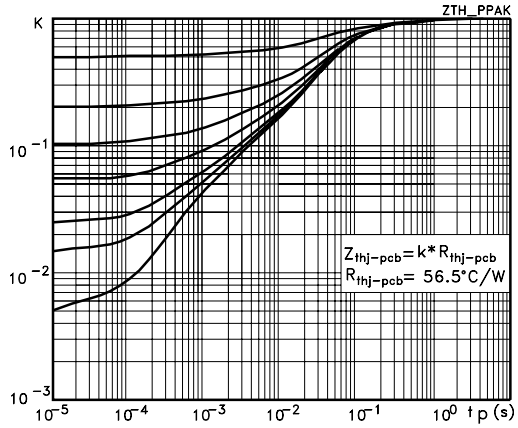


Figure 3. Output Characteristics

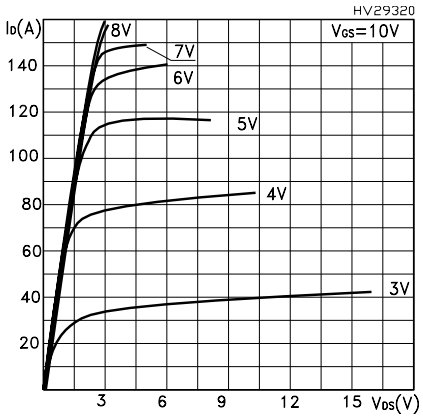


Figure 4. Transfer Characteristics

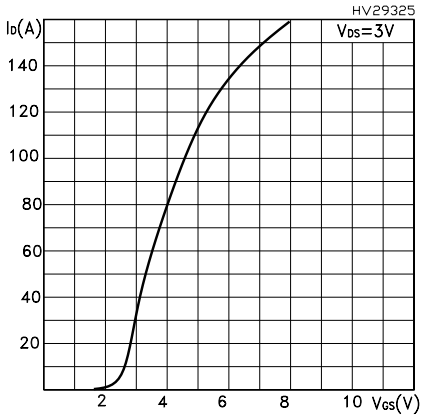


Figure 5. Transconductance

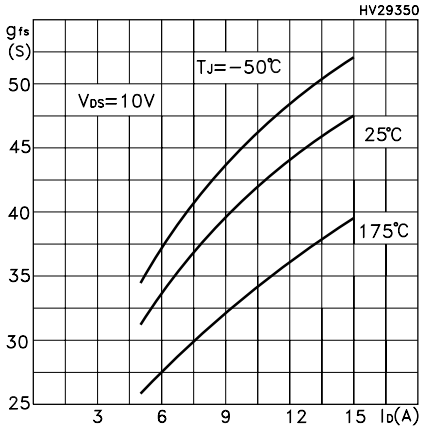


Figure 6. Static Drain-source on Resistance

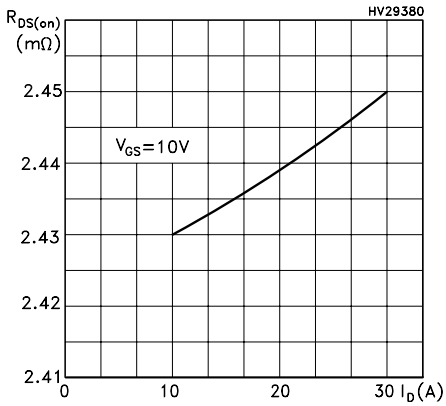


Figure 7. Gate Charge

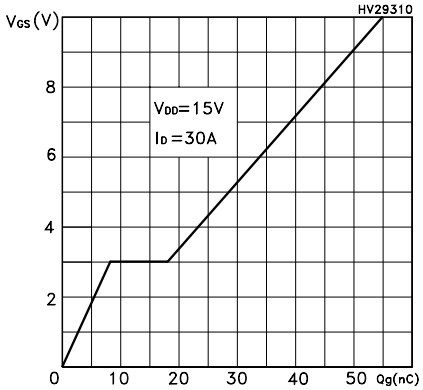


Figure 8. Capacitance Variations

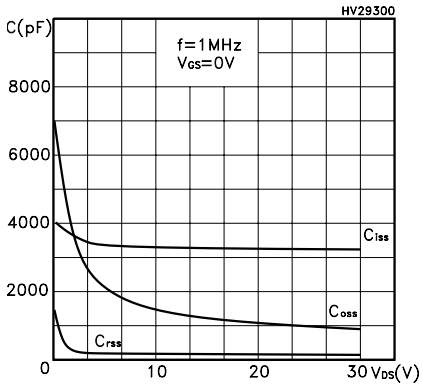


Figure 9. Normalized Gate Threshold Voltage vs Temperature

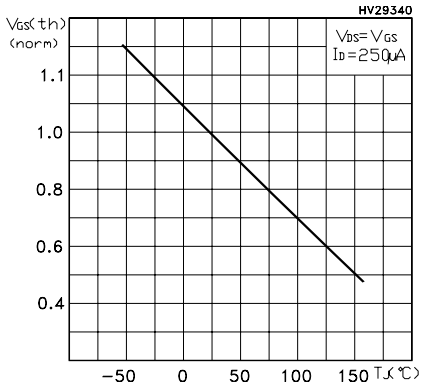


Figure 10. Normalized On Resistance vs Temperature

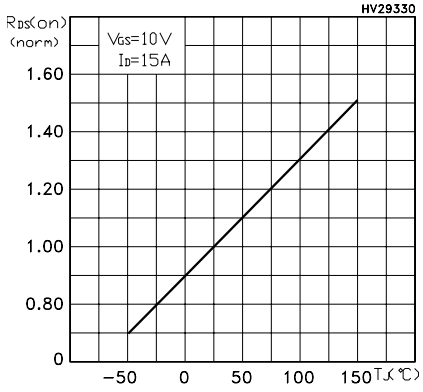


Figure 11. Source-drain Diode Forward Characteristics

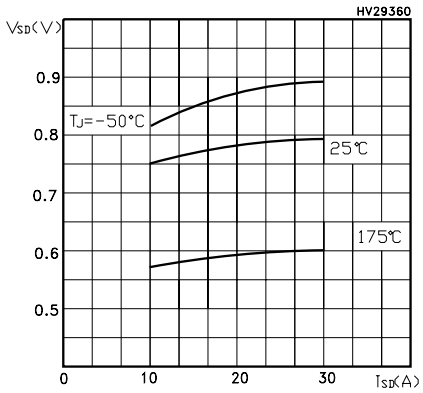
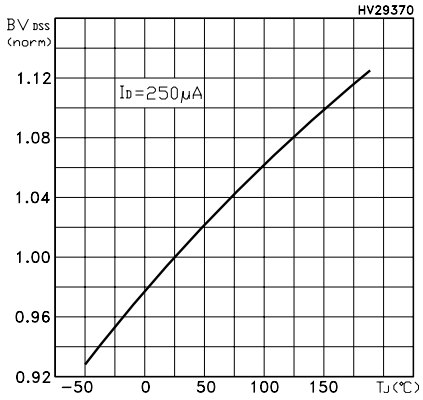


Figure 12. Normalized BVDSS vs Temperature



3 Test circuits

Figure 13. Switching Times Test Circuit For Resistive Load

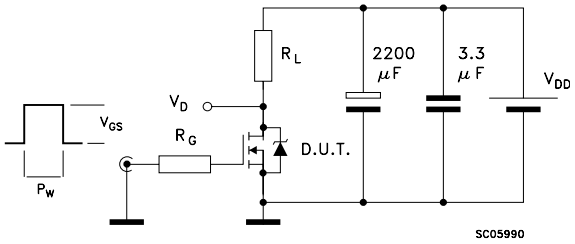


Figure 14. Gate Charge Test Circuit

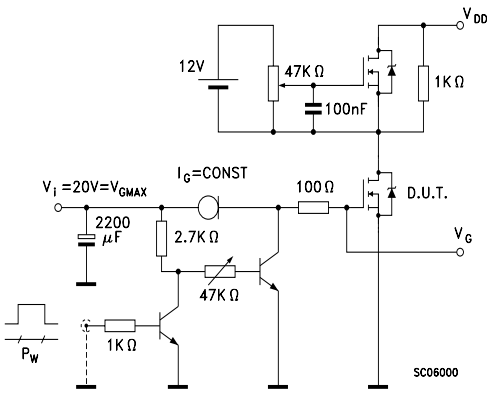
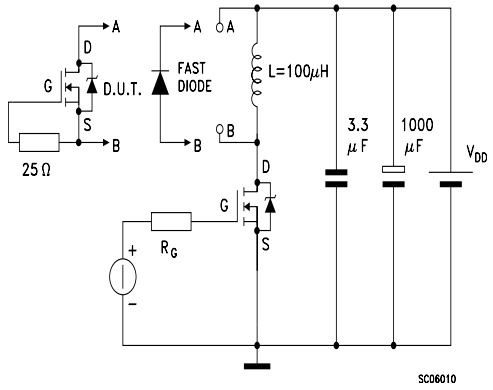


Figure 15. Test Circuit For Inductive Load Switching and Diode Recovery Times



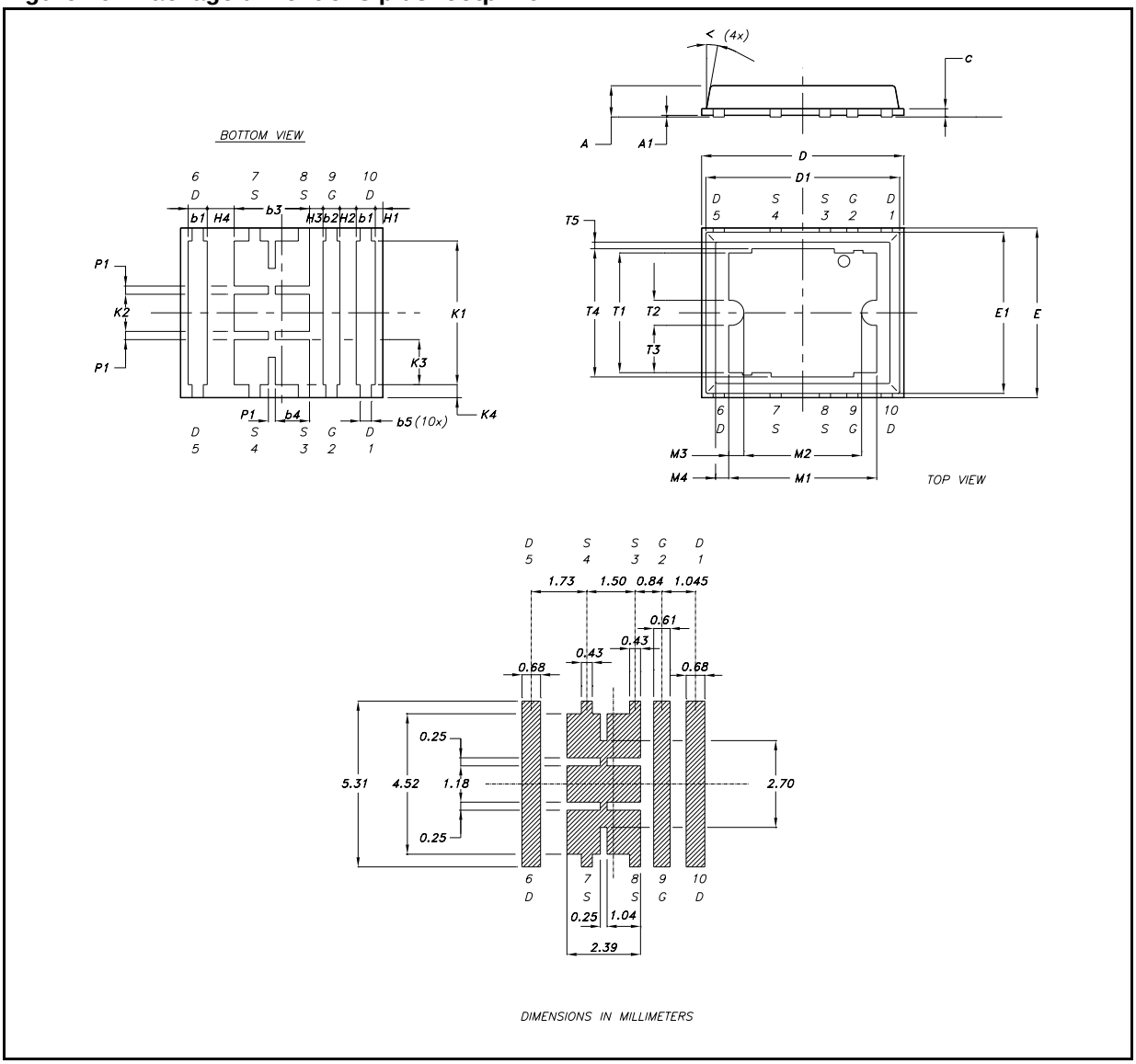
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Table 7. PolarPAK (Option L) mechanical data

Ref	Dimensions					
	Millimiters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.75	0.80	0.85	0.030	0.031	0.033
A1			0.05			0.002
b1	0.48	0.58	0.68	0.019	0.023	0.027
b2	0.41	0.51	0.61	0.016	0.020	0.024
b3	2.19	2.29	2.39	0.086	0.090	0.094
b4	0.89	1.04	1.19	0.035	0.041	0.047
b5	0.23	0.33	0.43	0.009	0.013	0.017
c	0.20	0.25	0.30	0.008	0.010	0.012
D	6	6.15	6.30	0.236	0.242	0.248
D1	5.74	5.89	6.04	2.226	2.232	0.238
E	5.01	5.16	5.31	0.197	0.203	0.209
E1	4.75	4.90	5.05	0.187	0.193	0.199
H1	0.23			0.009		
H2	0.45		0.56	0.020		0.022
H3	0.31	0.41	0.51	0.012	0.016	0.020
H4	0.45		0.56	0.020		0.022
K1	4.22	4.37	4.52	0.166	0.172	0.178
K2	1.08	1.13	1.18	0.043	0.044	0.046
K3	1.37			0.054		
K4	0.24			0.009		
M1	4.30	4.50	4.70	0.169	0.177	0.185
M2	3.43	3.58	3.73	0.135	0.141	0.147
M3	0.22			0.009		
M4	0.05			0.002		
P1	0.15	0.20	0.25	0.006	0.008	0.010
T1	3.48	3.64	4.10	0.137	0.143	0.150
T2	0.56	0.76	0.95	0.022	0.030	0.037
T3	1.20			0.051		
T4	3.90			0.154		
T5		0.18	0.36		0.007	0.014
<	0°	10°	12°	0°	10°	12°

Figure 16. Package dimentions plus footprint



5 Revision History

Date	Revision	Changes
10-Nov-2005	1	First version
19-Dec-2005	2	Complete version
02-Feb-2006	3	Modified description on first page, mechanical data updated