WT8801

Specification

V0.9

9/10/2001

1. Features

Digital Input Support

- 24 bit RGB input
- 8/16 bit YUV 4:2:2 Video input support
- CCIR601/656 support with built-in YUV to RGB color space converter
- DDWG/DVI1.0 compliant

High Quality Scaling Engine

- Fully programmable zoom ratios
- Independent Horizontal/Vertical scale
- Advanced de-interlacing algorithm for digital YUV video
- Enhanced sharpness filter for better text support
- Spatial color dithering algorithm to 16.7 million color
- Digital Brightness/Contrast adjustment

Output Support

- Single (18/24) or Dual (36/48) pixel output
- Support Multiple TFT LCD Panel
- Support VGA/SVGA/XGA/SXGA display resolution

OSD and Gamma Correction Support

- Fully programmable OSD Engine
- Downloadable font storage for internal OSD
- 32 Multi-Color fonts
- Glue less interface for external OSD chip
- User programmable 10-bit Gamma table

Display Synchronization

- Advanced Input mode detection
- Automatic Input Edge Adjustment
- Automatic Input Phase Calibration

Low System Cost Solution

- Plug and Display, support VGA mode up to 1280x1024 @ 60hz
- Support up to 135MHz incoming pixel clock
- Single-chip scaler solution. No external frame buffer required
- 2-wire I^2C serial interface for EEPROM and Micro-controller
- Glue less interface to external ADC/PLL or TMDS chip

- Power Management support

Electrical/Physical Specification

- 1P4M 0.25um CMOS process
- 3.3V pad power supply with 5V I/O tolerant, 2.5V core power supply
- Low cost 128 pin LQFP Package
- 96.6% fault coverage with scan test

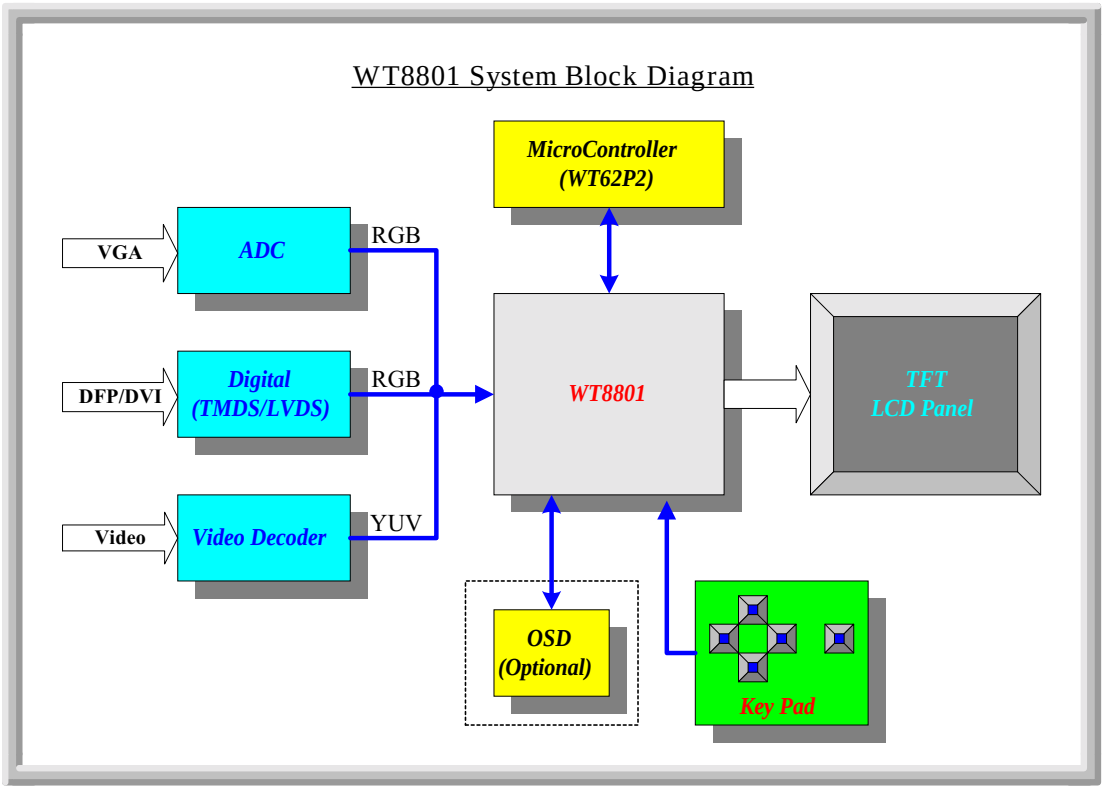
2. Overview

The WT8801 LCD (Liquid Crystal Display) Monitor Controller is an input format converter for the TFT-LCD Panels or LCD-TV applications. It accepts digtal signals from ADC's RGB output, YUV from digital video decoder or digital RGB graphics from PanelLink TMDS receiver and transforms these signals to TFT-LCD panel to display. The WT8801 performs image scaling on 24bit RGB or YUV data stream and feeds these scaled pixels to the output LCD panel. When displaying the image, instead of using external memory chips for scaling and temporary storage, the chip is using embedded line buffers such that the total system cost can be kept to minimum.

In order to provide the plug-n-display, the chip also performs functions like automatic input mode detection and automatic phase calibration. This is designed to keep the sampling clock of ADC is synchronized with the incoming data so that the final image in the LCD panel is free of distortion. The chip also provides the circuitry for contrast / brightness adjustment and gamma tables for intensity correction.

The chip is packaged in a cost-effective 128-pin LQFP Package.

Figure 1 shows a system configuration for the chip.



3. Signal Definitions

3.1 Pin Listing & Description

Symbol	Pin No	Type	Function Description
D_HS	1	I	Horizontal Sync from TMDS receiver
D_VS	2	I	Vertical Sync from TMDS receiver
VGA_HS	3	I	Horizontal Sync from VGA
VDD	4	P	Core Power (2.5V)
VGA_VS	5	I	Vertical Sync from VGA
VGA_DE	6	I	Data enable from TMDS receiver
VGA_CK	7	I	Pixel clock from ADC/TMDS receiver
VSS	8	G	System Ground
DR[0]	9	I	Digital Red Input Data Port Bit 0
DR[1]	10	I	Red Bit 1
DR[2]	11	I	Red Bit 2
DR[3]	12	I	Red Bit 3
VSS	13	G	System Ground
DR[4]	14	I	Red Bit 4
DR[5]	15	I	Red Bit 5
DR[6]	16	I	Red Bit 6
DR[7]	17	I	Red Bit 7
PVDD	18	P	Pad Power (3.3V)
DG[0]	19	I	Digital Green Input Data Port Bit 0 || Y Input Data for 16 Bit
DG[1]	20	I	Green Bit 1 || Y1
DG[2]	21	I	Green Bit 2 || Y2
DG[3]	22	I	Green Bit 3 || Y3
DG[4]	23	I	Green Bit 4 || Y4
VDD	24	P	Core Power (2.5V)
DG[5]	25	I	Green Bit 5 || Y5
DG[6]	26	I	Green Bit 6 || Y6
DG[7]	27	I	Green Bit 7 || Y7
DB[0]	28	I	Digital Blue Input Data Port Bit 0 || UV0 Blue Input Data Port A || UV Input Data for 16 Bit
DB[1]	29	I	Blue Bit 1 || UV1
VSS	30	G	System Ground
DB[2]	31	I	Blue Bit 2 || UV2
DB[3]	32	I	Blue Bit 3 || UV3
DB[4]	33	I	Blue Bit 4 || UV4
VSS	34	G	System Ground
DB[5]	35	I	Blue Bit 5 || UV5
DB[6]	36	I	Blue Bit 6 || UV6
DB[7]	37	I	Blue Bit 7 || UV7
AVSS	38	G	PLL Ground
AVDD	39	P	PLL Power (2.5V)
FPDR0	40	O	Display Red Output Data Port Bit 0
FPDR1	41	O	Red Bit 1

FPDR2	42	O	Red Bit 2
PVDD	43	P	Pad Power (3.3V)
FPDR3	44	O	Red Bit 3
FPDR4	45	O	Red Bit 4
FPDR5	46	O	Red Bit 5
FPDR6	47	O	Red Bit 6
FPDR7	48	O	Red Bit 7
FPDG0	49	O	Display Green Output Data Port Bit 0
VSS	50	G	System Ground
VDD	51	P	Core Power (2.5V)
FPDG1	52	O	Green Bit 1
FPDG2	53	O	Green Bit 2
FPDG3	54	O	Green Bit 3
FPDG4	55	O	Green Bit 4
PVDD	56	P	Pad Power (3.3V)
FPDG5	57	O	Green Bit 5
FPDG6	58	O	Green Bit 6
FPDG7	59	O	Green Bit 7
FPDB0	60	O	Display Blue Output Data Port Bit 0
FPDB1	61	O	Blue Bit 1
VSS	62	G	System Ground
FPDB2	63	O	Blue Bit 2
FPDB3	64	O	Blue Bit 3
FPDB4	65	O	Blue Bit 4
FPDB5	66	O	Blue Bit 5
FPDB6	67	O	Blue Bit 6
PVDD	68	P	Pad Power (3.3V)
FPDB7	69	O	Blue Bit 7
PDE	70	O	Display Enable (active area of display)
PVS	71	O	Flat Panel FRAME Signal (Display Vertical Sync)
PHS	72	O	Flat Panel Line Signal (Display Horizontal Sync)
PCK	73	O	Flat Panel Shift Clock (Flat Panel Pixel Clock)
VSS	74	G	System Ground
FPDR8	75	O	Display Red Output Data Port Bit 8
FPDR9	76	O	Red Bit 9
FPDR10	77	O	Red Bit 10
VDD	78	P	Core Power (2.5V)
FPDR11	79	O	Red Bit 11
FPDR12	80	O	Red Bit 12
PVDD	81	P	Pad Power (3.3V)
FPDR13	82	O	Red Bit 13
FPDR14	83	O	Red Bit 14
FPDR15	84	O	Red Bit 15
FPDG8	85	O	Display Blue Output Data Port Bit 0
FPDG9	86	O	Green Bit 9
VSS	87	G	System Ground
FPDG10	88	O	Green Bit 10
FPDG11	89	O	Green Bit 11
FPDG12	90	O	Green Bit 12
FPDG13	91	O	Green Bit 13
FPDG14	92	O	Green Bit 14

PVDD	93	P	Pad Power (3.3V)
FPDG15	94	O	Green Bit 15
FPDB8	95	O	Display Blue Output Data Port Bit 8
VDD	96	P	Core Power (2.5V)
FPDB9	97	O	Blue Bit 9
FPDB10	98	O	Blue Bit 10
FPDB11	99	O	Blue Bit 11
VSS	100	G	System Ground
FPDB12	101	O	Blue Bit 12
FPDB13	102	O	Blue Bit 13
FPDB14	103	O	Blue Bit 14
FPDB15	104	O	Blue Bit 15
PWM	105	O	Pulse Width Modulation
PVDD	106	P	Pad Power (3.3V)
DDC_SDA	107	I/O	DDC Serial Interface data
DDC_SCL	108	I/O	DDC Serial Interface clock
CPU_SDA	109	I/O	CPU Serial Interface data
CPU_SCL	110	I/O	CPU Serial Interface clock
INTB	111	I	CPU Interrupt
RESET	112	I	System Reset signal
OVR	113	I	External OSD Red signal
OVG	114	I	External OSD Green signal
VDD	115	P	Core Power (2.5V)
VSS	116	G	System Ground
TMS	117	I	Test Mode Select 0: Normal operation 1: Test Mode
OVB	118	I	External OSD Blue signal
OVI	119	I	External OSD Intensity signal
OVFB	120	I	Overlay enable from external OSD chip
VCK2	121	I/O	Video Clock 2
TV_CK	122	I	Clock from NTSC/PAL Decoder
TV_HS	123	I	VREF from NTSC/PAL Decoder
TV_VS	124	I	HREF from NTSC/PAL Decoder
PVDD	125	P	Pad Power (3.3V)
OSCO	126	O	14.318MHz Xtal Output
OSCI	127	I	14.318MHz Xtal Input
VSS	128	G	System Ground

Note: All input pins have internal pull down

3.2 Pin Diagram