



PRELIMINARY

**CYM74BP54
CYM74P54/55
CYM74SP54/55**

Intel® 82430NX Chipset Level II Cache Module Family

Features

- Pin-compatible secondary cache module family
- Asynchronous (CYM74BP54), synchronous pipelined (CYM74P54, CYM74P55), or synchronous (CYM74SP54, CYM74SP55) configurations with presence and configuration detect pins
- Ideal for Intel® P54C-based systems with the 82430NX (Neptune) chipset
- Operates at 60 and 66 MHz
- Uses cost-effective CMOS asynchronous SRAMs or high-performance synchronous SRAMs
- 160-position Burndy DIMM CELP2X80SC3Z48 connector
- 3.3V inputs/outputs

Functional Description

This family of secondary cache modules is designed for Intel P54C systems with the 82430NX (Neptune) chipset.

CYM74BP54 is an asynchronous 256-Kbyte cache module that provides a low-cost, high-performance solution with in-

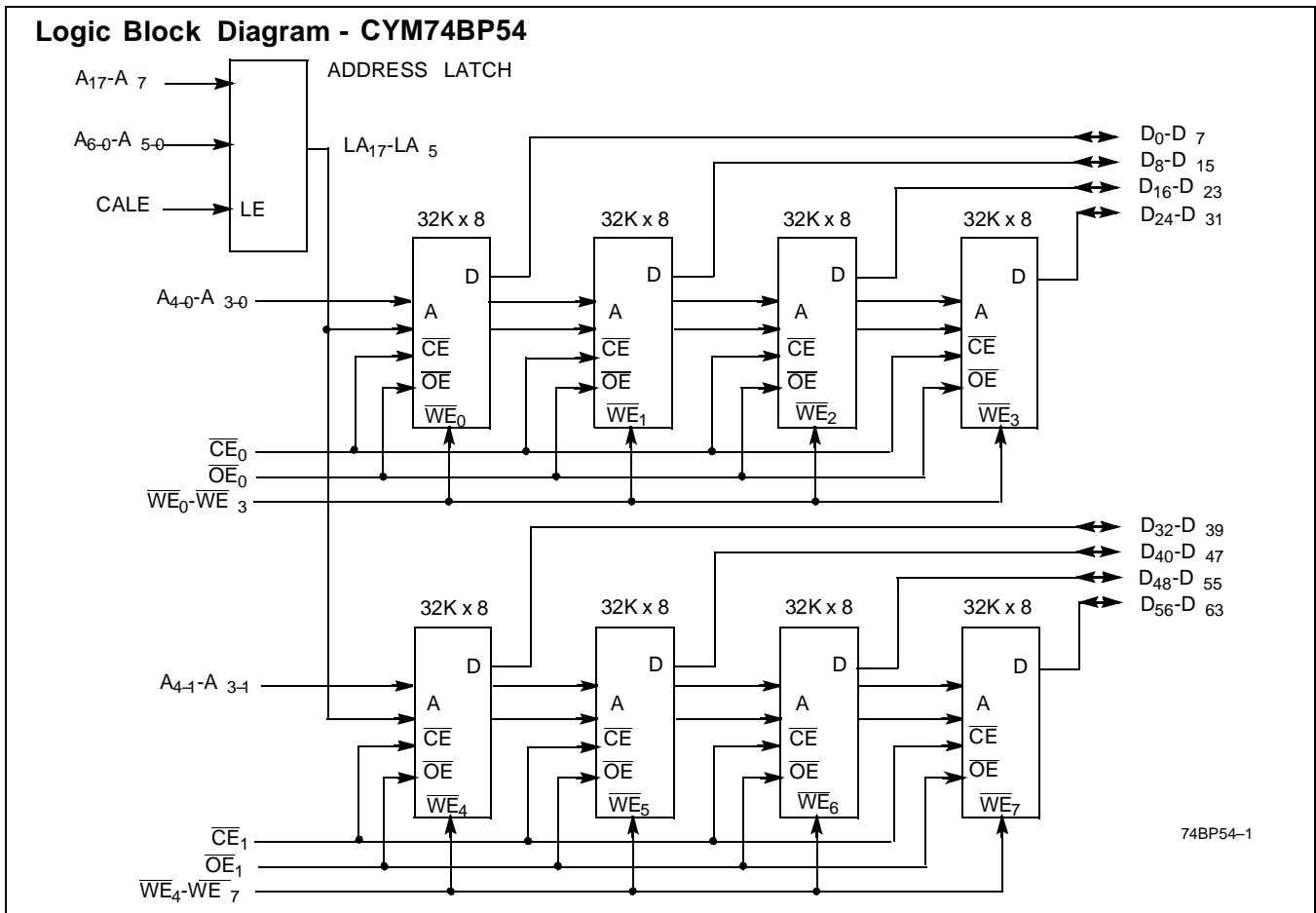
dustry standard 5V SRAMs and 3.3V level translators for CPU bus speeds up to 66 MHz. The CYM74BP54 is organized as 32K by 64-bits.

The synchronous modules are available with low-cost synchronous pipelined RAMs or higher performance synchronous burst RAMs. The synchronous pipelined modules are based on a 16Kx64 RAM. The CYM74P54 is a 256-KB module while the CYM74P55 is a 512-KB module. Both are modules without byte parity.

The CYM74SP54 and CYM74SP55 are synchronous burst cache modules that provide zero wait-state performance at a bus speed of 66 MHz. The CYM74SP54 is a 256-Kbyte cache module with byte parity. The CYM74SP55 is a 512-Kbyte cache module with byte parity.

Multiple ground pins and on-board decoupling capacitors ensure high performance with maximum noise immunity.

All components on the cache modules are surface mounted on a multi-layer epoxy laminate (multifunctional) substrate. The contact pins are plated with 150 micro-inches of nickel covered by 10 micro-inches of gold flash.



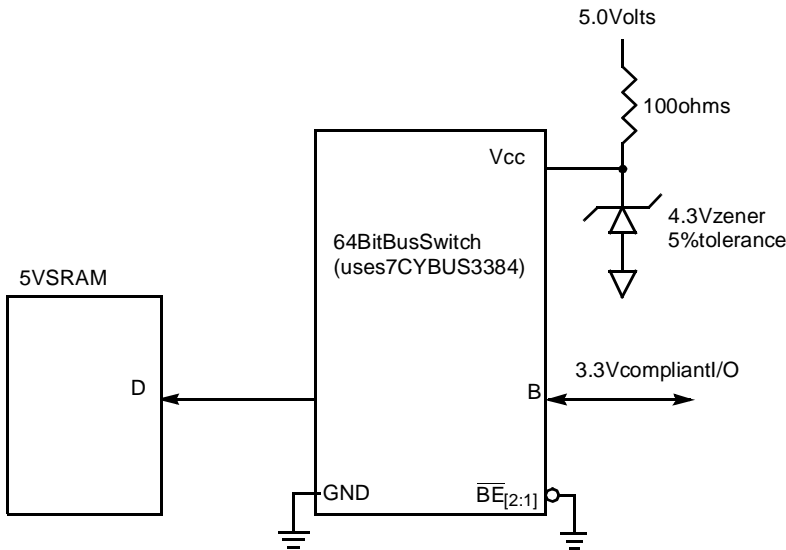
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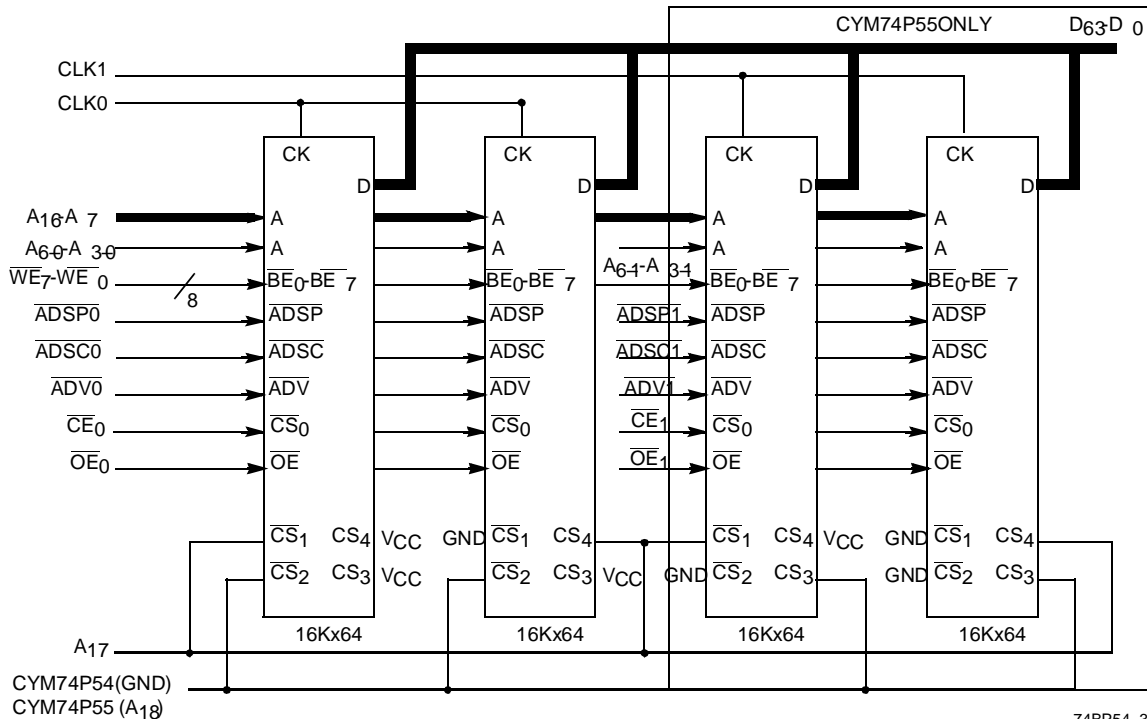
Block Diagram: 5V to 3.3V Level Conversion (CYM74BP54)



74BP54-2

Logic Block Diagram - CYM74P54, CYM74P55

| | PD ₂ | PD ₁ | PD ₀ |
|----------|-----------------|-----------------|-----------------|
| CYM74P54 | TBD | TBD | TBD |
| CYM74P55 | TBD | TBD | TBD |

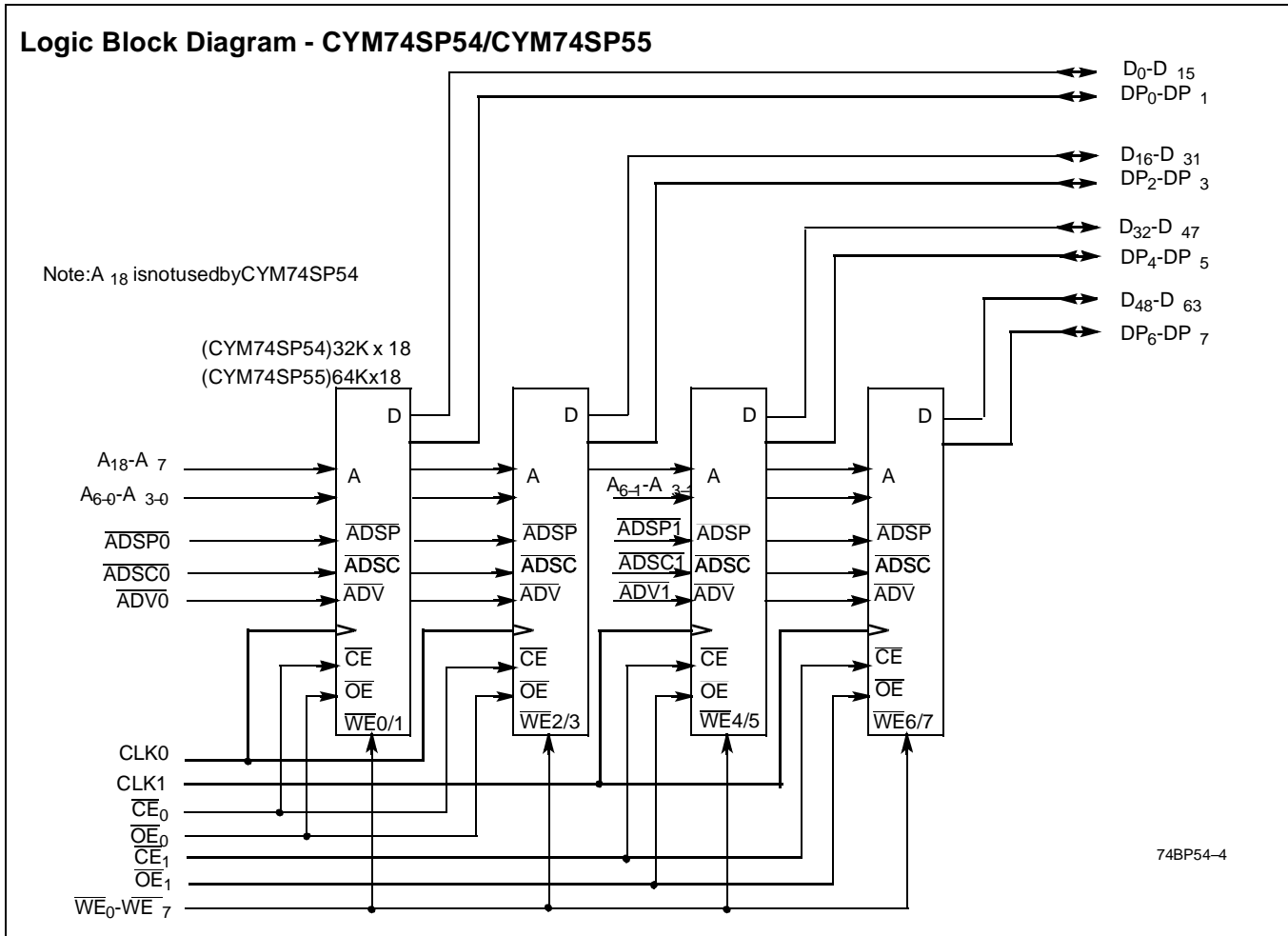


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PRELIMINARY

**CYM74BP54
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CYM74SP54/55**



Selection Guide

| Part Number | Asynchronous Cache Modules | |
|--------------------|----------------------------|------------------------|
| | CYM74BP54-60 | CYM74BP54-66 |
| Cache Size (KB) | 256 | |
| System Clock (MHz) | 60 | 66 |
| RAM Speed | t _{AA} =15 ns | t _{AA} =12 ns |

| Part Number | Synchronous Pipelined Cache Modules | | | |
|--------------------|-------------------------------------|--------------------------|---------------------------|--------------------------|
| | CYM74P54-60 | CYM74P54-66 | CYM74P55-60 | CYM74P55-66 |
| Cache Size (KB) | 256 | | 512 | |
| System Clock (MHz) | 60 | 66 | 60 | 66 |
| RAM Speed | t _{CDV} =10.5 ns | t _{CDV} =8.5 ns | t _{CDV} =10.5 ns | t _{CDV} =8.5 ns |

| Part Number | Synchronous Burst Cache Modules | | | |
|--------------------|---------------------------------|--------------------------|---------------------------|--------------------------|
| | CYM74SP54-60 | CYM74SP54-66 | CYM74SP55-60 | CYM74SP55-66 |
| Cache Size (KB) | 256 | | 512 | |
| System Clock (MHz) | 60 | 66 | 60 | 66 |
| RAM Speed | t _{CDV} =10.5 ns | t _{CDV} =8.5 ns | t _{CDV} =10.5 ns | t _{CDV} =8.5 ns |



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Pin Configuration

**Dual Read-Out SIMM (DIMM)
Top View**

| | | | |
|---|-----|----|---|
| GND | 81 | 1 | GND |
| D ₆₃ | 82 | 2 | D ₆₂ |
| V _{CC} | 83 | 3 | NC (74BP54) / V _{CCQ} (74P5X, 74SP5X) |
| D ₆₁ | 84 | 4 | D ₆₀ |
| V _{CC} | 85 | 5 | NC (74BP54) / V _{CCQ} (74P5X, 74SP5X) |
| D ₅₉ | 86 | 6 | D ₅₈ |
| D ₅₇ | 87 | 7 | D ₅₆ |
| GND | 88 | 8 | GND |
| (74P5X, 74SP5X) DP ₇ / (74BP54) NC | 89 | 9 | NC (74BP54) / DP ₆ (74P5X, 74SP5X) |
| D ₅₅ | 90 | 10 | D ₅₄ |
| D ₅₃ | 91 | 11 | D ₅₂ |
| D ₅₁ | 92 | 12 | D ₅₀ |
| GND | 93 | 13 | GND |
| D ₄₉ | 94 | 14 | D ₄₈ |
| D ₄₇ | 95 | 15 | D ₄₆ |
| D ₄₅ | 96 | 16 | D ₄₄ |
| D ₄₃ | 97 | 17 | D ₄₂ |
| GND | 98 | 18 | GND |
| D ₄₁ | 99 | 19 | D ₄₀ |
| (74P5X, 74SP5X) DP ₅ / (74BP54) NC | 100 | 20 | NC (74BP54) / DP ₄ (74P5X, 74SP5X) |
| D ₃₉ | 101 | 21 | D ₃₈ |
| D ₃₇ | 102 | 22 | D ₃₆ |
| D ₃₅ | 103 | 23 | D ₃₄ |
| GND | 104 | 24 | GND |
| D ₃₃ | 105 | 25 | D ₃₂ |
| D ₃₁ | 106 | 26 | D ₃₀ |
| D ₂₉ | 107 | 27 | D ₂₈ |
| D ₂₇ | 108 | 28 | D ₂₆ |
| D ₂₅ | 109 | 29 | D ₂₄ |
| GND | 110 | 30 | GND |
| (74P5X, 74SP5X) DP ₃ / (74BP54) NC | 111 | 31 | NC (74BP54) / DP ₂ (74P5X, 74SP5X) |
| D ₂₃ | 112 | 32 | D ₂₂ |
| D ₂₁ | 113 | 33 | D ₂₀ |
| V _{CC} | 114 | 34 | NC (74BP54) / V _{CCQ} (74P5X, 74SP5X) |
| D ₁₉ | 115 | 35 | D ₁₈ |
| GND | 116 | 36 | GND |
| D ₁₇ | 117 | 37 | D ₁₆ |
| V _{CC} | 118 | 38 | NC (74BP54) / V _{CCQ} (74P5X, 74SP5X) |
| D ₁₅ | 119 | 39 | D ₁₄ |
| D ₁₃ | 120 | 40 | D ₁₂ |
| GND | 121 | 41 | GND |
| D ₁₁ | 122 | 42 | D ₁₀ |
| V _{CC} | 123 | 43 | NC (74BP54) / V _{CCQ} (74P5X, 74SP5X) |
| D ₉ | 124 | 44 | D ₈ |
| (74P5X, 74SP5X) DP ₁ / (74BP54) NC | 125 | 45 | NC (74BP54) / DP ₀ (74P5X, 74SP5X) |
| V _{CC} | 126 | 46 | NC (74BP54) / V _{CCQ} (74P5X, 74SP5X) |
| D ₇ | 127 | 47 | D ₆ |
| D ₅ | 128 | 48 | D ₄ |
| D ₃ | 129 | 49 | D ₂ |
| D ₁ | 130 | 50 | D ₀ |
| GND | 131 | 51 | GND |
| A ₃₋₁ | 132 | 52 | A ₃₋₀ |
| A ₄₋₁ | 133 | 53 | A ₄₋₀ |
| (74P5X, 74SP5X) A ₅₋₁ / (74BP54) NC | 134 | 54 | A ₅₋₀ |
| (74P5X, 74SP5X) A ₆₋₁ / (74BP54) NC | 135 | 55 | A ₆₋₀ |
| A ₇ | 136 | 56 | A ₈ |
| GND | 137 | 57 | GND |
| A ₉ | 138 | 58 | A ₁₀ |
| A ₁₁ | 139 | 59 | A ₁₂ |
| A ₁₃ | 140 | 60 | A ₁₄ |
| A ₁₅ | 141 | 61 | A ₁₆ |
| A ₁₇ | 142 | 62 | NC (74BP54, 74SP54) / GND (74P54) / A ₁₈ (74P55, 74SP55) |
| GND | 143 | 63 | GND |
| (Reserved A ₁₉) NC | 144 | 64 | PD ₀ |
| PD ₁ | 145 | 65 | PD ₂ |
| (74P5X, 74SP5X) CLK ₀ / (74BP54) NC | 146 | 66 | NC (74BP54, 74P54) / CLK ₁ (74P55, 74SP5X) |
| (Reserved CLK ₂) NC | 147 | 67 | NC (Reserved CLK ₃) |
| GND | 148 | 68 | GND |
| WE ₇ | 149 | 69 | WE ₆ |
| WE ₅ | 150 | 70 | WE ₄ |
| WE ₃ | 151 | 71 | WE ₂ |
| WE ₁ | 152 | 72 | WE ₀ |
| GND | 153 | 73 | GND |
| (74P55, 74SP5X) $\overline{\text{ADSC}}_1$ / (74BP54, 74P54) NC | 154 | 74 | CALE (74BP54) / $\overline{\text{ADSC}}_0$ (74P5X, 74SP5X) |
| CE ₁ | 155 | 75 | CE ₀ |
| (74P55, 74SP5X) $\overline{\text{ADV}}_1$ / (74BP54, 74P54) NC | 156 | 76 | NC (74BP54) / $\overline{\text{ADV}}_0$ (74P5X, 74SP5X) |
| OE ₁ | 157 | 77 | OE ₀ |
| V _{CC} | 158 | 78 | NC (74BP54) / V _{CCQ} (74P5X, 74SP5X) |
| (74P55, 74SP5X) $\overline{\text{ADSP}}_1$ / (74BP54, 74P54) NC | 159 | 79 | NC (74BP54) / $\overline{\text{ADSP}}_0$ (74P5X, 74SP5X) |
| GND | 160 | 80 | GND |

74BP54-5



Pin Definitions

| Common Signals | Description |
|--|--|
| V _{CC} | 5V Supply |
| GND | Ground |
| A ₇ -A ₁₉ | Addresses from processor |
| A ₃₋₀ , A ₄₋₀ | Lower address from chipset, identical to the bank1 addresses |
| A ₃₋₁ , A ₄₋₁ | Lower address from chipset, identical to the bank0 addresses, A ₃₋₁ , A ₄₋₁ not used on CYM74P54 |
| A ₅₋₀ , A ₆₋₀ | Lower address from processor (CYM74P5X, CYM74SP5X- identical to the bank1 addresses) |
| \overline{CE}_0 , \overline{CE}_1 | Chip Enable (same signal), \overline{CE}_1 not used on CYM74P54 |
| \overline{OE}_0 , \overline{OE}_1 | Output Enable (same signal), \overline{OE}_1 not used on CYM74P54 |
| \overline{WE}_0 , \overline{WE}_1 , \overline{WE}_2 , \overline{WE}_3 \overline{WE}_4 , \overline{WE}_5 , \overline{WE}_6 , \overline{WE}_7 | Byte Write Enables |
| PD ₀ -PD ₂ | Presence Detect pins |
| D ₀ -D ₆₃ | Data lines from processor |
| NC | Signal not connected on module. |
| CYM74BP54 Only Signals | Description |
| CALE | Latch Enable |
| CYM74P5X, CYM74SP5X Signals | Description |
| V _{CCQ} | 3.3V Supply |
| DP ₀ -DP ₇ | Data Parity lines (Optional) |
| \overline{ADSP}_0 , \overline{ADSP}_1 | Processor Address Strobe, \overline{ADSP}_1 not used on CYM74P54 |
| \overline{ADSC}_0 , \overline{ADSC}_1 | Cache Controller Address Strobe, \overline{ADSC}_1 not used on CYM74P54 |
| \overline{ADV}_0 , \overline{ADV}_1 | Burst Address Advance, \overline{ADV}_1 not used on CYM74P54 |
| A ₅₋₁ , A ₆₋₁ | Lower address from processor, identical to the bank0 addresses, A ₅₋₁ , A ₆₋₁ not used on CYM74P54 |
| CLK0, CLK1, CLK2, CLK3 | Clock signals (each should be given own clk driver); CLK0 used on CYM74P5X, CYM74SP5X; CLK1 not used on CYM74P54; CLK2 and CLK3 are RSVD |

Presence Detect Pins

| | PD₂ | PD₁ | PD₀ |
|----------------------------------|-----------------------|-----------------------|-----------------------|
| Asynchronous – CYM74BP54 | NC | GND | NC |
| Synchronous Pipelined – CYM74P54 | TBD | TBD | TBD |
| Synchronous Pipelined – CYM74P55 | TBD | TBD | TBD |
| Synchronous Burst – CYM74SP54 | GND | GND | NC |
| Synchronous Burst – CYM74SP55 | GND | GND | GND |



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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -55°C to +125°C

Ambient Temperature with Power Applied -0°C to +70°C

3.3V Supply Voltage to Ground Potential..... -0.5V to +5.25V

5V Supply Voltage to Ground Potential..... -0.5V to +5.25V

DC Voltage Applied to Outputs in High Z State -0.5V to +4.6V

DC Input Voltage..... -0.5V to +4.6V

Output Current into Outputs (LOW)..... 20 mA

Operating Range

| Range | Ambient Temperature | V _{CC} | V _{CCQ} |
|----------------------------------|---------------------|-----------------|-------------------------------|
| Commercial (CYM74BP54) | 0°C to +70°C | 5V ± 5% | N/A |
| Commercial (CYM74P5X, CYM74SP5X) | 0°C to +70°C | 5V ± 5% | 5V ± 5% 3.3V + 10% - 5% |

Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Condition | Min. | Max. | Unit |
|--------------------------|--|--|------|------|------|
| V _{IH} | Input HIGH Voltage | | 2.2 | | V |
| V _{IL} | Input LOW Voltage | CYM74BP54 | -0.5 | 0.8 | V |
| V _{IL} | Input LOW Voltage | CYM74P5X, CYM74SP5X | -0.3 | 0.8 | V |
| V _{OH} | Output HIGH Voltage | V _{CC} =Min. I _{OH} = -4 mA | 2.4 | | V |
| V _{OL} | Output LOW Voltage | V _{CC} =Min. I _{OL} = 8 mA | | 0.4 | V |
| I _{CC} (74BP54) | V _{CC} Operating Supply Current | V _{CC} =Max., I _{OUT} =0 mA, f=f _{MAX} =1/t _{RC} | | 1700 | mA |
| I _{CC} (74P54) | V _{CC} Operating Supply Current | V _{CC} =Max., I _{OUT} =0 mA, f=f _{MAX} =1/t _{RC} | | TBD | mA |
| I _{CC} (74P55) | V _{CC} Operating Supply Current | V _{CC} =Max., I _{OUT} =0 mA, f=f _{MAX} =1/t _{RC} | | TBD | mA |
| I _{CC} (74SP54) | V _{CC} Operating Supply Current | V _{CC} =Max., I _{OUT} =0 mA, f=f _{MAX} =1/t _{RC} | | 1100 | mA |
| I _{CC} (74SP55) | V _{CC} Operating Supply Current | V _{CC} =Max., I _{OUT} =0 mA, f=f _{MAX} =1/t _{RC} | | 1400 | mA |

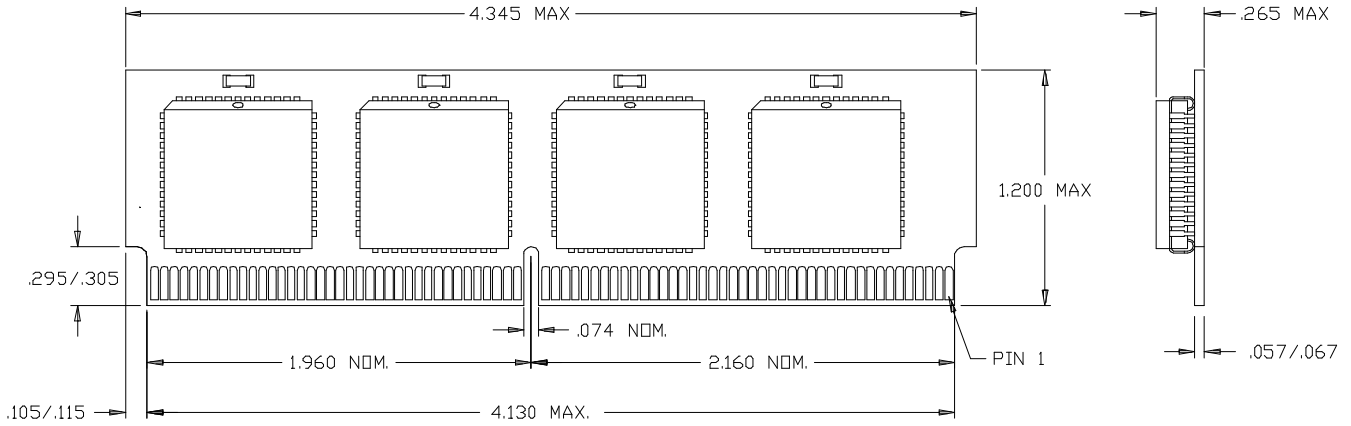
Ordering Information

| Speed (MHz) | Ordering Code | Package Name | Package Type | Description | Operating Range |
|-------------|----------------|--------------|---------------------------|-----------------------|-----------------|
| 60 | CYM74BP54PM-60 | PM36 | 160-Pin Dual-Readout SIMM | Asynchronous 256KB | Commercial |
| | CYM74P54PM-60 | TBD | 160-Pin Dual-Readout SIMM | Synch Pipelined 256KB | |
| | CYM74P55PM-60 | TBD | 160-Pin Dual-Readout SIMM | Synch Pipelined 512KB | |
| | CYM74SP54PM-60 | PM26 | 160-Pin Dual-Readout SIMM | Synch Burst 256KB | |
| | CYM74SP55PM-60 | PM26 | 160-Pin Dual-Readout SIMM | Synch Burst 512KB | |
| 66 | CYM74BP54PM-66 | PM36 | 160-Pin Dual-Readout SIMM | Asynchronous 256KB | Commercial |
| | CYM74P54PM-66 | TBD | 160-Pin Dual-Readout SIMM | Synch Pipelined 256KB | |
| | CYM74P55PM-66 | TBD | 160-Pin Dual-Readout SIMM | Synch Pipelined 512KB | |
| | CYM74SP54PM-66 | PM26 | 160-Pin Dual-Readout SIMM | Synch Burst 256KB | |
| | CYM74SP55PM-66 | PM26 | 160-Pin Dual-Readout SIMM | Synch Burst 512KB | |

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Package Diagrams

160-Pin Dual-Readout SIMM PM26



160-Pin Dual Readout SIMM PM36

