

## Low-Voltage Single SPDT Analog Switch

### FEATURES

- Low Voltage Operation (+2.7 to +5 V)
- Low On-Resistance -  $r_{DS(on)}$ : 40  $\Omega$
- Fast Switching -  $t_{ON}$ : 35 ns,  $t_{OFF}$ : 20 ns
- Low Leakage -  $I_{COM(on)}$ : 200-pA max
- Low Charge Injection -  $Q_{INJ}$ : 1 pC
- Low Power Consumption
- TTL/CMOS Compatible
- ESD Protection > 2000 V (Method 3015.7)
- Available in TSOP-6 and SOIC-8

### BENEFITS

- Reduced Power Consumption
- Simple Logic Interface
- High Accuracy
- Reduce Board Space (TSOP-6)

### APPLICATIONS

- Battery Operated Systems
- Portable Test Equipment
- Sample and Hold Circuits
- Cellular Phones
- Communication Systems
- Military Radio
- PBX, PABX Guidance and Control Systems

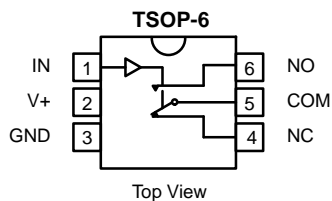
### DESCRIPTION

The DG9461 is a single-pole/double-throw monolithic CMOS analog device designed for high performance switching of analog signals. Combining low power, high speed ( $t_{ON}$ : 35 ns,  $t_{OFF}$ : 20 ns), low on-resistance ( $r_{DS(on)}$ : 40  $\Omega$ ) and small physical size (TSOP-6), the DG9461 is ideal for portable and battery powered applications requiring high performance and efficient use of board space.

The DG9461 is built on Vishay Siliconix's low voltage BCD-15 process. Minimum ESD protection, per Method 3015.7, is 2000 V. An epitaxial layer prevents latchup. Break-before-make is guaranteed for DG9461.

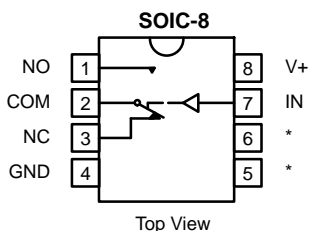
Each switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

### FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE		
Logic	NC	NO
0	ON	OFF
1	OFF	ON

Logic "0"  $\leq$  0.8 V  
 Logic "1"  $\geq$  2.4 V



ORDERING INFORMATION		
Temp Range	Package	Part Number
-40 to 85°C	TSOP-6	DG9461DV
	SOIC-8	DG9461DY

\*Not Connected



### ABSOLUTE MAXIMUM RATINGS

Reference to GND	
V+ .....	-0.3 to +13 V
IN, COM, NC, NO <sup>a</sup> .....	-0.3 to (V+ + 0.3 V)
Continuous Current (Any terminal) .....	± 20 mA
Peak Current .....	± 40 mA
(Pulsed at 1ms, 10% duty cycle)	
ESD (Method 3015.7) .....	> 2000 V

Storage Temperature (D Suffix) .....	-65 to 125°C
Power Dissipation (Packages) <sup>b</sup>	
8-Pin Narrow Body SOIC <sup>c</sup> .....	400 mW

Notes:

- Signals on S<sub>X</sub>, D<sub>X</sub>, or IN<sub>X</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.
- Derate 6.5 mW/°C above 75°C

SPECIFICATIONS (V+ = 3 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ± 10%, V <sub>IN</sub> = 0.8 or 2.4 V <sup>e</sup>	Temp <sup>a</sup>	D Suffix -40 to 85°C			Unit
				Min <sup>c</sup>	Typ <sup>b</sup>	Max <sup>c</sup>	
<b>Analog Switch</b>							
Analog Signal Range <sup>d</sup>	V <sub>ANALOG</sub>		Full	0		3	V
Drain-Source On-Resistance	r <sub>DS(on)</sub>	V <sub>NO</sub> or V <sub>NC</sub> = 1.5 V, V+ = 2.7 V I <sub>COM</sub> = 5 mA	Room Full		50	80 140	Ω
r <sub>DS(on)</sub> Match <sup>d</sup>	Δr <sub>DS(on)</sub>	V <sub>NO</sub> or V <sub>NC</sub> = 1.5 V	Room		0.4	2	
r <sub>DS(on)</sub> Flatness <sup>f</sup>	r <sub>DS(on)</sub> Flatness	V <sub>NO</sub> or V <sub>NC</sub> = 1 and 2 V	Room		4	8	
NO or NC Off Leakage Current <sup>g</sup>	I <sub>NO/NC(off)</sub>	V <sub>NO</sub> or V <sub>NC</sub> = 1 V / 2 V, V <sub>COM</sub> = 2 V / 1 V	Room Full	-100 -5000	5	100 5000	pA
COM Off Leakage Current <sup>g</sup>	I <sub>COM(off)</sub>	V <sub>COM</sub> = 1 V / 2 V, V <sub>NO</sub> or V <sub>NC</sub> = 2 V / 1 V	Room Full	-100 -5000	5	100 5000	
Channel-On Leakage Current <sup>g</sup>	I <sub>COM(on)</sub>	V <sub>COM</sub> = V <sub>NO</sub> or V <sub>NC</sub> = 1 V / 2 V	Room Full	-200 -10000	10	200 10000	
<b>Digital Control</b>							
Input Current	I <sub>INL</sub> or I <sub>INH</sub>		Full		1		μA
<b>Dynamic Characteristics</b>							
Turn-On Time	t <sub>ON</sub>	V <sub>NO</sub> or V <sub>NC</sub> = 1.5 V	Room Full		50	120 200	ns
Turn-Off Time	t <sub>OFF</sub>		Room Full		20	50 120	
Break-Before-Make Time	t <sub>d</sub>		Room	3	20		
Charge Injection	Q <sub>INJ</sub>	C <sub>L</sub> = 1 nF, V <sub>gen</sub> = 0 V, R <sub>gen</sub> = 0 Ω	Room		1	5	pC
Off-Isolation	OIRR	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 1 MHz	Room		-74		dB
Source-Off Capacitance	C <sub>S(off)</sub>	f = 1 MHz	Room		7		pF
Channel-On Capacitance	C <sub>D(on)</sub>		Room		32		
<b>Power Supply</b>							
Power Supply Range	V+			2.7		12	V
Power Supply Current	I+	V+ = 3.3 V, V <sub>IN</sub> = 0 or 3.3 V				1	μA

Notes:

- Room = 25°C, Full = as determined by the operating suffix.
- Typical values are for design aid only, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guarantee by design, not subjected to production test.
- V<sub>IN</sub> = input voltage to perform proper function.
- Difference of min and max values.
- Guaranteed by 5-V leakage testing, not production tested..



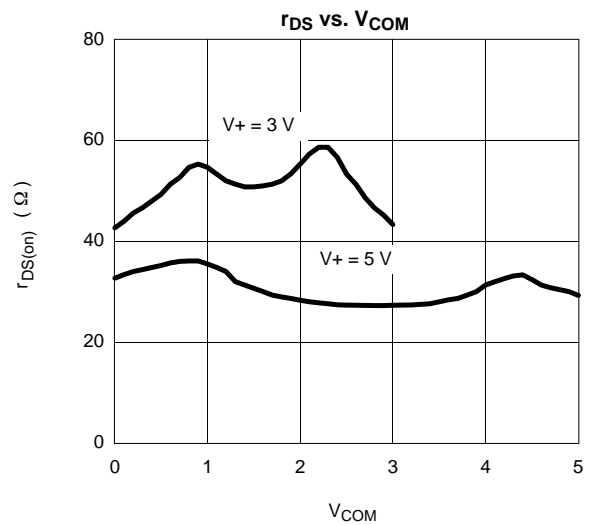
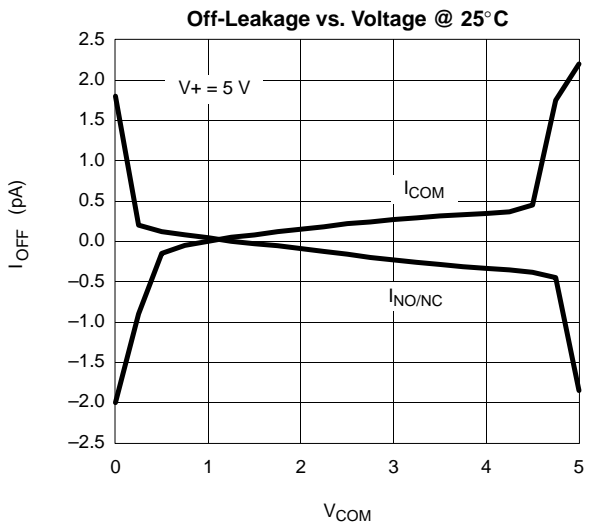
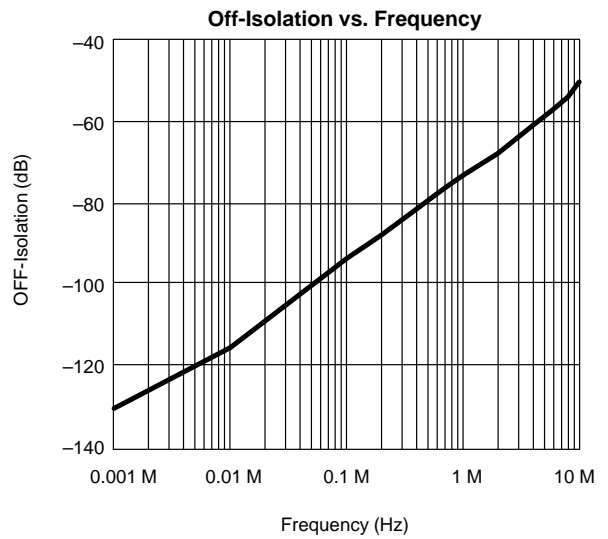
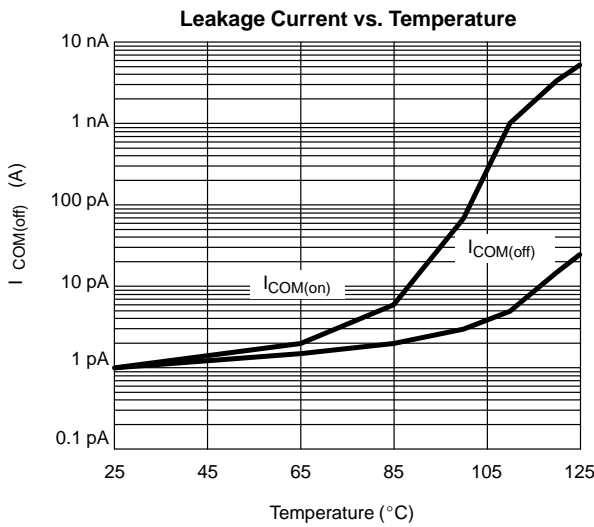
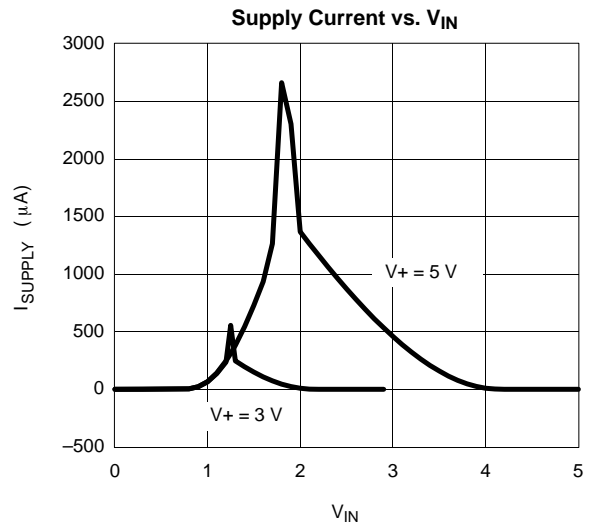
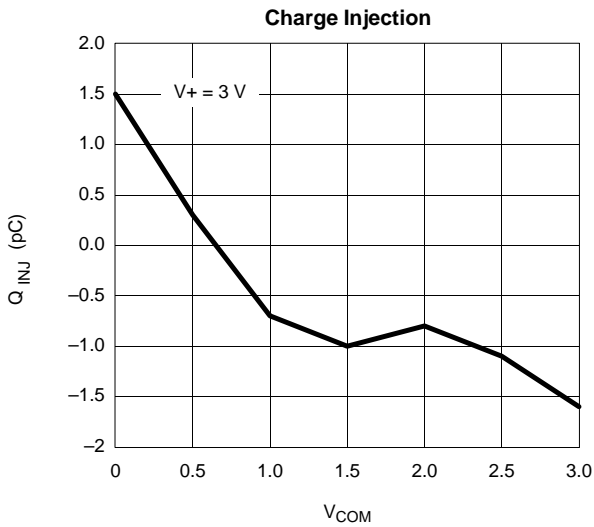
SPECIFICATIONS (V+ = 5 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 5 V, ±10%, VIN = 0.8 or 2.4 V <sup>e</sup>	Temp <sup>a</sup>	D Suffix -40 to 85°C			Unit
				Min <sup>c</sup>	Typ <sup>b</sup>	Max <sup>c</sup>	
<b>Analog Switch</b>							
Analog Signal Range <sup>d</sup>	V <sub>ANALOG</sub>		Full	0		5	V
Drain-Source On-Resistance	r <sub>DS(on)</sub>	V <sub>NO</sub> or V <sub>NC</sub> = 3.5 V, V+ = 4.5 V I <sub>COM</sub> = 5 mA	Room Full		30	60 75	Ω
r <sub>DS(on)</sub> Match <sup>d</sup>	Δr <sub>DS(on)</sub>	V <sub>NO</sub> or V <sub>NC</sub> = 1.5 V	Room		0.4	2	
r <sub>DS(on)</sub> Flatness <sup>f</sup>	r <sub>DS(on)</sub> Flatness	V <sub>NO</sub> or V <sub>NC</sub> = 1, 2, and 3 V	Room		2	6	
NO or NC Off Leakage Current	I <sub>NO/NC(off)</sub>	V <sub>NO</sub> or V <sub>NC</sub> = 1 V / 4 V, V <sub>COM</sub> = 4 V / 1 V	Room Full	-100 -5000	10	100 5000	pA
COM Off Leakage Current	I <sub>COM(off)</sub>	V <sub>COM</sub> = 1 V / 4 V, V <sub>NO</sub> or V <sub>NC</sub> = 4 V / 1 V	Room Full	-100 -5000	10	100 5000	
Channel-On Leakage Current	I <sub>COM(on)</sub>	V <sub>COM</sub> = V <sub>NO</sub> or V <sub>NC</sub> = 1 V / 4 V	Room Full	-200 -10000		200 10000	
<b>Digital Control</b>							
Input Current	I <sub>INL</sub> or I <sub>INH</sub>		Full		1		μA
<b>Dynamic Characteristics</b>							
Turn-On Time	t <sub>ON</sub>	V <sub>NO</sub> or V <sub>NC</sub> = 3.0 V	Room Full		35	75 150	ns
Turn-Off Time	t <sub>OFF</sub>		Room Full		20	50 100	
Break-Before-Make Time	t <sub>d</sub>		Room	3	10		
Charge Injection	Q <sub>INJ</sub>	C <sub>L</sub> = 1 nF, V <sub>gen</sub> = 0 V, R <sub>gen</sub> = 0 Ω	Room		2	5	pC
Off-Isolation	OIRR	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 1 MHz	Room		-74		dB
NC and NO Capacitance	C <sub>(off)</sub>	f = 1 MHz	Room		-7		pF
Channel-On Capacitance	C <sub>D(on)</sub>		Room		32		
<b>Power Supply</b>							
Power Supply Range	V+			2.7		12	V
Power Supply Current	I+	V+ = 5.5 V, V <sub>IN</sub> = 0 or 5.5 V				1	μA

Notes:

- a. Room = 25°C, Full = as determined by the operating suffix.
- b. Typical values are for design aid only, not guaranteed nor subject to production testing.
- c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- d. Guarantee by design, nor subjected to production test.
- e. V<sub>IN</sub> = input voltage to perform proper function.
- f. Difference of min and max values.

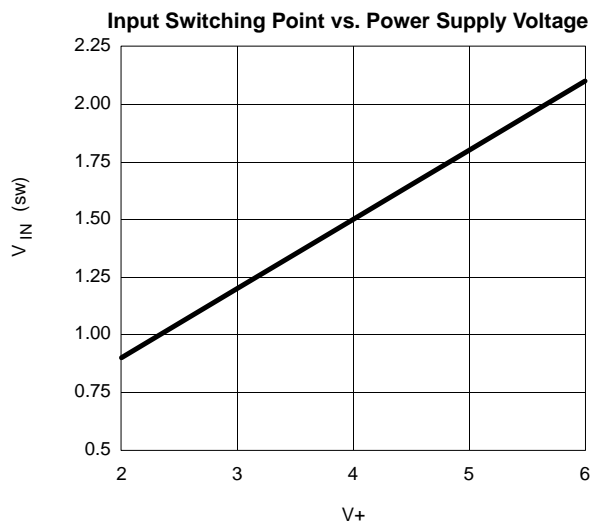
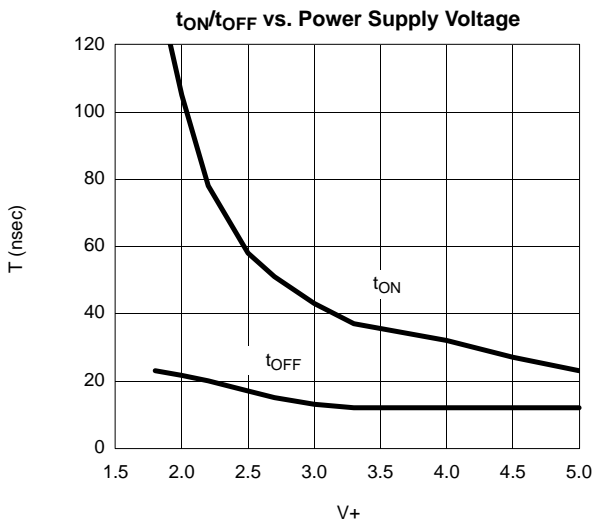
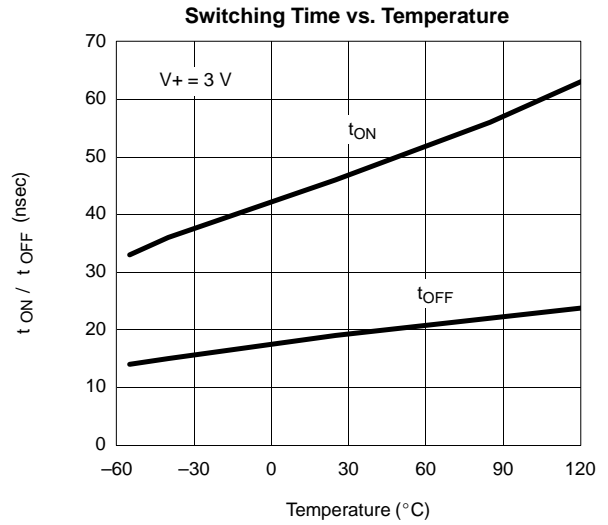
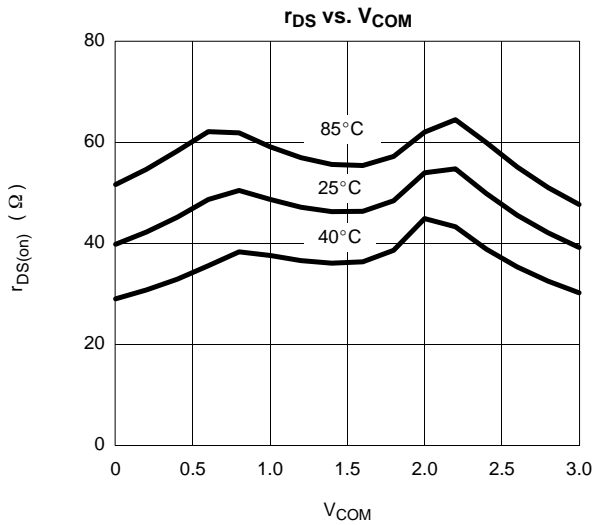


**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**

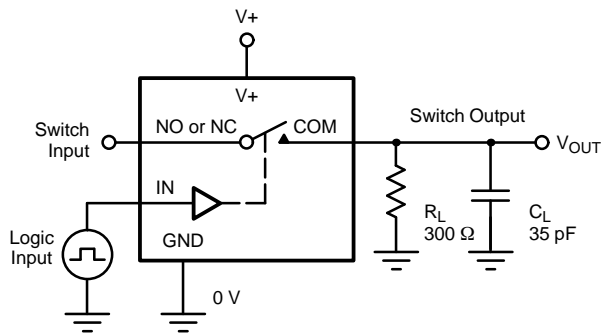




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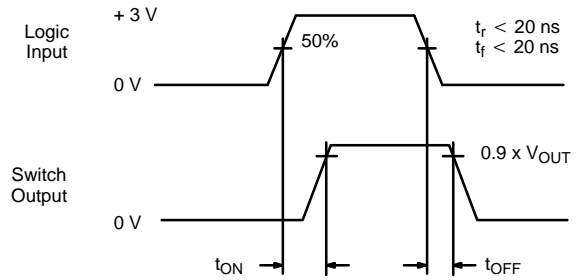


**TEST CIRCUITS**



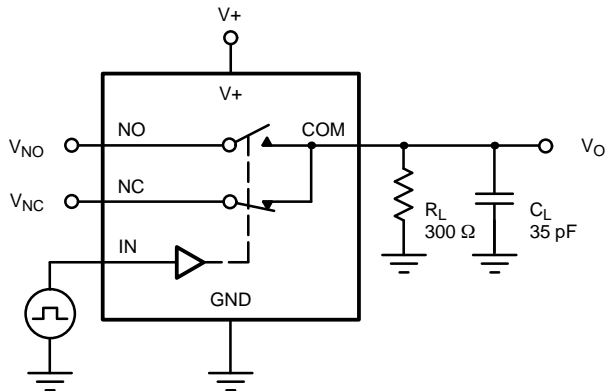
$C_L$  (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM} \left( \frac{R_L}{R_L + R_{ON}} \right)$$

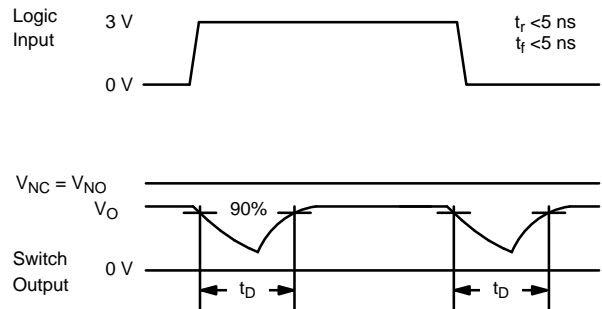


Logic "1" = Switch On  
Logic input waveforms inverted for switches that have the opposite logic sense.

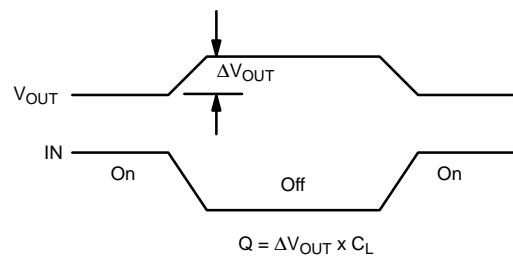
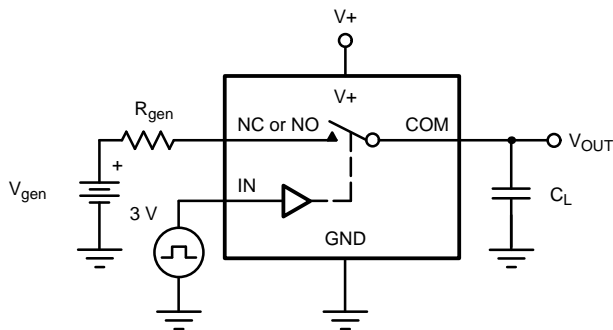
**FIGURE 1. Switching Time**



$C_L$  (includes fixture and stray capacitance)



**FIGURE 2. Break-Before-Make Interval**



IN depends on switch configuration: input polarity determined by sense of switch.

**FIGURE 3. Charge Injection**

**TEST CIRCUITS**

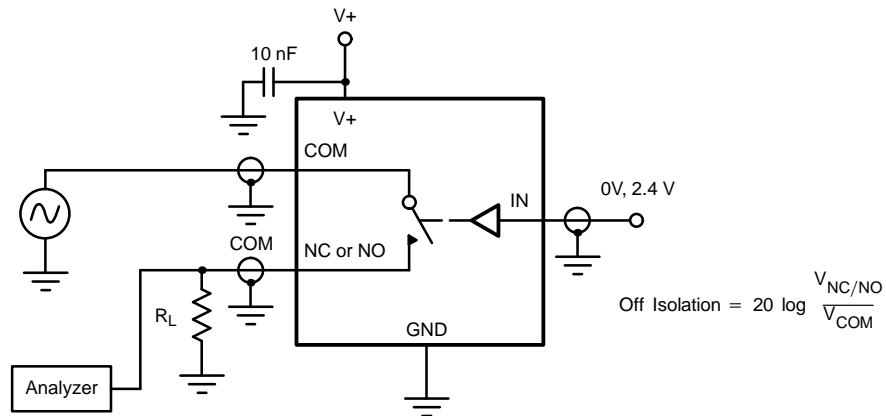


FIGURE 4. Off-Isolation

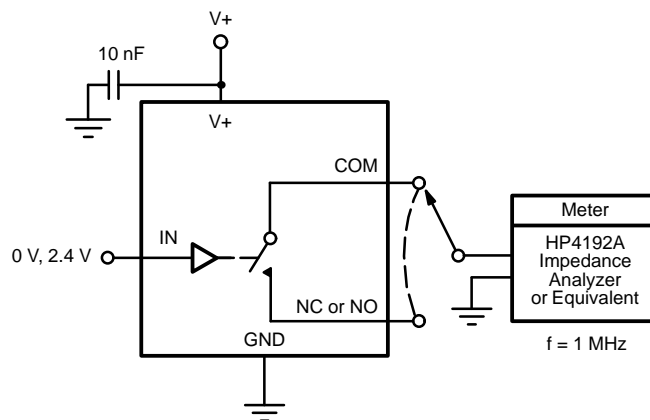


FIGURE 5. Channel Off/On Capacitance