

Features

- -3 dB bandwidth = 85 MHz, A_V = 1
- -3 dB bandwidth = 75 MHz, A_V = 2
- NTSC/PAL dG \leq 0.03%, dP \leq 0.1°
- 50 mA output current
- Drives $\pm\,2.5V$ into 100Ω load
- Low voltage noise = $4 \text{ nV}/\sqrt{\text{Hz}}$
- Current mode feedback
- Low cost

- Applications
- Video amplifier
- Video distribution amplifier
- Residue amplifiers in ADC
- Current to voltage converter
- Coaxial cable driver

Ordering Information

 Part No.
 Temp. Range
 Pkg.
 Outline*

 EL2130CN
 0°C to +75°C
 8-Pin P-DIP
 MDP0031

 EL2130CS
 0°C to +75°C
 8-Lead SO
 MDP0027

General Description

The EL2130 is a wideband current mode feedback amplifier optimized for gains between -10 and +10 while operating on $\pm 5V$ power supplies. Built using Elantec's Complementary Bipolar process, this device exhibits -3 dB bandwidths in excess of 85 MHz at unity gain and 75 MHz at a gain of two. The EL2130 is capable of output currents in excess of 50 mA giving it the ability to drive either double or single terminated 50 Ω coaxial cables.

Exhibiting a Differential Gain of 0.03% and a Differential Phase of 0.1° at NTSC and PAL frequencies. The EL2130 is an excellent low cost solution to most video applications.

In addition, the EL2130 exhibits very low gain peaking, typically below 0.1 dB to frequencies in excess of 40 MHz as well as 50 ns settling time to 0.2% making it an excellent choice for driving flash A/D converters.

The device is available in the plastic 8-lead narrow-body small outline (SO) and the 8-pin mini DIP packages, and operates over the temperature range of 0° C to $+75^{\circ}$ C.



Note: All information contained in this data sheet has been carefully checked and is believed to be accurate as of the date of publication; however, this data sheet cannot be a "controlled document". Current revisions, if any, to these specifications are maintained at the factory and are available upon your request. We recommend checking the revision level before finalization of your design documentation.

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Absolute Maximum Ratings $(T_A = 25^{\circ}C)$

VS	Supply Voltage	±6V	I _{OP}	Output Short Circuit Duration	\leq 5 sec
VIN	Input Voltage	$\pm V_S$	TA	Operating Temperature Range:	0° C to $+75^{\circ}$ C
ΔV_{IN}	Differential Input Voltage	± 6V	т _Ј	Operating Junction Temperature	150°C
PD	Maximum Power Dissipation	See Curves	T_{ST}	Storage Temperature	-65°C to +150°C
IIN	Input Current	$\pm 10 \text{ mA}$			

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Fest Level	Test Procedure
Ι	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at $T_{\rm A}=25^{\circ}{\rm C}$ and QA sample tested at $T_{\rm A}=25^{\circ}{\rm C}$,
	T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
v	Parameter is typical value at $T_A = 25^{\circ}C$ for information purposes only.

Open Loop DC Electrical Characteristics $V_S = \pm 5V$; $R_L = \infty$, unless otherwise specified

Parameter	Description	Condition	Temp	Min	Тур	Max	Test Level	Units
V _{OS}	Input Offset Voltage		25°C		2.0	10	I	mV
			T _{MIN} , T _{MAX}			15	III	mV
$\Delta V_{OS} / \Delta T$	Offset Voltage Drift				7		v	μV/°C
$+I_{IN}$	+Input Current		25°C		5.5	15	I	μA
			T_{MIN}, T_{MAX}			25	III	μA
$-I_{IN}$	+Input Current		25°C		10	40	I	μΑ
			T_{MIN}, T_{MAX}			50	III	μA
$+R_{IN}$	+Input Resistance		25°C	1.0	2.0		I	$\mathbf{M}\Omega$
C _{IN}	+Input Capacitance		25°C		1.0		v	\mathbf{pF}
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 2.5 V$	25°C	50	60		I	dB
-ICMR	Input Current Common	$V_{CM} = \pm 2.5 V$	25°C		5	10	I	μA/V
	Mode Rejection		$T_{\rm MIN}, T_{\rm MIN}$			20	III	$\mu A/V$
PSRR	Power Supply Rejection Ratio	$\pm 4.5V \leq V_S \leq \pm 6V$	25°C	60	70		I	dB
+IPSR	+ Input Current Power	$\pm 4.5V \le V_S \le \pm 6V$	25°C		0.1	0.5	I	$\mu A/V$
	Supply Rejection		$T_{\rm MIN}, T_{\rm MIN}$			1.0	III	$\mu A/V$
-IPSR	-Input Current Power	$\pm 4.5V \le V_S \le \pm 6V$	25°C		0.5	5.0	I	$\mu A/V$
	Supply Rejection		T_{MIN}, T_{MIN}			8.0	III	$\mu A/V$

Open Loop DC Electrical Characteristics

 $V_{S} = \pm 5V$; $R_{L} = \infty$, unless otherwise specified — Contd.

Parameter	Description	Condition	Temp	Min	Тур	Max	Test Level	Units
R _{OL}	Transimpedance	$V_{OUT} = \pm 2.5 V,$	25°C	80	145		I	V/mA
		$R_L = 100\Omega$	T_{MIN}, T_{MAX}	70			III	V/mA
A _{VOL}	Open Loop DC	$V_{OUT} = \pm 2.5 V,$	25°C	60	66		I	dB
	Voltage Gain	$R_L = 100\Omega$	T_{MIN}, T_{MAX}	56			III	dB
vo	Output Voltage Swing	$R_L = 100\Omega$	25°C	3	3.5		I	v
I _{OUT}	Output Current		25°C	30	50		I	mA
R _{OUT}	Output Resistance		25°C		5		v	Ω
IS	Quiescent Supply Current		Full		17	21	I	mA
I _{SC}	Short Circuit Current		25°C		85		v	mA

Closed Loop AC Electrical Characteristics

$V_{S} = \pm 5V, A_{V} = \pm 2, R_{F} = R_{G} = 820\Omega, R_{L} = 100\Omega, T_{A} = 25^{\circ}C$	
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Parameter	Description	Condition	Min	Тур	Max	Test Level	Units
SR	Slew Rate (Note 1)	$V_O = 5 V_{p-p}$		625		v	V/µs
t _r	Rise Time	$V_{O} = 200 \text{ mV}$		4.6		v	ns
t _f	Fall Time	$V_{O} = 200 \text{ mV}$		4.6		v	ns
t _{pd}	Prop Delay	$V_{O} = 200 \text{ mV}$		4.0		v	ns
SSBW	3 dB Bandwidth	$V_O = 100 \text{ mV}$		75		v	MHz
dG	NTSC/PAL Diff Gain			0.03		v	%
dP	NTSC/PAL Diff Phase			0.10		v	deg (°)
GFPL	Gain Flatness	f < 40 MHz		0.08		v	dB

Note 1: Slew rate is measured with $V_{O} = 5V_{p-p}$ between -1.25V and +1.25V and +1.25V and -1.25V.



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Applications Information

Power Supply Bypassing

The EL2130 will exhibit ringing or oscillation if the power supply leads are not adequately bypassed. 0.1 μ F ceramic disc capacitors are suggested for both supply pins at a distance no greater than $\frac{1}{2}$ inch from the device. Surface mounting chip capacitors are strongly recommended.

Lead Dress

A ground plane to which decoupling capacitors and gain setting resistors are terminated will eliminate overshoot and ringing. However, the ground plane should not extend to the vicinity of both the non-inverting and inverting inputs (pins 3 and 2) which would add capacitance to these nodes, and lead lengths from these pins should be made as short as possible. Use of sockets, particularly for the SO package, should be avoided if possible. Sockets add parasitic inductance and capacitance which will result in peaking and overshoot.

Video Characteristics and Applications

Frequency domain testing is performed at Elantec using a computer controlled HP model 8656B Signal Generator and an HP Model 4195A Network/Spectrum Analyzer. The DUT test board is built using microwave/strip line techniques, and solid coaxial cables route the stimulus to the DUT socket. Signals are routed to and from the DUT test fixture using subminiature coaxial cable.

Differential Gain and Phase are tested at a noise gain of 2 with 100Ω load. Gain and Phase measurements are made with a DC input reference

Applications Information - Contd.

voltage at 0V and compared to those made at $V_{\rm ref}$ equal to 0.7V at frequencies extending to 30 MHz.

The EL2130 is capable of driving 100Ω to a minimum of 2.5V peak which means that it can naturally drive double terminated (50 Ω) coaxial cables.

Equivalent Circuit

Capacitive Loads

As can be seen from the Bode plot, the EL2130 will peak into capacitive loads greater than 20 pf. In many applications such as flash A/D's, capacitive loading is unavoidable. In these cases, the use of a snubber network consisting of a 100 Ω resistor in series with 47 pF capacitor from the output to ground is recommended.





General Disclaimer

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