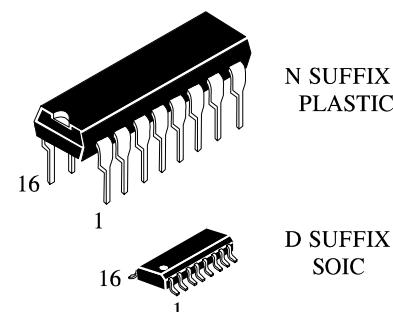


IL2010B

PHASE CONTROL CIRCUIT FOR CURRENT FEEDBACK

Description

The IL2010B is designed as a phase-control circuit in bipolar technology. It enables load-current detection and has a soft-start function as well as reference voltage output. Motor control with load-current feedback and overload protection are preferred applications.



Features

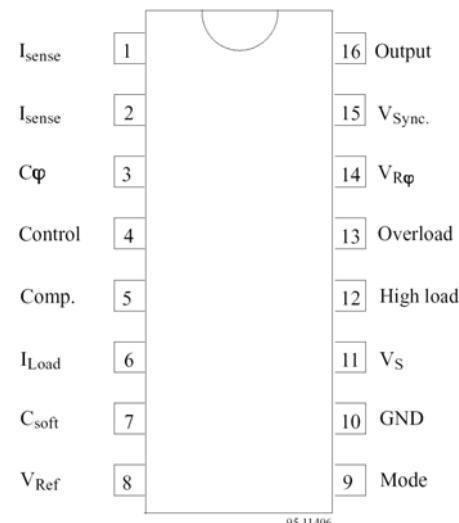
- Full wave current sensing
- Mains supply variation compensated
- Programmable load-current limitation with over- and high-load output
- Variable soft-start
- Voltage and current synchronization
- Automatic retriggering switchable
- Triggering pulse typical 125 mA
- Internal supply voltage monitoring
- Current requirement ≤ 3 mA
- Temperature compensated reference voltage

Applications

- Advanced motor control
- Grinder
- Drilling machine

Pin Description

Pin	Symbol	Function
1	I _{sense}	Load current sensing
2	I _{sense}	Load current sensing
3	C _φ	Ramp voltage
4	Control	Control input
5	Comp.	Compensation output
6	I _{Load}	Load current limitation
7	C _{soft}	Soft start
8	V _{Ref}	Reference voltage
9	Mode	Mode selection
10	GND	Ground
11	V _S	Supply voltage
12	High load	High load indication
13	Overload	Overload indication
14	V _{Rφ}	Ramp current adjust
15	V _{Sync.}	Voltage synchronization
16	Output	Trigger output

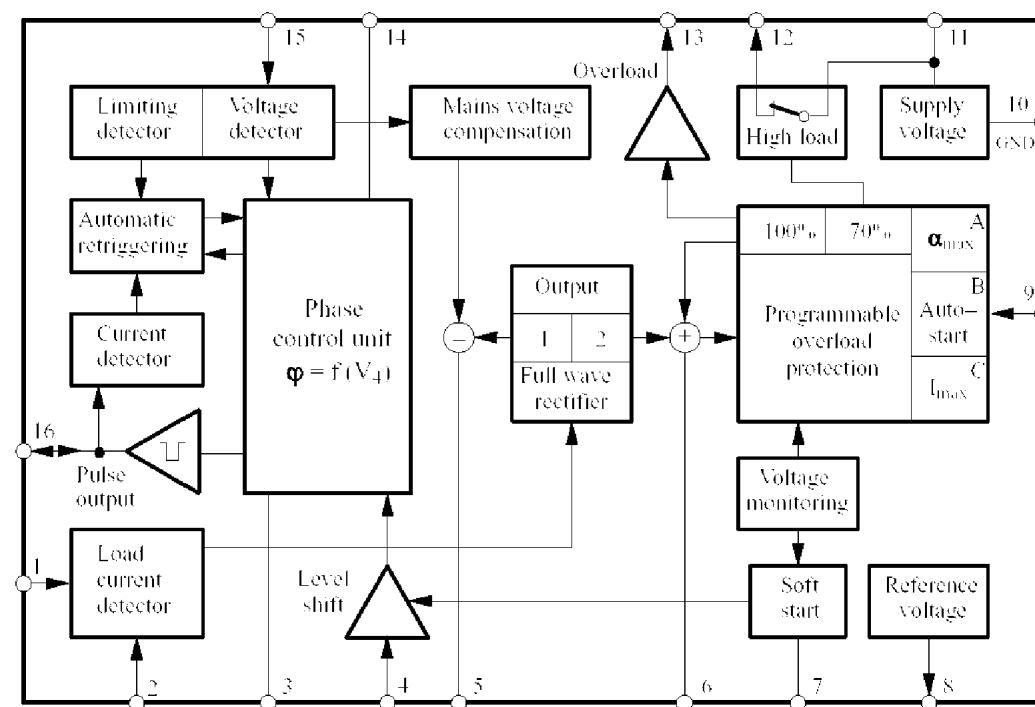


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Block Diagram



Absolute Maximum Ratings

Reference point Pin 10, unless otherwise specified

Parameters	Pin	Symbol	Value	Unit
Sink current t ≤ 10us	11	-I _S	30	mA
		-I _s	100	
Sync. currents t ≤ 10us	15	±I _{syncV}	5	mA
		±I _{syncV}	20	
Phase control				
Control voltage	4 and 8	-V _I	0 – V _B	V
Input current	4	± I _I	500	uA
Charging current	14	-I _{φ max}	0.5	mA
Soft-start				
Input voltage	7 and 8	-V _I	0 – V _B	V
Pulse output				
Input voltage	16	+V _I	2	V
		-V _I	V ₁₁	
Reference voltage source				
Output current t ≤ 10us	8	I ₀	10	mA
		i ₀	30	mA
Load current sensing				
Input currents	1 and 2	± I _i	1	mA
Input voltages	5 and 6	-V _i	0 – V _B	V
Overload output	13	I _L	1	mA
High-load output t ≤ 10us	12	I _L	30	mA
		i _L	100	mA
Storage temperature range		T _{stg}	-40 to +125	°C
Junction temperature range		T _j	125	°C
Ambient temperature range		T _{amb}	-10 to +100	°C



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IL2010B**Electrical Characteristics** $V_S = -13 \text{ V}$, $T_{\text{amb}} = 25^\circ\text{C}$, reference point Pin 10, unless otherwise specified

Parameters	Test Conditions	Pins	Symbol	Min.	Typ.	Max.	Unit			
Supply										
Supply voltage limitation	$-I_S = 5.5 \text{ mA}$	11	$-V_S$	14.5		16.5	V			
	$-I_S = 30 \text{ mA}$			14.6		16.8				
Current requirement	$-V_S = 13.0 \text{ V}$ (Pins 1, 2, 8 and 15 open)	Pin 11	$-I_S$			5.2	mA			
Reference voltage source										
Reference voltage	$I_L = 10 \text{ uA}$	8	$-V_{\text{Ref}}$	8.7	9.0	9.3	V			
	$I_L = 2.5 \text{ mA}$			8.5	8.8	9.2				
Temperature coefficient	$I_S = 2.5 \text{ mA}$		$TC_{V\text{Ref}}$		-0.004		%/K			
	$I_S = 10 \text{ uA}$				+0.006					
Voltage monitoring										
Turn-on threshold		11	$-V_{\text{Son}}$		11.3	12.3	V			
Phase control – synchronization										
Voltage limitation	$\pm I_L = 2 \text{ mA}$		$\pm V_{\text{syncV}}$	8.0	8.5	9.0	V			
Input current	Current sync.	16	$\pm I_{\text{syncI}}$	3		30	uA			
Reference ramp, fig. 1										
Charging current		14	$-I_\phi$	1		100	uA			
Start voltage		3	$-V_{\max}$	2.00	2.15	2.20	V			
Temperature coefficient of start voltage		3	TC_R		-0.003		%/K			
Final voltage		3	$-V_{\min}$	$(V_8 \pm 200 \text{ mV})$						
R_ϕ reference voltage	$I_\phi = 10 \text{ uA}$	14 and 11	$V_{R\phi}$	0.96	1.02	1.10	V			
Temperature coefficient	$I_{\phi} = 10 \text{ uA}$	14	$TC_{VR\phi}$		0.03		%/K			
	$I_\phi = 1 \text{ uA}$				0.06					
Pulse output current	$V_{16} = -1.2 \text{ V}$, fig. 2,	16	I_0	100	125	150	mA			
Output pulse width	$C_3 = 3.3 \text{ nF}$, fig. 3	16	t_p		50		us			
Automatic retriggering										
Repetition rate	$I_{15} = 150 \text{ uA}$		t_{pp}	3	5	7.5	t_p			
Threshold voltage		16	$\pm V_I$	20		100	mV			
Soft start, figure 7 and 8										
Starting current	$V_7 = V_8$	7	$-I_0$	5	10	20	uA			
Final current	$V_{7-10} = -1 \text{ V}$		$-I_0$	20	25	50	uA			
Discharge current			$+I_0$	0.5			mA			
Output current		4	$+I_0$	0.2		2	mA			
Supply voltage compensation,										
Transfer gain	fig. 6 I_{15}/I_5 Pin 15/5 (Pins 1 and 2 open)			G_i	12		18			
Output offset current	$V_{(R6)} = V_{15} = V_5 = 0$			$\pm I_0$		2	uA			
Load current detection $R_1 = R_2 = 3 \text{ k}\Omega$, $V_{15} = 0$, $V_5 = V_6 = V_8$, fig. 7										
Transfer gain	$I_5/150 \text{ mV}$, $I_6/150 \text{ mV}$			G_l	0.28	0.32	0.37	uA/mV		
Output offset currents	5, 6 - 8			$-I_0$	0	3	6	uA		
Reference voltage	$I_1, I_2 = 100 \text{ uA}$			$-V_{\text{Ref}}$	300		450	mV		
Shunt voltage amplitude				$\pm V_{(R6)}$		250	mV			



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Parameters	Test Conditions	Pins	Symbol	Min.	Typ.	Max.	Unit
Load current limitation figs. 8 to 13							
High load switching	Threshold V_{T70}	6-8	V_{T70}	4	4.35	4.7	V
Overload switching	Threshold V_{T100}		V_{T100}	5.8	6.2	6.6	V
Restart switching	Threshold V_{T25}		V_{T25}	1.25	1.55	1.85	V
Input current	Enquiry mode		I_i			1	uA
Output impedance	Switching mode		R_0	2	4	8	kΩ
Programming input							
Input voltage - auto-start	Pin 9 open	9	$-V_9$	3.8	4.3	4.7	V
Input current	$V_9 = 0 (\alpha_{max})$		$-I_9$	5	10	20	uA
	$V_9 = V_8 (I_{max})$		I_9	5	10	20	
High load output, V_{T70}, fig. 9, $I_{12} = -3$ mA,							
Saturation voltages	$V_{6-8} \leq V_{T70}$	11-12	V_{sat}	0.5	0.75	1.0	V
	$V_{6-8} \geq V_{T70}$		V_{lim}	7.3		8.1	
Overload output, V_{T100}, $V_9 = \text{open}$ or $V_9 = V_{10}$, fig. 10							
Leakage current	$V_{6-8} \geq V_{T25}$ $V_{13} = (V_{11}+1)V$	13	I_{lkg}			0.5	uA
Saturation voltages	$V_{6-8} \geq V_{T100}$, $I_{13} = 10$ uA	11-13	V_{sat}			0.15	V
Output current, max. load	$V_9 = V_8$, fig. 10	13	I_{13}			1	mA
Leakage current	$V_6 \leq V_{T100}$	13	I_{lkg}			4	uA
Output impedance	Open collector $V_6 \leq V_{T100}$	13	R_0	2	4	8	kΩ

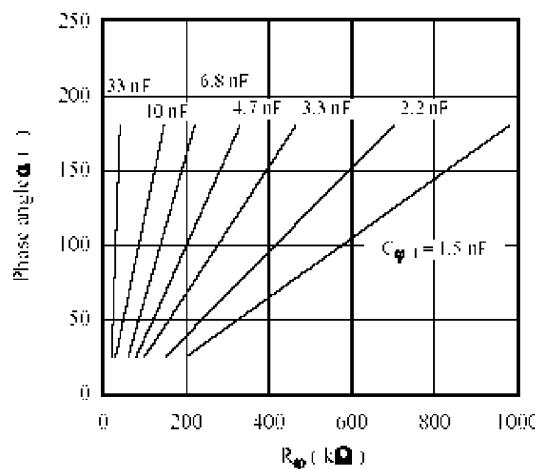


Fig.1

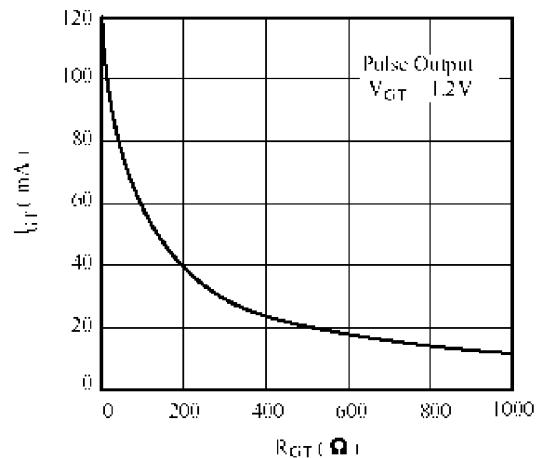


Fig.2



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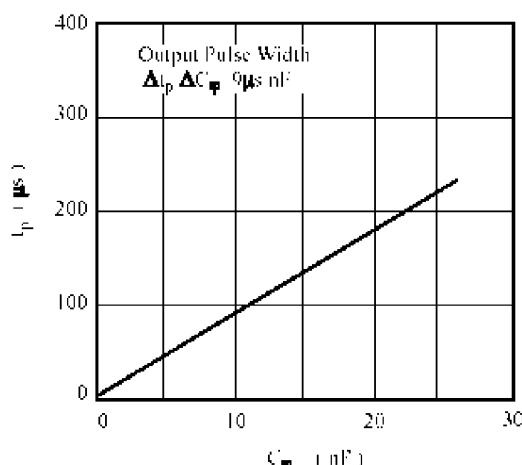


Fig.3

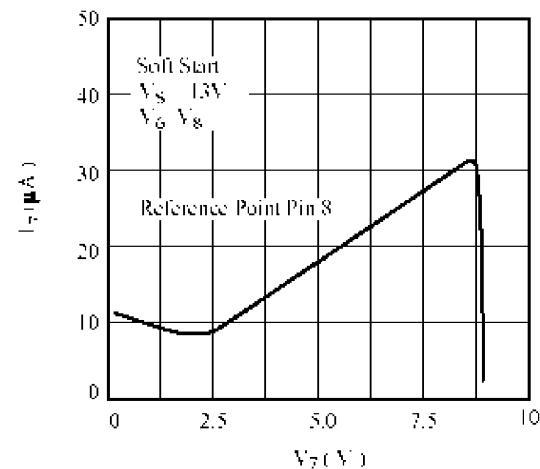


Fig.4

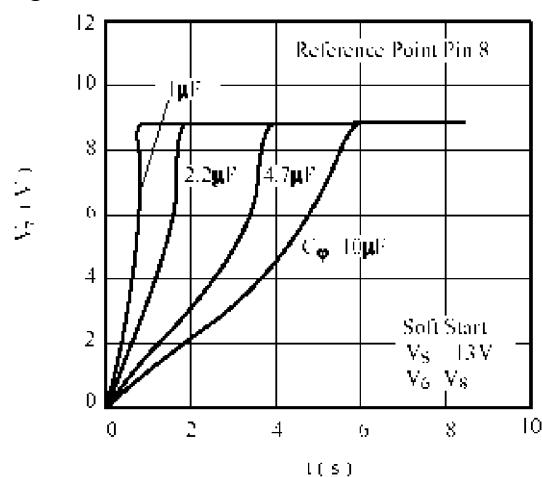


Fig.5

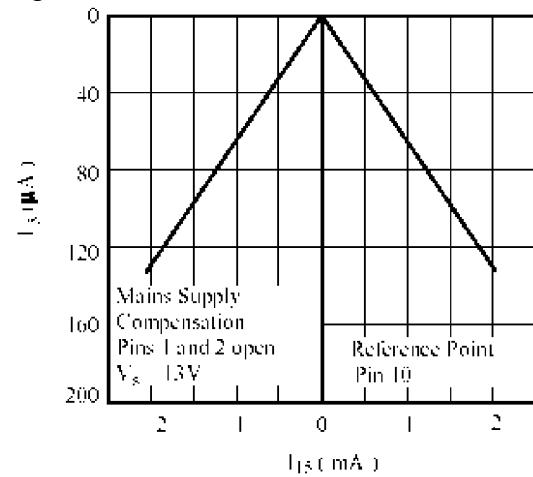


Fig.6

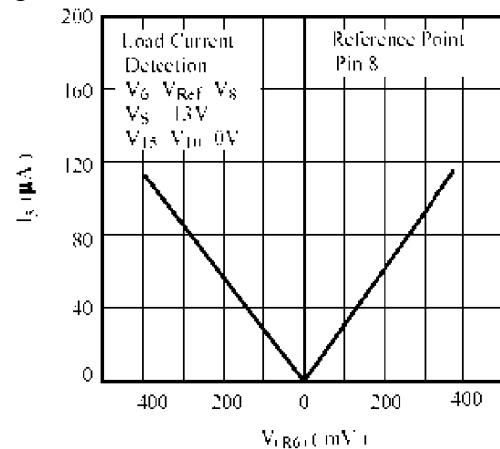


Fig.7

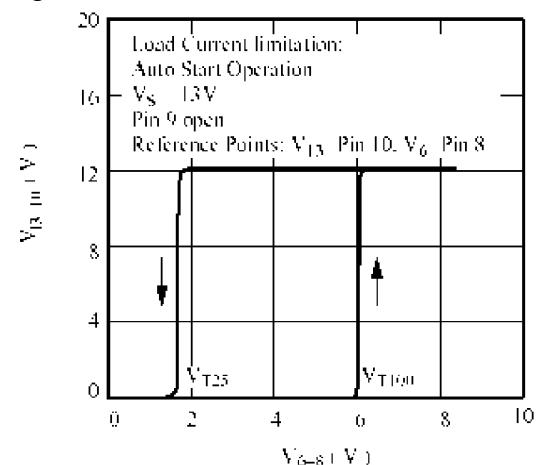


Fig.8



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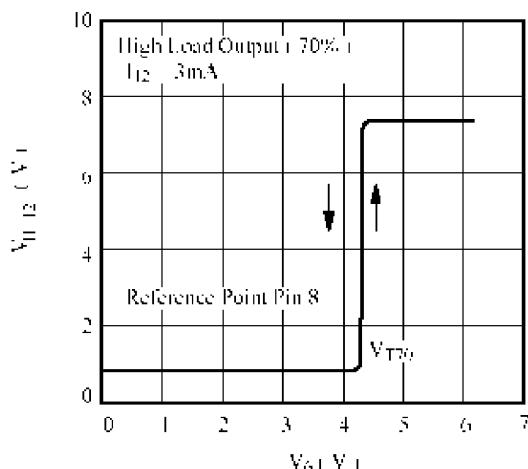


Fig.9

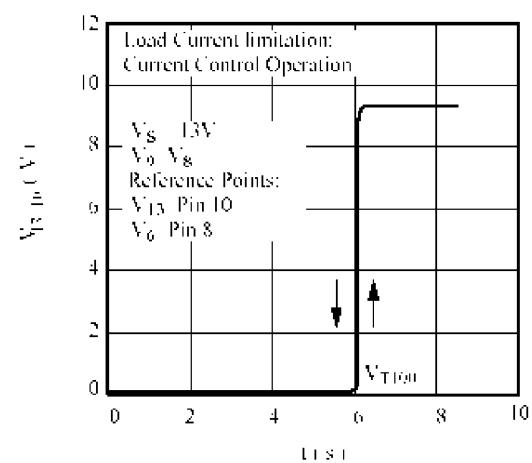


Fig.10

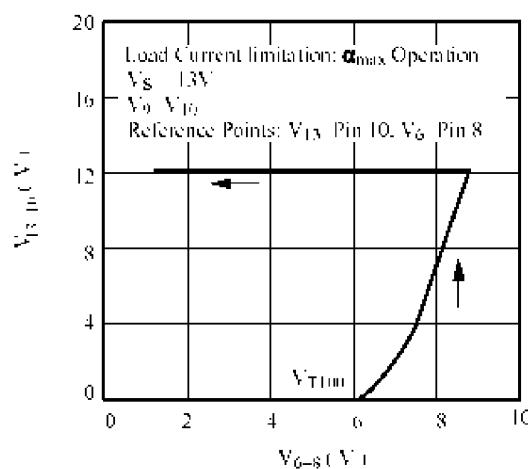


Fig.11

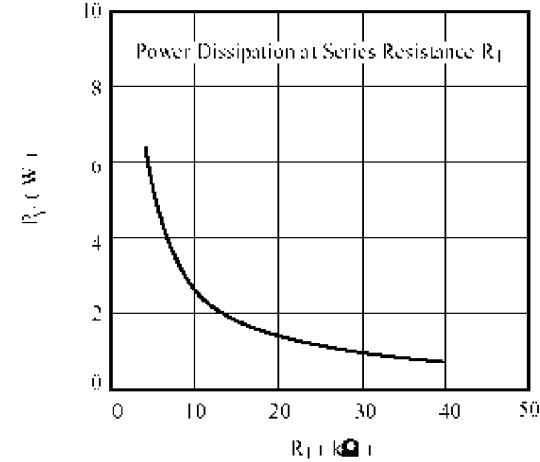


Fig.12

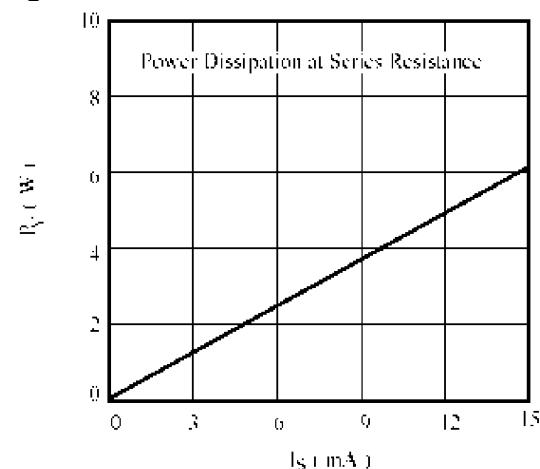


Fig.13

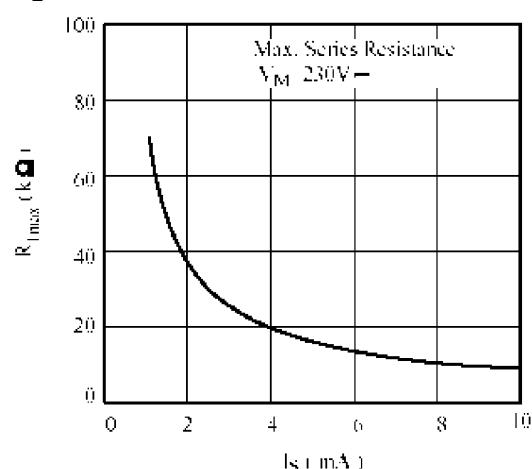


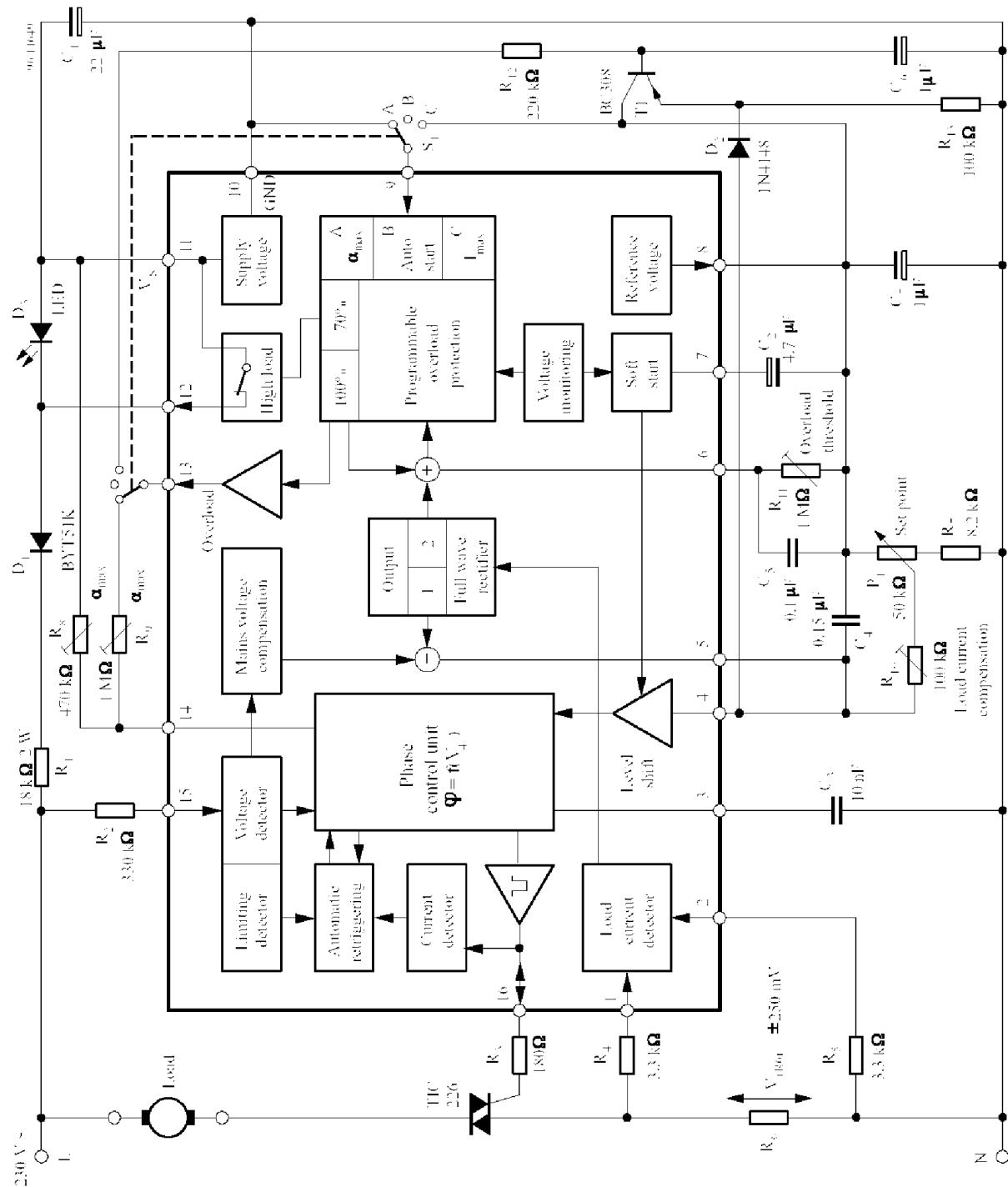
Fig.14



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