MC33501, MC33503

1.0 V, Rail-to-Rail, Single Operational Amplifiers

The MC33501/503 operational amplifier provides rail–to–rail operation on both the input and output. The output can swing within 50 mV of each rail. This rail–to–rail operation enables the user to make full use of the entire supply voltage range available. It is designed to work at very low supply voltages (1.0 V and ground), yet can operate with a supply of up to 7.0 V and ground. Output current boosting techniques provide high output current capability while keeping the drain current of the amplifier to a minimum.

- Low Voltage, Single Supply Operation (1.0 V and Ground to 7.0 V and Ground)
- High Input Impedance: Typically 40 fA Input Bias Current
- Typical Unity Gain Bandwidth @ 5.0 V = 4.0 MHz, @ 1.0 V = 3.0 MHz
- High Output Current (I_{SC} = 40 mA @ 5.0 V, 13 mA @ 1.0 V)
- Output Voltage Swings within 50 mV of Both Rails @ 1.0 V
- Input Voltage Range Includes Both Supply Rails
- High Voltage Gain: 100 dB Typical @ 1.0 V
- No Phase Reversal on the Output for Over–Driven Input Signals
- Input Offset Trimmed to 0.5 mV Typical
- Low Supply Current (I_D = 1.2 mA/per Amplifier, Typical)
- 600 Ω Drive Capability
- Extended Operating Temperature Range (–40 to 105°C)

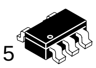
Applications

- Single Cell NiCd/Ni MH Powered Systems
- Interface to DSP
- Portable Communication Devices
- Low Voltage Active Filters
- Telephone Circuits
- Instrumentation Amplifiers
- Audio Applications
- Power Supply Monitor and Control
- Transistor Count: 98

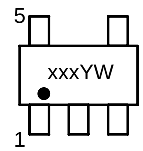
ON Semiconductor™

http://onsemi.com

MARKING DIAGRAM

5  1

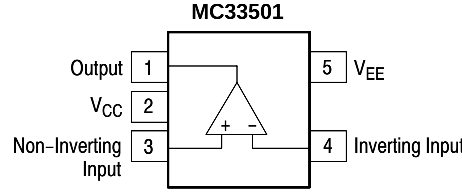
SOT23–5
(TSOP–5, SC59–5)
SN SUFFIX
CASE 483



xxx = 501 or 503
Y = Year
W = Work Week

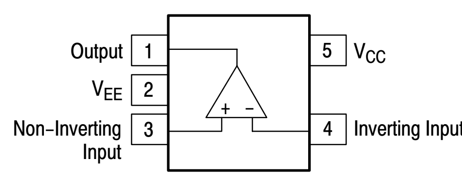
PIN CONNECTIONS

MC33501



(Top View)

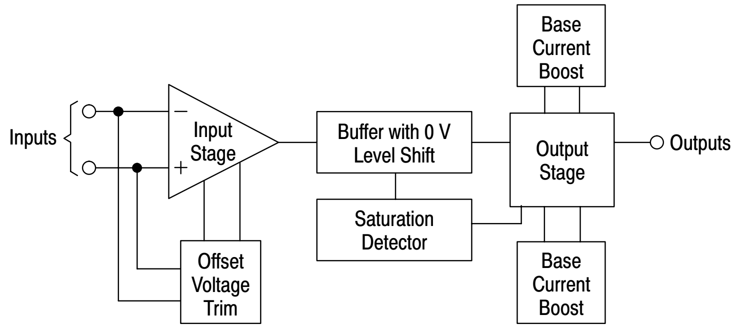
MC33503



(Top View)

ORDERING INFORMATION

Device	Package	Shipping
MC33501SNT1	SOT23–5	3000 Tape & Reel
MC33503SNT1	SOT23–5	3000 Tape & Reel



This device contains 98 active transistors per amplifier.

Figure 1. Simplified Block Diagram

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	7.0	V
ESD Protection Voltage at any Pin Human Body Model	V_{ESD}	2000	V
Voltage at Any Device Pin	V_{DP}	V_S ±0.3	V
Input Differential Voltage Range	V_{IDR}	V_{CC} to V_{EE}	V
Common Mode Input Voltage Range	V_{CM}	V_{CC} to V_{EE}	V
Output Short Circuit Duration	t_S	Note 1	s
Maximum Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	–65 to 150	°C
Maximum Power Dissipation	P_D	Note 1	mW

1. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.
2. ESD data available upon request.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = 0 V, V_{CM} = V_O = V_{CC}/2, R_L to V_{CC}/2, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (V_{CM} = 0 to V_{CC})	V_{IO}				mV
V_{CC} = 1.0 V					
T_A = 25°C		–5.0	0.5	5.0	
T_A = –40° to 105°C		–7.0	–	7.0	
V_{CC} = 3.0 V					
T_A = 25°C		–5.0	0.5	5.0	
T_A = –40° to 105°C		–7.0	–	7.0	
V_{CC} = 5.0 V					
T_A = 25°C		–5.0	0.5	5.0	
T_A = –40° to 105°C		–7.0	–	7.0	
Input Offset Voltage Temperature Coefficient (R_S = 50 Ω) T_A = –40° to 105°C	$\Delta V_{IO}/\Delta T$	–	8.0	–	µV/°C
Input Bias Current (V_{CC} = 1.0 to 5.0 V)	$\vert I_{IB}\vert$	–	0.00004	1.0	nA
Common Mode Input Voltage Range	V_{ICR}	V_{EE}	–	V_{CC}	V
Large Signal Voltage Gain	A_{VOL}				kV/V
V_{CC} = 1.0 V (T_A = 25°C)					
R_L = 10 kΩ		25	100	–	
R_L = 1.0 kΩ		5.0	50	–	
V_{CC} = 3.0 V (T_A = 25°C)					
R_L = 10 kΩ		50	500	–	
R_L = 1.0 kΩ		25	100	–	
V_{CC} = 5.0 V (T_A = 25°C)					
R_L = 10 kΩ		50	500	–	
R_L = 1.0 kΩ		25	200	–	
Output Voltage Swing, High (V_{ID} = ±0.2 V)	V_{OH}				V
V_{CC} = 1.0 V (T_A = 25°C)					
R_L = 10 kΩ		0.9	0.95	–	
R_L = 600 Ω		0.85	0.88	–	
V_{CC} = 1.0 V (T_A = –40° to 105°C)					
R_L = 10 kΩ		0.85	–	–	
R_L = 600 Ω		0.8	–	–	
V_{CC} = 3.0 V (T_A = 25°C)					
R_L = 10 kΩ		2.9	2.93	–	
R_L = 600 Ω		2.8	2.84	–	
V_{CC} = 3.0 V (T_A = –40° to 105°C)					
R_L = 10 kΩ		2.85	–	–	
R_L = 600 Ω		2.75	–	–	
V_{CC} = 5.0 V (T_A = 25°C)					
R_L = 10 kΩ		4.9	4.92	–	
R_L = 600 Ω		4.75	4.81	–	
V_{CC} = 5.0 V (T_A = –40° to 105°C)					
R_L = 10 kΩ		4.85	–	–	
R_L = 600 Ω		4.7	–	–	

DC ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 5.0 V, V_{EE} = 0 V, V_{CM} = V_O = $V_{CC}/2$, R_L to $V_{CC}/2$, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage Swing, Low (V_{ID} = ±0.2 V)	V_{OL}				V
V_{CC} = 1.0 V (T_A = 25°C)					
R_L = 10 kΩ		0.05	0.02	–	
R_L = 600 Ω		0.1	0.05	–	
V_{CC} = 1.0 V (T_A = –40° to 105°C)					
R_L = 10 kΩ		0.1	–	–	
R_L = 600 Ω		0.15	–	–	
V_{CC} = 3.0 V (T_A = 25°C)					
R_L = 10 kΩ		0.05	0.02	–	
R_L = 600 Ω		0.1	0.08	–	
V_{CC} = 3.0 V (T_A = –40° to 105°C)					
R_L = 10 kΩ		0.1	–	–	
R_L = 600 Ω		0.15	–	–	
V_{CC} = 5.0 V (T_A = 25°C)					
R_L = 10 kΩ		0.05	0.02	–	
R_L = 600 Ω		0.15	0.1	–	
V_{CC} = 5.0 V (T_A = –40° to 105°C)					
R_L = 10 kΩ		0.1	–	–	
R_L = 600 Ω		0.2	–	–	
Common Mode Rejection (V_{in} = 0 to 5.0 V)	CMR	60	75	–	dB
Power Supply Rejection V_{CC}/V_{EE} = 5.0 V/Ground to 3.0 V/Ground	PSR	60	75	–	dB
Output Short Circuit Current (V_{in} Diff = ±1.0 V)	I_{SC}				mA
V_{CC} = 1.0 V					
Source		6.0	13	26	
Sink		10	13	26	
V_{CC} = 3.0 V					
Source		15	32	60	
Sink		40	64	140	
V_{CC} = 5.0 V					
Source		20	40	140	
Sink		40	70	140	
Power Supply Current (Per Amplifier, V_O = 0 V)	I_D				mA
V_{CC} = 1.0 V		–	1.2	1.75	
V_{CC} = 3.0 V		–	1.5	2.0	
V_{CC} = 5.0 V		–	1.65	2.25	
V_{CC} = 1.0 V (T_A = –40 to 105°C)		–	–	2.0	
V_{CC} = 3.0 V (T_A = –40 to 105°C)		–	–	2.25	
V_{CC} = 5.0 V (T_A = –40 to 105°C)		–	–	2.5	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = 0 V, V_{CM} = V_O = V_{CC}/2, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Slew Rate (V_S = ±2.5 V, V_O = –2.0 to 2.0 V, R_L = 2.0 kΩ, A_V = 1.0)	SR				V/µs
Positive Slope		1.8	3.0	6.0	
Negative Slope		1.8	3.0	6.0	
Gain Bandwidth Product (f = 100 kHz)	GBW				MHz
V_{CC} = 0.5 V, V_{EE} = –0.5 V		2.0	3.0	6.0	
V_{CC} = 1.5 V, V_{EE} = –1.5 V		2.5	3.5	7.0	
V_{CC} = 2.5 V, V_{EE} = –2.5 V		3.0	4.0	8.0	
Gain Margin (R_L =10 kΩ, C_L = 0 pF)	Am	–	6.5	–	dB
Phase Margin (R_L = 10 kΩ, C_L = 0 pF)	ϕ_m	–	60	–	Deg
Channel Separation (f = 1.0 Hz to 20 kHz, R_L = 600 Ω)	CS	–	120	–	dB
Power Bandwidth (V_O = 4.0 V_{pp}, R_L = 1.0 kΩ, THD ≤1.0%)	BW_P	–	200	–	kHz
Total Harmonic Distortion (V_O = 4.5 V_{pp}, R_L = 600 Ω, A_V = 1.0)	THD				%
f = 1.0 kHz		–	0.004	–	
f = 10 kHz		–	0.01	–	
Differential Input Resistance (V_{CM} = 0 V)	R_{in}	–	>1.0	–	terraΩ
Differential Input Capacitance (V_{CM} = 0 V)	C_{in}	–	2.0	–	pF
Equivalent Input Noise Voltage (V_{CC} = 1.0 V, V_{CM} = 0 V, V_{EE} = Gnd, R_S = 100 Ω)	e_n				nV/√Hz
f = 1.0 kHz		–	30	–	

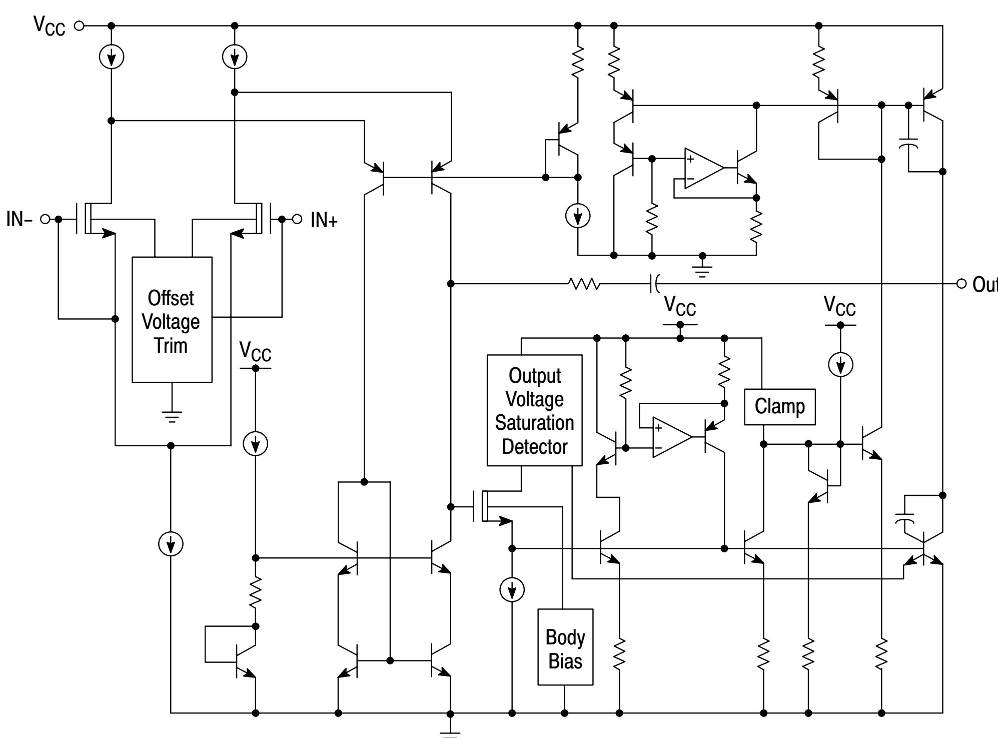


Figure 2. Representative Block Diagram

General Information

The MC33501/503 dual operational amplifier is unique in its ability to provide 1.0 V rail–to–rail performance on both the input and output by using a SMARTMOS™ process. The amplifier output swings within 50 mV of both rails and is able to provide 50 mA of output drive current with a 5.0 V supply, and 10 mA with a 1.0 V supply. A 5.0 MHz bandwidth and a slew rate of 3.0 V/µs is achieved with high speed depletion mode NMOS (DNMOS) and vertical PNP transistors. This device is characterized over a temperature range of –40°C to 105°C.

Circuit Information

Input Stage

One volt rail–to–rail performance is achieved in the MC33501/503 at the input by using a single pair of depletion mode NMOS devices (DNMOS) to form a differential amplifier with a very low input current of 40 fA. The normal input common mode range of a DNMOS device, with an ion implanted negative threshold, includes ground and relies on the body effect to dynamically shift the threshold to a positive value as the gates are moved from ground towards the positive supply. Because the device is manufactured in a p–well process, the body effect coefficient is sufficiently large to ensure that the input stage will remain substantially saturated when the inputs are at the positive rail. This also applies at very low supply voltages. The 1.0 V rail–to–rail input stage consists of a DNMOS differential amplifier, a folded cascode, and a low voltage balanced mirror. The low voltage cascoded balanced mirror provides high 1st stage gain and base current cancellation without sacrificing signal integrity. Also, the input offset voltage is trimmed to less than 1.0 mV because of the limited available supply voltage. The body voltage of the input DNMOS differential pair is internally trimmed to minimize the input offset voltage. A common mode feedback path is also employed to enable the offset voltage to track over the input common mode voltage. The total operational amplifier quiescent current drop is 1.3 mA/amp.

Output Stage

An additional feature of this device is an “on demand” base current cancellation amplifier. This feature provides base drive to the output power devices by making use of a buffer amplifier to perform a voltage–to–current conversion. This is done in direct proportion to the load conditions. This “on demand” feature allows these amplifiers to consume only a few micro–amps of current when the output stage is in its quiescent mode. Yet it provides high output current when required by the load. The rail–to–rail output stage current boost circuit provides 50 mA of output current with a 5.0 V supply (For a 1.0 V supply output stage will do 10 mA) enabling the operational amplifier to drive a 600 Ω load. A buffer is necessary to isolate the load current effects in the output stage from the input stage. Because of the low voltage conditions, a DNMOS follower is used to provide an essentially zero voltage level shift. This buffer isolates any load current changes on the output stage from loading the input stage. A high speed vertical PNP transistor provides excellent frequency performance while sourcing current. The operational amplifier is also internally compensated to provide a phase margin of 60 degrees. It has a unity gain of 5.0 MHz with a 5.0 V supply and 4.0 MHz with a 1.0 V supply.

Low Voltage Operation

The MC33501/503 will operate at supply voltages from 0.9 to 7.0 V and ground. When using the MC33501/503 at supply voltages of less than 1.2 V, input offset voltage may increase slightly as the input signal swings within approximately 50 mV of the positive supply rail. This effect occurs only for supply voltages below 1.2 V, due to the input depletion mode MOSFETs starting to transition between the saturated to linear region, and should be considered when designing high side dc sensing applications operating at the positive supply rail. Since the device is rail–to–rail on both input and output, high dynamic range single battery cell applications are now possible.

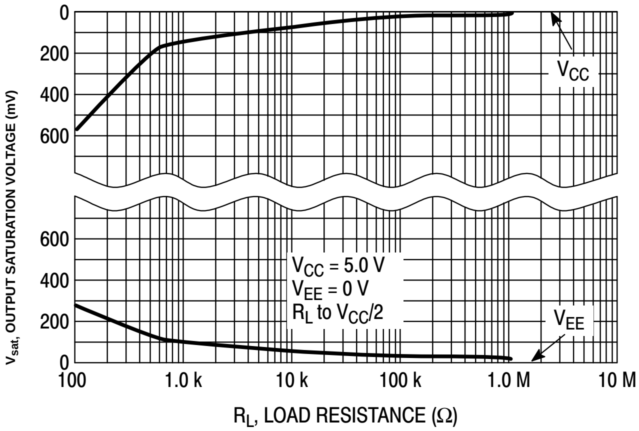


Figure 3. Output Saturation versus Load Resistance

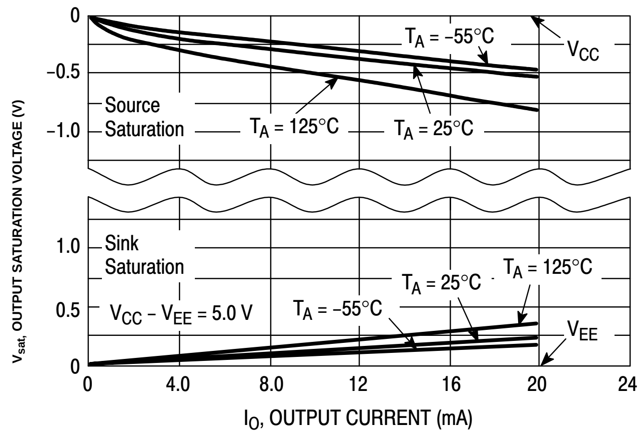


Figure 4. Drive Output Source/Sink Saturation Voltage versus Load Current

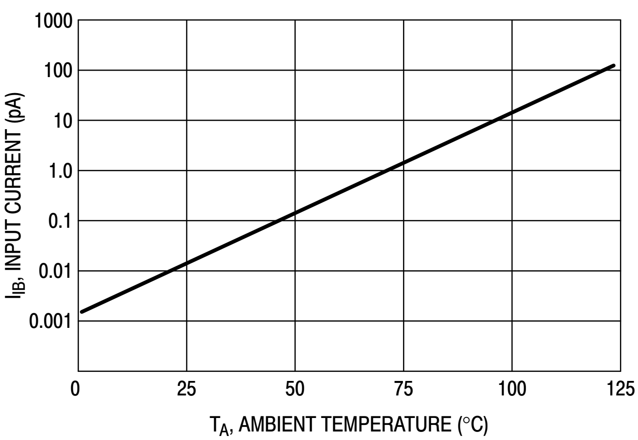


Figure 5. Input Current versus Temperature

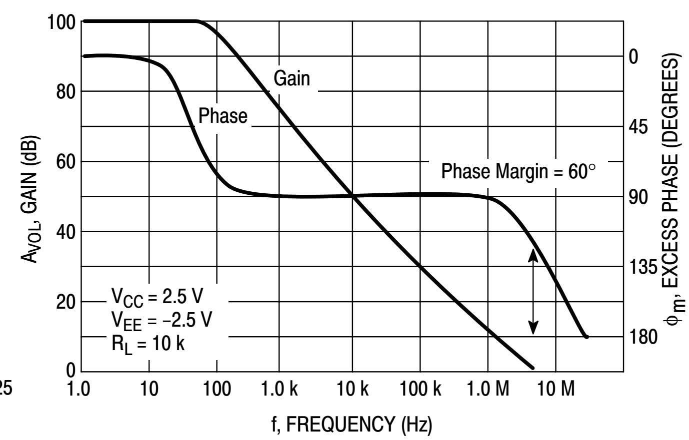


Figure 6. Gain and Phase versus Frequency

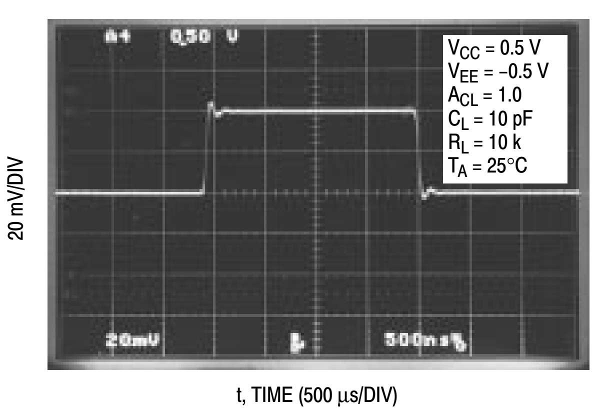


Figure 7. Transient Response

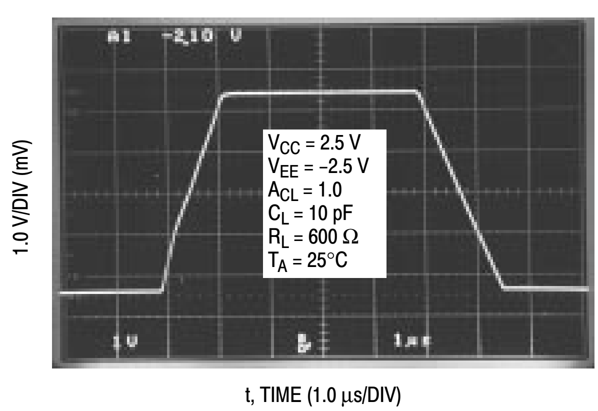


Figure 8. Slew Rate

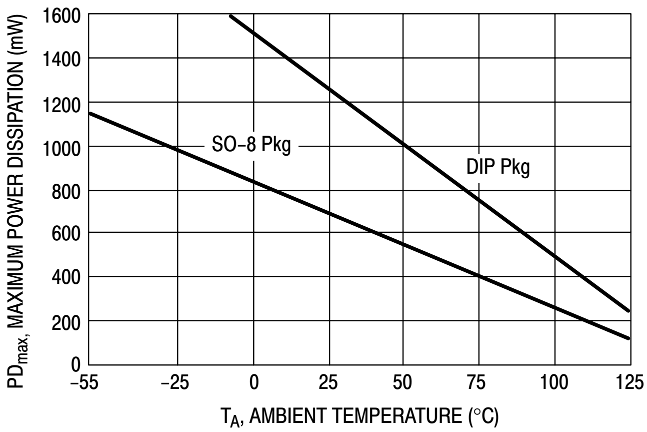


Figure 9. Maximum Power Dissipation versus Temperature

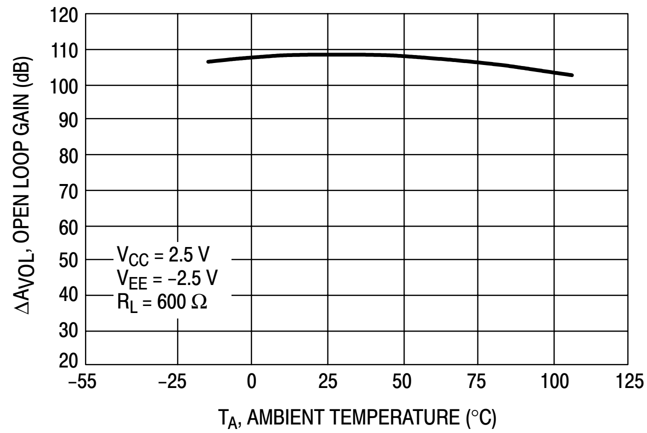


Figure 10. Open Loop Voltage Gain versus Temperature

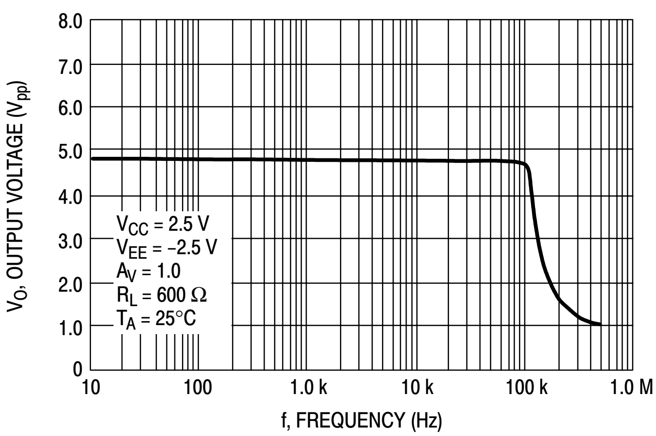


Figure 11. Output Voltage versus Frequency

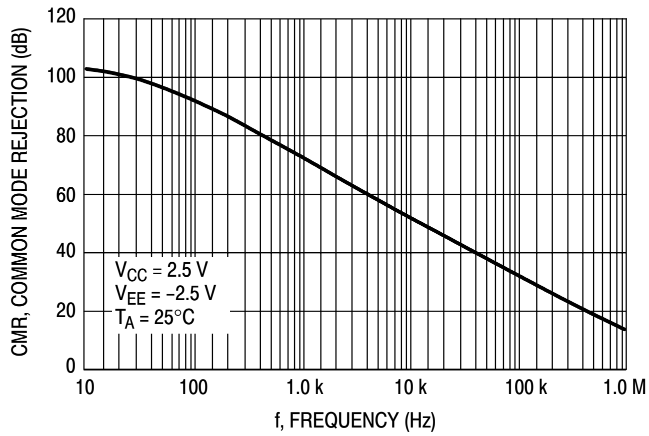


Figure 12. Common Mode Rejection versus Frequency

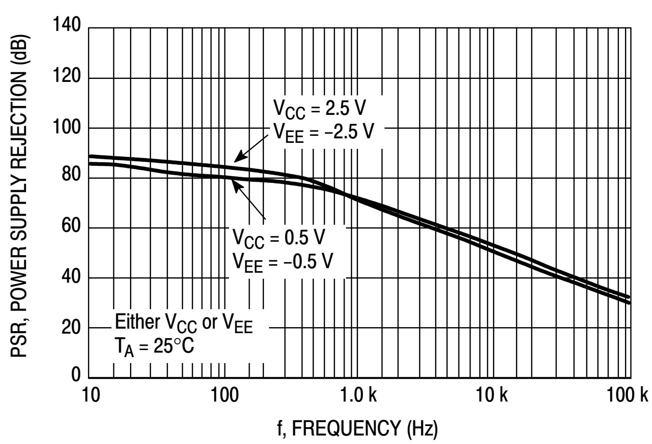


Figure 13. Power Supply Rejection versus Frequency

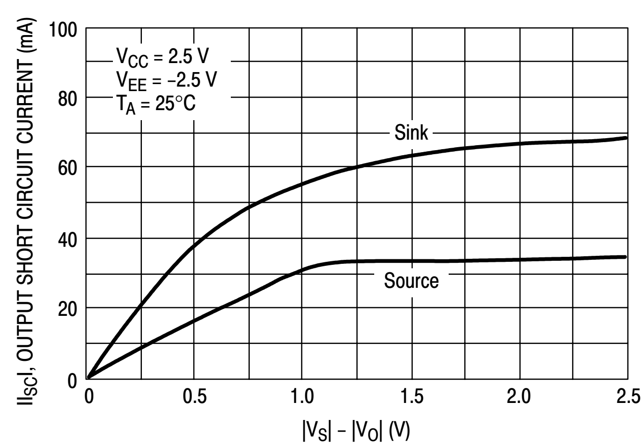


Figure 14. Output Short Circuit Current versus Output Voltage

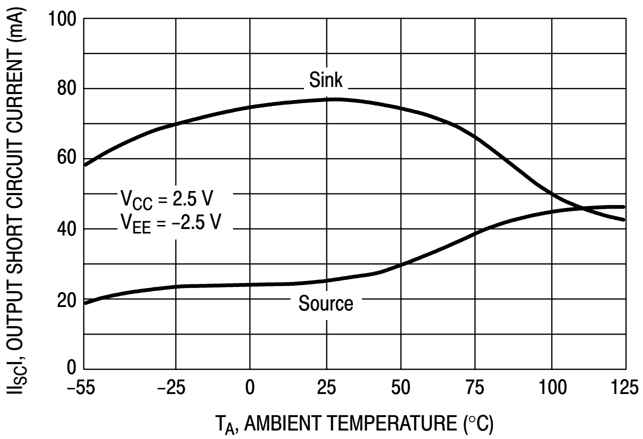


Figure 15. Output Short Circuit Current versus Temperature

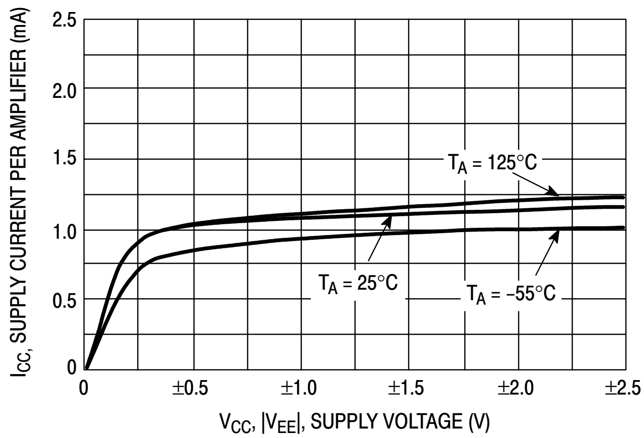


Figure 16. Supply Current per Amplifier versus Supply Voltage with No Load

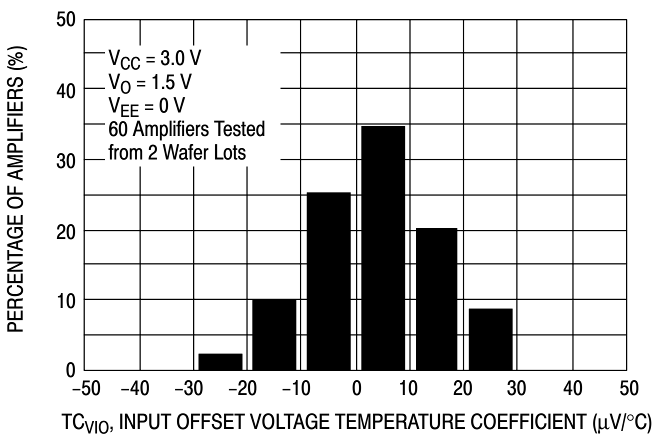


Figure 17. Input Offset Voltage Temperature Coefficient Distribution

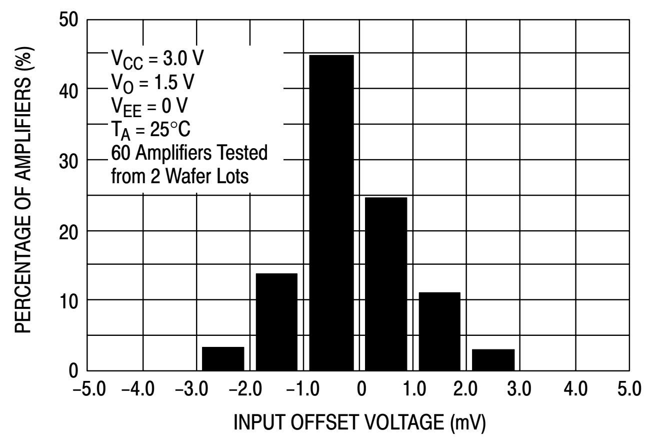


Figure 18. Input Offset Voltage Distribution

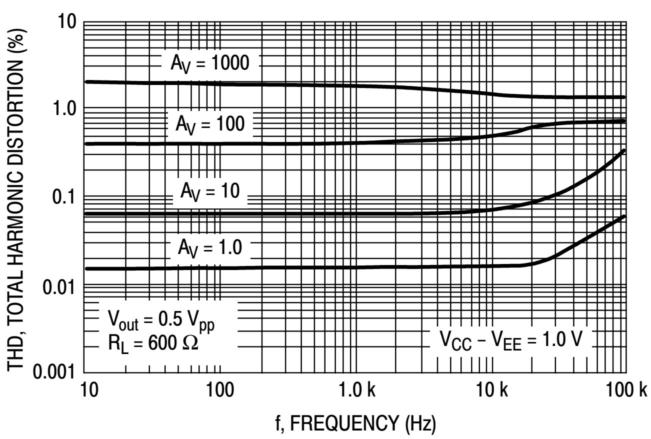


Figure 19. Total Harmonic Distortion versus Frequency with 1.0 V Supply

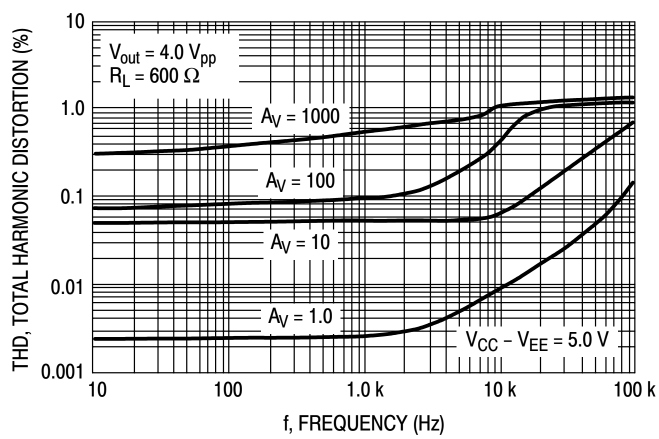


Figure 20. Total Harmonic Distortion versus Frequency with 5.0 V Supply

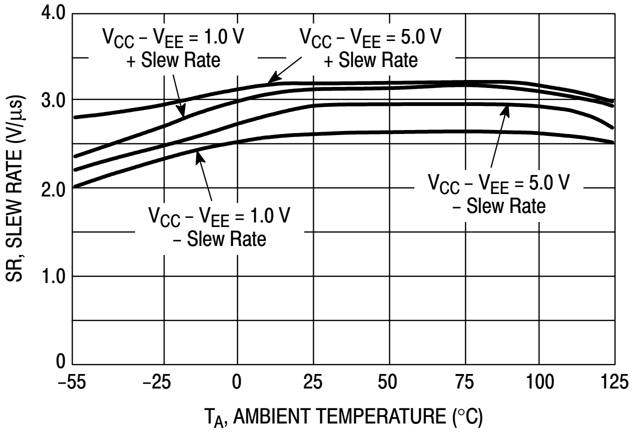


Figure 21. Slew Rate versus Temperature

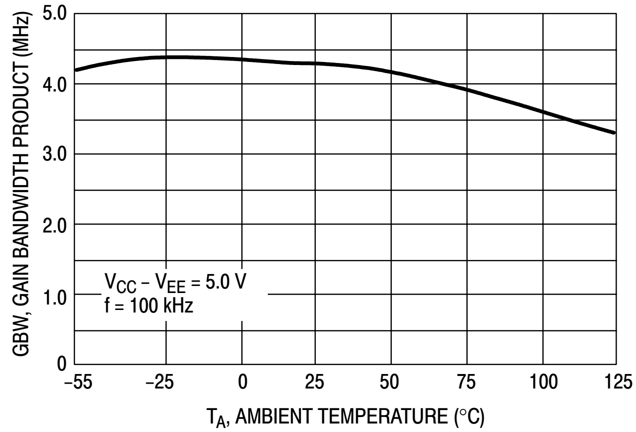


Figure 22. Gain Bandwidth Product versus Temperature

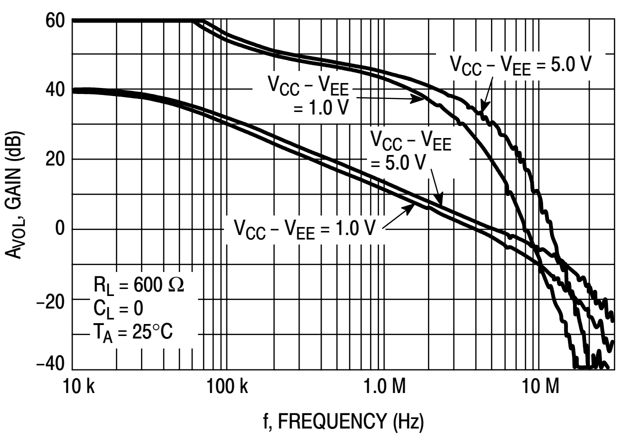


Figure 23. Voltage Gain and Phase versus Frequency

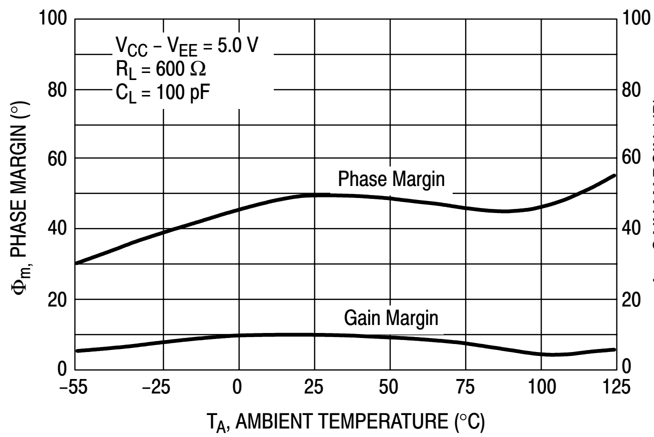


Figure 24. Gain and Phase Margin versus Temperature

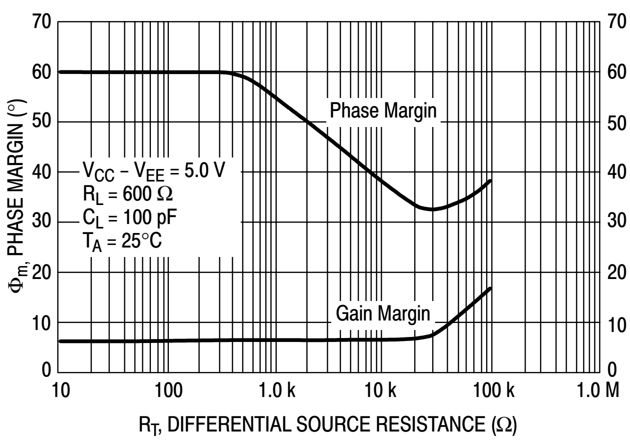


Figure 25. Gain and Phase Margin versus Differential Source Resistance

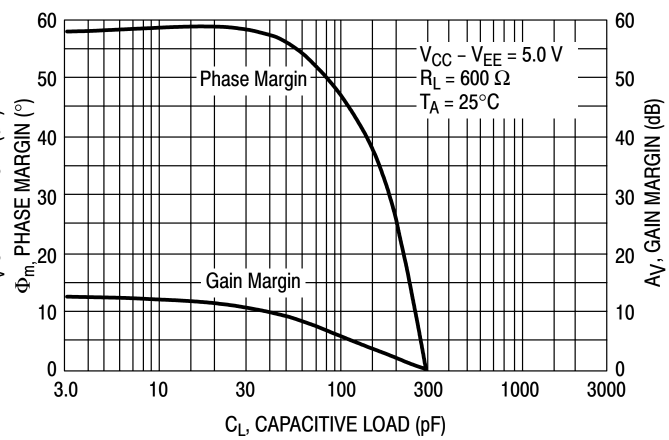


Figure 26. Feedback Loop Gain and Phase versus Capacitive Load

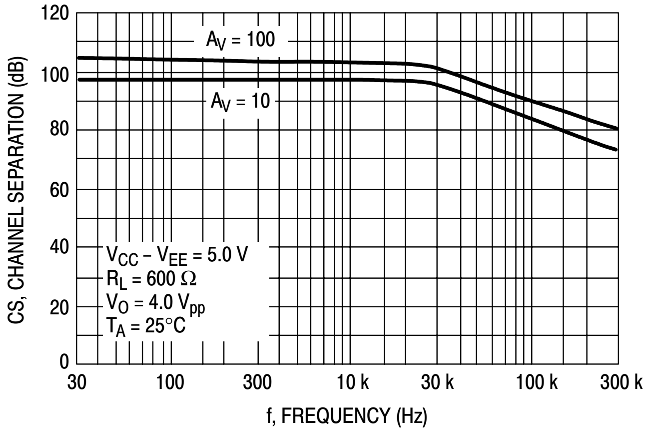


Figure 27. Channel Separation versus Frequency

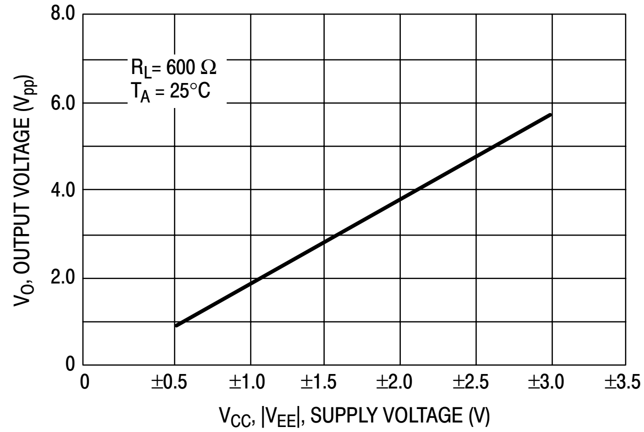


Figure 28. Output Voltage Swing versus Supply Voltage

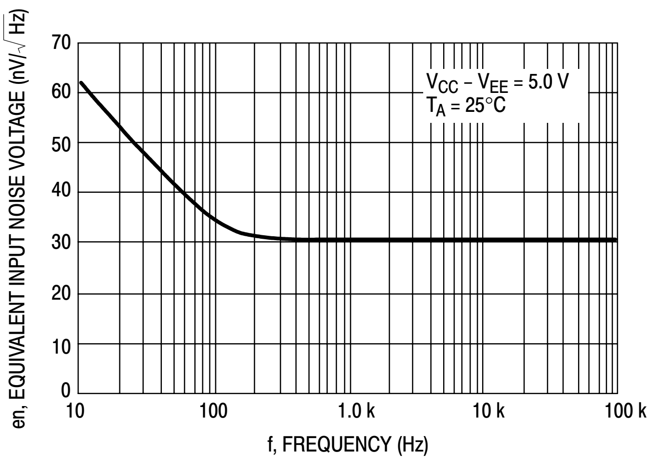


Figure 29. Equivalent Input Noise Voltage versus Frequency

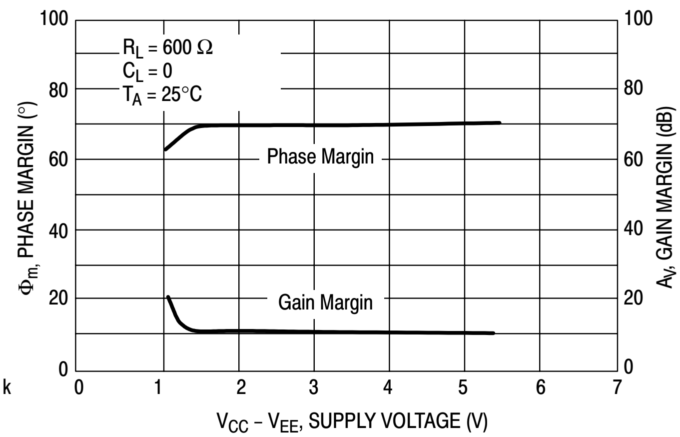


Figure 30. Gain and Phase Margin versus Supply Voltage

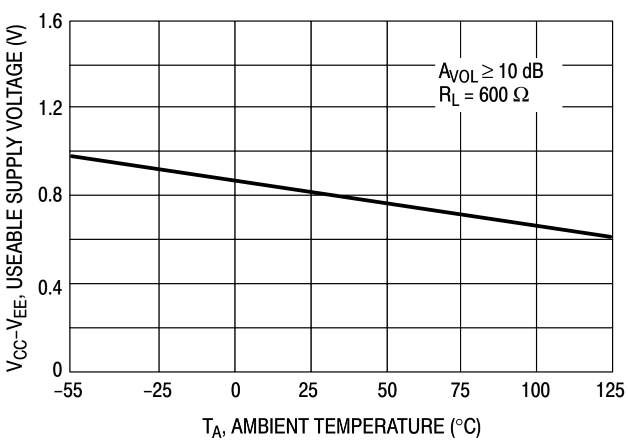


Figure 31. Useable Supply Voltage versus Temperature

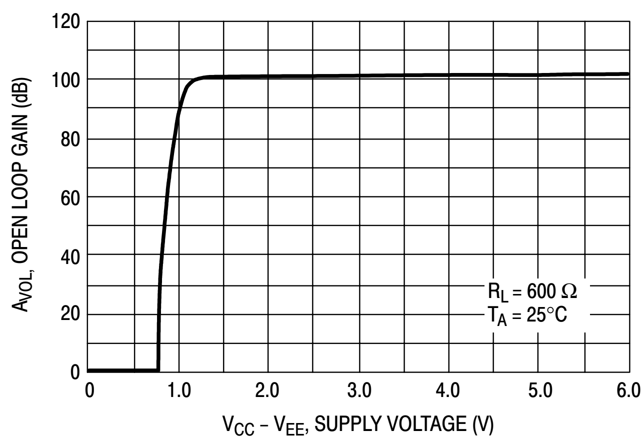
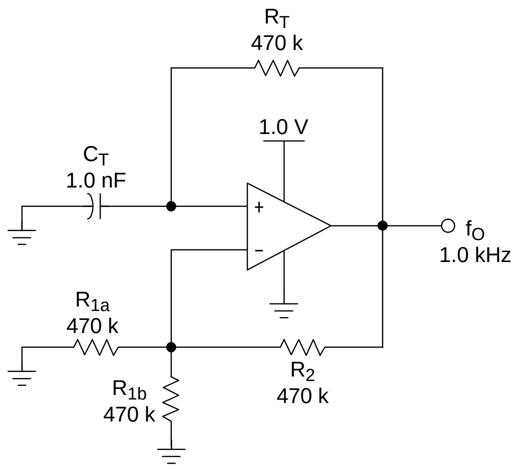
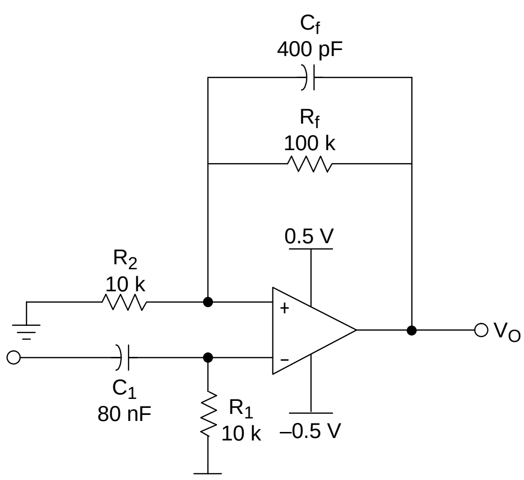


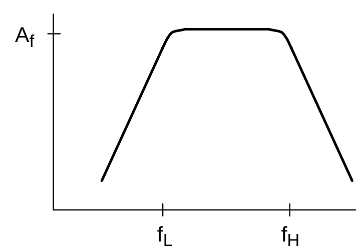
Figure 32. Open Loop Gain versus Supply Voltage



$$f_O = \frac{1}{2\,R_T C_T \ln\left[\frac{2\,(R_{1a} + R_{1b})}{R_2}\right]}$$

Figure 33. 1.0 V Oscillator





$$f_L = \frac{1}{2\,\pi\,R_1 C_1} \approx 200\text{ Hz}$$

$$f_H = \frac{1}{2\,\pi\,R_f C_f} \approx 4.0\text{ kHz}$$

$$A_f = 1 + \frac{R_f}{R_2} = 11$$

Figure 34. 1.0 V Voiceband Filter

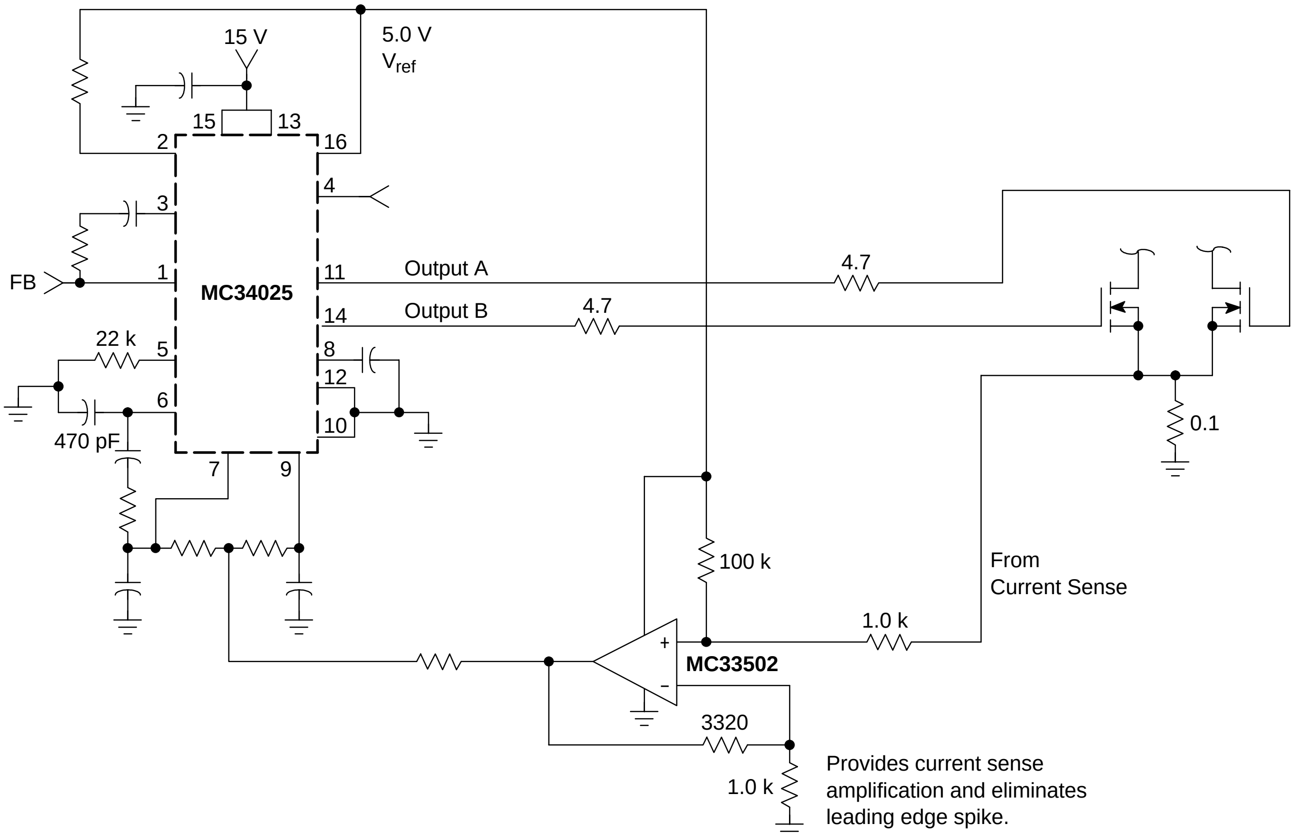
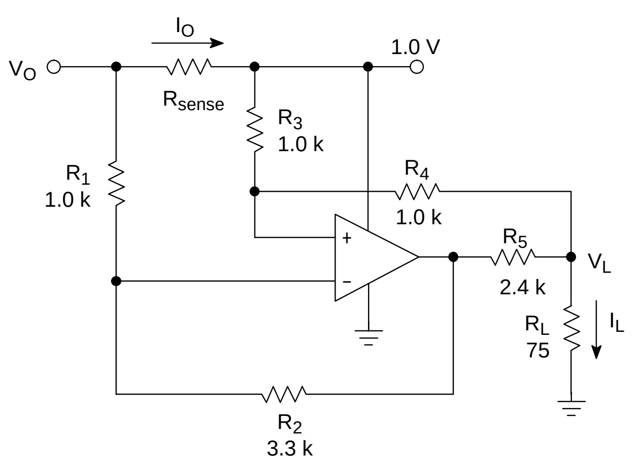


Figure 35. Power Supply Application



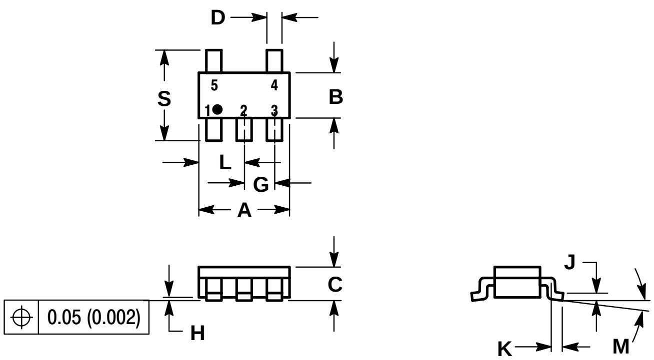
I_O	I_L	$\Delta I_O/\Delta I_L$
435 mA	463 µA	-120×10^{-6}
212 mA	492 µA	

For best performance, use low tolerance resistors.

Figure 36. 1.0 V Current Pump

PACKAGE DIMENSIONS

SOT23–5
(TSOP–5, SC59–5)
SN SUFFIX
CASE 483–01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.1142	0.1220
B	1.30	1.70	0.0512	0.0669
C	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.05	0.0335	0.0413
H	0.013	0.100	0.0005	0.0040
J	0.10	0.26	0.0040	0.0102
K	0.20	0.60	0.0079	0.0236
L	1.25	1.55	0.0493	0.0610
M	0°	10°	0°	10°
S	2.50	3.00	0.0985	0.1181

Notes

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303–675–2175 or 800–344–3860 Toll Free USA/Canada
Fax: 303–675–2176 or 800–344–3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com

N. American Technical Support: 800–282–9855 Toll Free USA/Canada

JAPAN: ON Semiconductor, Japan Customer Focus Center
4–32–1 Nishi–Gotanda, Shinagawa–ku, Tokyo, Japan 141–0031
Phone: 81–3–5740–2700
Email: r14525@onsemi.com

ON Semiconductor Website: http://onsemi.com

For additional information, please contact your local Sales Representative.