



## P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY		
V <sub>DS</sub> (V)	r <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)
-20	0.065 @ V <sub>GS</sub> = -4.5 V	-4.9
	0.095 @ V <sub>GS</sub> = -2.5 V	-4.1

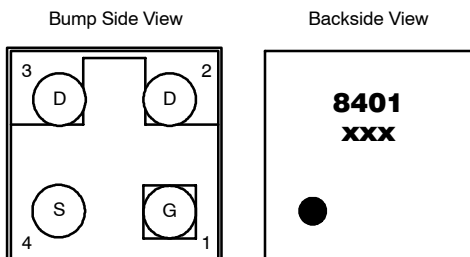
### FEATURES

- TrenchFET® Power MOSFET
- New MICRO FOOT® Chipscale Packaging Reduces Footprint Area Profile (0.62 mm) and On-Resistance Per Footprint Area
- Pin Compatible to Industry Standard Si3443DV

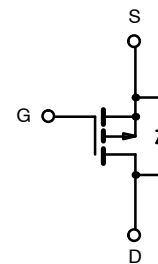
### APPLICATIONS

- PA, Battery and Load Switch
- Battery Charger Switch
- PA Switch

### MICRO FOOT



Device Marking: 8401  
xxx = Date/Lot Traceability Code



P-Channel MOSFET

Ordering Information: Si8401DB-T1  
Si8401DB-T1—E3 (Lead Free)

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C UNLESS OTHERWISE NOTED)					
Parameter	Symbol	5 secs	Steady State	Unit	
Drain-Source Voltage	V <sub>DS</sub>	-20		V	
Gate-Source Voltage	V <sub>GS</sub>	± 12			
Continuous Drain Current (T <sub>J</sub> = 150 °C) <sup>a</sup>	I <sub>D</sub>	T <sub>A</sub> = 25 °C	-4.9	-3.6	A
		T <sub>A</sub> = 70 °C	-3.9	-2.8	
Pulsed Drain Current	I <sub>DM</sub>	-10			
continuous Source Current (Diode Conduction) <sup>a</sup>	I <sub>S</sub>	-2.5	-2.5		
Maximum Power Dissipation <sup>a</sup>	P <sub>D</sub>	T <sub>A</sub> = 25 °C	2.77	1.47	W
		T <sub>A</sub> = 70 °C	1.77	0.94	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	-55 to 150		°C
Package Reflow Conditions <sup>b</sup>	VPR	215/245°			
	IR/Convection	220/250°			

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>a</sup>	R <sub>thJA</sub>	t ≤ 5 sec	35	45	°C/W
		Steady State	72	85	
Maximum Junction-to-Foot (drain)	R <sub>thJF</sub>	16	20		

**Notes**

- Surface Mounted on 1" x 1" FR4 Board.
- Refer to IPC/JEDEC (J-STD-020A), no manual or hand soldering.
- Package reflow conditions for lead-free.

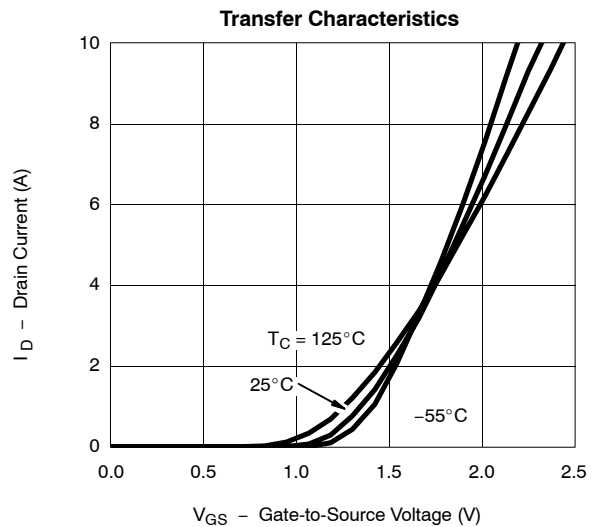
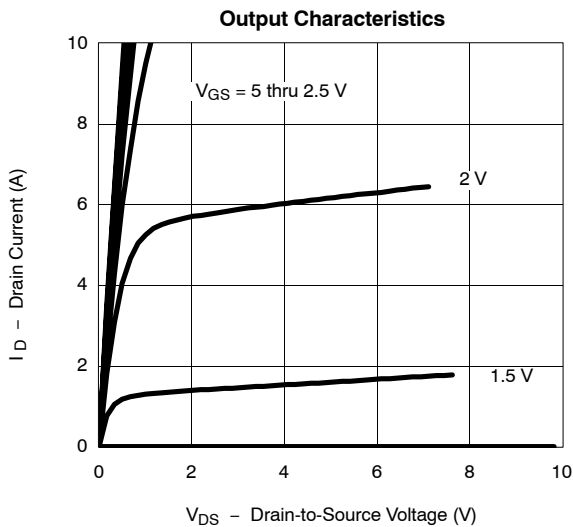
**SPECIFICATIONS (T<sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Static</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	-0.45	-0.9		V
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±12 V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -20 V, V <sub>GS</sub> = 0 V			-1	μA
		V <sub>DS</sub> = -20 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 70 °C			-5	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≤ -5 V, V <sub>GS</sub> = -4.5 V	-5			A
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -1 A		0.057	0.065	Ω
		V <sub>GS</sub> = -2.5 V, I <sub>D</sub> = -1 A		0.080	0.095	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -1 A		6		S
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = -1 A, V <sub>GS</sub> = 0 V		-0.73	-1.1	V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = -10 V, V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -1 A		11	17	nC
Gate-Source Charge	Q <sub>gs</sub>			2.1		
Gate-Drain Charge	Q <sub>gd</sub>			2.9		
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = -10 V, R <sub>L</sub> = 10 Ω I <sub>D</sub> ≅ -1 A, V <sub>GEN</sub> = -4.5 V, R <sub>G</sub> = 6 Ω		17	25	ns
Rise Time	t <sub>r</sub>			28	45	
Turn-Off Delay Time	t <sub>d(off)</sub>			88	135	
Fall Time	t <sub>f</sub>			60	90	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>		I <sub>F</sub> = - A, di/dt = 100 A/μs			

Notes

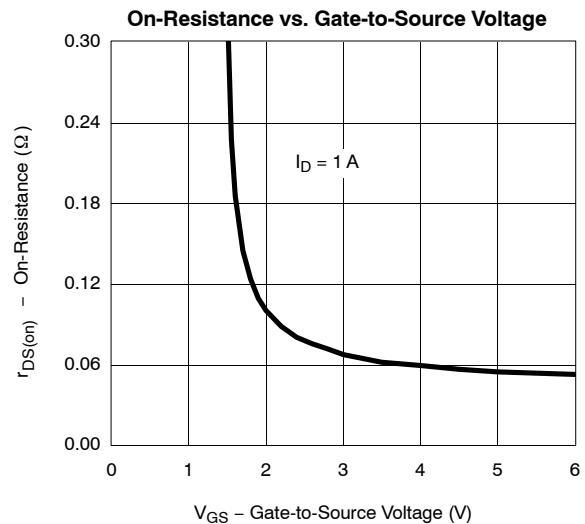
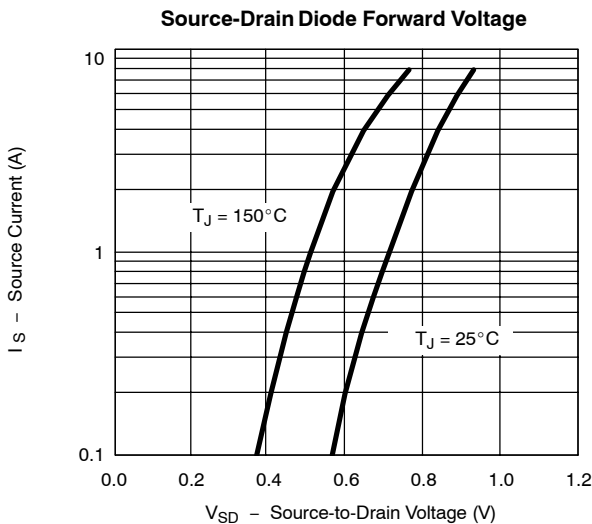
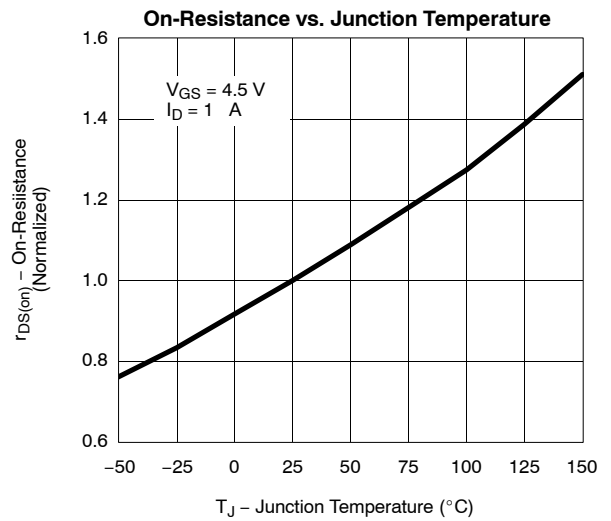
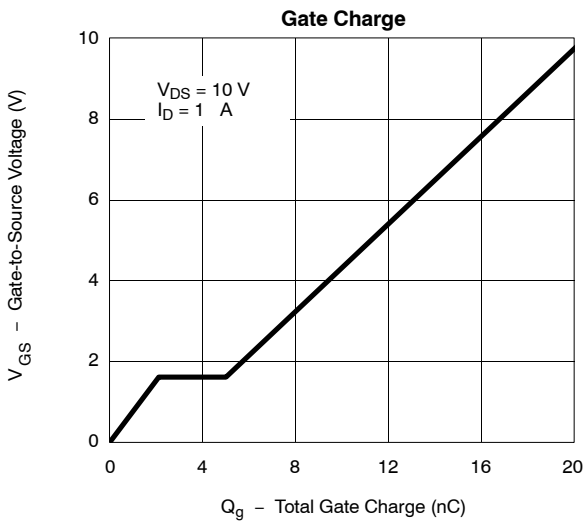
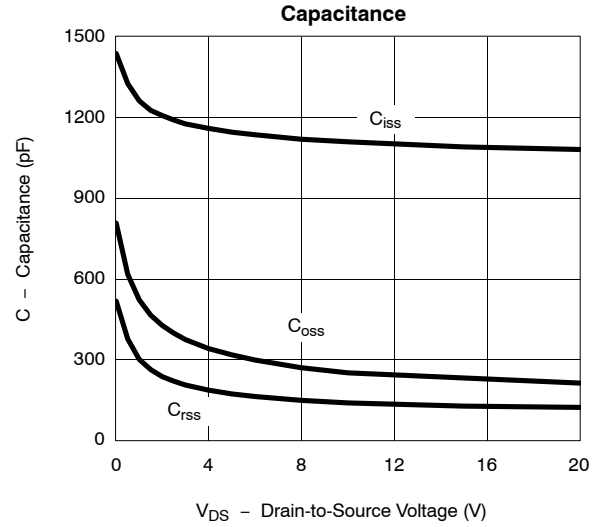
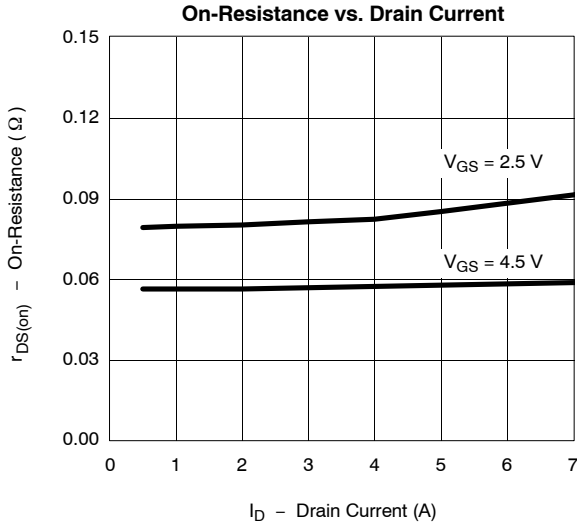
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)**

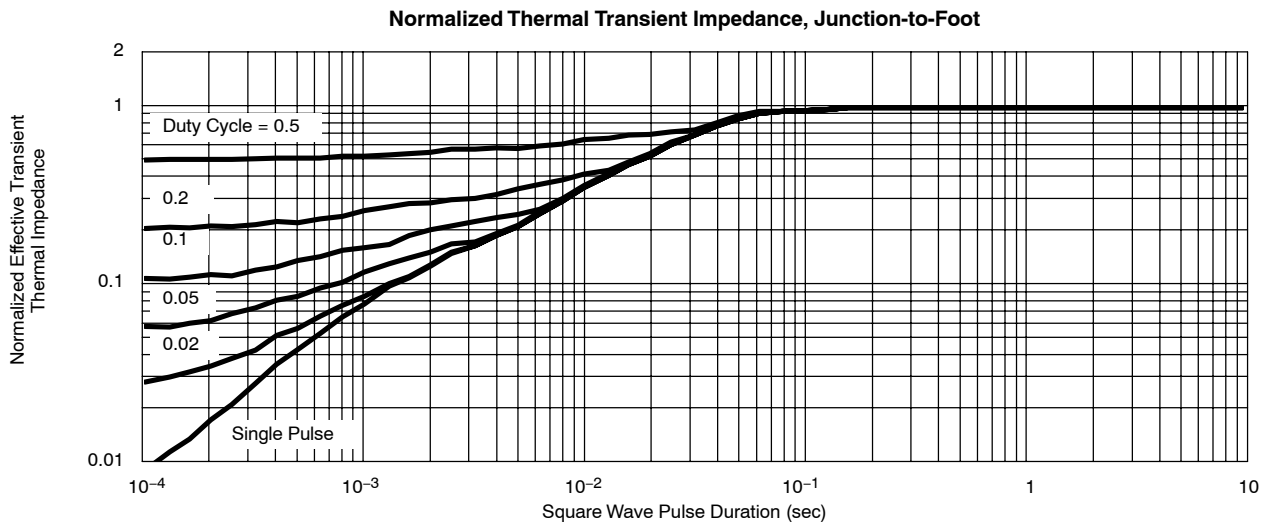
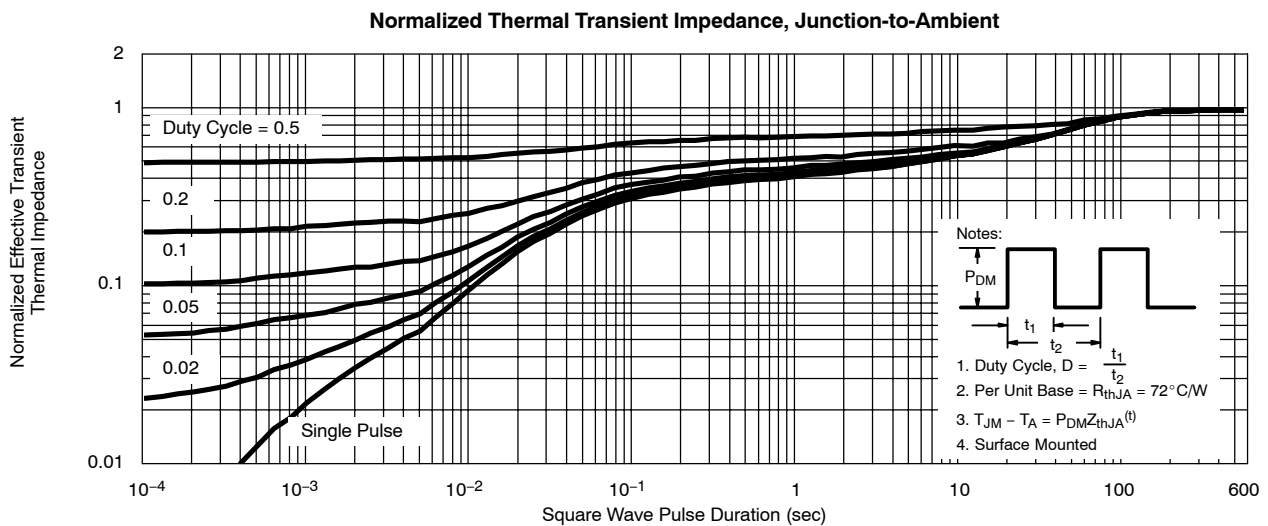
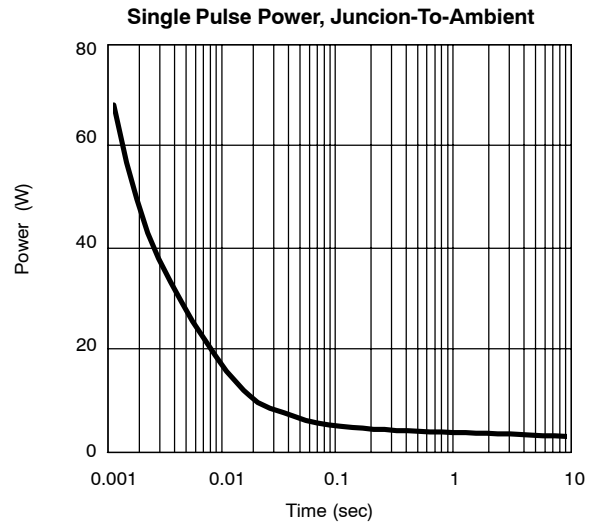
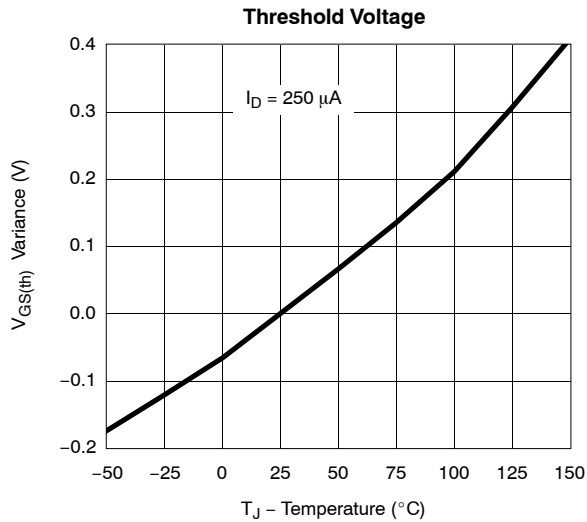




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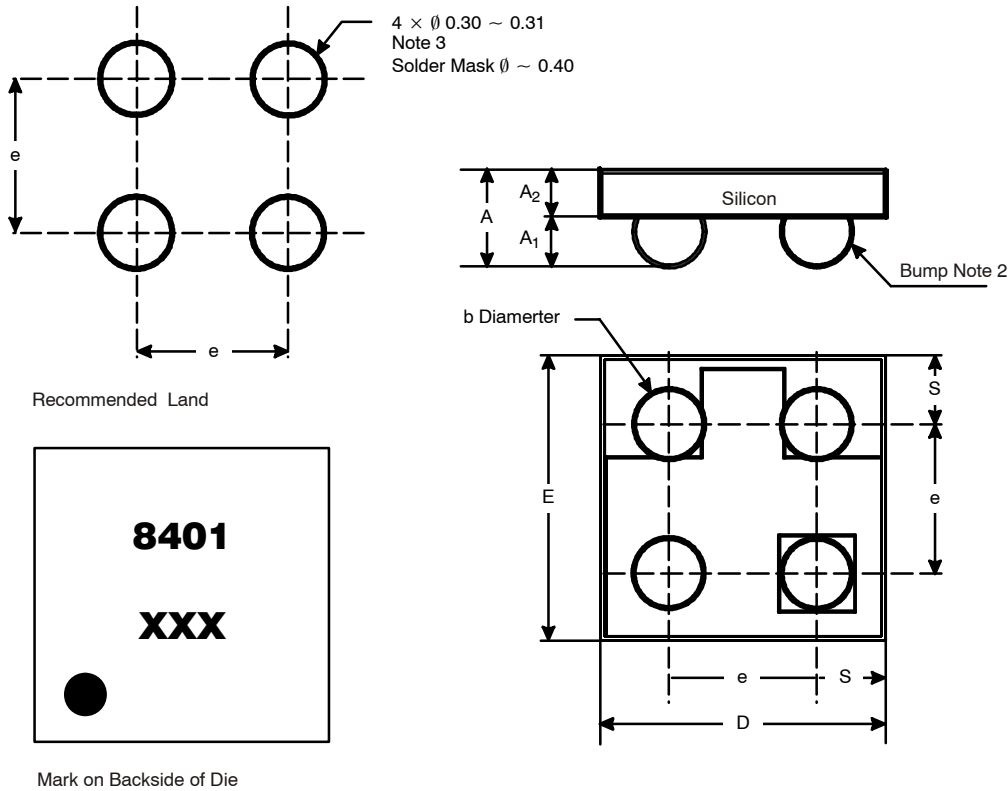


**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)**



**PACKAGE OUTLINE**

**MICRO FOOT: 4-BUMP (2 X 2, 0.8-mm PITCH)**



NOTES (Unless Otherwise Specified):

1. Laser mark on the silicon die back, coated with a thin metal.
2. Bumps are Eutectic solder 63/57 Sn/Pb. (Sn 3.8 Ag, 0.7 Cu for Pb-free bumps)
3. Non-solder mask defined copper landing pad.
4. The flat side of wafers is oriented at the bottom.

Dim	MILLIMETERS*		INCHES	
	Min	Max	Min	Max
<b>A</b>	0.600	0.650	0.0236	0.0256
<b>A<sub>1</sub></b>	0.260	0.290	0.0102	0.0114
<b>A<sub>2</sub></b>	0.340	0.360	0.0134	0.0142
<b>b</b>	0.370	0.410	0.0146	0.0161
<b>D</b>	1.520	1.600	0.0598	0.0630
<b>E</b>	1.520	1.600	0.0598	0.0630
<b>e</b>	0.750	0.850	0.0295	0.0335
<b>S</b>	0.370	0.380	0.0146	0.0150

\* Use millimeters as the primary measurement.