SIEMENS

TV Stereo Processor — TDA 6611

Preliminary Data — **Bipolar IC**

Features

The TDA 6611 represents a complete TV stereo system controlled by the I²C bus.

- All functions inclusive matrix adjustment are I²C bus controlled
- SCART-Interface
- Independent headphones
- Higher signal noise ratio
- Extremely low distorsion
- High security rata against mis-switching of the decoder performed by the digital interference suppression and the very narrow bandwidth

Type	Ordering Code	Package
TDA 6611	Q67000-A8260	P-DIP-28

The IC is divided into three functional blocks

1) **Stereo sound processing with high quality (exceeds DIN 45500; suitable for NICAM and CD)**
   a) matrix for G standard with crosstalk compensation controlled via the I²C Bus
   b) additional single-channel AF input (for e.g. AF signal accord. L standard)
   c) stereo SCART interface in accordance with FTZ official brochure
   d) stereo loudspeaker signal section with Ch1/Ch2 switch, high/low regulation, quasi-stereo/stereo basic processing and separate loudspeaker regulation for left and right
   e) signal section with Ch1/Ch2 switch and loudspeaker regulation for stereo headphones

2) **TV sound identification signal decoder consisting of:**
   a) active pilot signal filter
   b) phase-independent rectifier with very narrow bandwidth for evaluation of the identification signal
   c) digital integrator to reduce interference
   d) multiplexer for cyclical switch over between "stereo" or "dual" evaluation
   e) PLL for the generation of the reference signal. External synchronization with either the flyback pulse or external reference clock signals of 62.5 kHz or 4 MHz can also be generated using the internal crystal generator with an external crystal.

3) Control section for:

a) I^2C bus interface with listener/talker function
b) control of the complete AF sound processing
c) control of the identification signal decoder
d) reading of the identification signal decoder
e) test modes

Circuit Description

Signal Section

The audio signal processing in the matrix and the switch-over for multichannel TV sound signals according to the two-carrier system used in Germany takes place in the matrix and switching sections. Crosstalk compensation is carried out in the Sound 1 input. The compensation range has an adjustment range of ± 3 dB with a minimum step of 0.2 dB. In addition to the two inputs for the demodulated sound carrier, a two-channel scart input and an additional mono input (e.g. for demodulated L-standard sound) are provided. The two AF inputs can be bypassed internally in such a way that decoded stereo sound signals of other audio systems (NICAM) can be processed. The switching section is terminated with the SCART output and an independently switchable Ch1/Ch2 switch for the loudspeaker and headphone outputs.

In the loudspeaker signal path a switchable quasi-stereo section follows the Ch1/Ch2 switch. This section gives a special audio effect with mono signals due to a 180° phase shift at medium frequencies (about 1 kHz) in one channel. The following base control exhibits a step of 3 dB with an adjustment range of + 15/– 12 dB. The cutoff frequency is set for each channel with an external capacitor. The circuit for stereo basewidth expansion, which, with switchable stereo signals, provides a more special audio effect due to 50 % of frequency dependent crosstalk in opposing phases, operates with the same cutoff frequency as the base control, but the function is largely independent. The treble control, whose cutoff frequency is also controlled by a capacitor in each channel, also has a step of 3 dB with an adjustment range of ± 12 dB. The loudspeaker signal path is terminated with a loudspeaker control, independently adjustable for left and right. With 57 steps of 1.25 dB the adjustment range is 70 dB, where step 57 activates the "MUTE" function. Functions such as "balance" or "loudness" are realized by software adjustment of the appropriate tone and volume controls.

The signal path for the headphones contains a volume control after the Ch1/Ch2 switch with a common adjustment for left and right. Thirty-two steps of 2 dB give an adjustment range of 62 dB (31 × 2 dB = 62 dB, the 32nd step is MUTE).

Identification Signal Decoder

The input of the identification signal decoder consists of an op-amp for the pilot signal with its sidebands. An external LC circuit is used. The signal is then passed to a phase-independent active bandpass filter with a very narrow bandwidth (adjustable externally). This filter detects whether the lower sideband of the pilot carrier, which is modulated with the identification signal, is present. The center frequency of the filter is switched between "dual" and" stereo" by a multiplexer. The multiplexing frequency is adjustable by software. If a sideband is detected, the multiplexer stops. The first "detected" criterion is rendered free from interference by a digital integrator with a following comparator and can be read out via I^2C bus (talk mode) as the "stereo" or "dual" mode. The control of the corresponding signal can be either directly internally or through the µC. All the necessary clock signals are derived from a fast settling PLL which is synchronized by a reference frequency. This reference frequency must be sufficiently close to the horizontal frequency, but a **rigid phase coupling is not required**. Therefore, alternatively the use of a crystal-controlled 62.5-kHz frequency commonly found in PLL tuning systems is possible.

Control Section

All functions are controlled via I²C bus interface with listen/talk functions. The current applicable data are stored in a block of latches.

The telegram structure is formed in the following manner:

start condition – chip address – any number of bytes – stop condition

The following conditions apply to the data bytes:
Before the actual data byte (with the adjustment information), a subaddress by the I²C bus byte must **always** be transmitted. This byte is however interpreted by the I²C bus as a data byte interface.

Example: The headphone volume is to be increased in a number of steps.

Right	**Wrong**
start condition	start condition
chip address 84 (hex)	chip address 84 (hex)
subaddr. vol. HP 03 (hex)	subaddr. vol HP 03 (hex)
vol. step 8 08 (hex)	vol. step 8 08 (hex)
subaddr. vol. HP 03 (hex)	vol. step 9.09 (hex)
vol. step 9 09 (hex)	vol. step 10 0A (hex)
subaddr. HP 03 (hex)	stop condition
vol. step 10 0A (hex)	
stop condition	

Within a telegram (i.e. without a new start condition) any different subaddresses can be accessed. The changeover between "listen" and "talk" must however always occur via the sequence stop condition – start condition – chip address. Before each readout always a start condition and chip address (talk) must be transmitted. The data to be read out are loaded into the I²C bus interface and can be transferred to the µC.

Chip Address

	MSB	.	.	.	.	.	.	LSB
	1	0	0	0	0	1	0	R/W

R/W = 0 → read (listen)
R/W = 1 → write (talk)

Subaddress Bytes

	MSB	.	.	.	.	.	.	LSB
Vol. of left speaker	X	X	X	X	X	0	0	1
Vol. of right speaker	X	X	X	X	X	0	1	0
Vol. of headphones	X	X	X	X	X	0	1	1
Treble/bases	X	X	X	X	X	1	0	1
Switch byte I	X	X	X	X	X	1	1	1
Switch byte II	X	X	X	X	X	0	0	0
Crosstalk compensation	X	X	X	X	X	1	1	0

Setting Bytes

a) Volume of left/right loudspeaker

	MSB	.	.	.	.	.	.	LSB
Maximum volume	X	X	1	1	1	1	1	1
Max - 1	X	X	1	1	1	1	1	0
Max - 15	X	X	1	1	0	0	0	0
Max - 55	X	X	0	0	1	0	0	0
MUTE	X	X	0	0	0	1	1	1
MUTE	X	X	0	0	0	0	0	0
MUTE	X	X	0	0	0	X	X	X
Power on	0	0	0	0	0	0	0	1

b) Volume of headphones

	MSB	.	.	.	.	.	.	LSB
Max. volume	T2	T1	T0	1	1	1	1	1
Max - 1	T2	T1	T0	1	1	1	1	0
Max - 15	T2	T1	T0	1	0	0	0	0
Max - 31	T2	T1	T0	0	0	0	0	1
MUTE	T2	T1	T0	0	0	0	0	0
Power on	0	0	0	0	0	0	0	1

T0-T2 are test bits; these must be set to 0 for normal operation

c) Crosstalk compensation matrix (sound 1)

	MSB	.	.	.	.	.	.	LSB
Max. amplification	X	X	X	1	1	1	1	1
Max - 1	X	X	X	1	1	1	1	0
Gain 0 dB	X	X	X	1	0	0	0	0
Min. gain	X	X	X	0	0	0	0	1
Min. gain	X	X	X	0	0	0	0	X
Power on	0	0	0	0	0	0	0	1

d) Treble/bass

	MSB	.	.	.	.	.	.	LSB
Linear	1	0	0	0	1	0	0	0
Max. treble, lin. bass	1	1	0	0	1	0	0	0
Max. treble, lin. bass	1	1	X	X	1	0	0	0
Min. treble, lin. bass	0	1	0	0	1	0	0	0
Min. treble, lin. bass	0	0	X	X	1	0	0	0
Lin. treble, max. bass	1	0	0	0	1	1	0	1
Lin. treble, max. bass	1	0	0	0	1	1	X	1
Lin. treble, max. bass	1	0	0	0	1	1	1	X
Lin. treble, min. bass	1	0	0	0	0	1	0	0
Lin. treble, min. bass	1	0	0	0	0	0	X	X
Max. treble, max. bass	1	1	X	X	1	1	X	1
Min. treble, min. bass	0	0	X	X	0	0	X	X
Power on	0	0	0	0	0	0	0	1
	MSB treble			LSB treble	MSB bass			LSB bass

e) Switch byte I

MSB LSB

MUTE I MUTE II < $Ch1/Ch2_{vol}$ $Ch1/Ch2_{HP}$ Mono SCART SCART-D AM
MUTE I = 0 All AF outputs are muted (speakers, headphones, SCART); power on
MUTE I = 1 All AF outputs on
MUTE II = 0 Loudspeaker outputs muted; power on
MUTE II = 1 Loudspeaker outputs on
MUTE I and MUTE II are OR gated with respect to the loudspeaker outputs

MUTE I	MUTE II	loudspeaker outputs	headphones, SCART o/p
0	0	muted	muted
0	1	muted	muted
1	0	muted	on
1	1	on	on

$Ch1/Ch2_{vol}$	= 0	Sound 1 on the loudspeaker outputs; power on
$Ch1/Ch2_{vol}$	= 1	Sound 2 on the loudspeaker outputs
$Ch1/Ch2_{HP}$	= 0	Sound 1 on the headphone outputs; power on
$Ch1/Ch2_{HP}$	= 1	Sound 2 on the headphone outputs

$Ch1/Ch2_{vol}$ and $Ch1/Ch2_{HP}$ are only effective if the matrix is set to the position "dual sound".

Mono	= 0	identification signal decoder is set to the position mono and held; power on
Mono	= 1	normal operation of ID signal decoder
SCART	= 0	normal TV operation; power on
SCART	= 1	SCART playback; connection of SCART inputs – AF outputs. SCART = 1 has priority over AM = 1 (loudspeaker and headphones)
SCART-D	= 0	SCART playback stereo (mono); power on
SCART-D	= 1	Enable for the Ch1/Ch2 switch during SCART playback (only effective when SCART = 1)
AM	= 0	normal operation (G standard)
AM	= 1	AM AF input is activated; power on AM = 1 has priority over Bypass = 1

f) Switch byte II

MSB							LSB
MPX0	MPX1	quasi-st	Be	H pul	Matrix 0	Matrix 1	Bypass

MPX0	MPX1	MPX period		recommended $C_{25,26}$
0	0	2 s	power on	1 µF
0	1	4 s		2.2 µF
1	0	8 s		4.7 µF
1	1	1 s		470 nF

MPX period = 2 s signifies: ID signal decoder searches 1 second dual and 1 second stereo

Quasi-st	= 0	Quasi-stereo off; power on
Quasi-st	= 1	Quasi-stereo on
Be	= 0	stereo basewidth expansion off; power on
Bb	= 1	stereo basewidth expansion on;

H pul	= 0	ID signal decoder synchronization with f_H = 15.625 kHz; power on
H pul	= 1	ID synchronization with 4 × f_H

Matrix 0	Matrix 1	matrix status	
0	0	mono	power on
0	1	stereo	
1	0	dual	
1	1	automatic according to ID signal decoder	

Bypass	= 0	normal operation (G standard)
Bypass	= 1	matrix is bridged so that left/right signals can be fed in; power on (AM = 1 has priority over Bypass = 1)

Priority list of setting bits

1. MUTE I
2. MUTE II (only with regard to the loudspeaker output)
3. SCART
4. AM
5. Bypass
6. Matrix 0, 1

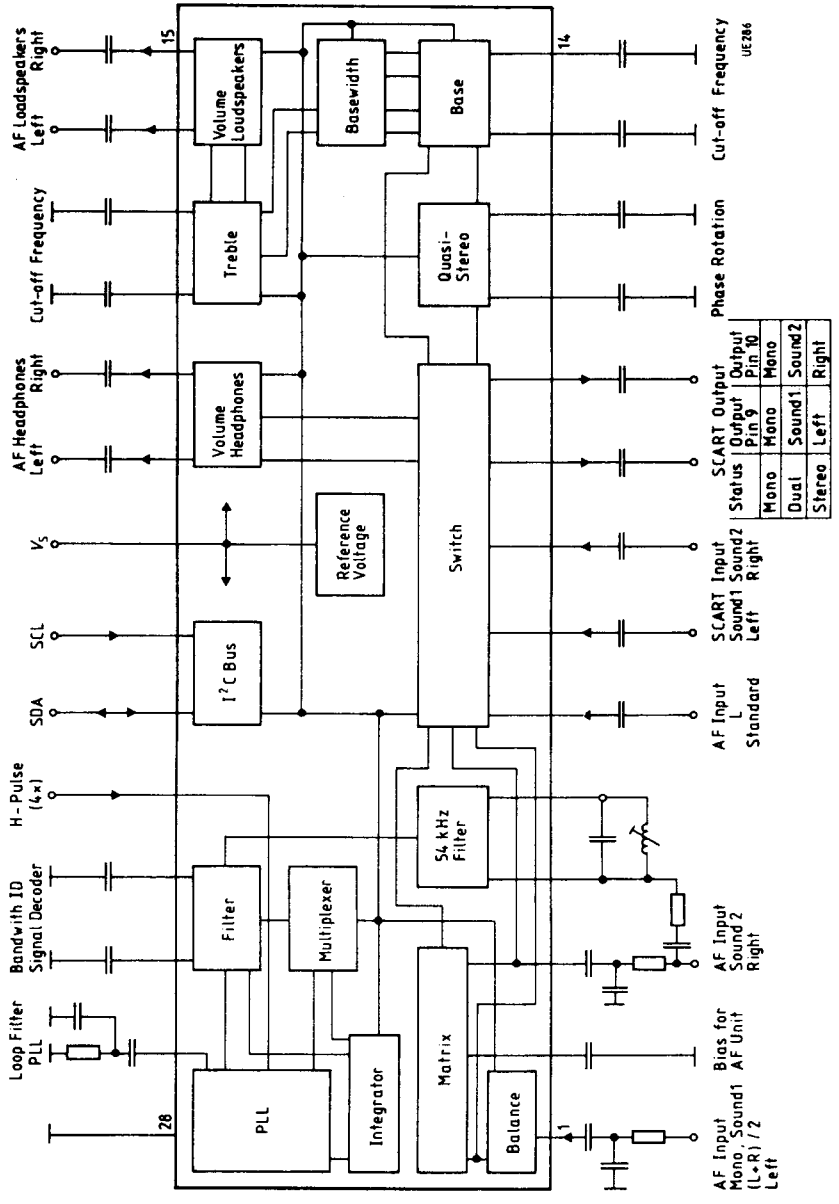
g) Talk mode

MSB	.	.	.	.	.	.	LSB
St	D	T5	T4	T3	X	X	X

0	0	decoder detects mono
1	0	decoder detects stereo
0	1	decoder detects dual
1	1	internally inhibited

T3 – T5 are test bits

Block Diagram

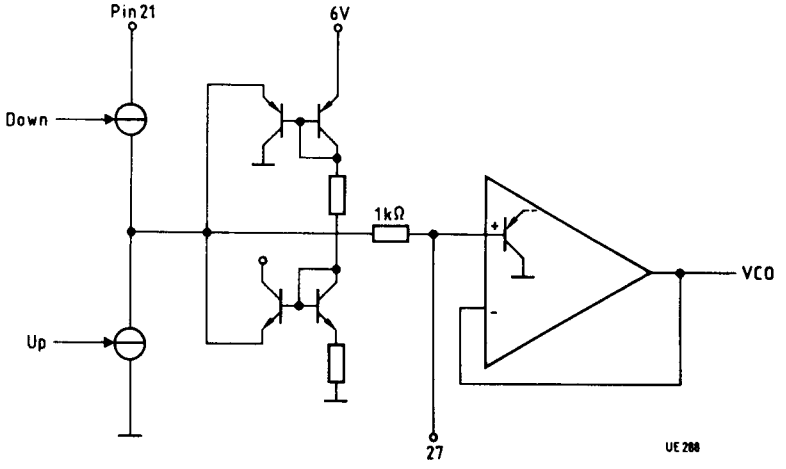


Pin Functions

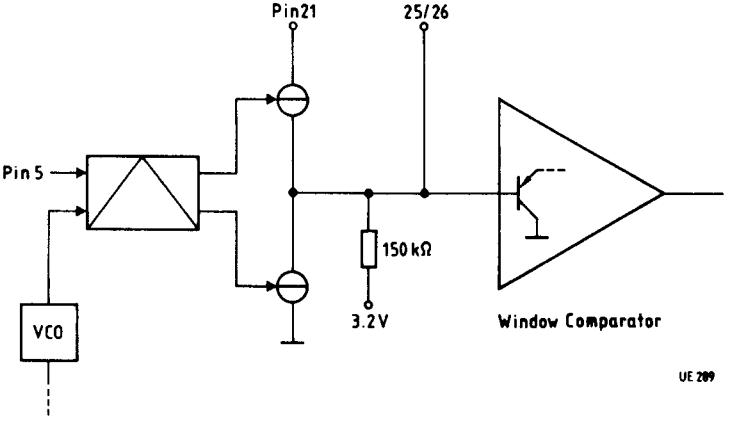
Pin No.	Function
1	AF input mono, left, sound 1 (may be balanced)
2	Bias for AF operating point
3	AF input right, sound 2
4	54-kHz input
5	54-kHz filter
6	AF input (L standard)
7	AF input SCART left (sound 1)
8	AF input SCART right (sound 2)
9	AF output SCART (mono, sound 1, left)
10	AF output SCART (mono, sound 2, right)
11	Phase-shifter quasi-stereo
12	Phase-shifter quasi-stereo
13	Cutoff frequency base (basewidth) left
14	Cutoff frequency base (basewidth) right
15	AF output, loudspeaker left
16	AF output, loudspeaker right
17	Cutoff frequency treble left
18	Cutoff frequency treble right
19	AF output, headphones left
20	AF output, headphones right
21	Supply voltage
22	I^2C bus SCL
23	I^2C bus SDA
24	Input H pulse (4 × H pulse)
25	Filter ID signal decoder
26	Filter ID signal decoder
27	PLL filter ID signal decoder
28	Ground

Pin Functions

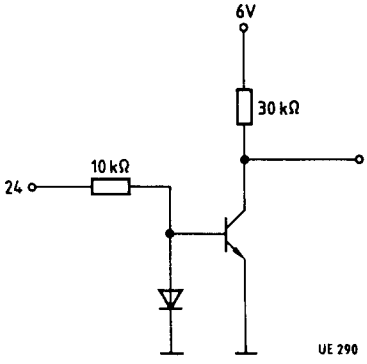
PLL Filter ID Signal Decoder (Pin 27)



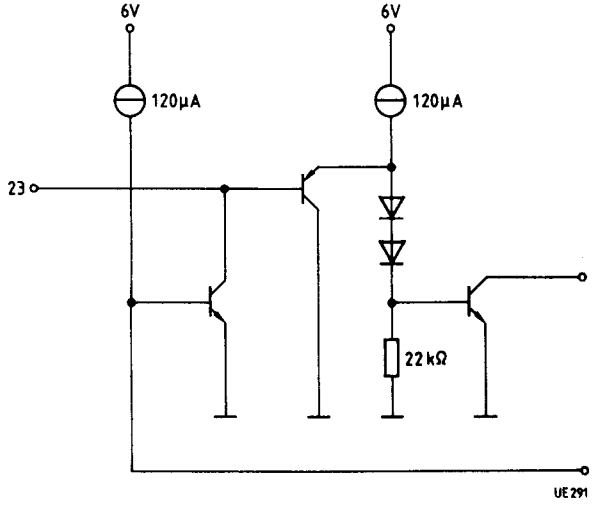
Filter ID Signal Decoder (Pin 25/26)



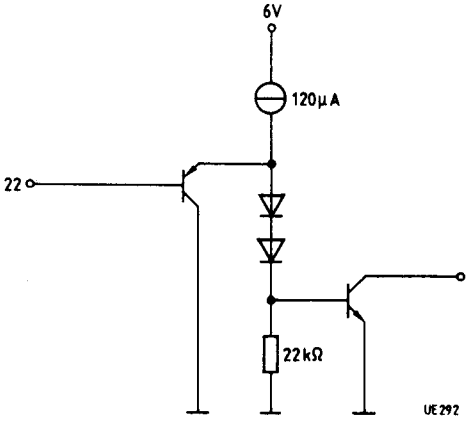
Input H Pulse (Pin 24)



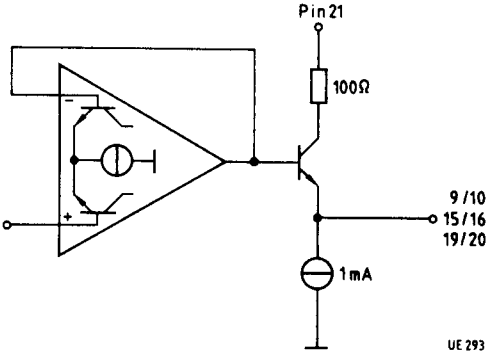
I²C Bus SDA (Pin 23)



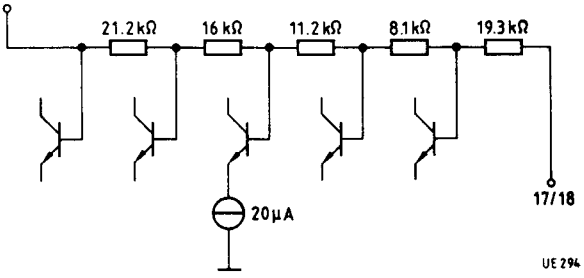
I²C Bus SCL (Pin 22)



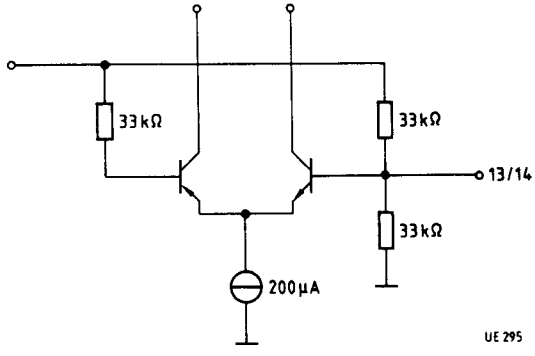
AF Outputs Headphones (Pin 19/20)
Loudspeaker (Pin 15/16)
SCART (Pin 9/10)



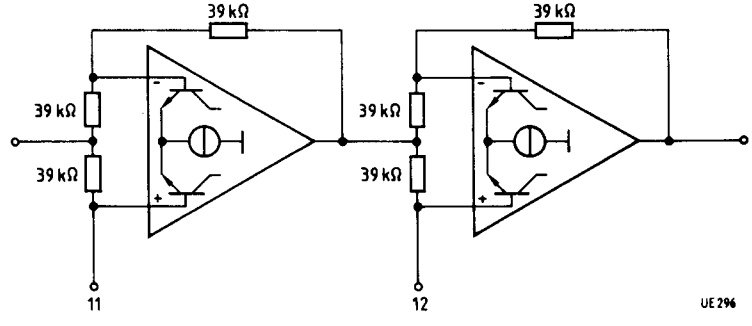
Cutoff Frequency Treble (Pin 17/18)



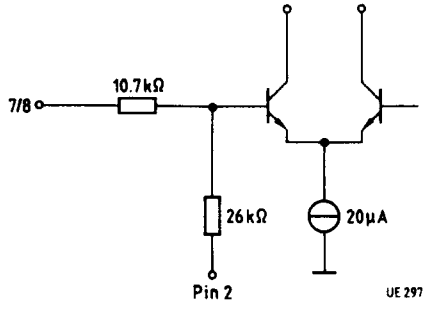
Cutoff Frequency Bass (Pin 13/14)



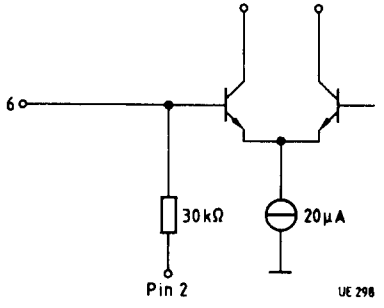
Phase Advancer Quasi Stereo (Pin 11/12)



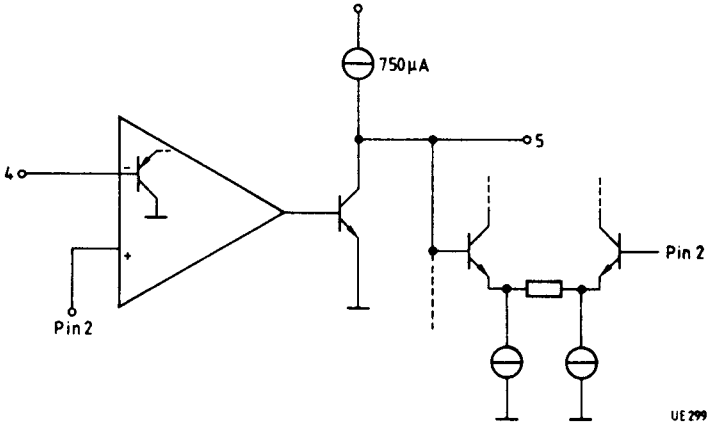
AF Inputs SCART (Pin 7/8)



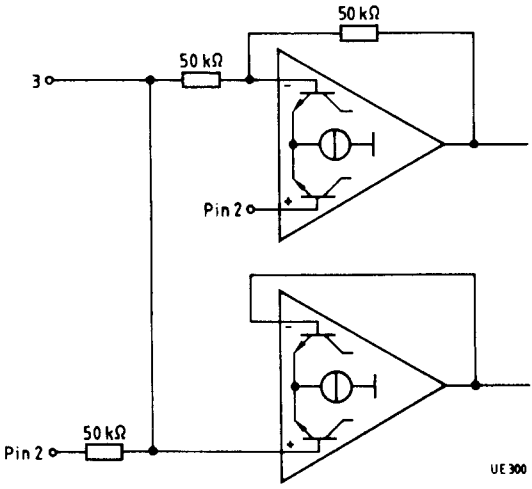
AF Input AM (Pin 6)



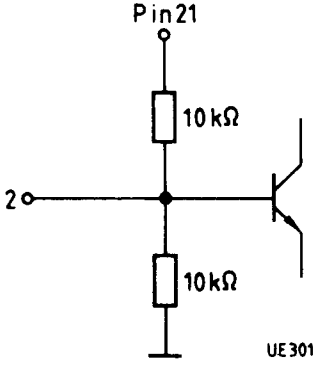
54 – kHz Filter (Pin 4/5)



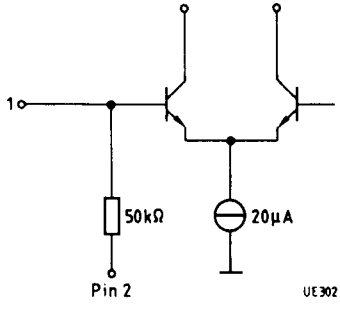
AF Input (Pin 3)



Input for AF Unit Bias Blocking Capacitor (Pin 2)



AF Input (Pin 1)



Absolute Maximum Ratings

T_A = 25 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_{21}	0	14	V
Max. DC voltage	V_1	0	V_{21}	V
Max. DC voltage	V_2	0	V_{21}	V
Max. DC voltage	V_3	0	V_{21}	V
Max. DC voltage	V_4	0	V_{21}	V
Max. DC voltage	V_6	0	V_{21}	V
Max. DC voltage	V_7	0	V_{21}	V
Max. DC voltage	V_8	0	V_{21}	V
Max. DC voltage	V_{11}	0	V_{21}	V
Max. DC voltage	V_{12}	0	V_{21}	V
Max. DC voltage	V_{12}	0	V_{21}	V
Max. DC voltage	V_{14}	0	V_{21}	V
Max. DC voltage	V_{17}	0	V_{21}	V
Max. DC voltage	V_{18}	0	V_{21}	V
Max. DC voltage	V_{22}	0	V_{21}	V
Max. DC voltage	V_{23}	0	V_{21}	V
Max. DC voltage	V_{24}	0	V_{21}	V
Max. DC voltage	V_{25}	0	V_{21}	V
Max. DC voltage	V_{26}	0	V_{21}	V
Max. DC current	I_5	0	2	mA
Max. DC current	I_9	0	2	mA
Max. DC current	I_{10}	0	2	mA
Max. DC current	I_{15}	0	2	mA
Max. DC current	I_{16}	0	2	mA
Max. DC current	I_{19}	0	2	mA
Max. DC current	I_{20}	0	2	mA
Max. DC current	I_{27}	0	1	mA
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	– 40	125	°C
Thermal resistance (system-ambient)	$T_{th\ SA}$		53	K/W

Operating Range

Supply voltage	V_6	10	13.2	V
Ambient temperature	T_A	0	70	°C
Input frequency range	f	0.01	20	kHz

Characteristics
V_S = 12 V; T_A = 25 °C, in accordance with test circuit 1

I²C bus present: start-84-01,3F-0 2,3F-0 3,1F-0 5,88-0 6,10-07,C8-00,01-stop
Chip address - Vol_{LSI}63-Vol_{LSr}63.-.Vol_{HP}31 - tone lin - adj 0dB - MUTE I,MUTE II, mono-bypass
The basic setting for each point in the specification is always preset; only settings which deviate from this are given in the test conditions. Details in *italics* only provide explanation of the hexadecimal code and with switch bits on the set bits and features are stated.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current consumption	I_{21}		50		mA	
Signal Section						
Max. gain	$V_{16\text{-}1}$	– 2	0	2	dB	
Max. gain	$V_{15\text{-}3}$	– 2	0	2	dB	
Max. gain	$V_{20\text{-}1}$	– 2	0	2	dB	
Max. gain	$V_{19\text{-}3}$	– 2	0	2	dB	
Max. gain	$V_{16\text{-}3}$	– 2	0	2	dB	00,02; V_1 = 01 Matrix: stereo
Max. gain	$V_{15\text{-}3}$	– 2	0	2	dB	00,02; V_1 = 01 Matrix: stereo
Max. gain	$V_{20\text{-}3}$	– 2	0	2	dB	00,02; V_1 = 0 Matrix: stereo
Max. gain	$V_{19\text{-}3}$	– 2	0	2	dB	00,02; V_1 = 0 Matrix: stereo
Max. gain	$V_{16\text{-}1}$	4	6	8	dB	00,02; V_3 = 0 Matrix: stereo
Max. gain	$V_{20\text{-}1}$	4	6	8	dB	00,02; V_3 = 0 Matrix: stereo
Max. gain	$V_{16\text{-}7}$	– 5	– 3	– 1	dB	07,CC, SCART
Max. gain	$V_{15\text{-}8}$	– 5	– 3	– 1	dB	07,CC, SCART
Max. gain	$V_{20\text{-}7}$	– 5	– 3	– 1	dB	07,CC, SCART
Max. gain	$V_{19\text{-}8}$	– 5	– 3	– 1	dB	07,CC, SCART
Max. gain	$V_{16\text{-}6}$	– 2	0	2	dB	07,C9, AM
Max. gain	$V_{15\text{-}6}$	– 2	0	2	dB	07,C9, AM
Max. gain	$V_{20\text{-}6}$	– 2	0	2	dB	07,C9, AM
Max. gain	$V_{19\text{-}6}$	– 2	0	2	dB	07,C9, AM
Gain	$V_{9\text{-}1}$	– 2	0	2	dB	
Gain	$V_{10\text{-}3}$	– 2	0	2	dB	
Gain	$V_{9\text{-}3}$	– 2	0	2	dB	00,02; V_1 = 0 Matrix: stereo
Gain	$V_{10\text{-}3}$	– 2	0	2	dB	00,02; V_1 = 0 Matrix:stereo
Gain	$V_{9\text{-}1}$	4	6	8	dB	00,02; V_3 = 0 Matrix: stereo

Characteristics (cont'd)
V_S = 12 V; T_A = 25 °C, in accordance with test circuit 1

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Gain	$V_{10\text{-}6}$	– 2	0	2	dB	07,C9, *AM*
Gain	$V_{9\text{-}6}$	– 2	0	2	dB	07,C9, *AM*
Min. gain	$V_{16\text{-}1}$		– 70		dB	01,08-02,08 VolLSI8-VolLSr8
Min. gain	$V_{15\text{-}3}$		– 70		dB	01,08-02,08 VolLSI8-VolLSr8 01,08-02,08
Min. gain	$V_{20\text{-}1}$		– 62		dB	03,01 Vol HP1
Min. gain	$V_{19\text{-}3}$		– 62		dB	03,01 Vol HP1
Min. gain	$V_{16\text{-}7}$		– 73		dB	07,CC-01,08-02,08 SCART-VolLSI8-VolLSr8
Min. gain	$V_{15\text{-}8}$		– 73		dB	07,CC-01,08-02,08 SCART-VolLSI8-VolLSr8
Min. gain	$V_{20\text{-}7}$		– 65		dB	07,CC-03,01 SCART-VolKH1
Min. gain	$V_{19\text{-}8}$		– 65		dB	07,CC-03,01 SCART-VolKH1
Min. gain	$V_{16\text{-}6}$		– 70		dB	07,C9-01,08-02,08 AM-VolLSI8-VolLSr8
Min. gain	$V_{15\text{-}6}$		– 70		dB	07,C9-01,08-02,08 AM-VolLSI8-VolLSr8
Min. gain	$V_{20\text{-}6}$		– 62		dB	07,C9-03,01 SCART-VolKH1
Min. gain	$V_{19\text{-}6}$		– 62		dB	07,C9-03,01 SCART-VolKH1
Flutter and wow	$\Delta V_{15\text{-}16}$			± 2	dB	01,3F to 01,24 02,3F to 02,24 *Vol* LSI63-36-*Vol* LSr63-36
Flutter and wow	$\Delta V_{19\text{-}20}$			± 2	dB	03,1F to 03,13 *Vol* KH31-19
Step width Vol 15	ΔV_{15}	0	1.25	2.5	dB	01,X-01,(X±1) *Vol* LSIX-*Vol* LSI(X±1)
Step width Vol 16	ΔV_{16}	0	1.25	2.5	dB	02,X-02,(X±1) *Vol* LSrX-*Vol* LSr(X±1)
Step width Vol 19	ΔV_{19}	0	2	4	dB	03,X-03,(X±1) *Vol* KHX-*Vol* KH(X±1)
Step width Vol 20	ΔV_{20}	0	2	4	dB	03,X-03,(X±1) *Vol* KHX-*Vol* KH(X±1)

Characteristics (cont'd)
V_S = 12 V; T_A = 25 °C, in accordance with test circuit 1

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Matrix adjustment	$V_{16\text{-}1}$	2.5	3	3.5	dB	06, 1F, *Adjust. max*
Matrix adjustment	$V_{20\text{-}1}$	2.5	3	3.5	dB	06, 1F, *Adjust. max*
Matrix adjustment	$V_{9\text{-}1}$	2.5	3	3.5	dB	06, 1F, *Adjust. max*
Matrix adjustment	$V_{16\text{-}1}$	– 3.5	– 3	– 2.5	dB	06, 01, *Adjust. min*
Matrix adjustment	$V_{20\text{-}1}$	– 3.5	– 3	– 2.5	dB	06, 01, *Adjust. min*
Matrix adjustment	$V_{9\text{-}1}$	– 3.5	– 3	– 2.5	dB	06, 01, *Adjust. min*
Adjust. step wide	ΔV_{16}	0.1	0.2	0.3	dB	06, X- 06(X ± 1) *Adjust.X -Adjust.*(X ±1)
Adjust. step wide	ΔV_{20}	0.1	0.2	0.3	dB	06, X- 06(X ± 1) *Adjust.X-Adjust.*(X ± 1)
Adjust. step wide	ΔV_9	0.1	0.2	0.3	dB	06, X- 06(X ± 1) *Adjust.X-Adjust.*(X ± 1)
Bass boost	$V_{16\text{-}1}$	13	15		dB	05,8F; f_i = 40 Hz *Bass max, treble lin.*
Bass boost	$V_{15\text{-}3}$	13	15		dB	05,8F; f_i = 40 Hz *Bass max, treble lin.*
Bass boost	$V_{16\text{-}1}$		– 12		dB	05,8 0; f_i = 40 Hz *Bass min, treble lin.*
Bass boost	$V_{15\text{-}3}$		– 12		dB	05,8 0; f_i = 40 Hz *Bass min, treble lin.*
Step wide bass	ΔV_{15}	1	3	5	dB	05,8X- 05,8(X ± 1) *Bass X-bass*(X ± 1)
Step wide bass	ΔV_{16}	1	3	5	dB	05,8X- 05,8(X ± 1) *Bass X-bass*(X ± 1)
High-frequency emphasis	$V_{16\text{-}1}$	10	12		dB	05,F8 f_i = 15kHz *Treble max, bass lin.*
High-frequency emphasis	$V_{15\text{-}3}$	10	12		dB	05,F8 f_i = 15kHz *Treble max, bass lin.*
High-frequency emphasis	$V_{16\text{-}1}$		– 12		dB	05, 08 f_i = 15kHz *Treble min, bass lin.*
High-frequency emphasis	$V_{15\text{-}3}$		– 12		dB	05, 08 f_i = 15kHz *Treble min, bass lin.*
Step wide treble	ΔV_{15}	1	3	5	dB	05,X8- 05,(X ± 1)8 *Treble X-treble*(X ± 1)
Step wide treble	ΔV_{16}	1	3	5	dB	05,X8- 05,(X ± 1)8 *Treble X-treble*(X ± 1)
Linearity sound	ΔV_{15}			± 2	dB	05,88; fi = 40 Hz -15 kHz *Treble, bass lin.*
Linearity sound	ΔV_{16}			± 2	dB	05,88; f_i = 40 Hz -15 kHz *Treble, bass lin.*

Characteristics (cont'd)
V_S = 12 V; T_A = 25 °C, in accordance with test circuit 1

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Channel separation	$\Delta V_{15\text{-}16}$	50			dB	V_3 or V_1 = 600 mV rms
Channel separation	$\Delta V_{19\text{-}20}$	50			dB	V_3 or V_1 = 600 mV rms
Channel separation	$\Delta V_{9\text{-}10}$	50			dB	V_3 or V_1 = 600 mV rms
Cross talk attenuation switch	a Input interf/ Output rms					V Irms = 0 $V_{I\,Int1,3,6}$ = 600 mV rms
		60			dB	$V_{I\,Int\,7,8}$ = 2 V rms
Attenuation MUTE	$a_{1\text{-}16}$	80			dB	01, 0 0- 02, 0 0 *Vol* $_{LSI}$*0-Vol* $_{LSr}$*0* V_1 = 600 mV rms
Attenuation MUTE	$a_{1\text{-}16}$	80			dB	07,48; V_1 = 600 mV rms *MUTE I:0*
Attenuation MUTE	$a_{1\text{-}16}$	80			dB	07,88; V_1 = 600 mV rms *MUTE II:0*
Attenuation MUTE	$a_{3\text{-}15}$	80			dB	01, 0 0- 02, 0 0 $Vol_{LSI}0$-$Vol_{LSr}0$ V_3 = 600 mV rms
Attenuation MUTE	$a_{3\text{-}15}$	80			dB	07,48; V_3 = 600 mV rms *MUTE I:0*
Attenuation MUTE	$a_{3\text{-}15}$	80			dB	07,88; V_3 = 600 mV rms *MUTE II:0*
Attenuation MUTE	$a_{1\text{-}20}$	80			dB	03, 0 0; V_1 = 600 mV rms $Vol_{KH}0$
Attenuation MUTE	$a_{1\text{-}20}$	80			dB	07,48; V_1 = 600 mV rms *MUTE I:0*
Attenuation MUTE	$a_{3\text{-}19}$	80			dB	03, 0 0; V_3 = 600 mV rms $Vol_{KH}0$
Attenuation MUTE	$a_{3\text{-}19}$	80			dB	07,48; V_3 = 600 mV rms *MUTE I:0*
Analogous values are valid for feed-in at the pin 6, 7, 8; $V_{7,8}$ = 2 V rms; V_6 = 600 mV rms						
Attenuation MUTE	$a_{3\text{-}10}$	80			dB	07,48; V_3 = 600 mV rms *MUTE I:0*
Attenuation MUTE	$a_{1\text{-}9}$	80			dB	07,48; V_1 = 600 mV rms *MUTE I:0*
Attenuation MUTE	$a_{6\text{-}10}$	80			dB	07,49; V_6 = 600 mV rms *MUTE I:0, AM*
Attenuation MUTE	$a_{6\text{-}9}$	80			dB	07,49; V_6 = 600 mV rms *MUTE I:0, AM*

Characteristics (cont'd)
V_S = 12 V; T_A = 25 °C, in accordance with test circuit 1

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Max.input voltage	V_6	600			mV_{rms}	$THD_{15,16}$ = 1 %
Max.input voltage	V_3	600			mV_{rms}	THD_{15} = 1 %
Max.input voltage	V_1	600			mV_{rms}	THD_{16} = 1 %
Max.input voltage	V_1	300			mV_{rms}	THD_{16} = 1 %; 00,02 *Matrix: Stereo*
Max.input voltage	V_7	2			V_{rms} V_{rms}	THD_{16} = 3 %; 07, CC, *SCART*
Max.input voltage	V_8	2			%	THD_{15} = 3 %; 07, CC, *SCART*
Distorsion	THD_{19}	0	0.01	0.1	%	V_3 = 250 mV_{rms}
Distorsion	THD_{20}		0.01	0.1	%	V_1 = 250 mV_{rms}
Distorsion	THD_{19}		0.01	0.1	%	V_3 = 250 mV_{rms}; 03,15 *Vol KH21*
Distorsion	THD_{20}		0.01	0.1	%	V_1 = 250 mV_{rms}; 03,15 *Vol KH21*

Analogous values are valid for feed-in at the pin 6, 7, 8 ; $V_{7,8}$ = 400 mV_{rms}; V_6 = 250 mV_{rms}

Distorsion	THD_{16}		0.01	0.1	%	V_1 = 250 mV_{rms}
Distorsion	THD_{15}		0.01	0.1	%	V_3 = 250 mV_{rms}
Distorsion	THD_{16}		0.01	0.2	%	V_1 = 250 mV_{rms}; 01, 2 F-02,2F *Vol LSI47-Vol LSr47*
Distorsion	THD_{15}		0.01	0.2	%	V_3 = 250 mV_{rms}; 01, 2 F-02,2F *Vol LSI47-Vol LSr47*
Distorsion	THD_{16}		0.1	0.4	%	V_1 = 250 mV_{rms}; 05,XX *any sound*
Distorsion	THD_{15}		0.1	0.4	%	V_3 = 250 mV_{rms}; 05,XX *any sound*

Analogous values are valid for feed-in at the pin 6, 7, 8 ; $V_{7,8}$ = 400 mV_{rms}; V_6 = 250 mV_{rms}

Characteristics (cont'd)
V_S = 12 V; T_A = 25 °C, in accordance with test circuit 1

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.0	typ.0	max.0		
Distorsion	THD_{10}		0.01	0.1	%	V_3 = 250 mV rms
Distorsion	THD_9		0.01	0.1	%	V_1 = 250 mV rms
Distorsion	THD_{10}		0.01	0.1	%	V_6 = 250 mV rms, 07,C9,*AM*
Distorsion	THD_9		0.01	0.1	%	V_6 = 250 ,mV rms; 07,C9, *AM*
Antiphase Cross talk atten.	$\Delta V_{16\text{-}15}$					V_3 = 600 mV rms
Base width		0.5	0.55			f_i = 2kHz; 00,11, *Basis width*
Antiphase Cross talk atten.	$\Delta V_{15\text{-}16}$					V_1 = 600 mV rms
Base width		0.5	0.55			f_i = 2 kHz; 0011, *Basis width*
Base width phase	$\Phi_{16\text{-}15}$	150	180	210	deg	V_1 = 600 mV rms; 00,11 *Basis width*, f = 2 kHz
Base width phase	$\Phi_{15\text{-}16}$	150	180	210	deg	V_3 = 600 mV rms; 0011 *Basis width*, f = 2 kHz
Phase rotation quasi-stereo	$\Phi_{16\text{-}15}$	0	10	40	deg	$V_{3,1}$ = 600 mV rms; 00,21 *Quasi-stereo*, f = 40 Hz

Characteristics (cont'd)
V_S = 12 V; T_A = 25 °C, in accordance with test circuit 1

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.0	typ.	max.		
Phase rotation quasi-stereo	$\Phi_{16\text{-}15}$	130	180	230	deg	$V_{3,1}$ = 600 mV rms; 0021 *Quasi-stereo*, f = 1 kHz
Phase rotation quasi-stereo	$\Phi_{16\text{-}15}$	– 30	10	0	deg	$V_{3,1}$ = 600 mV rms; 00,21 *Quasi-stereo*, f = 15 kHz
Unweighted signal-to-noise ratio	$a_{S/N\,16}$	1	90	97	dB	$V_{N\,rms\,20\,Hz\text{-}20\,kHz}$; V_1 = 0,6 V rms
Unweighted signal-to-noise ratio	$a_{S/N\,15}$	1	90	97	dB	$V_{N\,rms\,20\,Hz\text{-}20\,kHz}$; V_3 = 0,6 V rms
Unweighted signal-to-noise ratio	$a_{S/N\,16}$	70	80		dB	$V_{N\,rms\,20\,Hz\text{-}20\,kHz}$; V_1 = 0,6 V rms 01,27-02,27 *Vol* $_{LSl}$*39*-*Vol* $_{LSr}$*39*
Unweighted signal-to-noise ratio	$a_{S/N\,15}$	70	80		dB	$V_{N\,rms\,20\,hz\text{-}20\,kHz}$; V_3 = 0,6 V rms 01,27-02,27 *Vol* $_{LSl}$*39*-*Vol* $_{LSr}$*39*
External voltage	V_{N15}		2	10	µV rms	$V_{N\,rms\,20\,Hz\text{-}20\,kHz}$ 01,00-02,00 *Vol* $_{LSl}$*0*-*Vol* $_{LSr}$*0*
External voltage	V_{N16}		2	10	µV rms	$V_{N\,rms\,20\ Hz\text{-}20\,kHz}$ 01,00-02,00 *Vol* $_{LSl}$*0*-*Vol* $_{LSr}$*0*
Unweighted signal-to-noise ratio	$a_{S/N\,20}$	90	97		dB	$V_{N\,rms\,20\,Hz\text{-}20\,kHz}$; V_1 = 0,6 V rms
Unweighted signal-to-noise ratio	$a_{S/N\,19}$	1	90	97	dB	$V_{N\,rms\,20\,Hz\text{-}20\,kHz}$; V_3 = 0,6 V rms
Unweighted signal-to-noise ratio	$a_{S/N\,20}$	70	80		dB	$V_{N\,rms\,20\,Hz\text{-}20\,kHz}$; V_1 = 0,6 V rms 03, 10, Vol $_{KH}$16
Unweighted signal-to-noise ratio	$a_{S/N\,19}$	70	80		dB	$V_{N\,rms\,20\,Hz\text{-}20\,kHz}$; V_3 = 0,6 V rms 03, 10, Vol $_{KH}$16
External voltage	V_{N20}		2	10	µV rms	$V_{N\,rms\,20\,Hz\text{-}20\,kHz}$; 03,00 *Vol* $_{KH}$*0*
External voltage	V_{N19}		2	10	µV rms	$V_{N\,rms\,20\,Hz\text{-}20\,kHz}$; 03,00 *Vol* $_{KH}$*0*
Unweighted signal-to-noise ratio	$a_{S/N\,9}$	1	90	97	dB	$V_{N\,rms\,20\,Hz\text{-}20\,kHz}$; V_1 = 0,6 V rms
Unweighted signal-to-noise ratio	$a_{S/N\,10}$	1	90	97	dB	$V_{N\,rms\,20\,Hz\text{-}20\,kHz}$; V_3 = 0,6 V rms

Characteristics (cont'd)
V_S = 12 V; T_A = 25 °C, in accordance with test circuit 1

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Change of DC-switch Δ1 Bit	ΔV_{16}			± 10	mV	01,X-01,X ± 1 *Vol_{LSl}X-Vol_{LSl}(X ± 1)*
Change of DC-switch Δ1 Bit	ΔV_{15}			± 10	mV	02,X-02,X±1 *Vol_{LSr}X-Vol_{LSr}* (X ± 1)
Change of DC-switch Δ1 Bit	ΔV_{16}			± 10	mV	05,X-05,X 1 *Sound X-Sound (X ± 1)*
Change of DC-switch Δ1 Bit	ΔV_{15}			± 10	mV	0,X-05,X ± 1 *Sound X-Sound (X ± 1)*
Change of DC-switch Δ1 Bit	ΔV_{19}			± 10	mV	03,X-03,X ± 1 *Vol_{KH}X-Vol_{KH} (X ± 1)*
Change of DC-switch Δ1 Bit	ΔV_{20}			± 10	mV	03,X-03,X ± 1 *Vol_{KH}X-Vol_{KH} (X ± 1)*
Design-Related Data						
Input resistance	R_7	35			kΩ	
Input resistance	R_8	35			kΩ	
Input resistance	R_6	20			kΩ	
Input resistance	R_3	20			kΩ	
Input resistance	R_1	20			kΩ	
Output resistance	R_{19}			200	Ω	
Output resistance	R_{20}			200	Ω	
Output resistance	R_{15}			200	Ω	
Output resistance	R_{16}			200	Ω	
Output resistance	R_9			200	Ω	
Output resistance	R_{10}			200	Ω	

Characteristics (cont'd)
V_S = 12 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
ID Signal Decoder							
Gain Filter OP-amp	V_5	13	14	15	dB	V_{IF} = 80 mV$_{pp}$	1
Max. input voltage	V_5	600			mV$_{pp}$	Function	2
VCO voltage PLL	V_{27}	tbf			V	f_{24} = 14.6 kHz; V_{24} = 2.5 V$_{os}$	2
VCO voltage PLL	V_{27}	tbf	3	tbf	V	f_{24} = 15.625 kHz; V_{24} = 2.5 V$_{os}$	2
VCO voltage PLL	V_{27}			tbf	V	f_{24} = 16.6 kHz; V_{24} = 2.5 V$_{os}$	2
VCO voltage PLL	V_{27}					f_{24} = 58.4 kHz; V_{24} = 2.5 V$_{os}$	
		tbf			V	00,09, H-Imp	2
VCO voltage PLL	V_{27}					f_{24} = 66.4 kHz; V_{24} = 2.5 V$_{os}$	
				tbf	V	00,09, H-Imp	2

$$V_{KT\ Filter} = \frac{\sqrt{(V_{25} - V_{25}^*)^2 + (V_{26} - V_{26}^*)^2}}{V_5}$$

V_{25} or V_{26} when V_5 = 0
V_{25}^* or V_{26}^* when V_5 = 400 mV$_{pp}$

ID filter gain		tbf		tbf		$V_{KT\ Filter}$ f_5 = 54.962 kHz I²C talk: Dual	2
ID filter gain		tbf		tbf		$V_{KT\ Filter}$ f_5 = 54.805 kHz I²C talk: Stereo	2

$V_{25\ test} = V_{25\,(V_{5\,=\,0})} \pm \Delta V_{25}$; $V_{26\ test} = V_{26\,(V_{5\,=\,0})} \pm \Delta V_{26}$

Characteristics (cont'd)
V_S = 12 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Detection threshold	ΔV_{25}	tbf			mV	I²C talk: Stereo o. Dual	3
Detection threshold	$-\Delta V_{25}$	tbf			mV	I²C talk: Stereo o. Dual	3
Detection threshold	ΔV_{26}	tbf			mV	I²C talk: Stereo o. Dual	3
Detection threshold	$-\Delta V_{26}$	tbf			mV	I²C talk: Stereo o. Dual	3
Mono threshold	ΔV_{25}	0		tbf	mV	I²C talk: Mono	3
Mono threshold	$-\Delta V_{25}$	0		tbf	mV	I²C talk: Mono	3
Mono threshold	ΔV_{26}	0		tbf	mV	I²C talk: Mono	3
Mono threshold	$-\Delta V_{26}$	0		tbf	mV	I²C talk: Mono	3
Response of detection	t_{det}	1/4		1/2	t_{MPX}	I²C talk: Stereo o Dual $\pm \Delta V_{25}$ = 1V	3
Response of detection	t_{det}	1/4		1/2	t_{MPX}	I²C talk: Stereo o Dual $\pm \Delta V_{26}$ = 1V	3
Switching threshold f_{REF}-input	V_{24L}	0		1.5	V		2
Switching threshold f_{REF}-input	V_{24H}	3.5		V_{21}	V		2
Multiplexer takt	t_{MPX}		1.08		s	00,C0, MPX = 1 s	
Multiplexer takt	t_{MPX}		2.17		s	00,00, MPX = 2 s	
Multiplexer takt	t_{MPX}		4.34		s	00,40, MPX = 4 s	
Multiplexer takt	t_{MPX}		8.68		s	00,80, MPX = 8 s	

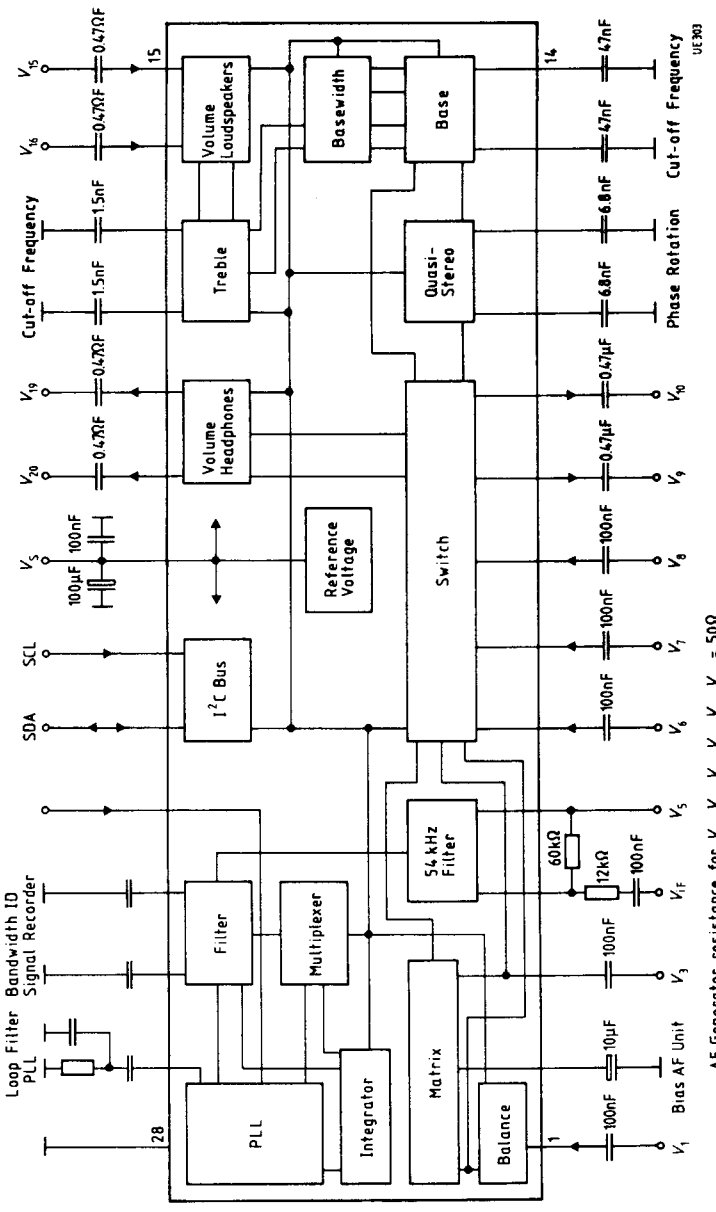
Design-Related Data

Filter output resistance	$R_{25,26}$	110			kΩ		
f_{REF} input resistance	R_{24}	7			kΩ		

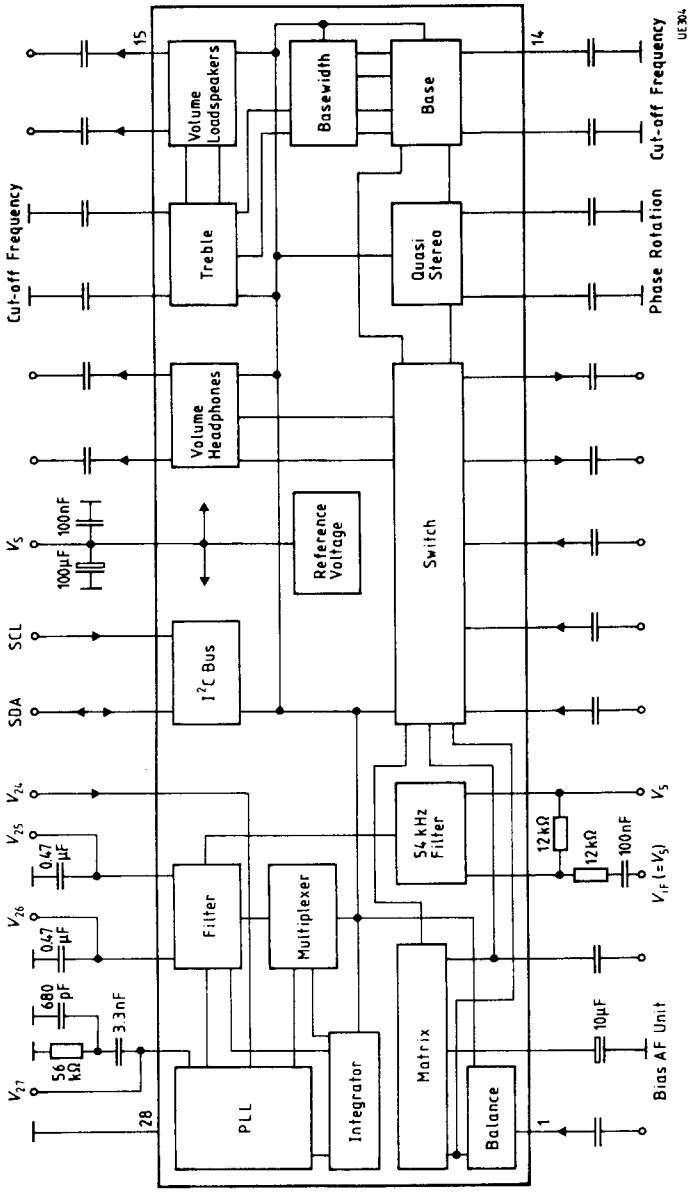
Characteristics (cont'd)
V_S = 12 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
I²C-B Bus (SCL, SDA)					
SCL, SDA edges Rise time Fall time	 t_R t_F			 1 300	 µs ns
Shift register clock pulse SCL Frequency H-pulse width L-pulse width	 f_{SCL} t_{HIGH} t_{LOW}	 0 4 4		 100	 kHz µs µs
Start Set-up time Hold time	 t_{SUSTA} t_{HDSTA}	 4 4			 µs µs
Stop Set-up time Bus free time	 t_{SUSTO} t_{BUF}	 4 4			 µs µs
Data transfer Set-up time Hold time	 t_{SUDAT} t_{HDDAT}	 1 1			 µs µs
Input SCL, SDA Input voltage Input current	 V_{QH} V_{QL} I_{QH} I_{QL}	 2.4		 5.5 1 50 100	 V V µA µA
Output SDA (open collector) Output voltage R_L = 2.5 kΩ I_{QL} = 3 mA	 V_{QH} V_{QL}	 5.4		 0.4	 V V

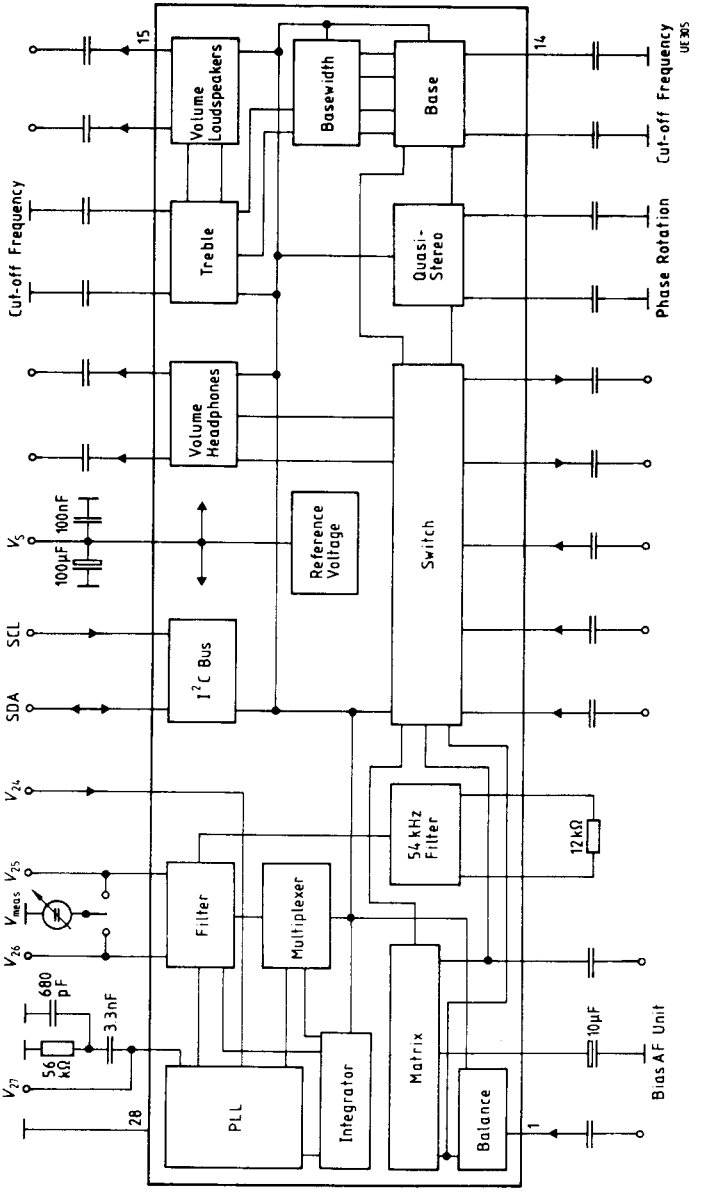
Test Circuit 1



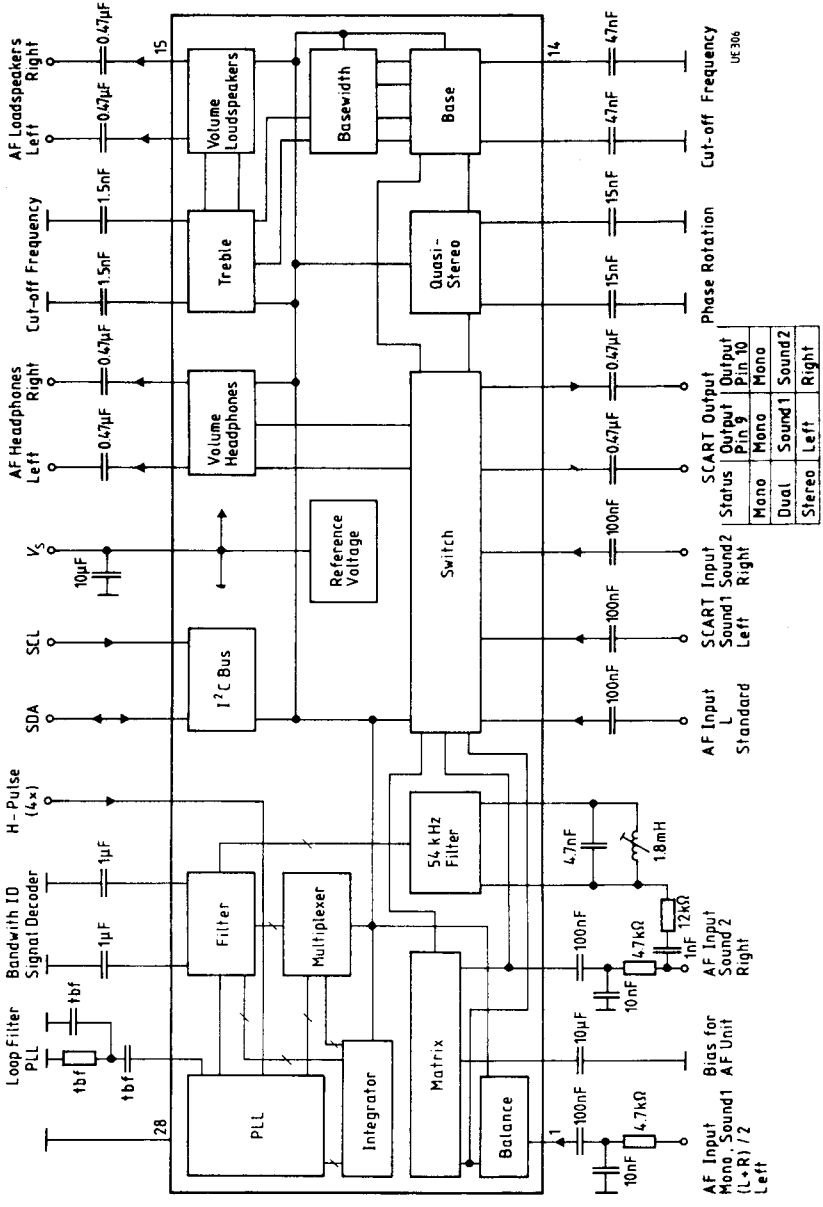
Test Circuit 2



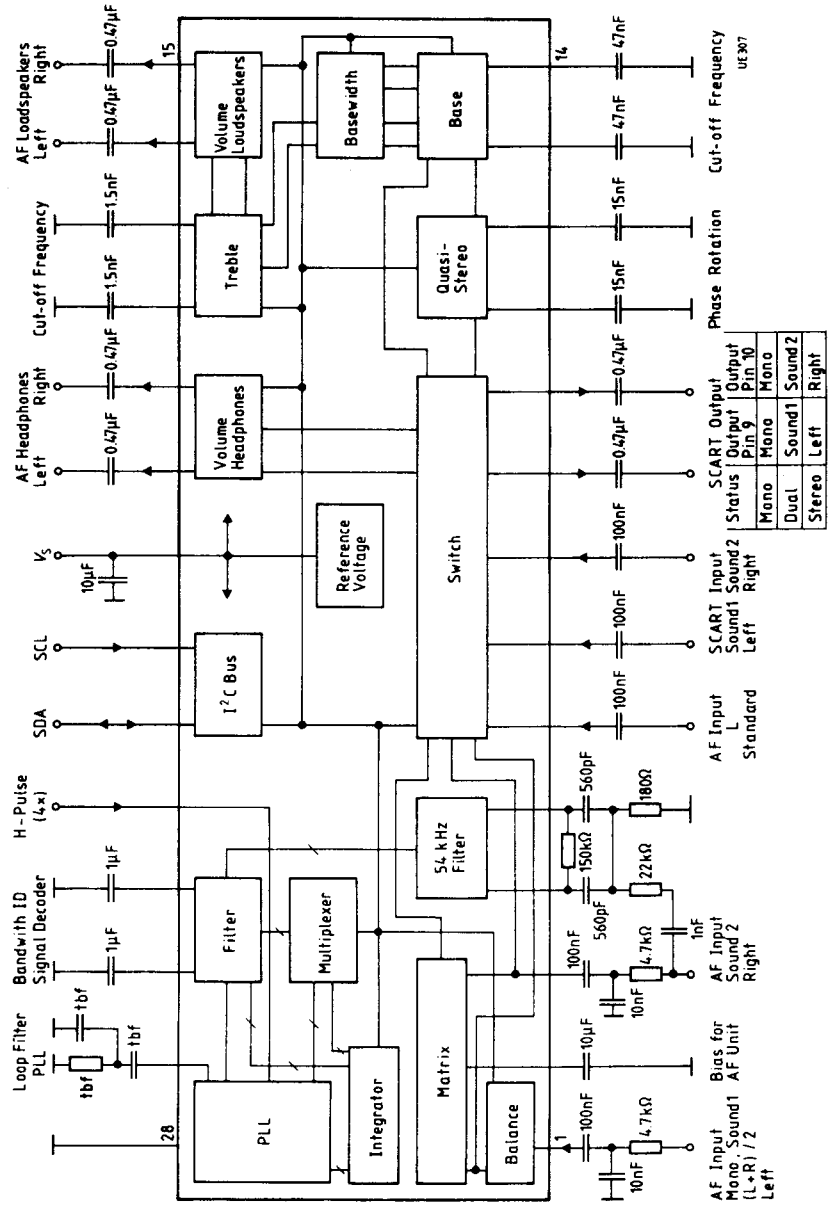
Test Circuit 3



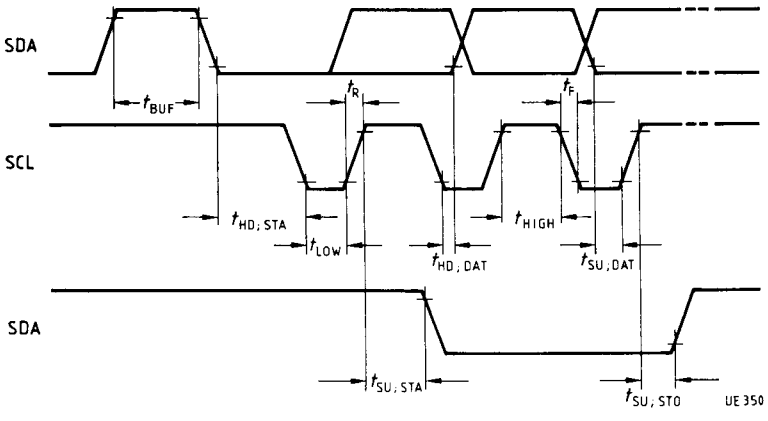
Application Circuit 1



Application Circuit 2



I²C Bus Timing Diagram



t_{SUSTA}	Set-up time (start)
t_{HDSTA}	Hold time (start)
t_{HIGH}	HIGH pulse width (clock)
t_{LOW}	LOW pulse width (clock)
t_{SUDAT}	Set-up time (data transfer)
t_{HDDAT}	Hold time (data transfer)
t_{SUSTO}	Set-up time (stop)
t_{BUF}	Bus free time
t_F	Fall time
t_R	Rise time

All times are referenced to the V_{IH} and V_{IL} values