06/26/01

Errata: CS4220/21/23/24 Data Sheet

Reference CS4220/21 Data Sheet revision DS284PP3 dated APR '00 and CS4223/24 Data Sheet revision DS290PP3 dated APR '00

The CS4220/21/23/24 exhibits a one-sample delay between the left and right channels. The phase difference introduced by the DAC is complementary to that introduced by the ADC so that stereo signals which pass through both converters in a loopback configuration are reconstructed with no phase error between the channels. The group delays are listed below.

ADC Decimation Filter Characteristics

Group Delay, left channel	t_{gd}	18 / Fs	s
Group Delay, right channel	t_{gd}	17 / Fs	s

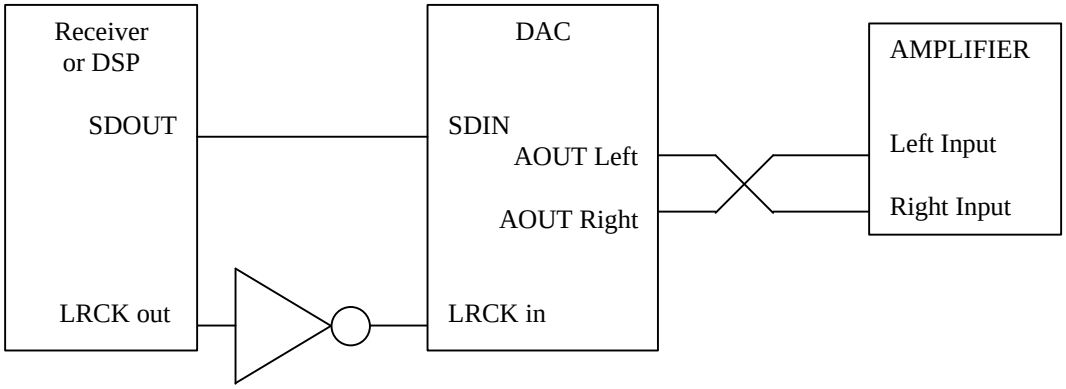
DAC Combined Digital and Analog Filter Characteristics

Group Delay, left channel	t_{gd}	26 / Fs	s
Group Delay, right channel	t_{gd}	27 / Fs	s

Workarounds:

Workaround #1: In situations where software can be used to manipulate the audio content, it may be feasible to introduce a one-sample delay in one channel of the ADC output and to introduce a complementary delay in the DAC input. The input to the DSP and the output of the DAC would then both be free of errors.

Workaround # 2: In situations where a normal signal must be fed to the DAC and the DAC is operating in slave mode, it is possible to eliminate the phase shift by inverting the LRCK signal and swapping the left and right DAC analog outputs. See Figure 1. We do not have a comparable hardware workaround for the ADC.



Figue 1. Typical application of workaround #2.

Contacting Cirrus Logic Support

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