PRELIMINARY

ISD5100 – SERIES

SINGLE-CHIP VOICE RECORD/PLAYBACK DEVICES WITH DIGITAL STORAGE CAPABILITY

1. GENERAL DESCRIPTION

The ISD5100-Series ChipCorder® products provide high quality, fully integrated, single-chip Record/Playback solutions for 2- to 16-minute messaging applications that are ideal for use in cellular phones, automotive communications, GPS/navigation systems and other portable products. The ISD5100-Series products are an enhancement of the ISD5000 architecture, providing: 1) the I^2C serial port - address, control and duration selection are accomplished through an I^2C interface to minimize pin count (ONLY two control lines required); 2) the capability of storing digital data, in addition to analog, information. These features allow customers to store phone book numbers, system configuration parameters and message address pointers for message management capability.

The ISD5100-Series includes:

- ISD5116 from 8 to 16 minutes
- ISD5108 from 4 to 8 minutes
- ISD5104 from 2 to 4 minutes

Analog functions and audio gating have also been integrated into the ISD5100-Series products to allow easy interface with integrated digital cellular chip sets on the market. Audio paths have been designed to enable full duplex conversation record, voice memo, answering machine (including outgoing message playback) and call screening features. This product enables playback of messages while the phone is in standby, AND both simplex and duplex playback of messages while on a phone call.

Additional voice storage features for digital cellular phones include: 1) a personalized outgoing message can be sent to the person by getting caller-ID information from the host chipset 2) a private call announce while on call can be heard from the host by giving caller-ID on call waiting information from the host chipset.

Logic Interface Options of 2.0V and 3.0V are supported by the ISD5100-Series to accommodate portable communication products customers (2.0- and 3.0-volt required).

Like other ChipCorder® products, the ISD5100-Series integrate the sampling clock, anti-aliasing and smoothing filters, and the multi-level storage array on a single-chip. For enhanced voice features, the ISD5100-Series eliminate external circuitry by integrating automatic gain control (AGC), a power amplifier/speaker driver, volume control, summing amplifiers, analog switches, and a car kit interface. Input level adjustable amplifiers are also included, providing a flexible interface for multiple applications.

Recordings are stored into on-chip nonvolatile memory cells, providing zero-power message storage. This unique, single-chip solution is made possible through Winbond's patented multilevel storage technology. Voice and audio signals are stored directly into solid-state memory in their natural, uncompressed form, providing superior quality voice and music reproduction.

2. FEATURES

Fully-Integrated Solution

- Single-chip voice record/playback solution
- Dual storage of digital and analog information
- Durations
  - 8 to 16-minute duration (ISD5116)
  - 4 to 8-minute duration (ISD5108)
  - 2 to 4-minute duration (ISD5104)

Low Power Consumption

- +2.7 to +3.3V (V_{CC}) Supply Voltage
- Supports 2.0V and 3.0V interface logic
- Operating Current:
  - $I_{CC\ Play}$ = 15 mA (typical)
  - $I_{CC\ Rec}$ = 30 mA (typical)
  - $I_{CC\ Feedthrough}$ = 12 mA (typical)
- Standby Current:
  - I_{SB} = 1μA (typical)
- Most stages can be individually powered down to minimize power consumption

Enhanced Voice Features

- One or two-way conversation record
- One or two-way message playback
- Voice memo record and playback
- Private call screening
- In-terminal answering machine
- Personalized outgoing message
- Private call announce while on call

Digital Memory Features

- Up to 4 Mb available (ISD5116)
- Up to 2 Mb available (ISD5108)
- Up to 1 Mb available (ISD5104)
- Storage of phone numbers, system configuration parameters and message address table in cellular application

Easy-to-use and Control

- No compression algorithm development required
- User-controllable sampling rates
- Programmable analog interface
- Standard & Fast mode I^2C serial interface (100kHz – 400 kHz)
- Fully addressable to handle multiple messages

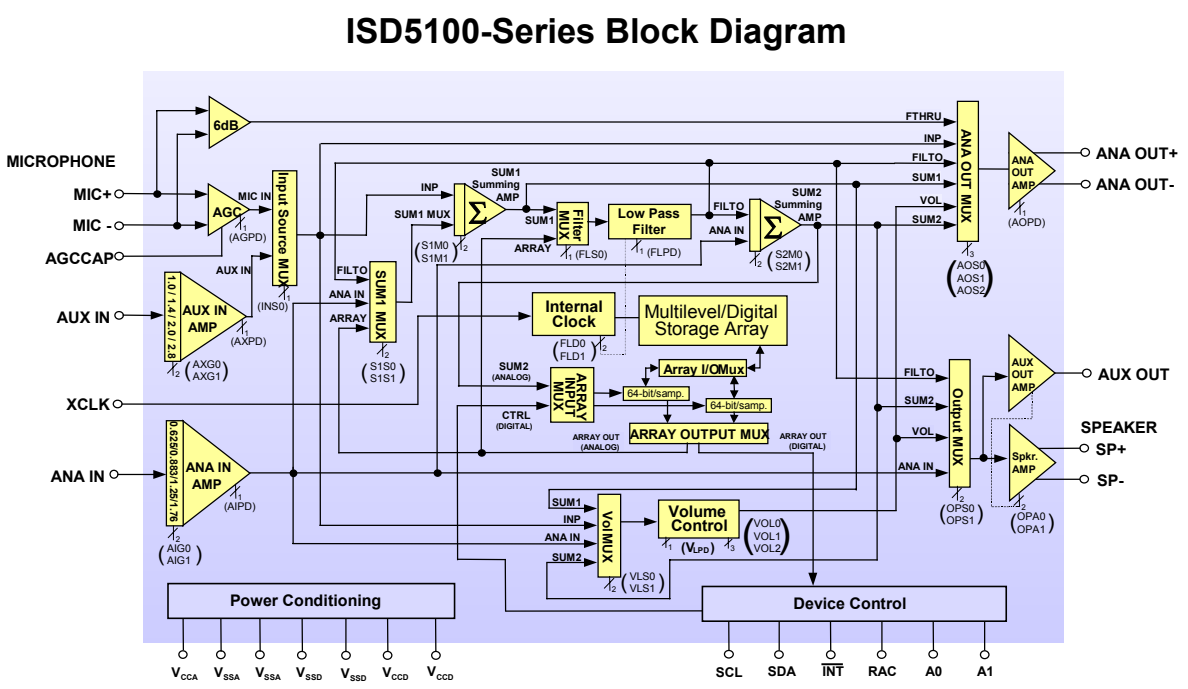
High Quality Solution

- High quality voice and music reproduction
- Winbond's standard 100-year message retention (typical)
- 100K record cycles (typical) for analog data
- 10K record cycles (typical) for digital data

Options

- Available in die form,TSOP and SOIC and PDIP (ISD5116 Only)
- Commercial (0 to +70°C) and Industrial (-40 to +85°C) available

3. BLOCK DIAGRAM



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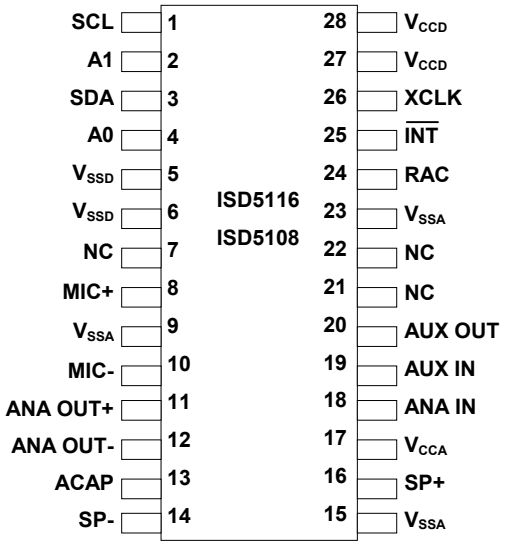
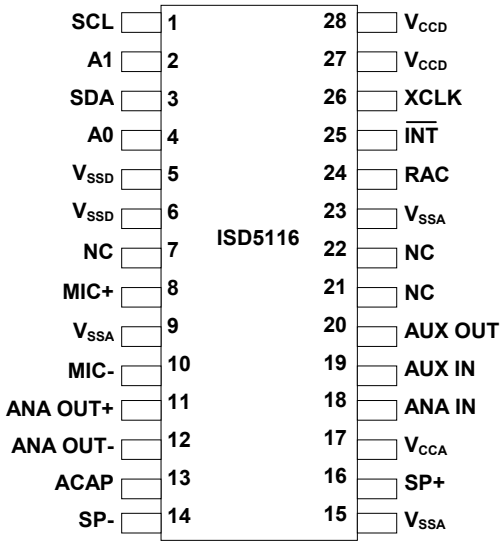
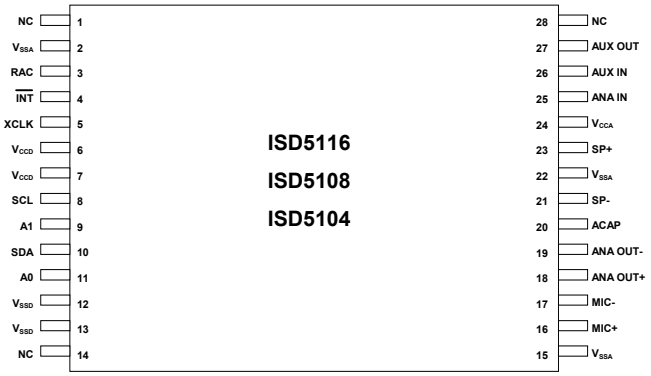
5. PIN CONFIGURATION



SOIC



PDIP



28-PIN TSOP

6. PIN DESCRIPTION

Pin Name	Pin No. 28-pin SOIC/PDIP	Pin No. 28-pin TSOP	Functionality
SCL	1	8	Serial Clock Line is part of the I^2C interface. It is used to clock the data into and out of the I^2C interface.
A1	2	9	Input pin that supplies the LSB +1 bit for the I^2C Slave Address.
SDA	3	10	Serial Data Line is part of the I^2C interface. Data is passed between devices on the bus over this line.
A0	4	11	Input pin that supplies the LSB for the I^2C Slave Address.
V_{SSD}	5,6	12,13	Digital Ground pins.
NC	7,21,22	1,14,28	No Connect.
MIC+	8	16	Differential Positive Input to the microphone amplifier.
V_{SSA}	9,15,23	2,15,22	Analog Ground pins.
MIC-	10	17	Differential Negative Input to the microphone amplifier.
ANA OUT+	11	18	Differential Positive Analog Output for ANA OUT of the device.
ANA OUT-	12	19	Differential Negative Analog Output for ANA OUT of the device.
ACAP	13	20	AGC/AutoMute Capacitor connection. Required for the on-chip AGC amplifier during record and AutoMute function during playback.
SP-	14	21	Differential Negative Speaker Driver Output. When the speaker outputs are in use, the AUX OUT output is disabled.
SP+	16	23	Differential Positive Speaker Driver Output.
V_{CCA}	17	24	Positive Analog Supply pin. This pin supplies the low level audio sections of the device. It should be carefully bypassed to Analog Ground to insure correct device operation.
ANA IN	18	25	Analog Input. This is one of the gain adjustable analog inputs of the device.
AUX IN	19	26	Auxiliary Input. This is one of the gain adjustable analog inputs of the device.
AUX OUT	20	27	Auxiliary Output. This is one the analog outputs of the device. When this output is in use, the SP+ and SP- outputs are disabled.
RAC	24	3	Row Address Clock; an open drain output. The RAC pin goes LOW T_{RACL}[1] before the end of each row of memory and returns HIGH at exactly the end of each row of memory.
$\overline{INT}$	25	4	Interrupt Output; an open drain output that indicates that a set EOM bit has been found during Playback or that the chip is in an Overflow (OVF) condition. This pin remains LOW until a Read Status command is executed.
XCLK	26	5	This pin allows the internal clock of the device to be driven externally for enhanced timing precision. This pin is grounded for most applications.
V_{CCD}	27,28	6,7	Positive Digital Supply pins. These pins carry noise generated by internal clocks in the chip. They must be carefully bypassed to Digital Ground to insure correct device operation.

[1] See the Parameters section of on page 64

7. FUNCTIONAL DESCRIPTION

7.1. OVERVIEW

7.1.1 Speech/Sound Quality

The ISD5100-Series ChipCorder products can be configured via software to operate at 4.0, 5.3, 6.4 or 8.0 kHz sampling frequencies, allowing the user a choice of speech quality. Increasing the duration decreases the sampling frequency and bandwidth, which affects sound quality. The table in the following section compares filter pass band and product durations.

7.1.2. Duration

To meet end-system requirements, the ISD5100-Series devices are single-chip solutions, which provide from 2 to 16 minutes of voice record and playback, depending on base device ad the sample rates defined by customer software.

Input Sample Rate (kHz)	ISD5116 Duration[1]	ISD5108 Duration[1]	ISD5104 Duration[1]	Typical Filter Knee (kHz)
8.0	8 min 44 sec	4 min 22 sec	2 min 11 sec	3.4
6.4	10 min 55 sec	5 min 27 sec	2 min 43 sec	2.7
5.3	13 min 6 sec	6 min 33 sec	3 min 16 sec	2.3
4.0	17 min 28 sec	8 min 44 sec	4 min 22 sec	1.7

[1.] Minus any pages selected for digital storage

7.1.3. Flash Technology

One of the benefits of Winbond's ChipCorder technology is the use of on-chip Flash memory, which provides zero-power message storage. The message is retained for up to 100 years (typically) without power. In addition, the device can be re-recorded over 10,000 times (typically) for the digital data and over 100,000 times (typically) for the analog messages.

A new feature has been added that allows memory space in the ISD5100-Series to be allocated to either digital or analog storage when recorded. The fact that a section has been assigned digital or analog data is stored in the Message Address Table by the system microcontroller when the recording is made.

7.1.4. Microcontroller Interface

The ISD5100-Series are controlled through an I^2C 2-wire interface. This synchronous serial port allows commands, configurations, address data, and digital data to be loaded to the device, while allowing status, digital data and current address information to be read back from the device. In addition to the serial interface, two other pins can be connected to the microcontroller for enhanced interface. These are the $\overline{RAC}$ timing pin and the $\overline{INT}$ pin for interrupts to the controller. Communications with all the internal registers are through the serial bus, as well as digital memory Read and Write operations.

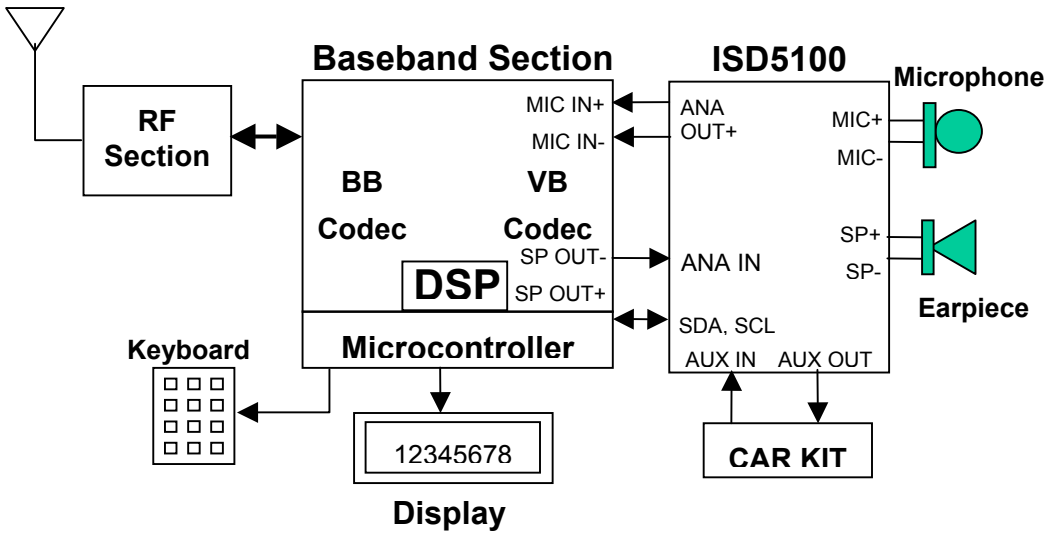
7.1.5. Programming

The ISD5100-Series are also ideal for playback-only applications, where single or multiple messages may be played back when desired. Playback is controlled through the I^2C interface. Once the desired message configuration is created, duplicates can easily be generated via a third-party programmer. For more information on available application tools and programmers, please see the Winbond web site at www.winbond-usa.com

7.2. FUNCTIONAL DETAILS

The ISD5100-Series are single chip solutions for voice and analog storage that also include the capability to store digital data in the memory array. The array may be divided between analog and digital storage, as the user chooses, when configuring the device. The device consists of several sections that will be described in the following paragraphs.

Looking at the block diagram below, one can see that the ISD5100-Series may be very easily designed into a cellular phone. Placing the device between the microphone and the existing voice encoder chip takes care of the transmit path. The ANA IN is connected between one of the speaker leads on the voice decoder chip and the speaker is connected to the SPEAKER pins of the ISD5100-Series. Two pins are needed for the I^2C digital control and digital information for storage.



Starting at the MICROPHONE inputs, the signal from the microphone can be routed directly through the chip to the ANA OUT pins through a 6 dB amplifier stage (Feed Through Mode). Or, the signal can be passed through the AGC amplifier and directed to the ANA OUT pins, directed to the storage array, or mixed with voice from the receive path coming from ANA IN and be directed to the same places.

In addition, if the phone is inserted into a "hands-free" car kit, then the signal from the pickup microphone in the car can be passed through to the same places from the AUX IN pin and the phone's microphone is switched off. Under this situation, the other party's voice from the phone is played into ANA IN and passed through to the AUX OUT pin that drives the car kit's loudspeaker.

Depending upon whether one desires recording one side (simplex) or both sides (duplex) of a conversation, the various paths will also be switched through to the low pass filter (for anti-aliasing) and into the storage array. Later, the cell phone owner can playback the messages from the array. When this happens, the Array Output MUX is connected to the volume control through the Output MUX to the Speaker Amplifier.

For applications other than a cell phone, the audio paths can be switched into many different configurations, providing greater flexibility.

7.2.1. Internal Registers

The ISD5100-Series have multiple internal registers that are used to store the address information and the configuration or set-up of the device. The two 16-bit configuration registers control the audio paths through the device, the sample frequency, the various gains and attenuations, power up and down of different sections, and the volume settings. These registers are discussed in detail in section 7.3.5 on page 21.

7.2.2. Memory Architecture

The ISD5100-Series memory array are arranged in various pages (or rows) of each 2048 bits as follows. The primary addressing for the pages are handled by 11 bits of address input in the analog mode.

A memory page is 2048 bits organized as thirty-two 64-bit "blocks" when used for digital storage. The contents of a page are either analog or digital. This is determined by instruction (op code) at the time the data is written. A record of where is analog and where is digital, is stored in a message address table (MAT) by the system microcontroller. The MAT is a table kept in the microcontroller memory that defines the status of each message “page”. It can be stored back into the ISD5100-Series if the power fails or the system is turned off. Using this table allows for efficient message management. Segments of messages can be stored wherever there is available space in the memory array. [This is explained in detail for the ISD5008 in Applications Note #9 and will be similarly described in a later Note for the ISD5100-Series.]

	Pages (Rows)	Bits/Page	Total Memory Size	Max Duration @ 8kHz
ISD5116	2048	2048	4,194,304 bits	8 min 44 sec
ISD5108	1024	2048	2,097,152 bits	4 min 22 sec
ISD5104	512	2048	1,048,576 bits	2 min 11 sec

When a page is used for analog storage, the same 32 blocks are present but there are 8 EOM (End-of-Message) markers. This means that for each 4 blocks there is an EOM marker at the end. Thus, when recording, the analog recording will stop at any one of eight positions. At 8 kHz sampling frequency, this results in a resolution of 32 msec when ENDING an analog recording. Beginning an analog recording is limited to the 256 msec resolution provided by the 11-bit address. A recording does not immediately stop when the Stop command is given, but continues until the 32 millisecond block is filled. Then a bit is placed in the EOM memory to develop the interrupt that signals a message is finished playing in the Playback mode.

Digital data is sent and received serially over the I^2C interface. The data is serial-to-parallel converted and stored in one of two alternating (commutating) 64-bit shift registers. When an input register is full, it becomes the register that is parallel written into the array. The prior write register becomes the new serial input register. A mechanism is built-in to ensure there is always a register available for storing new data.

Storing data in the memory is accomplished by accepting data one byte at a time and issuing an acknowledge. If data is coming in faster than it can be written, the chip issues an acknowledge to the host microcontroller, but holds SCL LOW until it is ready to accept more data.

The read mode is the opposite of the write mode. Data is read into one of two 64-bit registers from the array and serially sent to the I^2C interface. (See section 7.5.3 on page 39 for details).

7.3. Operational Modes Description

7.3.1. I^2C Interface

To use more than four ISD5100-Series devices in an application requires some external switching of the I^2C interface.

I^2C interface

Important note: *The rest of this data sheet will assume that the reader is familiar with the I^2C serial interface. Additional information on I^2C may be found in section 10 on page 72 of this document. If you are not familiar with this serial protocol, please read this section to familiarize yourself with it. A large amount of additional information on I^2C can also be found on the Philips web page at* http://www.philips.com/.

I^2C Slave Address

The ISD5100-Series have 7-bit slave address of <100 00xy> where x and y are equal to the state, respectively, of the external address pins A1 and A0. Because all data bytes are required to be 8 bits, the LSB of the address byte is the Read/Write selection bit that tells the slave whether to transmit or receive data. Therefore, there are 8 possible slave addresses for the ISD5100-Series. These are:

Pinout Table

A1	A0	Slave Address	$\overline{R/W}$ Bit	HEX Value
0	0	<100 0000>	0	80
0	1	<100 0001>	0	82
1	0	<100 0010>	0	84
1	1	<100 0011>	0	86
0	0	<100 0000>	1	81
0	1	<100 0001>	1	83
1	0	<100 0010>	1	85
1	1	<100 0011>	1	87

ISD5100-Series I^2C Operation Definitions

There are many control functions used to operate the ISD5100-Series. Among them are:

7.3.1.1. Read Status Command:

The Read Status command is a read request from the Host processor to the ISD5100-Series without delivering a Command Byte. The Host supplies all the clocks (SCL). In each case, the entity sending the data drives the data line (SDA). The Read Status Command is executed by the following I^2C sequence.

1. Host executes I^2C START
2. Send Slave Address with R/W bit = “1” (Read) 81h
3. Slave (ISD5100-Series) responds back to Host an Acknowledge (ACK) followed by 8-bit Status word
4. Host sends an Acknowledge (ACK) to Slave
5. Wait for SCL to go HIGH
6. Slave responds with Upper Address byte of internal address register
7. Host sends an ACK to Slave
8. Wait for SCL to go HIGH

9. Slave responds with Lower Address byte of internal address register (A[4:0] will always return set to 0.)
10. Host sends a NO ACK to Slave, then executes I^2C STOP

Note that the processor could have sent an I^2C STOP after the Status Word data transfer and aborted the transfer of the Address bytes.

A graphical representation of this operation is found below. See the caption box above for more explanation.

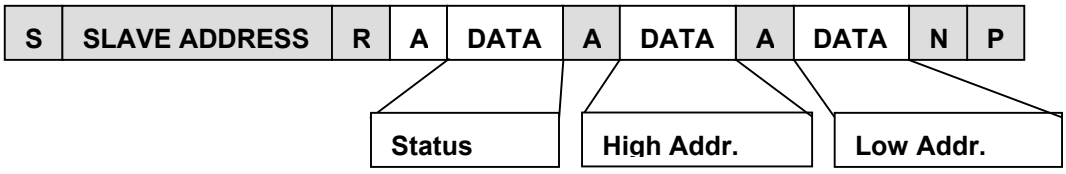
Conventions used in I^2C Data Transfer Diagrams

S	= START Condition
P	= STOP Condition
DATA	= 8-bit data transfer
R	= "1" in the R/W bit
W	= "0" in the R/W bit
A	= ACK (Acknowledge)
N	= No ACK
SLAVE ADDRESS	= 7-bit Slave Address

The Box color indicates the direction of data flow

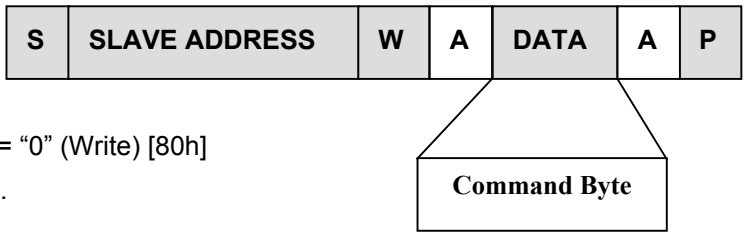
= Host to Slave (Gray)

= Slave to Host (White)



7.3.1.2. Load Command Byte Register (Single Byte Load):

A single byte may be written to the Command Byte Register in order to power up the device, start or stop Analog Record (if no address information is needed), or do a Message Cueing function. The Command Byte Register is loaded as follows:

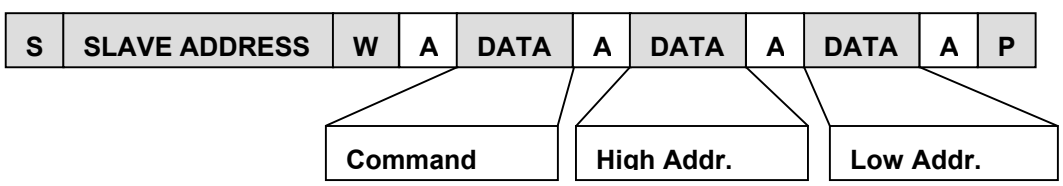


1. Host executes I^2C START
2. Send Slave Address with R/W bit = “0” (Write) [80h]
3. Slave responds back with an ACK.
4. Wait for SCL to go HIGH
5. Host sends a command byte to Slave
6. Slave responds with an ACK
7. Wait for SCL to go HIGH
8. Host executes I^2C STOP

7.3.1.3. Load Command Byte Register (Address Load)

For the normal addressed mode the Registers are loaded as follows:

1. Host executes I^2C START
2. Send Slave Address with R/W bit = “0” (Write)
3. Slave responds back with an ACK.
4. Wait for SCL to go HIGH
5. Host sends a byte to Slave - (Command Byte)
6. Slave responds with an ACK
7. Wait for SCL to go HIGH
8. Host sends a byte to Slave - (High Address Byte)
9. Slave responds with an ACK
10. Wait for SCL to go HIGH
11. Host sends a byte to Slave - (Low Address Byte)
12. Slave responds with an ACK
13. Wait for SCL to go HIGH
14. Host executes I^2C STOP



7.3.2. I²C Control Registers

The ISD5100-Series are controlled by loading commands to, or, reading from, the internal command, configuration and address registers. The Command byte sent is used to start and stop recording, write or read digital data and perform other functions necessary for the operation of the device.

Command Byte

Control of the ISD5100-Series are implemented through an 8-bit command byte, sent after the 7-bit device address and the 1-bit Read/Write selection bit. The 8 bits are:

- Global power up bit
- DAB bit: determines whether device is performing an analog or digital function
- 3 function bits: these determine which function the device is to perform in conjunction with the DAB bit.
- 3 register address bits: these determine if and when data is to be loaded to a register

Power Up Bit

C7	C6	C5	C4	C3	C2	C1	C0
PU	DAB	FN2	FN1	FN0	RG2	RG1	RG0
	Function Bits				Register Bits		

Function Bits

The command byte function bits are detailed in the table to the right. C6, the DAB bit, determines whether the device is performing an analog or digital function. The other bits are decoded to produce the individual commands. Not all decode combinations are currently used, and are reserved for future use. Out of 16 possible codes, the ISD5100-Series uses 7 for normal operation. The other 9 are undefined

Function Bits				Function
C6	C5	C4	C3	
DAB	FN2	FN1	FN0	
0	0	0	0	STOP (or do nothing)
0	1	0	1	Analog Play
0	0	1	0	Analog Record
0	1	1	1	Analog MC
1	1	0	0	Digital Read
1	0	0	1	Digital Write
1	0	1	0	Erase (row)

Register Bits

The register load may be used to modify a command sequence (such as load an address) or used with the null command sequence to load a configuration or test register. Not all registers are accessible to the user. [RG2 is always 0 as the four additional combinations are undefined.]

RG2	RG1	RG0	Function
C2	C1	C0	
0	0	0	No action
0	0	1	Load Address
0	1	0	Load CFG0
0	1	1	Load CFG1

7.3.3. Opcode Summary

OpCode Command Description

The following commands are used to access the chip through the I^2C interface.

- Play: analog play command
- Record: analog record command
- Message Cue: analog message cue command
- Read: digital read command
- Write: digital write command
- Erase: digital page and block erase command
- Power up: global power up/down bit. (C7)
- Load address: load address register (is incorporated in play, record, read and write commands)
- Load CFG0: load configuration register 0
- Load CFG1: load configuration register 1
- Read STATUS: Read the interrupt status and address register, including a hardwired device ID

Winbond Electronics Corp.

OPCODE COMMAND BYTE TABLE

		Pwr	Function Bits				Register Bits		
OPCODE	**HEX**	**PU**	**DAB**	**FN2**	**FN1**	**FN0**	**RG2**	**RG1**	**RG0**
COMMAND BIT NUMBER	**CMD**	**C7**	**C6**	**C5**	**C4**	**C3**	**C2**	**C1**	**C0**
POWER UP	80	1	0	0	0	0	0	0	0
POWER DOWN	00	0	0	0	0	0	0	0	0
STOP (DO NOTHING) STAY ON	80	1	0	0	0	0	0	0	0
STOP (DO NOTHING) STAY OFF	00	0	0	0	0	0	0	0	0
LOAD ADDRESS	81	1	0	0	0	0	0	0	1
LOAD CFG0	82	1	0	0	0	0	0	1	0
LOAD CFG1	83	1	0	0	0	0	0	1	1
RECORD ANALOG	90	1	0	0	1	0	0	0	0
RECORD ANALOG @ ADDR	91	1	0	0	1	0	0	0	1
PLAY ANALOG	A8	1	0	1	0	1	0	0	0
PLAY ANALOG @ ADDR	A9	1	0	1	0	1	0	0	1
MSG CUE ANALOG	B8	1	0	1	1	1	0	0	0
MSG CUE ANALOG @ ADDR	B9	1	0	1	1	1	0	0	1
ENTER DIGITAL MODE	C0	1	1	0	0	0	0	0	0
EXIT DIGITAL MODE	40	0	1	0	0	0	0	0	0
DIGITAL ERASE PAGE	D0	1	1	0	1	0	0	0	0
DIGITAL ERASE PAGE @ ADDR	D1	1	1	0	1	0	0	0	1
DIGITAL WRITE	C8	1	1	0	0	1	0	0	0
DIGITAL WRITE @ ADDR	C9	1	1	0	0	1	0	0	1
DIGITAL READ	E0	1	1	1	0	0	0	0	0
DIGITAL READ @ ADDR	E1	1	1	1	0	0	0	0	1
READ STATUS[1]	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

1. See section 7.2 on page 12 for details.

7.3.4. Data Bytes

In the I^2C write mode, the device can accept data sent after the command byte. If a register load option is selected, the next two bytes are loaded into the selected register. The format of the data is MSB first, the I^2C standard. Thus to load DATA<15:0> into the device, DATA<15:8> is sent first, the byte is acknowledged, and DATA<7:0> is sent next. The address register consists of two bytes. The format of the address is as follows:

ADDRESS<15:0> = PAGE_ADDRESS<10:0>, BLOCK_ADDRESS<4:0>

Note: if an analog function is selected, the block address bits must be set to 00000. Digital Read and Write are block addressable.

When the device is polled with the Read Status command, it will return three bytes of data. The first byte is the status byte, the next the upper address byte and the last the lower address byte. The status register is one byte long and its bit function is:

STATUS<7:0> = EOM, OVF, READY, PD, PRB, DEVICE_ID<2:0>

Lower address byte will always return the block address bits as zero, either in digital or analog mode.

The functions of the bits are:

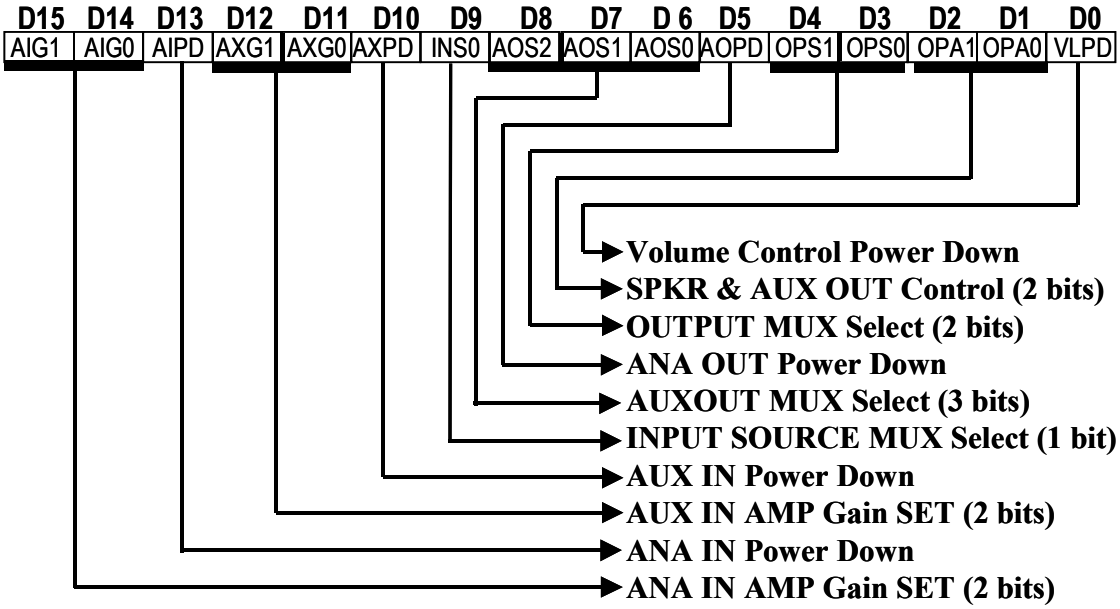
EOM	BIT 7	Indicates whether an EOM interrupt has occurred.
OVF	BIT 6	Indicates whether an overflow interrupt has occurred.
READY	BIT 5	Indicates the internal status of the device – if READY is LOW no new commands should be sent to device.
PD	BIT 4	Device is powered down if PD is HIGH.
PRB	BIT 3	Play/Record mode indicator. HIGH=Play/LOW=Record.
DEVICE_ID	BIT 0, 1, 2	An internal device ID. This is 001 for the ISD5116. This is 010 for the ISD5108. This is 100 for the ISD5104.

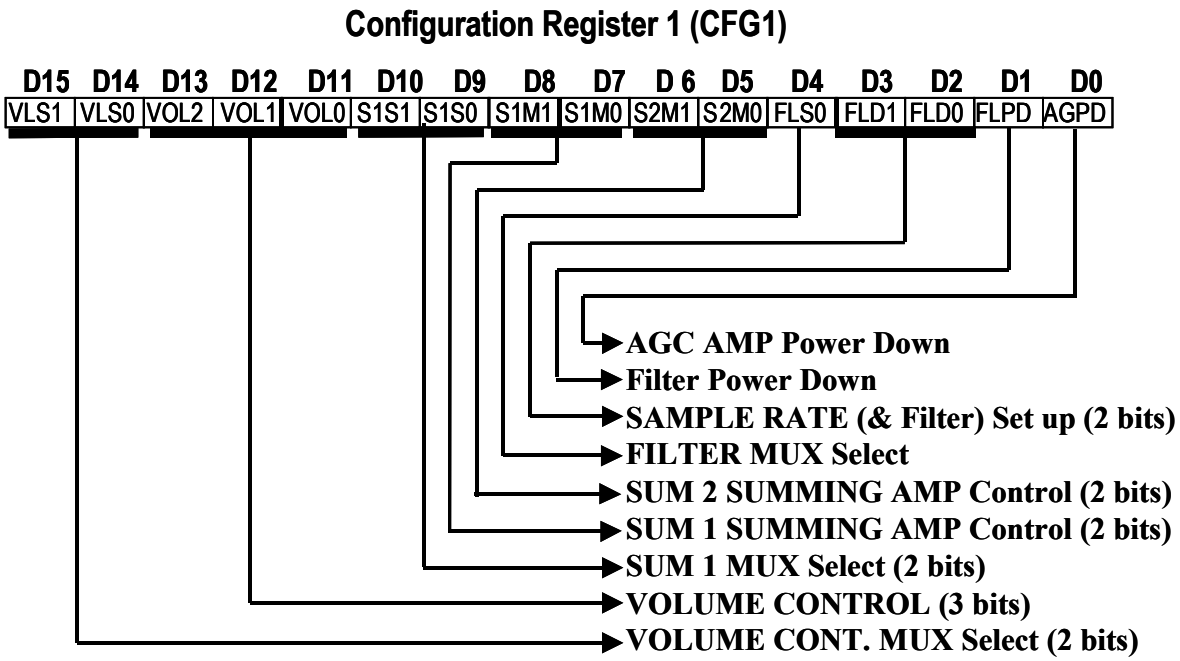
It is recommended that you read the status register after a Write or Record operation to ensure that the device is ready to accept new commands. Depending upon the design and the number of pins available on the controller, the polling overhead can be reduced. If $\overline{INT}$ and $\overline{RAC}$ are tied to the microcontroller, it does not have to poll as frequently to determine the status of the ISD5100-SERIES.

7.3.5. Configuration Resiter Bytes

The configuration register bytes are defined, in detail, in the drawings of section 7.4 on page 29. The drawings display how each bit enables or disables a function of the audio paths in the ISD5100-Series. The tables below give a general illustration of the bits. There are two configuration registers, CFG0 and CFG1, so there are four 8-bit bytes to be loaded during the set-up of the device.

Configuration Register 0 (CFG0)





7.3.6. Power-up Sequence

This sequence prepares the ISD5100-Series for an operation to follow, waiting the Tpud time before sending the next command sequence.

1. Send I^2C POWER UP
2. Send one byte 10000000 {Slave Address, R/W = 0} 80h
3. Slave ACK
4. Wait for SCL High
5. Send one byte 10000000 {Command Byte = Power Up} 80h
6. Slave ACK
7. Wait for SCL High
8. Send I^2C STOP

Playback Mode

The command sequence for an analog Playback operation can be handled several ways. One technique would be to do a Load Address (81h), which requires sending a total of four bytes, and then sending a Play Analog, which would be a Command Byte (A8h) proceeded by the Slave Address Byte. This is a total of six bytes plus the times for Start, ACK, and Stop.

Another approach would be to incorporate both into a single four byte exchange, which consists of the Slave Address (80h), the Command Byte (A9h) for Play Analog @ Address, and the two address bytes.

Record Mode

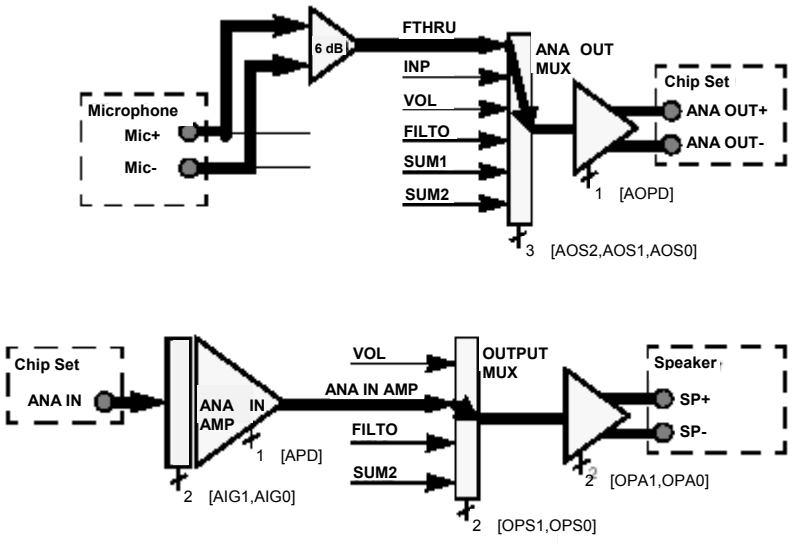
The command sequence for an Analog Record would be a four byte sequence consisting of the Slave Address (80h), the Command Byte (91h) for Record Analog @ Address, and the two address bytes. See "Load Command Byte Register (Address Load)" in section 7.3.2 on page 17.

7.3.7. Feed Through Mode

The previous examples were dependent upon the device already being powered up and the various paths being set through the device for the desired operation. To set up the device for the various paths requires loading the two 16-bit Configuration Registers with the correct data. For example, in the Feed Through Mode the device only needs to be powered up and a few paths selected.

This mode enables the ISD5100-Series to connect to a cellular or cordless base band phone chip set without affecting the audio source or destination. There are two paths involved, the transmit path and the receive path. The transmit path connects the Winbond chip's microphone source through to the microphone input on the base band chip set. The receive path connects the base band chip set's speaker output through to the speaker driver on the Winbond chip. This allows the Winbond chip to substitute for those functions and incidentally gain access to the audio to and from the base band chip set.

To set up the environment described above, a series of commands need to be sent to the ISD5100-Series. First, the chip needs to be powered up as described in this section. Then the Configuration Registers must be filled with the specific data to connect the paths desired. In the case of the Feed Through Mode, most of the chip can remain powered down. The following figure illustrates the affected paths.



The figure above shows the part of the ISD5100-Series block diagram that is used in Feed Through Mode. The rest of the chip will be powered down to conserve power. The bold lines highlight the audio paths. Note that the Microphone to ANA OUT +/– path is differential.

To select this mode, the following control bits must be configured in the ISD5100-Series configuration registers. To set up the transmit path:

1. Select the FTHRU path through the ANA OUT MUX—Bits AOS0, AOS1 and AOS2 control the state of the ANA OUT MUX. These are the D6, D7 and D8 bits respectively of Configuration Register 0 (CFG0) and they should all be ZERO to select the FTHRU path.

2. Power up the ANA OUT amplifier—Bit AOPD controls the power up state of ANA OUT. This is bit D5 of CFG0 and it should be a ZERO to power up the amplifier.

To set up the receive path:

1. Set up the ANA IN amplifier for the correct gain—Bits AIG0 and AIG1 control the gain settings of this amplifier. These are bits D14 and D15 respectively of CFG0. The input level at this pin determines the setting of this gain stage. The **ANA IN Amplifier Gain Settings table** on page 36 will help determine this setting. In this example, we will assume that the peak signal never goes above 1 volt p-p single ended. That would enable us to use the 9 dB attenuation setting, or where D14 is ONE and D15 is ZERO.

2. Power up the ANA IN amplifier—Bit AIPD controls the power up state of ANA IN. This is bit D13 of CFG0 and should be a ZERO to power up the amplifier.

3. Select the ANA IN path through the OUTPUT MUX—Bits OPS0 and OPS1 control the state of the OUTPUT MUX. These are bits D3 and D4 respectively of CFG0 and they should be set to the state where D3 is ONE and D4 is ZERO to select the ANA IN path.

4. Power up the Speaker Amplifier—Bits OPA0 and OPA1 control the state of the Speaker and AUX amplifiers. These are bits D1 and D2 respectively of CFG0. They should be set to the state where D1 is ONE and D2 is ZERO. This powers up the Speaker Amplifier and configures it for its higher gain setting for use with a piezo speaker element and also powers down the AUX output stage.

The status of the rest of the functions in the ISD5100-Series chip must be defined before the configuration registers settings are updated:

1. Power down the Volume Control Element—Bit VLPD controls the power up state of the Volume Control. This is bit D0 of CFG0 and it should be set to a ONE to power down this stage.

2. Power down the AUX IN amplifier—Bit AXPD controls the power up state of the AUX IN input amplifier. This is bit D10 of CFG0 and it should be set to a ONE to power down this stage.

3. Power down the SUM1 and SUM2 Mixer amplifiers—Bits S1M0 and S1M1 control the SUM1 mixer and bits S2M0 and S2M1 control the SUM2 mixer. These are bits D7 and D8 in CFG1 and bits D5 and D6 in CFG1 respectively. All 4 bits should be set to a ONE to power down these two amplifiers.

4. Power down the FILTER stage—Bit FLPD controls the power up state of the FILTER stage in the device. This is bit D1 in CFG1 and should be set to a ONE to power down the stage.
5. Power down the AGC amplifier—Bit AGPD controls the power up state of the AGC amplifier. This is bit D0 in CFG1 and should be set to a ONE to power down this stage.
6. Don't Care bits—The following stages are not used in Feed Through Mode. Their bits may be set to either level. In this example, we will set all the following bits to a ZERO. (a). Bit INS0, bit D9 of CFG0 controls the Input Source Mux. (b). Bits AXG0 and AXG1 are bits D11 and D12 respectively in CFG0. They control the AUX IN amplifier gain setting. (c). Bits FLD0 and FLD1 are bits D2 and D3 respectively in CFG1. They control the sample rate and filter band pass setting. (d). Bit FLS0 is bit D4 in CFG1. It controls the FILTER MUX. (e). Bits S1S0 and S1S1 are bits D9 and D10 of CFG1. They control the SUM1 MUX. (f). Bits VOL0, VOL1 and VOL2 are bits D11, D12 and D13 of CFG1. They control the setting of the Volume Control. (g). Bits VLS0 and VLS1 are bits D14 and D15 of CFG1. They control the Volume Control MUX.

The end result of the above set up is

CFG0=0100 0100 0000 1011 (hex 440B)

and

CFG1=0000 0001 1110 0011 (hex 01E3).

Since both registers are being loaded, CFG0 is loaded, followed by the loading of CFG1. These two registers must be loaded in this order. The internal set up for both registers will take effect synchronously with the rising edge of SCL.

7.3.8. Call Record

The call record mode adds the ability to record an incoming phone call. In most applications, the ISD5100-Series would first be set up for Feed Through Mode as described above. When the user wishes to record the incoming call, the setup of the chip is modified to add that ability. For the purpose of this explanation, we will use the 6.4 kHz sample rate during recording.

The block diagram of the ISD5100-Series shows that the Multilevel Storage array is always driven from the SUM2 SUMMING amplifier. The path traces back from there through the LOW PASS Filter, THE FILTER MUX, THE SUM1 SUMMING amplifier, the SUM1 MUX, then from the ANA in amplifier. Feed Through Mode has already powered up the ANA IN amp so we only need to power up and enable the path to the Multilevel Storage array from that point:

1. Select the ANA IN path through the SUM1 MUX—Bits S1S0 and S1S1 control the state of the SUM1 MUX. These are bits D9 and D10 respectively of CFG1 and they should be set to the state where both D9 and D10 are ZERO to select the ANA IN path.
2. Select the SUM1 MUX input (only) to the S1 SUMMING amplifier—Bits S1M0 and S1M1 control the state of the SUM1 SUMMING amplifier. These are bits D7 and D8 respectively of

CFG1 and they should be set to the state where D7 is ONE and D8 is ZERO to select the SUM1 MUX (only) path.

3. Select the SUM1 SUMMING amplifier path through the FILTER MUX—Bit FLS0 controls the state of the FILTER MUX. This is bit D4 of CFG1 and it must be set to ZERO to select the SUM1 SUMMING amplifier path.

4. Power up the LOW PASS FILTER—Bit FLPD controls the power up state of the LOW PASS FILTER stage. This is bit D1 of CFG1 and it must be set to ZERO to power up the LOW PASS FILTER STAGE.

5. Select the 6.4 kHz sample rate—Bits FLD0 and FLD1 select the Low Pass filter setting and sample rate to be used during record and playback. These are bits D2 and D3 of CFG1. To enable the 6.4 kHz sample rate, D2 must be set to ONE and D3 set to ZERO.

6. Select the LOW PASS FILTER input (only) to the S2 SUMMING amplifier—Bits S2M0 and S2M1 control the state of the SUM2 SUMMING amplifier. These are bits D5 and D6 respectively of CFG1 and they should be set to the state where D5 is ZERO and D6 is ONE to select the LOW PASS FILTER (only) path.

In this mode, the elements of the original PASS THROUGH mode do not change. The sections of the chip not required to add the record path remain powered down. In fact, CFG0 does not change and remains

CFG0=0100 0100 0000 1011 (hex 440B).

CFG1 changes to

CFG1=0000 0000 1100 0101 (hex 00C5).

Since CFG0 is not changed, it is only necessary to load CFG1. Note that if only CFG0 was changed, it would be necessary to load both registers.

7.3.9. Memo Record

The Memo Record mode sets the chip up to record from the local microphone into the chip's Multilevel Storage Array. A connected cellular telephone or cordless phone chip set may remain powered down and is not active in this mode. The path to be used is microphone input to AGC amplifier, then through the INPUT SOURCE MUX to the SUM1 SUMMING amplifier. From there the path goes through the FILTER MUX, the LOW PASS FILTER, the SUM2 SUMMING amplifier, then to the MULTILEVEL STORAGE ARRAY. In this instance, we will select the 5.3 kHz sample rate. The rest of the chip may be powered down.

1. Power up the AGC amplifier—Bit AGPD controls the power up state of the AGC amplifier. This is bit D0 of CFG1 and must be set to ZERO to power up this stage.

2. Select the AGC amplifier through the INPUT SOURCE MUX—Bit INS0 controls the state of the INPUT SOURCE MUX. This is bit D9 of CFG0 and must be set to a ZERO to select the AGC amplifier.

3. Select the INPUT SOURCE MUX (only) to the S1 SUMMING amplifier—Bits S1M0 and S1M1 control the state of the SUM1 SUMMING amplifier. These are bits D7 and D8 respectively of CFG1 and they should be set to the state where D7 is ZERO and D8 is ONE to select the INPUT SOURCE MUX (only) path.

4. Select the SUM1 SUMMING amplifier path through the FILTER MUX—Bit FLS0 controls the state of the FILTER MUX. This is bit D4 of CFG1 and it must be set to ZERO to select the SUM1 SUMMING amplifier path.

5. Power up the LOW PASS FILTER—Bit FLPD controls the power up state of the LOW PASS FILTER stage. This is bit D1 of CFG1 and it must be set to ZERO to power up the LOW PASS FILTER STAGE.

6. Select the 5.3 kHz sample rate—Bits FLD0 and FLD1 select the Low Pass filter setting and sample rate to be used during record and playback. These are bits D2 and D3 of CFG1. To enable the 5.3 kHz sample rate, D2 must be set to ZERO and D3 set to ONE.

7. Select the LOW PASS FILTER input (only) to the S2 SUMMING amplifier—Bits S2M0 and S2M1 control the state of the SUM2 SUMMING amplifier. These are bits D5 and D6 respectively of CFG1 and they should be set to the state where D5 is ZERO and D6 is ONE to select the LOW PASS FILTER (only) path.

To set up the chip for Memo Record, the configuration registers are set up as follows:

CFG0=0010 0100 0010 0001 (hex 2421).

CFG1=0000 0001 0100 1000 (hex 0148).

Only those portions necessary for this mode are powered up.

7.3.10. Memo and Call Playback

This mode sets the chip up for local playback of messages recorded earlier. The playback path is from the MULTILEVEL STORAGE ARRAY to the FILTER MUX, then to the LOW PASS FILTER stage. From there, the audio path goes through the SUM2 SUMMING amplifier to the VOLUME MUX, through the VOLUME CONTROL then to the SPEAKER output stage. We will assume that we are driving a piezo speaker element. This audio was previously recorded at 8 kHz. All unnecessary stages will be powered down.

1. Select the MULTILEVEL STORAGE ARRAY path through the FILTER MUX—Bit FLS0, the state of the FILTER MUX. This is bit D4 of CFG1 and must be set to ONE to select the MULTILEVEL STORAGE ARRAY.

2. Power up the LOW PASS FILTER—Bit FLPD controls the power up state of the LOW PASS FILTER stage. This is bit D1 of CFG1 and it must be set to ZERO to power up the LOW PASS FILTER STAGE.

3. Select the 8.0 kHz sample rate—Bits FLD0 and FLD1 select the Low Pass filter setting and sample rate to be used during record and playback. These are bits D2 and D3 of CFG1. To enable the 8.0 kHz sample rate, D2 and D3 must be set to ZERO.

4. Select the LOW PASS FILTER input (only) to the S2 SUMMING amplifier —Bits S2M0 and S2M1 control the state of the SUM2 SUMMING amplifier. These are bits D5 and D6

respectively of CFG1 and they should be set to the state where D5 is ZERO and D6 is ONE to select the LOW PASS FILTER (only) path.

5. Select the SUM2 SUMMING amplifier path through the VOLUME MUX—Bits VLS0 and VLS1 control the state VOLUME MUX. These bits are bits D14 and D15, respectively of CFG1. They should be set to the state where D14 is ONE and D15 is ZERO to select the SUM2 SUMMING amplifier.

6. Power up the VOLUME CONTROL LEVEL—Bit VLPD controls the power-up state of the VOLUME CONTROL attenuator. This is Bit D0 of CFG0. This bit must be set to a ZERO to power-up the VOLUME CONTROL.

7. Select a VOLUME CONTROL LEVEL—Bits VOL0, VOL1, and VOL2 control the state of the VOLUME CONTROL LEVEL. These are bits D11, D12, and D13, respectively, of CFG1. A binary count of 000 through 111 controls the amount of attenuation through that state. In most cases, the software will select an attenuation level according to the desires of the current users of the product. In this example, we will assume the user wants an attenuation of –12 dB. For that setting, D11 should be set to ONE, D12 should be set to ONE, and D13 should be set to a ZERO.

8. Select the VOLUME CONTROL path through the OUTPUT MUX—These are bits D3 and D4, respectively, of CFG0. They should be set to the state where D3 is ZERO and D4 is a ZERO to select the VOLUME CONTROL.

9. Power up the SPEAKER amplifier and select the HIGH GAIN mode—Bits OPA0 and OPA1 control the state of the speaker (SP+ and SP–) and AUX OUT outputs. These are bits D1 and D2 of CFG0. They must be set to the state where D1 is ONE and D2 is ZERO to power-up the speaker outputs in the HIGH GAIN mode and to power-down the AUX OUT.

To set up the chip for Memo or Call Playback, the configuration registers are set up as follows:

CFG0=0010 0100 0010 0010 (hex 2422).

CFG1=0101 1001 1101 0001 (hex 59D1).

Only those portions necessary for this mode are powered up.

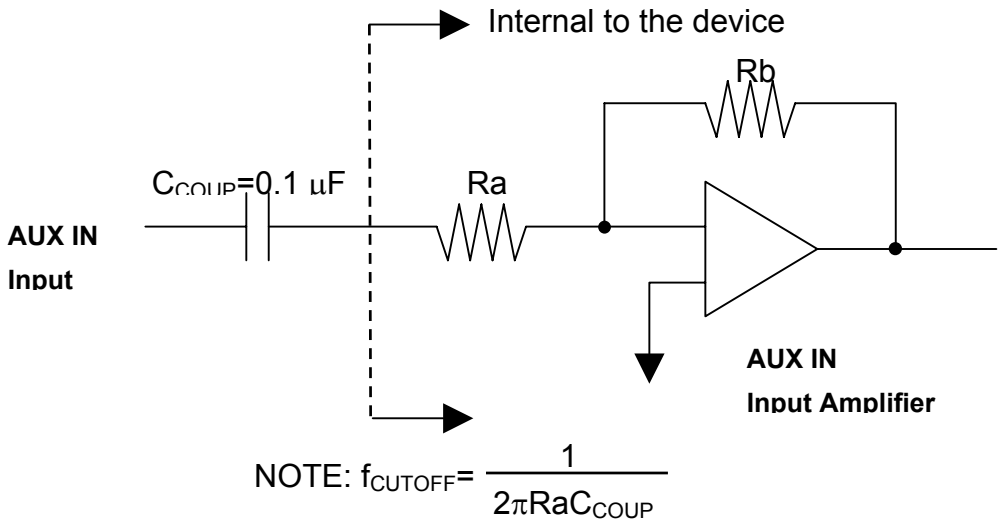
7.3.11. Message Cueing

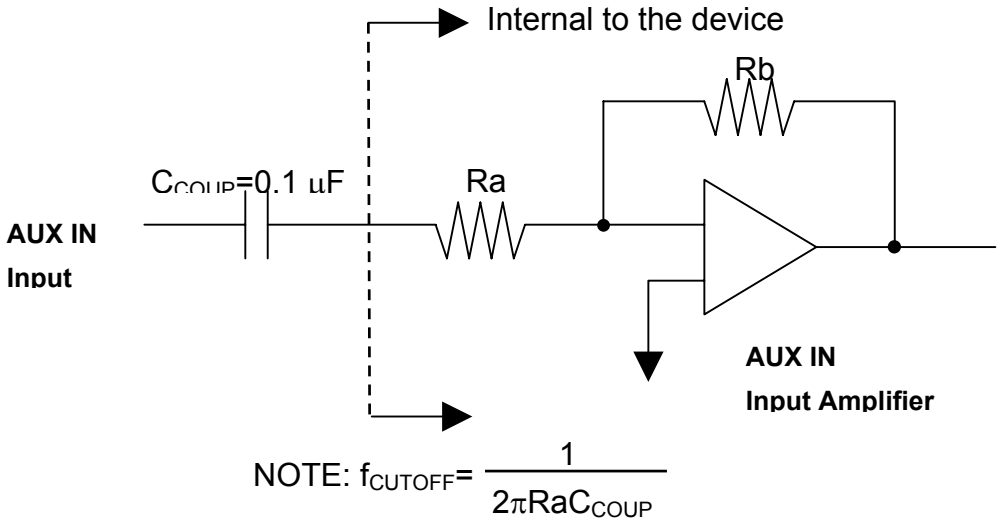
Message cueing allows the user to skip through analog messages without knowing the actual physical location of the message. This operation is used during playback. In this mode, the messages are skipped 512 times faster than in normal playback mode. It will stop when an EOM marker is reached. Then, the internal address counter will be pointing to the next message.

7.4. ANALOG MODE

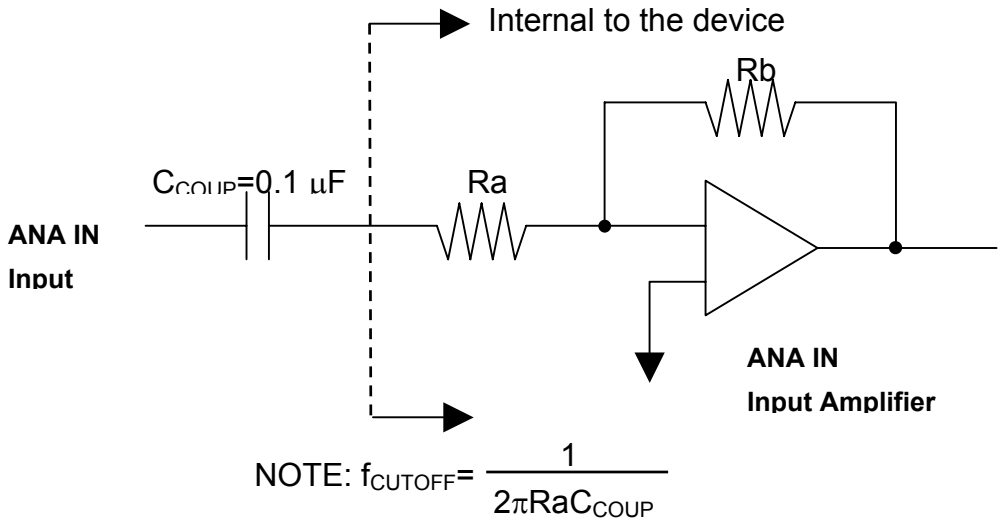
7.4.1. Aux In and Ana In Description

The AUX IN is an additional audio input to the ISD5100-Series, such as from the microphone circuit in a mobile phone “car kit.” This input has a nominal 694 mV p-p level at its minimum gain setting (0 dB). See the **AUX IN Amplifier Gain Settings table** on page 37. Additional gain is available in 3 dB steps (controlled by the I^2C serial interface) up to 9 dB.

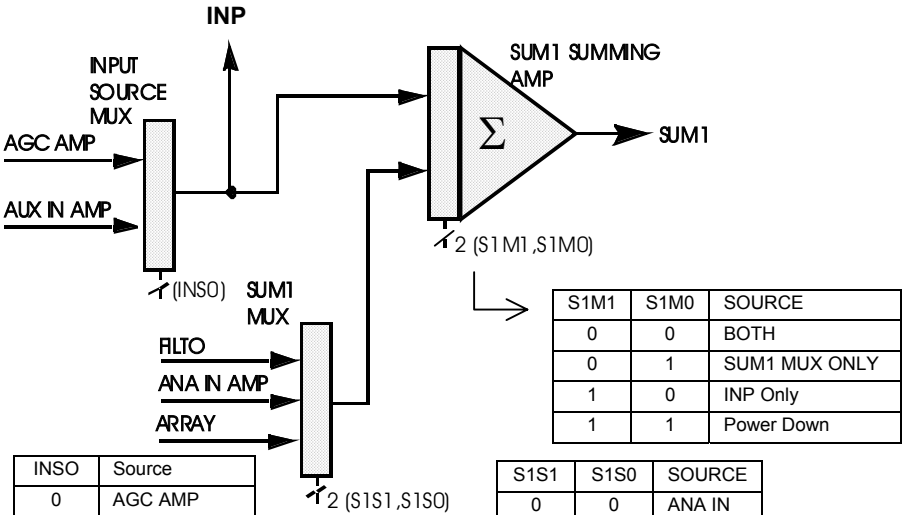




The ANA IN pin is the analog input from the telephone chip set. It can be switched (by the serial bus) to the speaker output, the array input or to various other paths. This pin is designed to accept a nominal 1.11 Vp-p when at its minimum gain (6 dB) setting. See the **ANA IN Amplifier Gain Settings table** on page 37. There is additional gain available in 3 dB steps controlled from the I^2C interface, if required, up to 15 dB.



7.4.2. ISD5100-Series Analog Structure (left half) Description



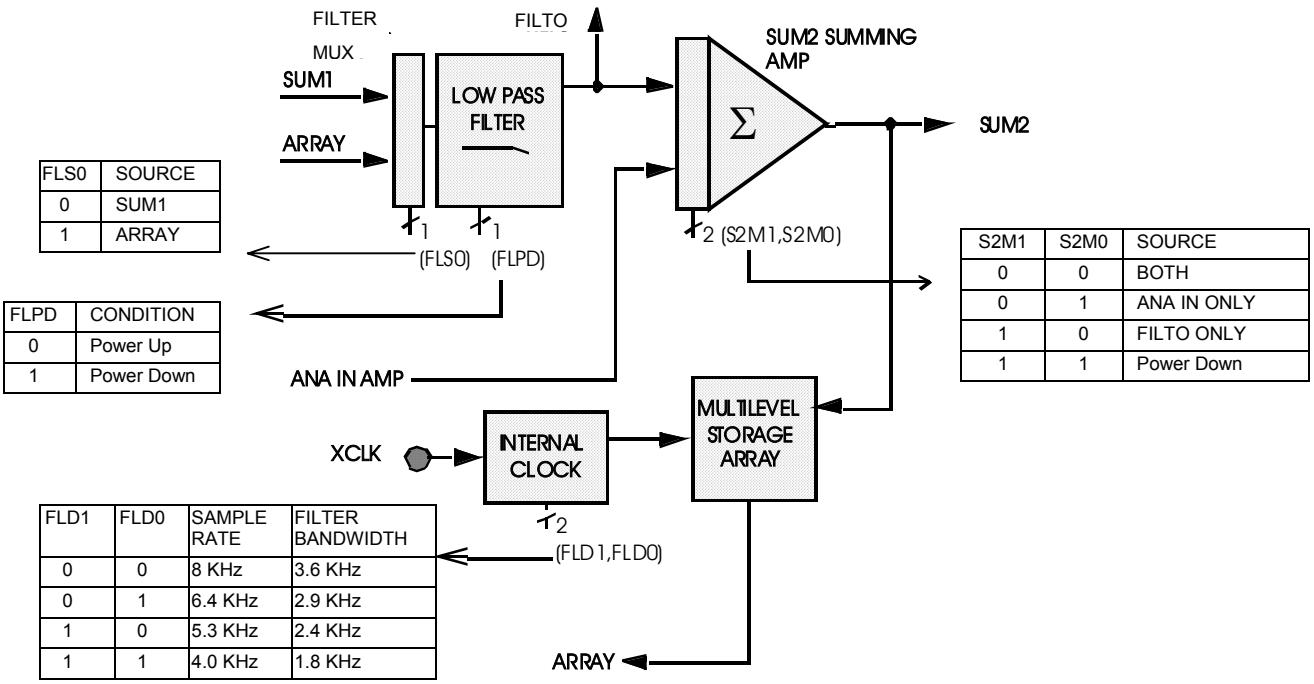
INSO	Source
0	AGC AMP
1	AUX IN AMP

S1M1	S1M0	SOURCE
0	0	BOTH
0	1	SUM1 MUX ONLY
1	0	INP Only
1	1	Power Down

S1S1	S1S0	SOURCE
0	0	ANA IN
0	1	ARRAY
1	0	FILTO
1	1	N/C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
AIG1	AIG0	AIPD	AXG1	AXG0	AXPD	**INS0**	AOS2	AOS1	AOS0	AOPD	OPS1	OPS0	OPA1	OPA0	VLPD	CFG0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
VLS1	VLS0	VOL2	VOL1	VOL0	**S1S1**	**S1S0**	**S1M1**	**S1M0**	S2M1	S2M0	FLS0	FLD1	FLD0	FLPD	AGPD	CFG1

7.4.3. ISD5100-Series Aanalog Structure (right half) Description



FLS0	SOURCE
0	SUM1
1	ARRAY

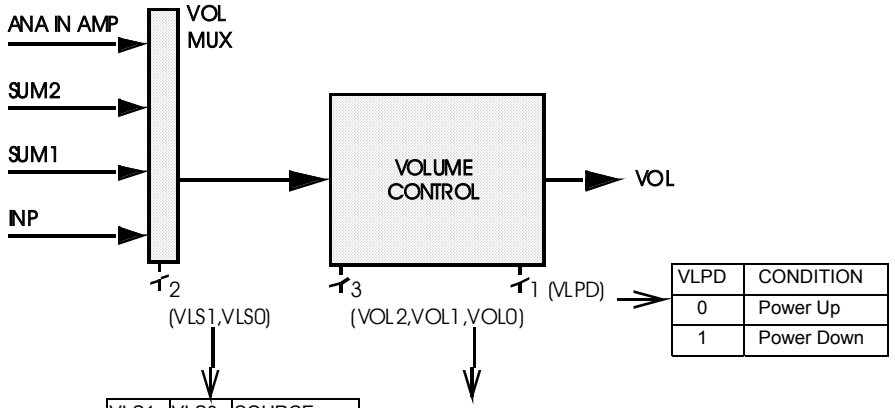
FLPD	CONDITION
0	Power Up
1	Power Down

S2M1	S2M0	SOURCE
0	0	BOTH
0	1	ANA IN ONLY
1	0	FILTO ONLY
1	1	Power Down

FLD1	FLD0	SAMPLE RATE	FILTER BANDWIDTH
0	0	8 KHz	3.6 KHz
0	1	6.4 KHz	2.9 KHz
1	0	5.3 KHz	2.4 KHz
1	1	4.0 KHz	1.8 KHz

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
VLS1	VLS0	VOL2	VOL1	VOL0	S1S1	S1S0	S1M1	S1M0	S2M1	S2M0	FLS0	FLD1	FLD0	FLPD	AGPD	CFG1

7.4.4. Volume Control Description



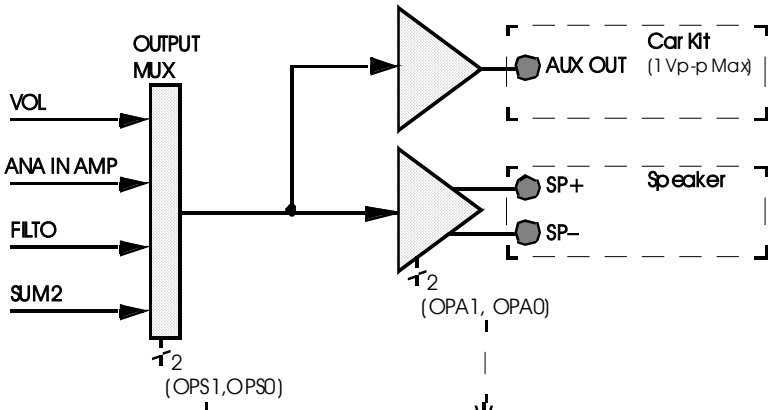
VLPD	CONDITION
0	Power Up
1	Power Down

VLS1	VLS0	SOURCE
0	0	ANA IN AMP
0	1	SUM2
1	0	SUM1
1	1	INP

VOL2	VOL1	VOL 0	ATTENUATION
0	0	0	0 dB
0	0	1	4 dB
0	1	0	8 dB
0	1	1	12 dB
1	0	0	16 dB
1	0	1	20 dB
1	1	0	24 dB
1	1	1	28 dB

AIG1	AIG0	AIPD	AXG1	AXG0	AXPD	INS0	AOS2	AOS1	AOS0	AOPD	OPS1	OPS0	OPA1	OPA0	VLPD	CFG0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
VLS1	VLS0	VOL2	VOL1	VOL0	S1S1	S1S0	S1M1	S1M0	S2M1	S2M0	FLS0	FLD1	FLD0	FLPD	AGPD	CFG1

7.4.5. Speaker and Aux Out Description

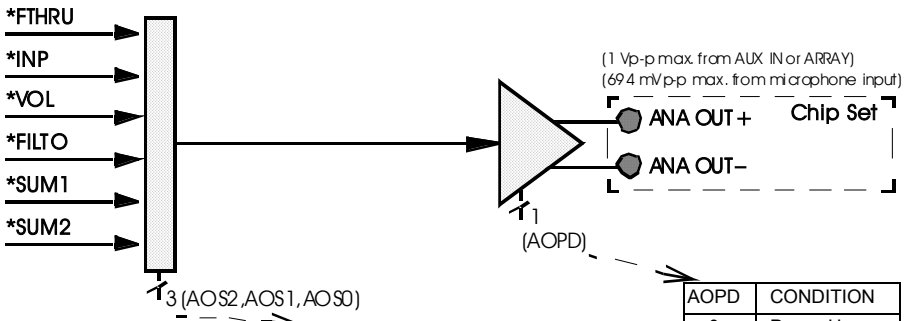


OPS1	OPS0	SOURCE
0	0	VOL
0	1	ANA IN
1	0	FILTO
1	1	SUM2

OPA1	OPA0	SPKR DRIVE	AUX OUT
0	0	Power Down	Power Down
0	1	3.6 V_{P-P} @ 150 Ω	Power Down
1	0	23.5 mWatt @ 8 Ω	Power Down
1	1	Power Down	1 V_{P-P} Max @ 5 KΩ

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
AIG1	AIG0	AIPD	AXG1	AXG0	AXPD	INS0	AOS2	AOS1	AOS0	AOPD	OPS1	OPS0	OPA1	OPA0	VLPD	CFG0

7.4.6. Ana Out Description



AOPD	CONDITION
0	Power Up
1	Power Down

*DIFFERENTIAL PATH

AOS2	AOS1	AOS0	SOURCE
0	0	0	FTHRU
0	0	1	INP
0	1	0	VOL
0	1	1	FILTO
1	0	0	SUM1
1	0	1	SUM2
1	1	0	N/C
1	1	1	N/C

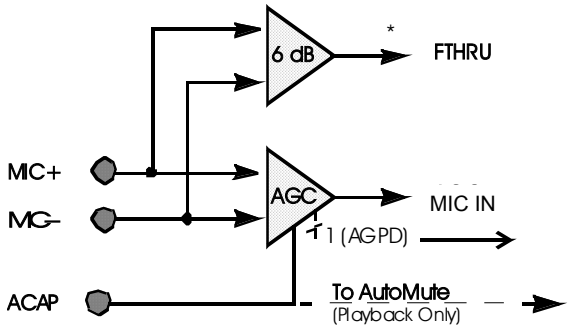
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
AIG1	AIG0	AIPD	AXG1	AXG0	AXPD	INS0	AOS2	AOS1	AOS0	AOPD	OPS1	OPS0	OPA1	OPA0	VLPD	CFG0

7.4.7. Analog Inputs

Microphone Inputs

The microphone inputs transfer the voice signal to the on-chip AGC preamplifier or directly to the ANA OUT MUX, depending on the selected path. The direct path to the ANA OUT MUX has a gain of 6 dB so a 208 mV p-p signal across the differential microphone inputs would give 416 mV p-p across the ANA OUT pins. The AGC circuit has a range of 45 dB in order to deliver a nominal 694 mV p-p into the storage array from a typical electric microphone output of 2 to 20 mV p-p. The input impedance is typically 10kΩ.

The ACAP pin provides the capacitor connection for setting the parameters of the microphone AGC circuit. It should have a 4.7 µF capacitor connected to ground. It cannot be left floating. This is because the capacitor is also used in the playback mode for the AutoMute circuit. This circuit reduces the amount of noise present in the output during quiet pauses. Tying this pin to ground gives maximum gain; to VCCA gives minimum gain for the AGC amplifier but will cancel the AutoMute function.

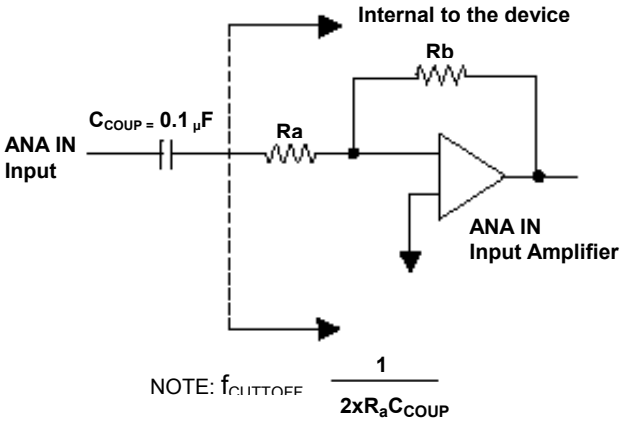


AGPD	CONDITION
0	Power Up
1	Power Down

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
VLS1	VLS0	VOL2	VOL1	VOL0	S1S1	S1S0	S1M1	S1M0	S2M1	S2M0	FLS0	FLD1	FLD0	FLPD	AGPD	CFG1

ANA IN (Analog Input)

The ANA IN pin is the analog input from the telephone chip set. It can be switched (by the I^2C interface) to the speaker output, the array input or to various other paths. This pin is designed to accept a nominal 1.11 V p-p when at its minimum gain (6 dB) setting. There is additional gain available, if required, in 3 dB steps, up to 15 dB. The gain settings are controlled from the I^2C interface.



Gain Setting	Resistor Ratio (Rb/Ra)	Gain	Gain[2] (dB)
00	63.9 / 102	0.625	-4.1
01	77.9 / 88.1	0.883	-1.1
10	92.3 / 73.8	1.250	1.9
11	106 / 60	1.767	4.9

ANA IN Amplifier Gain Settings

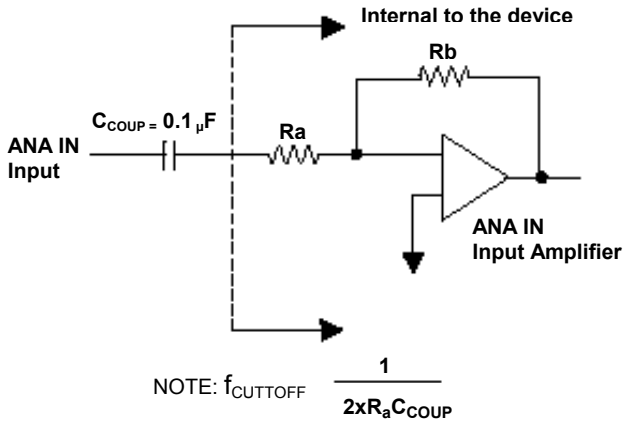
Setting[1]	0TLP Input V_{P-P}[3]	CFG0		Gain[2]	Array In/Out V_{P-P}	Speaker Out V_{P-P}[4]
		AIG1	AIG0			
6 dB	1.110	0	0	0.625	0.694	2.22
9 dB	0.785	0	1	0.883	0.694	2.22
12 dB	0.555	1	0	1.250	0.694	2.22
15 dB	0.393	1	1	1.767	0.694	2.22

1. *Gain from ANA IN to SP+/-*
2. *Gain from ANA IN to ARRAY IN*
3. *0TLP Input is the reference Transmission Level Point that is used for testing. This level is typically 3 dB below clipping*
4. *Speaker Out gain set to 1.6 (High). (Differential)*

AUX IN (Auxiliary Input)

The AUX IN is an additional audio input to the ISD5100-Series, such as from the microphone circuit in a mobile phone "car kit." This input has a nominal 694 mV p-p level at its minimum gain setting (0 dB). See the following table. Additional gain is available in 3 dB steps (controlled by the I^2C interface) up to 9 dB.

AUX IN Input Modes



Gain Setting	Resistor Ratio (Rb/Ra)	Gain	Gain[2] (dB)
00	40.1 / 40.1	1.0	0
01	47.0 / 33.2	1.414	3
10	53.5 / 26.7	2.0	6
11	59.2 / 21	2.82	9

AUX IN Amplifier Gain Settings

Setting[1]	0TLP Input V_{P-P}[3]	CFG0		Gain[2]	Array In/Out V_{P-P}	Speaker Out V_{P-P}[4]
		AIG1	AIG0			
0 dB	0.694	0	0	1.00	0.694	0.694
3 dB	0.491	0	1	1.41	0.694	0.694
6 dB	0.347	1	0	2.00	0.694	0.694
9 dB	0.245	1	1	2.82	0.694	0.694

1. *Gain from AUX IN to ANA OUT*
2. *Gain from AUX IN to ARRAY IN*
3. *0TLP Input is the reference Transmission Level Point that is used for testing. This level is typically 3 dB below clipping*
4. *Differential*

7.5. DIGITAL MODE

7.5.1. Erasing Digital Data

The Digital Erase command can only erase an entire page at a time. This means that the D1 command only needs to include the 11-bit page address; the 5-bit for block address are left at 00000.

Once a page has been erased, each block may be written separately, 64 bits at a time. But, if a block has been previously written then the entire page of 2048 bits must be erased in order to re-write (or change) a block.

A sequence might be look like:

- read the entire page
- store it in RAM
- change the desired bit(s)
- erase the page
- write the new data from RAM to the entire page

7.5.2. Writing Digital Data

The Digital Write function allows the user to select a portion of the array to be used as digital memory. The partition between analog and digital memory is left up to the user. A page can only be either Digital or Analog, but not both. The minimum addressable block of memory in the digital mode is one block or 64 bits, when reading or writing. The address sent to the device is the 11-bit row (or page) address with the 5-bit scan (or block) address. However, one must send a Digital Erase before attempting to change digital data on a page. This means that even when changing only one of the 32 blocks, all 32 blocks will need to be rewritten to the page. Command Sequence: The chip enters digital mode by sending the ENTER DIGITAL MODE command from power down. Send the DIGITAL WRITE @ ADDR command with the row address. After the address is entered, the data is sent in one-byte packets followed by an I^2C acknowledge generated by the chip. Data for each block is sent MSB first. The data transfer is ended when the master generates an I^2C STOP condition. If only a partial block of data is sent before the STOP condition, “zero” is written in the remaining bytes; that is, they are left at the erase level. An erased page (row) will be read as all zeros. The device can buffer up to two blocks of data. If the device is unable to accept more data due to the internal write process, the SCL line will be held LOW indicating to the master to halt data transfer. If the device encounters an overflow condition, it will respond by generating an interrupt condition and an I^2C Not Acknowledge signal after the last valid byte of data. Once data transfer is terminated, the device needs up to two cycles (64 us) to complete its internal write cycle before another command is sent. If an active command is sent before the internal cycle is finished, the part will hold SCL LOW until the current command is finished. After writing is complete, send the EXIT DIGITAL MODE command.

7.5.3. Reading Digital Data

The Digital Read command utilizes the combined I^2C command format. That is, a command is sent to the chip using the write data direction. Then the data direction is reversed by sending a repeated start condition, and the slave address with R/W set to 1. After this, the slave device (ISD5100-Series) begins to send data to the master until the master generates a NACK. If the part encounters an overflow condition, the $\overline{INT}$ pin is pulled LOW. No other communication with the master is possible due to the master generating ACK signals.

Digital Write and Digital Read can be done a "block" at a time. Thus, only 64 bits need be read in each Digital Read command sequence.

7.5.4. Example Command Sequences

An explanation and graphical representation of the Erase, Write and Read operations are found below.

Note: All sequences assumes that the chip is in power-down mode before the commands are sent.

7.5.4.1. Erase Digital Data

```
Erase
=====
I2CStart
SendByte(0x80)        - Write, Slave address zero
WaitACK
WaitSCLHigh
SendByte(0xc0)        - Enter Digital Mode Command
WaitACK
WaitSCLHigh
I2CStop

I2CStart
SendByte(0x80)        - Write, Slave address zero
WaitACK
WaitSCLHigh
SendByte(0xd1)        - Digital Erase Command
WaitACK
WaitSCLHigh
SendByte(row/256)   - high address byte
```

WaitACK
WaitSCLHigh
SendByte(row%256) - low address byte
WaitACK
WaitSCLHigh
I2CStop

repeat until the number of RAC pulses are one less
than the number of rows to delete
{
    wait RAC low
    WAIT RAC high
}

Note: If only one row is going to be erased,
send the following STOP command immediately after
ERASE command and skip the loop above

I2CStart
SendByte(0x80) - Write, Slave address zero
WaitACK
WaitSCLHigh
SendByte(0xc0) - Stop digital erase
WaitACK
WaitSCLHigh
I2CStop

wait until erase of the last row has completed
{
    wait RAC low
    WAIT RAC high
}

I2CStart
SendByte(0x80) - Write, Slave address zero

WaitACK
WaitSCLHigh
SendByte(0x40) - Exit Digital Mode Command
WaitACK
WaitSCLHigh
I2Cstop

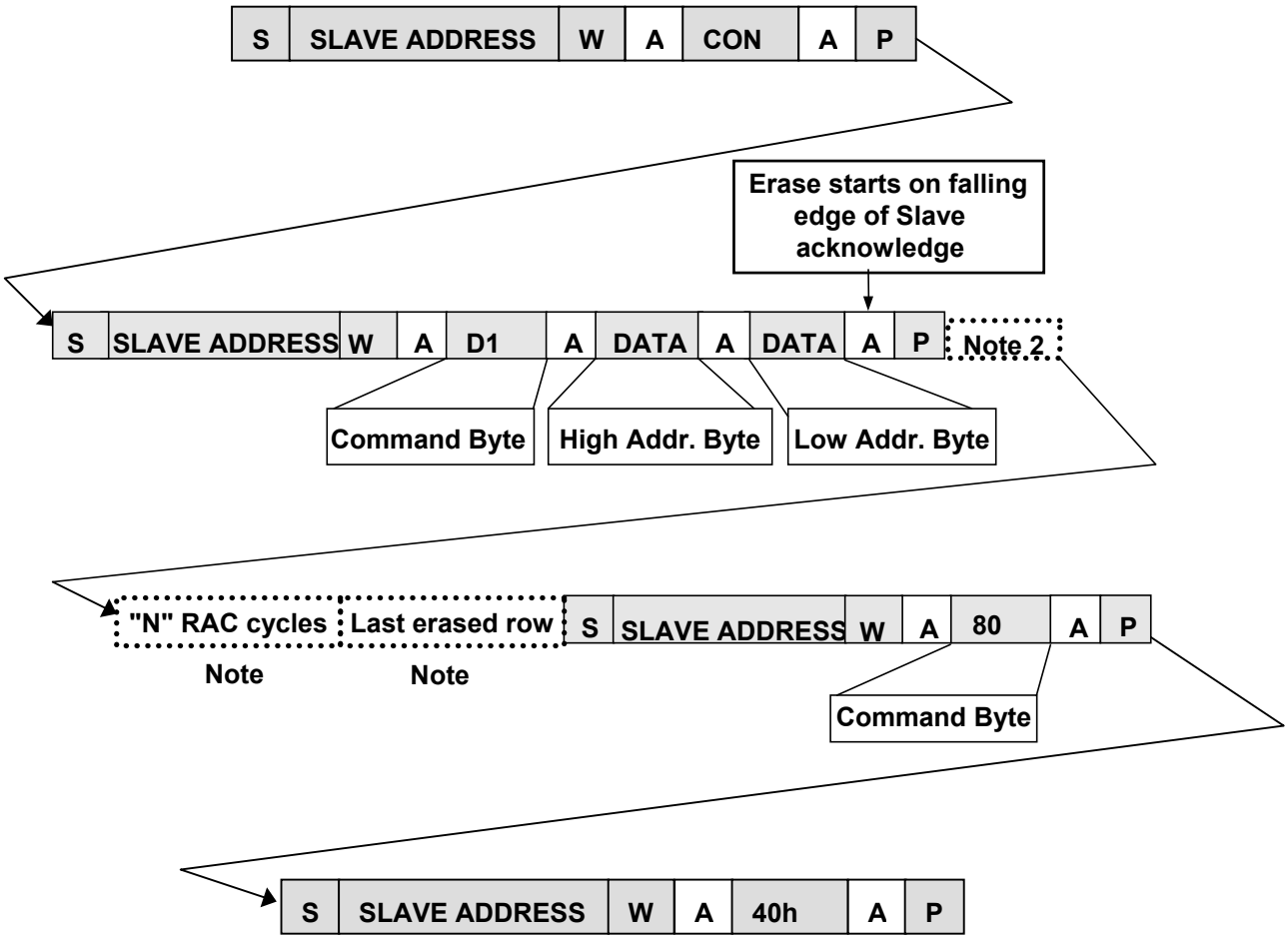
Notes

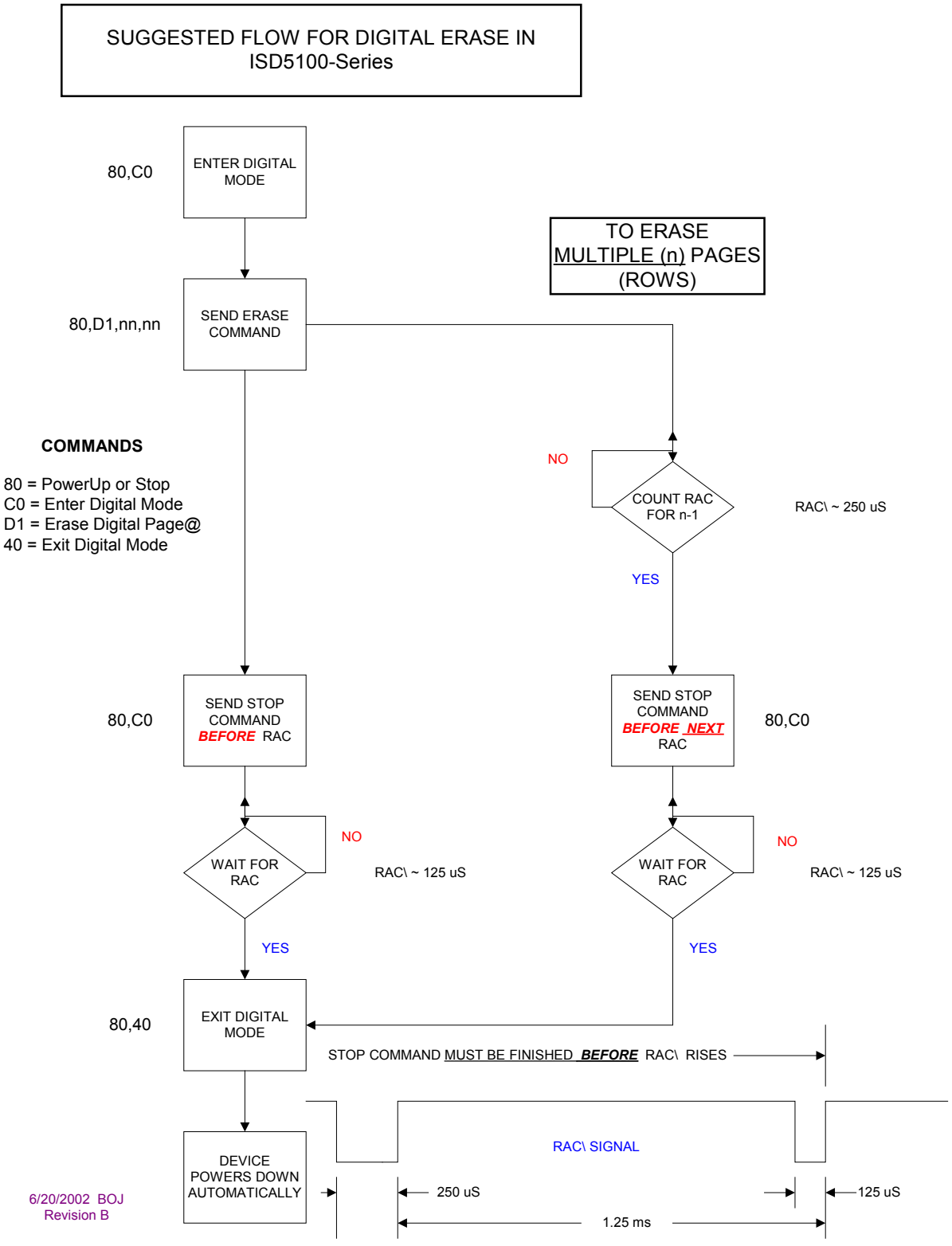
1. Erase operations must be addressed on a Row boundary. The 5 LSB bits of the Low Address Byte will be ignored.

2. I^2C bus is released while erase proceeds. Other devices may use the bus until it is time to execute the STOP command that causes the end of the Erase operation.

3. Host processor must count RAC cycles to determine where the chip is in the erase process, one row per RAC cycle. RAC pulses LOW for 0.25 millisecond at the end of each erased row. The erase of the "next" row begins with the rising edge of RAC. See the Digital Erase RAC timing diagram on page 51.

4. When the erase of the last desired row begins, the following STOP command (Command Byte = 80 hex) must be issued. This command must be completely given, including receiving the ACK from the Slave before the RAC pin goes HIGH at the end of the row.

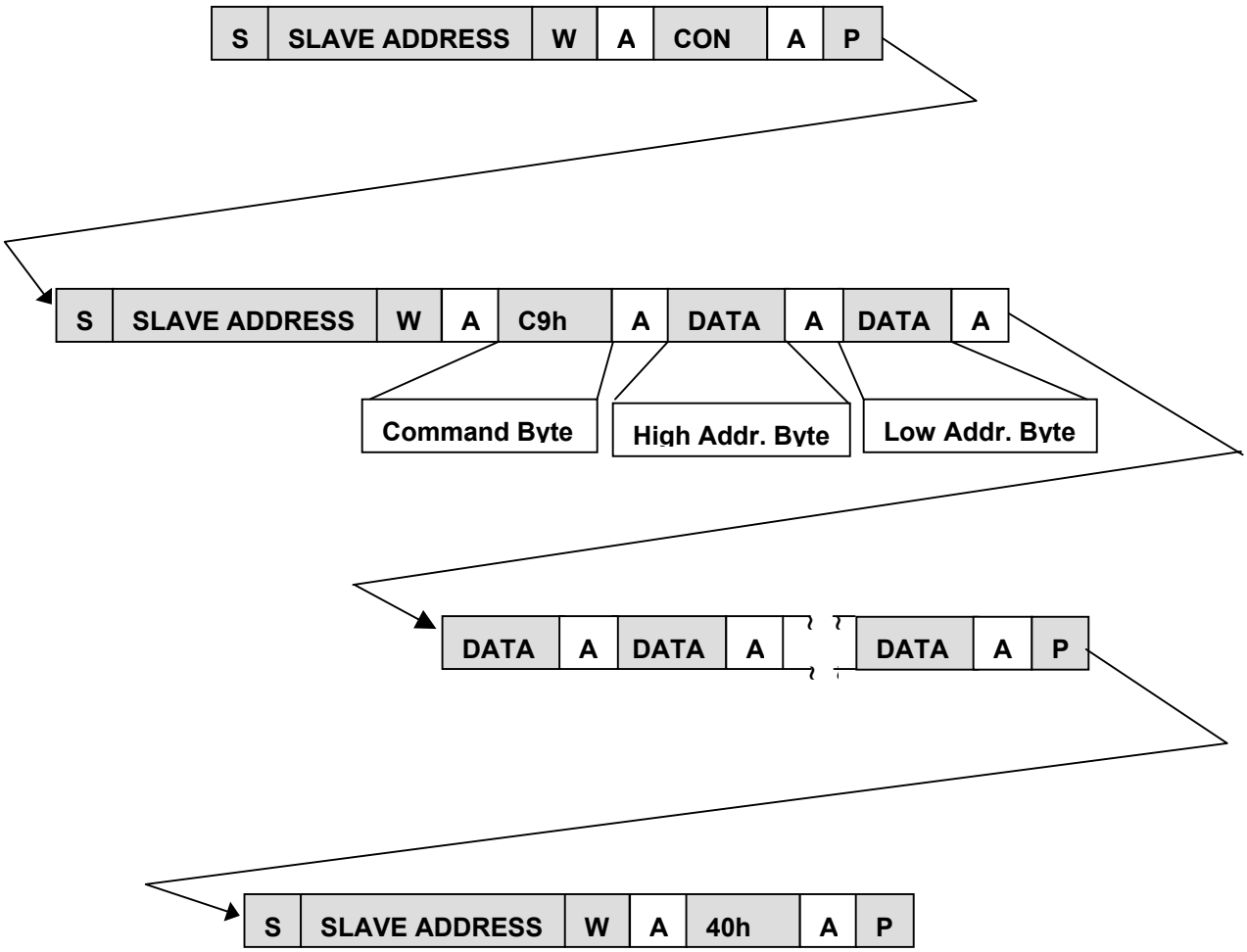

S
SLAVE ADDRESS
W
A
CON
A
P
Erase starts on falling edge of Slave acknowledge
S
SLAVE ADDRESS
W
A
D1
A
DATA
A
DATA
A
P
Note 2
Command Byte
High Addr. Byte
Low Addr. Byte
"N" RAC cycles
Note
Last erased row
Note
S
SLAVE ADDRESS
W
A
80
A
P
Command Byte
S
SLAVE ADDRESS
W
A
40h
A
P


SUGGESTED FLOW FOR DIGITAL ERASE IN ISD5100-Series
80,C0
ENTER DIGITAL MODE
TO ERASE MULTIPLE (n) PAGES (ROWS)
80,D1,nn,nn
SEND ERASE COMMAND
COMMANDS
80 = PowerUp or Stop
C0 = Enter Digital Mode
D1 = Erase Digital Page@
40 = Exit Digital Mode
NO
COUNT RAC FOR n-1
RAC\ ~ 250 uS
YES
80,C0
SEND STOP COMMAND BEFORE RAC
SEND STOP COMMAND BEFORE NEXT RAC
80,C0
NO
WAIT FOR RAC
RAC\ ~ 125 uS
NO
WAIT FOR RAC
RAC\ ~ 125 uS
YES
YES
80,40
EXIT DIGITAL MODE
STOP COMMAND MUST BE FINISHED BEFORE RAC\ RISES
RAC\ SIGNAL
DEVICE POWERS DOWN AUTOMATICALLY
250 uS
125 uS
1.25 ms
6/20/2002 BOJ
Revision B

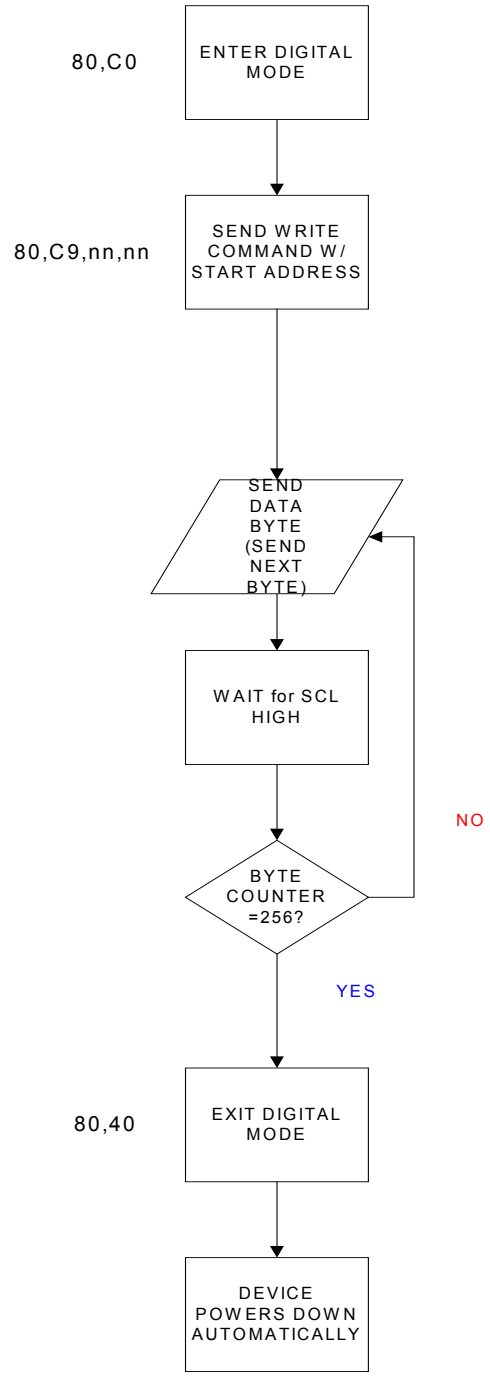
7.5.4.2. Write Digital Data

```
Write
=====

I2CStart
SendByte(0x80)          - Write, Slave address zero
WaitACK
WaitSCLHigh
SendByte(0xc0)          - Enter Digital Mode Command
WaitACK
WaitSCLHigh
I2CStop

I2CStart
SendByte(0x80)          - Write, Slave address zero
WaitACK
WaitSCLHigh
SendByte(0xc9)          - Write Digital Data Command
WaitACK
WaitSCLHigh
SendByte(row/256)       - high address byte
WaitACK
WaitSCLHigh
SendByte(row%256)       - low address byte
WaitACK
WaitSCLHigh

repeat until all data is sent
{
    SendByte(data)      - send data byte
    WaitACK()
    WaitSCLHigh()
}
```

I2CStop
I2CStart
SendByte(0x80) - Write, Slave address zero
WaitACK
WaitSCLHigh
SendByte(0x40) - Exit Digital Mode Command
WaitACK
WaitSCLHigh
I2CStop



SUGGESTED FLOW FOR DIGITAL WRITE IN ISD5100-Series



COMMANDS

80 = PowerUp or Stop
C0 = Enter Digital Mode
C9 = Write Digital Page@
40 = Exit Digital Mode

6/24/2002 BOJ
Revision N/C

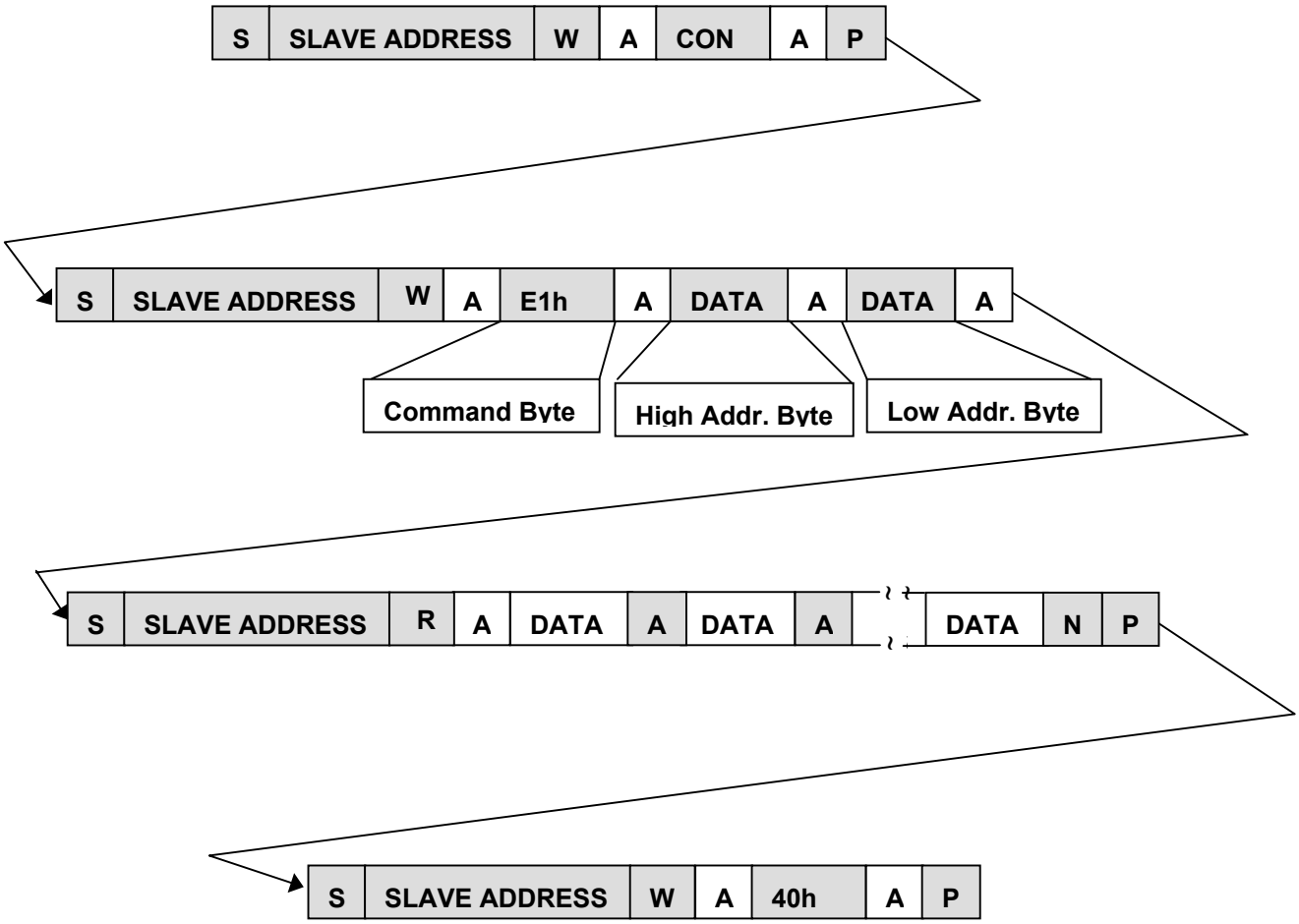
7.5.4.3. Read Digital Data

```
Read
=====

I2CStart
SendByte(0x80)          - Write, Slave address zero
WaitACK
WaitSCLHigh
SendByte(0xc0)          - Enter Digital Mode
WaitACK
WaitSCLHigh
I2CStop

I2CStart
SendByte(0x80)          - Write, Slave address zero
WaitACK
WaitSCLHigh
SendByte(0xe1)          - Read Digital Data Command
WaitACK
WaitSCLHigh
SendByte(row/256)       - high address byte
WaitACK
WaitSCLHigh()
SendByte(row%256)       - low address byte
WaitACK
WaitSCLHigh

I2CStart                - Send repeat start command
SendByte(0x81)          - Read, Slave address zero

repeat until all data is read
{
      data = ReadByte()     - send clocks to read data byte
      SendACK                 - send NACK on the last byte
      WaitSCLHigh             - The only flow control available
```

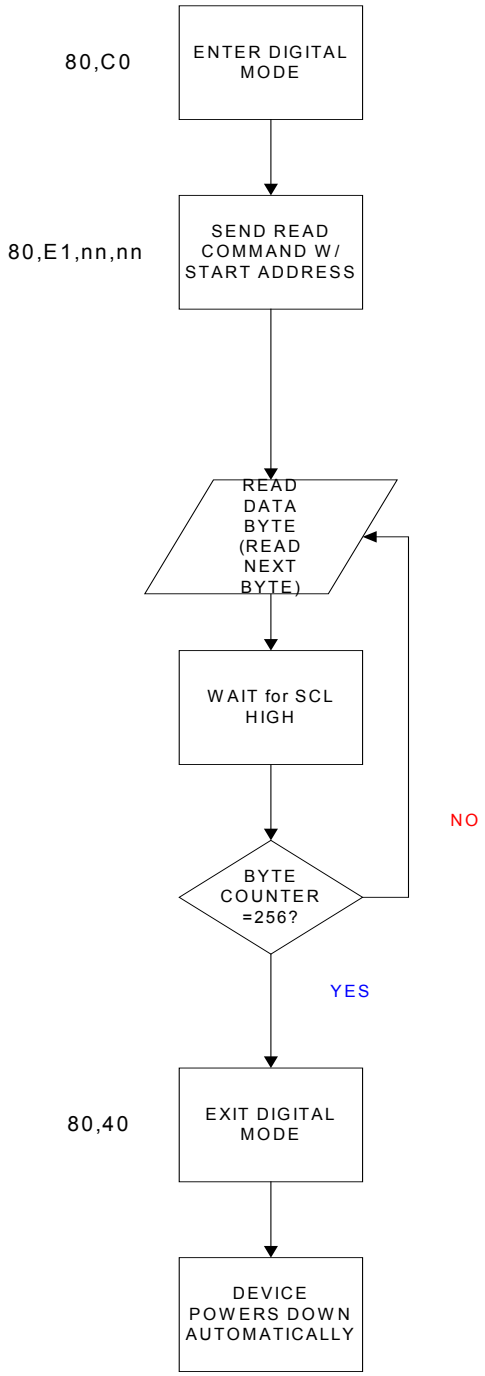
}

I2CStop()

I2CStart
SendByte(0x80) - Write, Slave address zero
WaitACK
WaitSCLHigh
SendByte(0x40) - Exit Digital Mode
WaitACK
WaitSCLHigh
I2CStop



SUGGESTED FLOW FOR DIGITAL READ IN ISD5100-Series



COMMANDS

80 = PowerUp or Stop
C0 = Enter Digital Mode
E1 = Read Digital Page@
40 = Exit Digital Mode

6/24/2002 BOJ
Revision N/C

7.6. PIN DETAILS

7.6.1. Digital I/O Pins

SCL (Serial Clock Line)

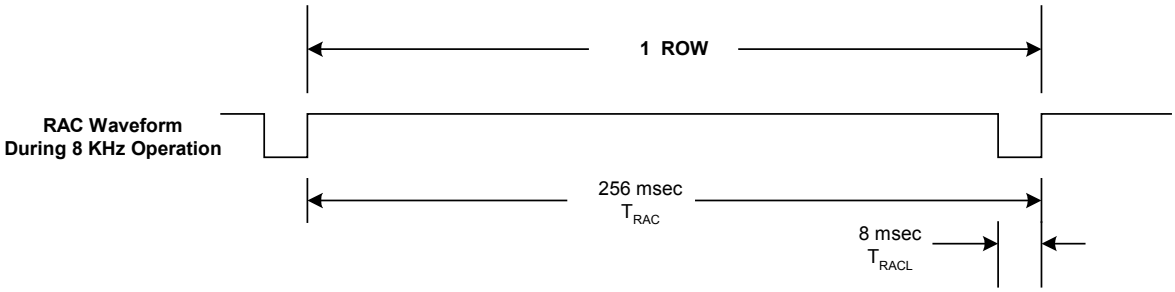
The Serial Clock Line is a bi-directional clock line. It is an open-drain line requiring a pull-up resistor to Vcc. It is driven by the "master" chips in a system and controls the timing of the data exchanged over the Serial Data Line.

SDA (Serial Data Line)

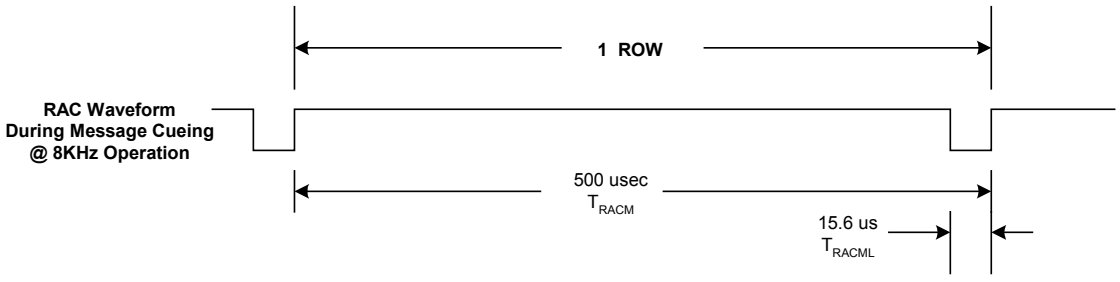
The Serial Data Line carries the data between devices on the I^2C interface. Data must be valid on this line when the SCL is HIGH. State changes can only take place when the SCL is LOW. This is a bi-directional line requiring a pull-up resistor to Vcc.

RAC (Row Address Clock)

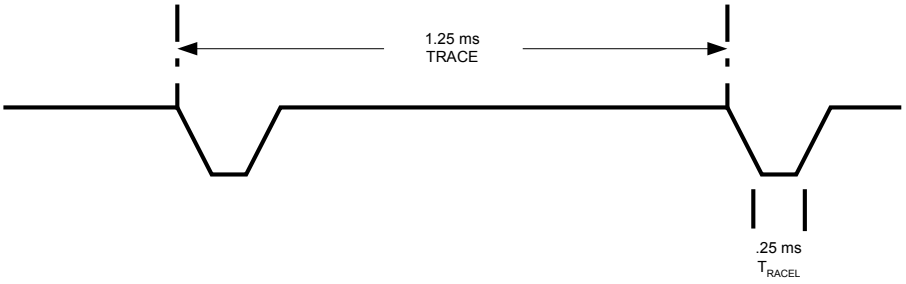
RAC is an open drain output pin that normally marks the end of a row. At the 8 kHz sample frequency, the duration of this period is 256 ms. There are 2048 pages of memory in the ISD5116 devices, 1024 pages in the ISD5108, and 572 pages in the ISD5104. RAC stays HIGH for 248 ms and stays LOW for the remaining 8 ms before it reaches the end of the page.



The RAC pin remains HIGH for 500 µsec and stays LOW for 15.6 µsec under the Message Cueing mode. See the **Timing Parameters table** on page 64 for RAC timing information at other sample rates. When a record command is first initiated, the RAC pin remains HIGH for an extra T_{RACML} period, to load sample and hold circuits internal to the device. The RAC pin can be used for message management techniques.



RAC Waveform During Digital Erase @ 8kHz Operation



$\overline{\text{INT}}$ (Interrupt)

$\overline{\text{INT}}$ is an open drain output pin. The ISD5100-Series interrupt pin goes LOW and stays LOW when an Overflow (OVF) or End of Message (EOM) marker is detected. Each operation that ends in an EOM or OVF generates an interrupt, including the message cueing cycles. The interrupt is cleared by a READ STATUS instruction that will give a status byte out the SDA line.

XCLK (External Clock Input)

The external clock input for the ISD5100-Series product has an internal pull-down device. Normally, the ISD5100-Series are operated at one of four internal rates selected for its internal oscillator by the Sample Rate Select bits. If greater precision is required, the device can be clocked through the XCLK pin at 4.096 MHz as described in section 7.4.3 on page 32.

Because the anti-aliasing and smoothing filters track the Sample Rate Select bits, one must, for optimum performance, maintain the external clock at 4.096 MHz *AND* set the Sample Rate Configuration bits to one of the four values to properly set the filters to the correct cutoff frequency as described in section 7.4.3 on page 32. The duty cycle on the input clock is not critical, as the clock is immediately divided by two internally. If the XCLK is not used, this input should be connected to V_{SSD}.

External Clock Input Table

ISD5116 Duration (Minutes)	ISD5108 Duration (Minutes)	ISD5104 Duration (Minutes)	Sample Rate (kHz)	Required Clock (kHz)	FLD 1	FLD 0	Filter Knee (kHz)
8.73	4.36	2.18	8.0	4096	0	0	3.4
10.9	5.45	2.72	6.4	4096	0	1	2.7
13.1	6.55	3.27	5.3	4096	1	0	2.3
17.5	8.75	4.37	4.0	4096	1	1	1.7

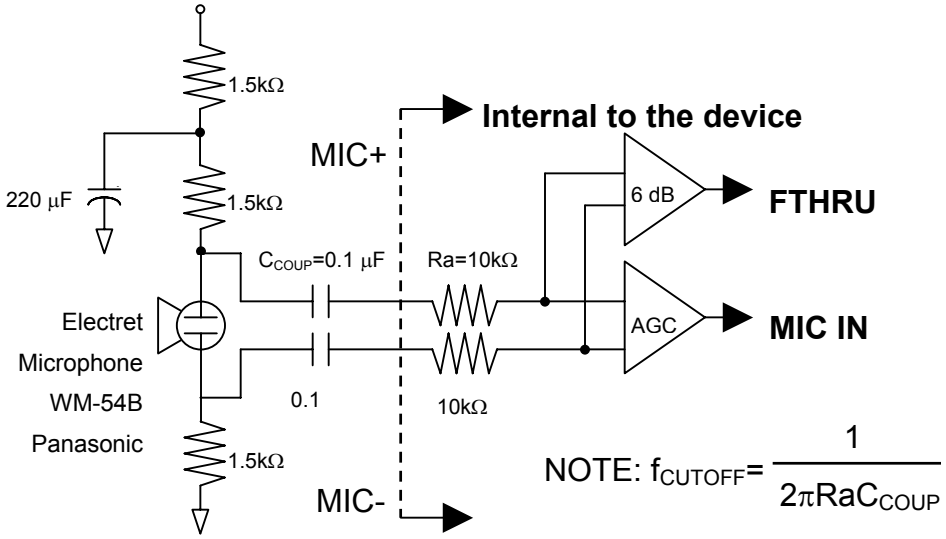
A0, A1 (Address Pins)

These two pins are normally strapped for the desired address that the ISD5100-Series will have on the I^2C serial interface. If there are four of these devices on the bus, then each must be strapped differently in order to allow the Master device to address them individually. The possible addresses range from 80h to 87h, depending upon whether the device is being written to, or read from, by the host. The ISD5100-Series have a 7-bit slave address of which only A0 and A1 are pin programmable. The eighth bit (LSB) is the R/W bit. Thus, the address will be 1000 0xy0 or 1000 0xy1. (See the table in section 7.3.1 on page 13.)

7.6.2. Analog I/O Pins

MIC+, MIC- (Microphone Input +/-)

The microphone input transfers the voice signal to the on-chip AGC preamplifier or directly to the ANA OUT MUX, depending on the selected path. The direct path to the ANA OUT MUX has a gain of 6 dB so a 208 mV p-p signal across the differential microphone inputs would give 416 mV p-p across the ANA OUT pins. The AGC circuit has a range of 45 dB in order to deliver a nominal 694 mV p-p into the storage array from a typical electret microphone output of 2 to 20 mV p-p. The input impedance is typically 10kΩ.



ANA OUT+, ANA OUT- (Analog Output +/-)

This differential output is designed to go to the microphone input of the telephone chip set. It is designed to drive a minimum of 5 kΩ between the "+" and "–" pins to a nominal voltage level of 694 mV p-p. Both pins have DC bias of approximately 1.2 VDC. The AC signal is superimposed upon this analog ground voltage. These pins can be used single-ended, getting only half the voltage. Do **NOT** ground the unused pin.

ACAP (AGC Capacitor)

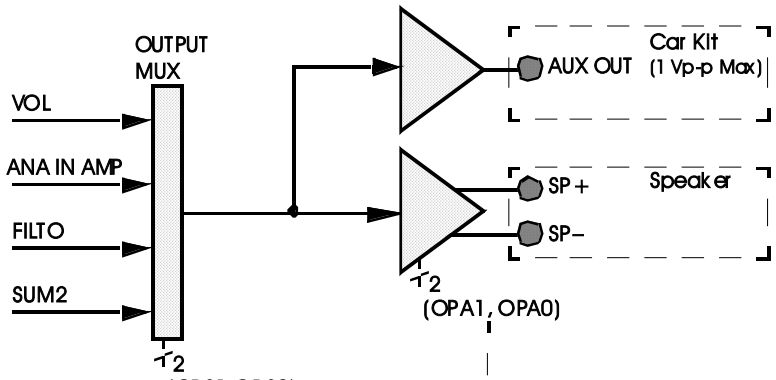
This pin provides the capacitor connection for setting the parameters of the microphone AGC circuit. It should have a 4.7 µF capacitor connected to ground. It cannot be left floating. This is because the capacitor is also used in the playback mode for the AutoMute circuit. This circuit reduces the amount of noise present in the output during quiet pauses. Tying this pin to ground gives maximum gain; tying it to V_{CCA} gives minimum gain for the AGC amplifier but cancels the AutoMute function.

SP +, SP- (Speaker +/-)

This is the speaker differential output circuit. It is designed to drive an 8Ω speaker connected across the speaker pins up to a maximum of 23.5 mW RMS power. This stage has two selectable gains, 1.32 and 1.6, which can be chosen through the configuration registers. These pins are biased to approximately 1.2 VDC and, if used single-ended, must be capacitively coupled to their load. Do **NOT** ground the unused pin.

AUX OUT (Auxiliary Output)

The AUX OUT is an additional audio output pin to be used, for example, to drive the speaker circuit in a "car kit." It drives a minimum load of 5kΩ and up to a maximum of 1V p-p. The AC signal is superimposed on approximately 1.2 VDC bias and must be capacitively coupled to the load.



OPS1	OPS0	SOURCE
0	0	VOL
0	1	ANA IN
1	0	FILTO
1	1	SUM2

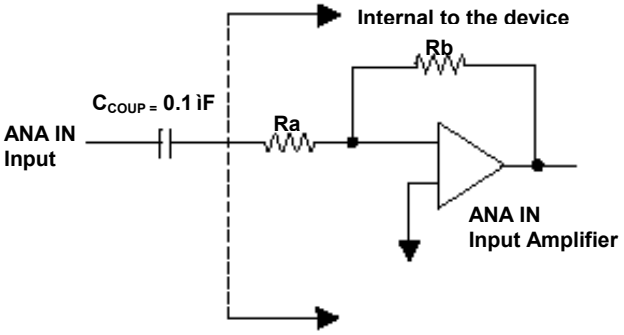
OPS1	OPA0	SPKR DRIVE	AUX OUT
0	0	Power Down	Power Down
0	1	3.6 $V_{p.p}$ @150Ω	Power Down
1	0	23.5 mWatt @ 8Ω	Power Down
1	1	Power Down	1 $V_{p.p}$ Max @ 5KΩ

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
AIG1	AIG0	AIPD	AXG1	AXG0	AXPD	INS0	AOS2	AOS1	AOS0	AOPD	OPS1	OPS0	OPA1	OPA0	VLPD	CFG0

ANA IN (Analog Input)

The ANA IN pin is the analog input from the telephone chip set. It can be switched (by the I^2C interface) to the speaker output, the array input or to various other paths. This pin is designed to accept a nominal 1.11 V p-p when at its minimum gain (6 dB) setting. There is additional gain available, if required, in 3 dB steps, up to 15 dB. The gain settings are controlled from the I^2C interface.

ANA IN Input Modes



NOTE: $f_{CUTTOFF} \quad \frac{1}{2xR_aC_{CCUP}}$

Gain Setting	Resistor Ration (Rb/Ra)	Gain	Gain[2] (dB)
00	63.9 / 102	0.625	-4.1
01	77.9 / 88.1	0.88	-1.1
10	92.3 / 73.8	1.25	1.9
11	106 / 60	1.77	4.9

ANA IN Amplifier Gain Settings

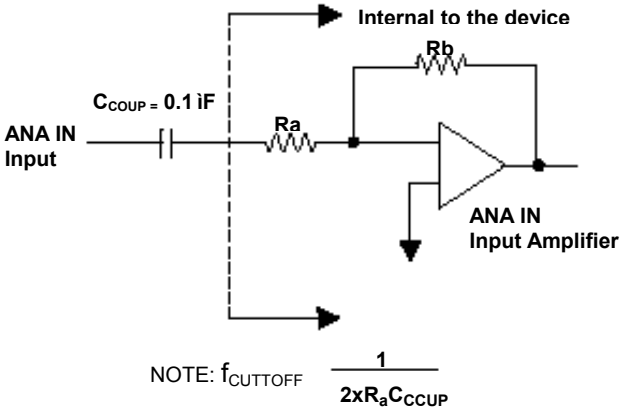
Setting(1)	0TLP Input V_{P-P}(3)	CFG0		Gain(2)	Array In/Out V_{P-P}	Speaker Out V_{P-P}(4)
		AIG1	AIG0			
6 dB	1.110	0	0	0.625	0.694	2.22
9 dB	0.785	0	1	0.883	0.694	2.22
12 dB	0.555	1	0	1.250	0.694	2.22
15 dB	0.393	1	1	1.767	0.694	2.22

1. *Gain from ANA IN to SP+/-*
2. *Gain from ANA IN to ARRAY IN*
3. *0TLP Input is the reference Transmission Level Point that is used for testing. This level is typically 3 dB below clipping*
4. *Speaker Out gain set to 1.6 (High). (Differential)*

AUX IN (Auxiliary Input)

The AUX IN is an additional audio input to the ISD5100-Series, such as from the microphone circuit in a mobile phone "car kit." This input has a nominal 694 mV p-p level at its minimum gain setting (0 dB). See the **AUX IN Amplifier Gain Settings table** on page 56. Additional gain is available in 3 dB steps (controlled by the I^2C interface) up to 9 dB.

AUX IN Input Modes



Gain Setting	Resistor Ratio (Rb/Ra)	Gain	Gain[2] (dB)
00	40.1 / 40.1	1.0	0
01	47.0 / 33.2	1.414	3
10	53.5 / 26.7	2.0	6
11	59.2 / 21	2.82	9

AUX IN Amplifier Gain Settings

Setting[1]	0TLP Input V_{P-P}[3]	CFG0		Gain[2]	Array In/Out V_{P-P}	Speaker Out V_{P-P}[4]
		AIG1	AIG0			
0 dB	0.694	0	0	1.00	0.694	0.694
3 dB	0.491	0	1	1.41	0.694	0.694
6 dB	0.347	1	0	2.00	0.694	0.694
9 dB	0.245	1	1	2.82	0.694	0.694

1. *Gain from AUX IN to ANA OUT*
2. *Gain from AUX IN to ARRAY IN*
3. *0TLP Input is the reference Transmission Level Point that is used for testing. This level is typically 3 dB below clipping*
4. *Differential*

7.6.3. Power and Ground Pins

V_{CCA}, V_{CCD} (Voltage Inputs)

To minimize noise, the analog and digital circuits in the ISD5100-Series devices use separate power busses. These +3 V busses lead to separate pins. Tie the V_{CCD} pins together as close as possible and decouple both supplies as near to the package as possible.

V_{SSA}, V_{SSD} (Ground Inputs)

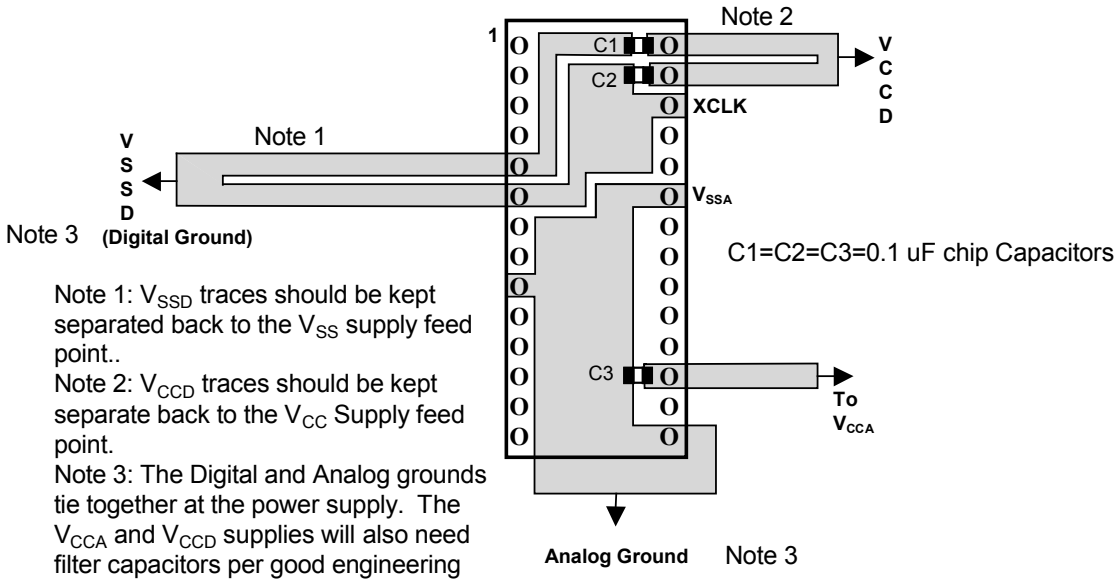
The ISD5100-Series utilizes separate analog and digital ground busses. The analog ground (V_{SSA}) pins should be tied together as close to the package as possible and connected through a low-impedance path to power supply ground. The digital ground (V_{SSD}) pin should be connected through a separate low impedance path to power supply ground. These ground paths should be large enough to ensure that the impedance between the V_{SSA} pins and the V_{SSD} pin is less than 3Ω. The backside of the die is connected to V_{SSD} through the substrate resistance. In a chip-on-board design, the die attach area must be connected to V_{SSD}.

NC (Not Connect)

These pins should not be connected to the board at any time. Connection of these pins to any signal, ground or $V_{CC,}$ may result in incorrect device behavior or cause damage to the device.

7.6.4. Sample PC Layout

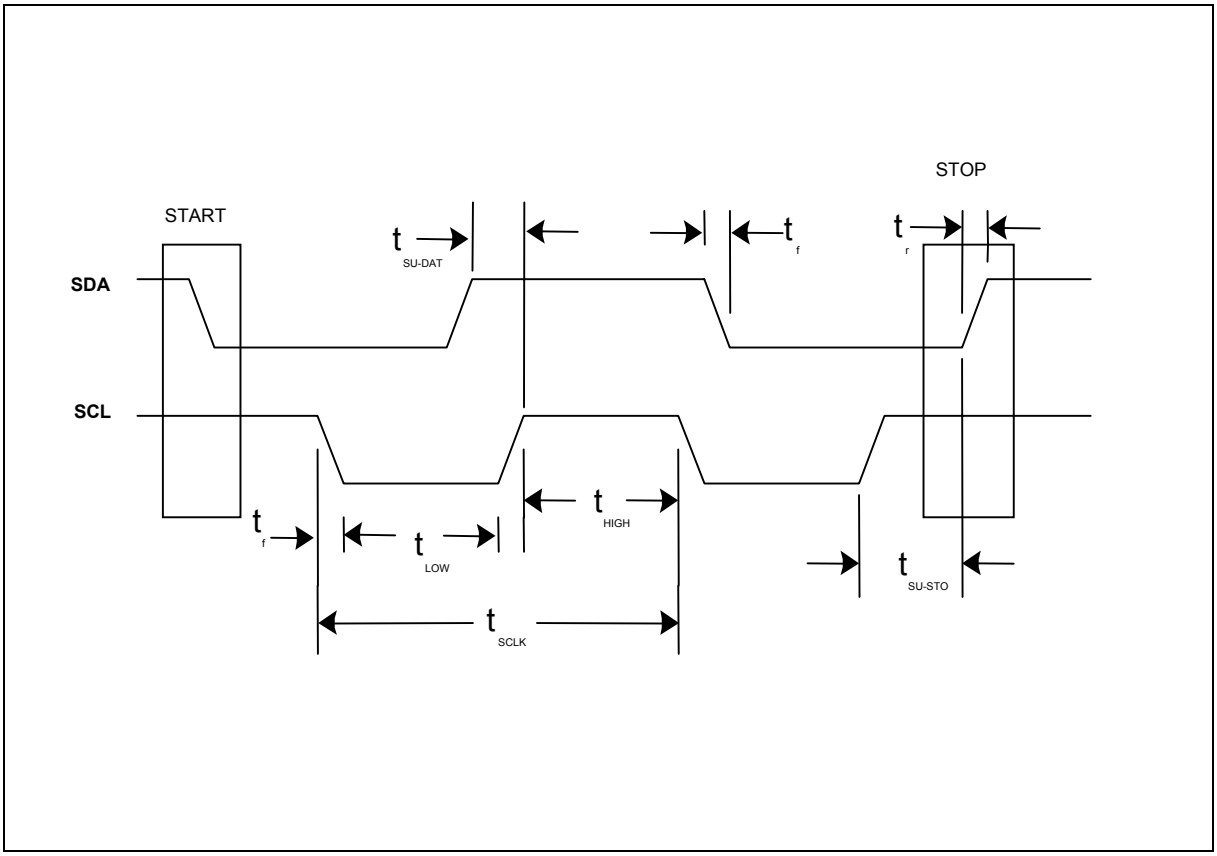
The SOIC package is illustrated from the top. PC board traces and the three chip capacitors are on the bottom side of the board.



Note 1: V_{SSD} traces should be kept separated back to the V_{SS} supply feed point..
Note 2: V_{CCD} traces should be kept separate back to the V_{CC} Supply feed point.
Note 3: The Digital and Analog grounds tie together at the power supply. The V_{CCA} and V_{CCD} supplies will also need filter capacitors per good engineering practice (typ. 50 to 100 uF).

8.TIMING DIAGRAMS

8.1. I²C TIMING DIAGRAM



I^2C INTERFACE TIMING

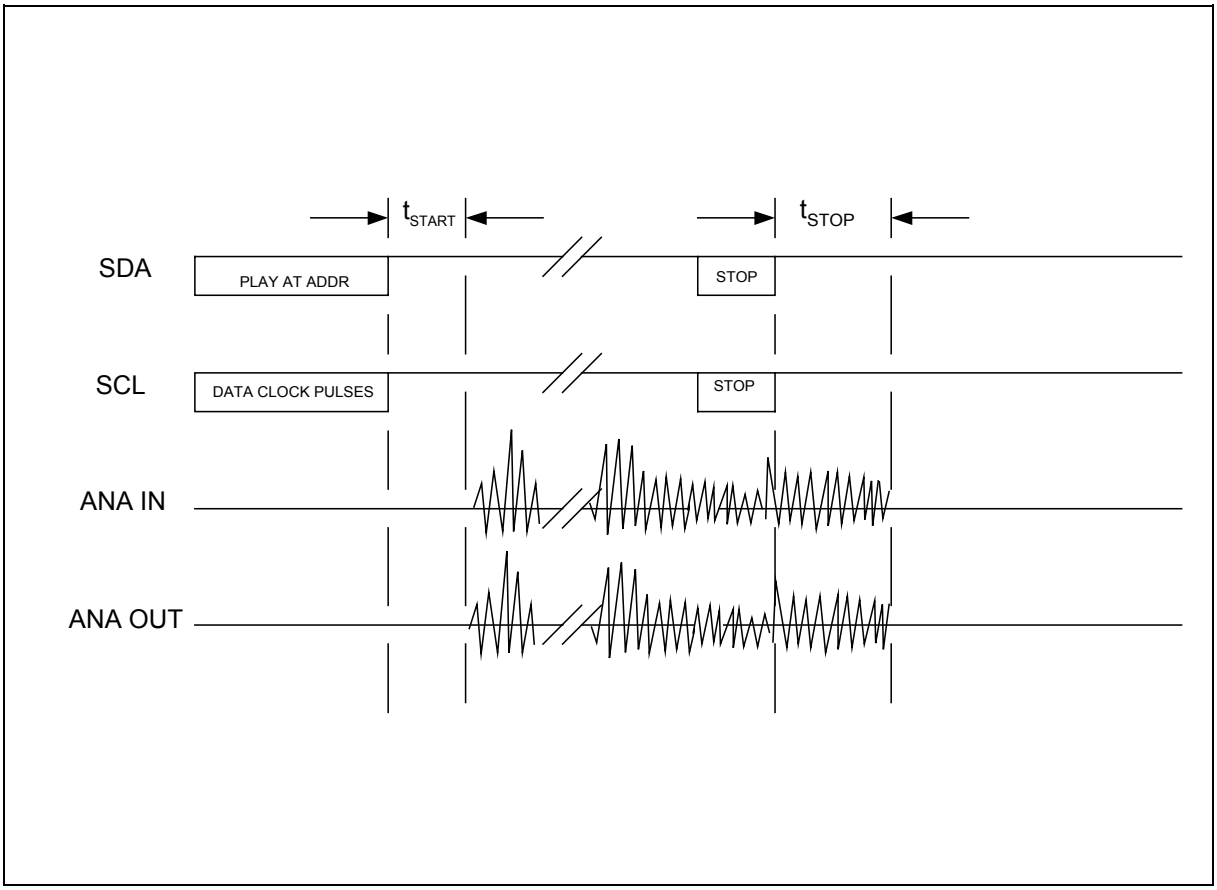
PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		UNIT
		MIN.	MAX.	MIN.	MAX.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	t_{HD-STA}	4.0	-	0.6	-	µs
LOW period of the SCL clock	t_{LOW}	4.7	-	1.3	-	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	-	0.6	-	µs
Set-up time for a repeated START condition	t_{SU-STA}	4.7	-	0.6	-	µs
Data set-up time	t_{SU-DAT}	250	-	100(1)	-	ns
Rise time of both SDA and SCL signals	t_r	-	1000	$20 + 0.1C_b$(2)	300	ns
Fall time of both SDA and SCL signals	t_f	-	300	$20 + 0.1C_b$(2)	300	ns
Set-up time for STOP condition	t_{SU-STO}	4.0	-	0.6	-	µs
Bus-free time between a STOP and START condition	t_{BUF}	4.7	-	1.3	-	µs
Capacitive load for each bus line	C_b	-	400	-	400	pF
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nL}	0.1 V_{DD}	-	0.1 V_{DD}	-	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{nH}	0.2 V_{DD}	-	0.2 V_{DD}	-	V

1. *A Fast-mode I^2C-interface device can be used in a Standard-mode I^2C-interface system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal.*

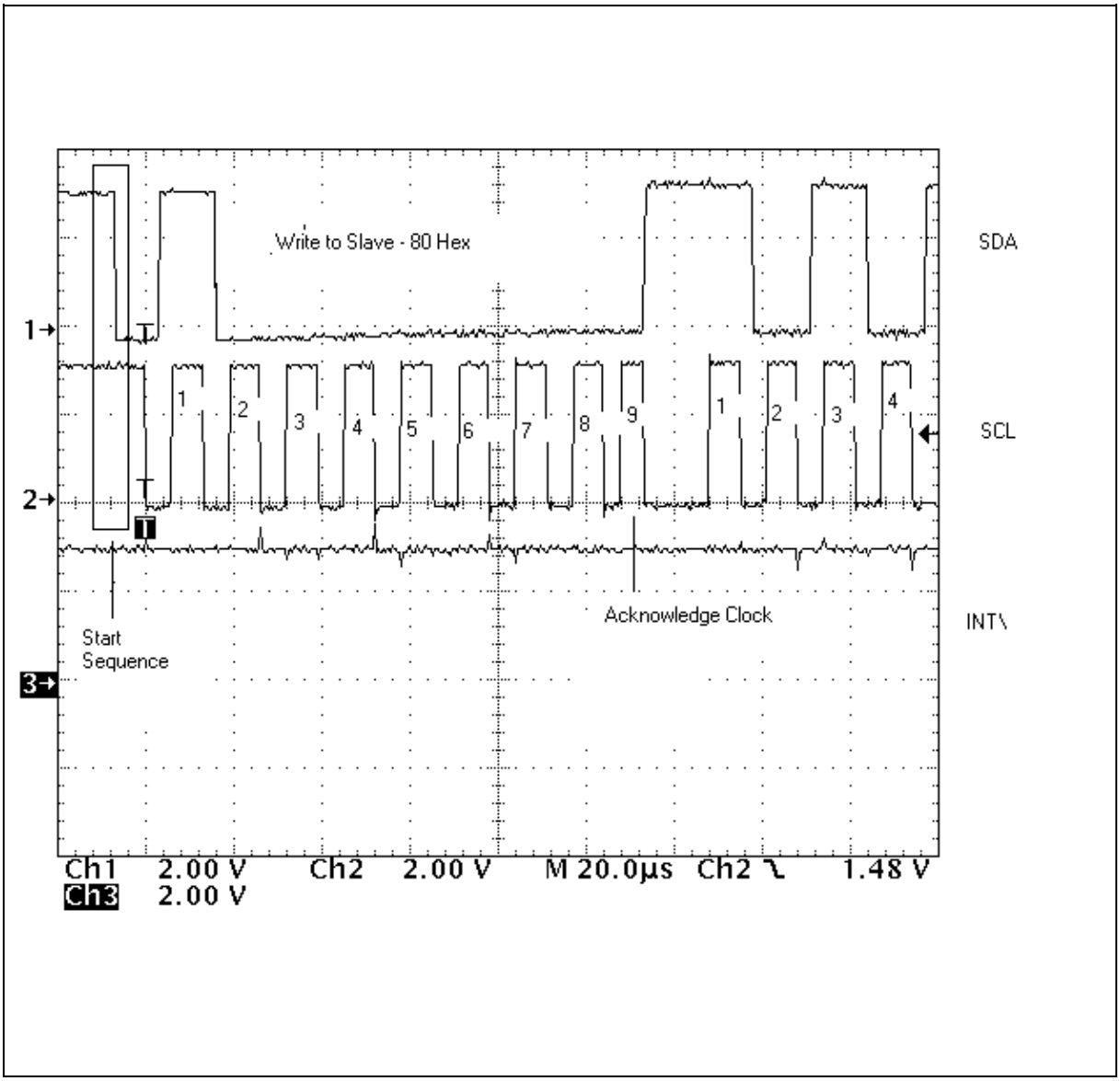
If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line; $t_{r\,max} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-mode I^2C -interface specification) before the SCL line is released.

2. *C_b = total capacitance of one bus line in pF. If mixed with HS mode devices, faster fall-times are allowed.*

8.2. PLAYBACK AND STOP CYCLE



8.3. EXAMPLE OF POWER UP COMMAND (FIRST 12 BITS)



9. ABSOLUTE MAXIMUM RATINGS

ABSOLUTE MAXIMUM RATINGS (PACKAGED PARTS)[1]

Condition	Value
Junction temperature	150^0C
Storage temperature range	-65^0C to $+150^0$C
Voltage Applied to any pin	(V_{SS} - 0.3V) to (V_{CC} + 0.3V)
Voltage applied to any pin (Input current limited to +/-20 mA)	(V_{SS} – 1.0V) to (V_{CC} + 1.0V)
Lead temperature (soldering – 10 seconds)	300^0C
V_{CC} - V_{SS}	-0.3V to +5.5V

1. *Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.*

ABSOLUTE MAXIMUM RATINGS (DIE)[1]

Condition	Value
Junction temperature	150^0C
Storage temperature range	-65^0C to $+150^0$C
Voltage Applied to any pad	(V_{SS} - 0.3V) to (V_{CC} + 0.3V)
V_{CC} - V_{SS}	-0.3V to +5.5V

1. *Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.*

OPERATING CONDITIONS (PACKAGED PARTS)

Condition	Value
Commercial operating temperature range(1)	0^0C to +70^0C
Extended operating temperature(1)	-20^0C to +70^0C
Industrial operating temperature(1)	-40^0C to +85^0C
Supply voltage (V_{CC})(2)	+2.7V to +3.3V
Ground voltage (V_{SS})(3)	0V

1. *Case temperature* 2. $V_{CC} = V_{CCA} = V_{CCD}$ 3. $V_{SS} = V_{SSA} = V_{SSD}$

OPERATING CONDITIONS (DIE)

Condition	Value
Die operating temperature range(1)	0^0C to +50^0C
Supply voltage (V_{CC})(2)	+2.7V to +3.3V
Ground voltage (V_{SS})(3)	0V

1. *Case temperature* 2. $V_{CC} = V_{CCA} = V_{CCD}$ 3. $V_{SS} = V_{SSA} = V_{SSD}$

10. ELECTRICAL CHARACTERISTICS

10.1. GENERAL PARAMETERS

Symbol	Parameters	Min(2)	Typ(1)	Max(2)	Units	Conditions
V_{IL}	Input Low Voltage			V_{CC} x 0.2	V	
V_{IH}	Input High Voltage	V_{CC} x 0.8			V	
V_{OL}	SCL, SDA Output Low Voltage			0.4	V	I_{OL} = 3 µA
V_{IL2V}	Input low voltage for 2V interface			0.4	V	Apply only to SCL, SDA
V_{IH2V}	Input high voltage for 2V interface	1.6			V	Apply only to SCL, SDA
V_{OL1}	RAC, $\overline{INT}$ Output Low Voltage			0.4	V	I_{OL} = 1 mA
V_{OH}	Output High Voltage	V_{CC} – 0.4			V	I_{OL} = -10 µA
I_{CC}	V_{CC} Current (Operating)					
	- Playback		15	25	mA	No Load(3)
	- Record		30	40	mA	No Load(3)
	- Feedthrough		12	15	mA	No Load(3)
I_{SB}	V_{CC} Current (Standby)		1	10	µA	(3)
I_{IL}	Input Leakage Current			+/-1	µA	

1. *Typical values: T_A = 25°C and Vcc = 3.0 V.*
2. *All min/max limits are guaranteed by Winbond via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *V_{CCA} and V_{CCD} summed together.*

10.2. TIMING PARAMETERS

Symbol	Parameters	Min(2)	Typ(1)			Max(2)	Units	Conditions
F_S	Sampling Frequency		8.0				kHz	(5)
			6.4				kHz	(5)
			5.3				kHz	(5)
			4.0				kHz	(5)
F_{CF}	Filter Knee							
	8.0 kHz (sample rate)		3.4				kHz	Knee Point(3)(7)
	6.4 kHz (sample rate)		2.7				kHz	Knee Point(3)(7)
	5.3 kHz (sample rate)		2.3				kHz	Knee Point(3)(7)
	4.0 kHz (sample rate)		1.7				kHz	Knee Point(3)(7)
T_{REC}	Record Duration		ISD5116	ISD5108	ISD5104			
	8.0 kHz (sample rate)		8.73	4.36	2.18		min	(6)
	6.4 kHz (sample rate)		10.9	5.45	2.72		min	(6)
	5.3 kHz (sample rate)		13.1	6.55	3.27		min	(6)
	4.0 kHz (sample rate)		17.5	8.75	4.37		min	(6)
T_{PLAY}	Playback Duration		ISD5116	ISD5108	ISD5104			
	8.0 kHz (sample rate)		8.73	4.36	2.18		min	(6)
	6.4 kHz (sample rate)		10.9	5.45	2.72		min	(6)
	5.3 kHz (sample rate)		13.1	6.55	3.27		min	(6)
	4.0 kHz (sample rate)		17.5	8.75	4.37		min	(6)
T_{PUD}	Power-Up Delay							
	8.0 kHz (sample rate)		1				msec	
	6.4 kHz (sample rate)		1				msec	
	5.3 kHz (sample rate)		1				msec	
	4.0 kHz (sample rate)		1				msec	
T_{STOP} OR $_{PAUSE}$	Stop or Pause Record or Play							
	8.0 kHz (sample rate)		32				msec	
	6.4 kHz (sample rate)		40				msec	
	5.3 kHz (sample rate)		48				msec	
	4.0 kHz (sample rate)		64				msec	
T_{RAC}	RAC Clock Period							
	8.0 kHz (sample rate)		256				msec	(9)

	6.4 kHz (sample rate) 5.3 kHz (sample rate) 4.0 kHz (sample rate)		320 384 512		msec msec msec	(9) (9) (9)
T_{RACL}	RAC Clock Low Time 8.0 kHz (sample rate) 6.4 kHz (sample rate) 5.3 kHz (sample rate) 4.0 kHz (sample rate)		 8 10 12.1 16		 msec msec msec msec	
T_{RACM}	RAC Clock Period in Message Cueing Mode 8.0 kHz (sample rate) 6.4 kHz (sample rate) 5.3 kHz (sample rate) 4.0 kHz (sample rate)		 500 625 750 1000		 µsec µsec µsec µsec	
T_{RACML}	RAC Clock Low Time in Message Cueing Mode 8.0 kHz (sample rate) 6.4 kHz (sample rate) 5.3 kHz (sample rate) 4.0 kHz (sample rate)		 15.6 19.5 23.4 31.2		 µsec µsec µsec µsec	
T_{RACE}	RAC Clock Period in Digital Erase Mode 8.0 kHz (sample rate) 6.4 kHz (sample rate) 5.3 kHz (sample rate) 4.0 kHz (sample rate)		 1.25 1.56 1.87 2.50		 msec msec msec msec	
T_{RACEL}	RAC Clock Low Time in Digital Erase mode 8.0 kHz (sample rate) 6.4 kHz (sample rate) 5.3 kHz (sample rate) 4.0 kHz (sample rate)		 0.25 0.31 0.37 0.50		 msec msec msec msec	
THD	Total Harmonic Distortion ANA IN to ARRAY, ARRAY to SPKR		 1 1	 2 2	 % %	@1 kHz at 0TLP, sample rate = 5.3 kHz

10.3. ANALOG PARAMETERS

MICROPHONE INPUT(14)

Symbol	Parameters	Min(2)	Typ(1)(14)	Max(2)	Units	Conditions
$V_{MIC+/-}$	MIC +/- Input Voltage			300	mV	Peak-to-Peak(4)(8)
$V_{MIC\ (0TLP)}$	MIC +/- input reference transmission level point (0TLP)		208		mV	Peak-to-Peak(4)(10)
A_{MIC}	Gain from MIC +/- input to ANA OUT	5.5	6.0	6.5	dB	1 kHz at $V_{MIC\ (0TLP)}$(4)
$A_{MIC\ (GT)}$	MIC +/- Gain Tracking		+/-0.1		dB	1 kHz, +3 to –40 dB 0TLP Input
R_{MIC}	Microphone input resistance		10		kΩ	MIC- and MIC+ pins
A_{AGC}	Microphone AGC Amplifier Range	6		40	dB	Over 3-300 mV Range

ANA IN(14)

Symbol	Parameters	Min(2)	Typ(1)(14)	Max(2)	Units	Conditions
$V_{ANA\ IN}$	ANA IN Input Voltage			1.6	V	Peak-to-Peak (6 dB gain setting)
$V_{ANA\ IN\ (0TLP)}$	ANA IN (0TLP) Input Voltage		1.1		V	Peak-to-Peak (6 dB gain setting)(10)
$A_{ANA\ IN\ (sp)}$	Gain from ANA IN to SP+/-		+6 to +15		dB	4 Steps of 3 dB
$A_{ANA\ IN\ (AUX\ OUT)}$	Gain from ANA IN to AUX OUT		-4 to +5		dB	4 Steps of 3 dB
$A_{ANA\ IN\ (GA)}$	ANA IN Gain Accuracy	-0.5		+0.5	dB	(11)
$A_{ANA\ IN\ (GT)}$	ANA IN Gain Tracking		+/-0.1		dB	1000 Hz, +3 to –45 dB 0TLP Input, 6 dB setting
$R_{ANA\ IN}$	ANA IN Input Resistance (6 dB to +15 dB)		10 to 100		kΩ	Depending on ANA IN Gain

AUX IN[14]

Symbol	Parameters	Min[2]	Typ[1][14]	Max[2]	Units	Conditions
$V_{AUX\ IN}$	AUX IN Input Voltage			1.0	V	Peak-to-Peak (0 dB gain setting)
$V_{AUX\ IN\ (0TLP)}$	AUX IN (0TLP) Input Voltage		694.2		mV	Peak-to-Peak (0 dB gain setting)
$A_{AUX\ IN\ (ANA\ OUT)}$	Gain from AUX IN to ANA OUT		0 to +9		dB	4 Steps of 3 dB
$A_{AUX\ IN\ (GA)}$	AUX IN Gain Accuracy	-0.5		+0.5	dB	(11)
$A_{AUX\ IN\ (GT)}$	AUX IN Gain Tracking		+/-0.1		dB	1000 Hz, +3 to –45 dB 0TLP Input, 0 dB setting
$R_{AUX\ IN}$	AUX IN Input Resistance		10 to 100		kΩ	Depending on AUX IN Gain

SPEAKER OUTPUTS[14]

Symbol	Parameters	Min[2]	Typ[1][14]	Max[2]	Units	Conditions
V_{SPHG}	SP+/- Output Voltage (High Gain Setting)			3.6	V	Peak-to-Peak, differential load = 150Ω, OPA1, OPA0 = 01
R_{SPLG}	SP+/- Output Load Imp. (Low Gain)	8			Ω	OPA1, OPA0 = 10
R_{SPHG}	SP+/- Output Load Imp. (High Gain)	70	150		Ω	OPA1, OPA0 = 01
C_{SP}	SP+/- Output Load Cap.			100	pF	
V_{SPAG}	SP+/- Output Bias Voltage (Analog Ground)		1.2		VDC	
V_{SPDCO}	Speaker Output DC Offset			+/-100	mV DC	With ANA IN to Speaker, ANA IN AC coupled to V_{SSA}
$ICN_{ANA\ IN/(SP+/-)}$	ANA IN to SP+/- Idle Channel Noise			-65	dB	Speaker Load = 150Ω[12][13]
$C_RT_{(SP+/-)/ANA\ OUT}$	SP+/- to ANA OUT Cross Talk			-65	dB	1 kHz 0TLP input to ANA IN, with MIC+/- and AUX IN AC coupled to V_{SS}, and measured at ANA OUT feed through mode[12]
PSRR	Power Supply Rejection Ratio		-55		dB	Measured with a 1 kHz, 100 mV p-p

						sine wave input at V_{CC} and V_{CC} pins
F_R	Frequency Response (300-3400 Hz)		±0.5		dB	With 0TLP input to ANA IN, 6 dB setting (12) Guaranteed by design
P_{OUTLG}	Power Output (Low Gain Setting)	23.5			mW RMS	Differential load at 8Ω
SINAD	SINAD ANA IN to SP+/-	62.5			dB	0TLP ANA In input minimum gain, 150Ω load (12)(13)

ANA OUT (14)

Symbol	Parameters	Min (2)	Type (1)(14)	Max (2)	Units	Conditions
SINAD	SINAD, MIC IN to ANA OUT	62.5			dB	Load = 5kΩ(12)(13)
SINAD	SINAD, AUX IN to ANA OUT (0 to 9 dB)	62.5			dB	Load = 5kΩ(12)(13)
$ICO_{NIC/ANA\ OUT}$	Idle Channel Noise – Microphone			-65	dB	Load = 5kΩ(12)(13)
$ICN_{AUX\ IN/ANA\ OUT}$	Idle Channel Noise – AUX IN (0 to 9 dB)			-65	dB	Load = 5kΩ(12)(13)
$PSRR_{(ANA\ OUT)}$	Power Supply Rejection Ratio		-40		dB	Measured with a 1 kHz, 100 mV_{P-P} sine wave to V_{CCA}, V_{CCD} pins
V_{BIAS}	ANA OUT+ and ANA OUT-		1.2		VDC	Inputs AC coupled to V_{SSA}
V_{OFFSET}	ANA OUT+ to ANA OUT-			+/- 100	mV DC	Inputs AC coupled to V_{SSA}
R_L	Minimum Load Impedance	5			kΩ	Differential Load
F_R	Frequency Response (300-3400 Hz)		±0.5		dB	0TLP input to MIC+/- in feedthrough mode. 0TLP input to AUX IN in feedthrough mode(12)
$CRT_{ANA\ OUT/(SP+/-)}$	ANA OUT to SP+/- Cross Talk			-65	dB	1 kHz 0TLP output from ANA OUT, with ANA IN AC coupled to V_{SSA}, and measured at

						SP+/-[12]
$C_RT_{ANA\ OUT/AUX\ OUT}$	ANA OUT to AUX OUT Cross Talk			-65	dB	1 kHz 0TLP output from ANA OUT, with ANA IN AC coupled to V_{SSA}, and measured at AUX OUT[12]

AUX OUT[14]

Symbol	Parameters	Min[2]	Typ[1(14)]	Max[2]	Units	Conditions
$V_{AUX\ OUT}$	AUX OUT – Maximum Output Swing			1.0	V	5kΩ Load
R_L	Minimum Load Impedance	5			KΩ	
C_L	Maximum Load Capacitance			100	pF	
V_{BIAS}	AUX OUT		1.2		VDC	
SINAD	SINAD – ANA IN to AUX OUT	62.5			dB	0TLP ANA IN input, minimum gain, 5k load[12][13]
$ICN_{(AUX\ OUT)}$	Idle Channel Noise – ANA IN to AUX OUT			-65	dB	Load=5kΩ[12][13]
$C_RT_{AUX\ OUT/ANA\ OUT}$	AUX OUT to ANA OUT Cross Talk			-65	dB	1 kHz 0TLP input to ANA IN, with MIC +/- and AUX IN AC coupled to V_{SSA}, measured at SP+/-, load = 5kΩ. Referenced to nominal 0TLP @ output

VOLUME CONTROL[14]

Symbol	Parameters	Min[2]	Typ[1][14]	Max[2]	Units	Conditions
A_{OUT}	Output Gain		-28 to 0		dB	8 steps of 4 dB, referenced to output
	Tolerance for each step	-1.0		+1.0	dB	ANA IN 1.0 kHz 0TLP, 6 dB gain setting measured differentially at SP+/-

Conditions

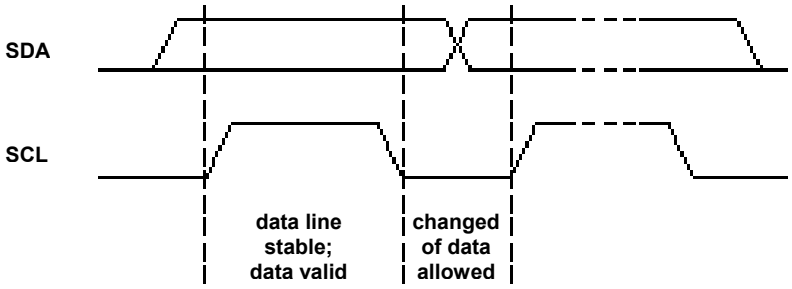
1. *Typical values: T_A = 25°C and Vcc = 3.0V.*
2. *All min/max limits are guaranteed by Winbond via electrical testing or characterization. Not all specifications are 100 percent tested.*
3. *Low-frequency cut off depends upon the value of external capacitors (see Pin Descriptions).*
4. *Differential input mode. Nominal differential input is 208 mV p-p. (0TLP)*
5. *Sampling frequency can vary as much as –6/+4 percent over the industrial temperature and voltage ranges. For greater stability, an external clock can be utilized (see Pin Descriptions).*
6. *Playback and Record Duration can vary as much as –6/+4 percent over the industrial temperature and voltage ranges. For greater stability, an external clock can be utilized (See Pin Descriptions).*
7. *Filter specification applies to the low pass filter.*
8. *For optimal signal quality, this maximum limit is recommended.*
9. *When a record command is sent, T_{RAC} = T_{RAC} + T_{RACL} on the first page addressed.*
10. *The maximum signal level at any input is defined as 3.17 dB higher than the reference transmission level point. (0TLP) This is the point where signal clipping may begin.*
11. *Measured at 0TLP point for each gain setting. See the **ANA IN table** and **AUX IN table** on pages 54 and 55 respectively.*
12. *0TLP is the reference test level through inputs and outputs. See the **ANA IN table** and **AUX IN table** on pages 54 and 55 respectively.*
13. *Referenced to 0TLP input at 1 kHz, measured over 300 to 3,400 Hz bandwidth.*
14. *For die, only typical values are applicable.*

10.4. CHARACTERISTICS OF THE I²C SERIAL INTERFACE

The I²C interface is for bi-directional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the interface bus is not busy.

Bit transfer

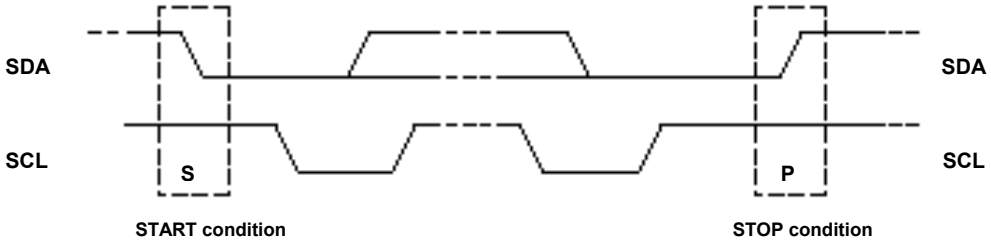
One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse, as changes in the data line at this time will be interpreted as a control signal.



Bit transfer on the I²C-Bus

Start and stop conditions

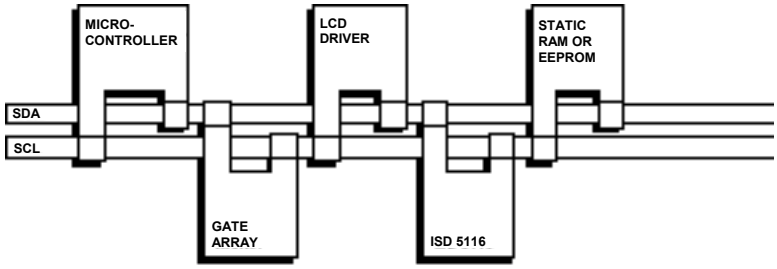
Both data and clock lines remain HIGH when the interface bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).



Definition of START and STOP conditions

System Configuration

A device generating a message is a ‘transmitter’; a device receiving a message is the ‘receiver’. The device that controls the message I sthe ‘master’ and the devices that are controlled by the master are the ‘slaves’.

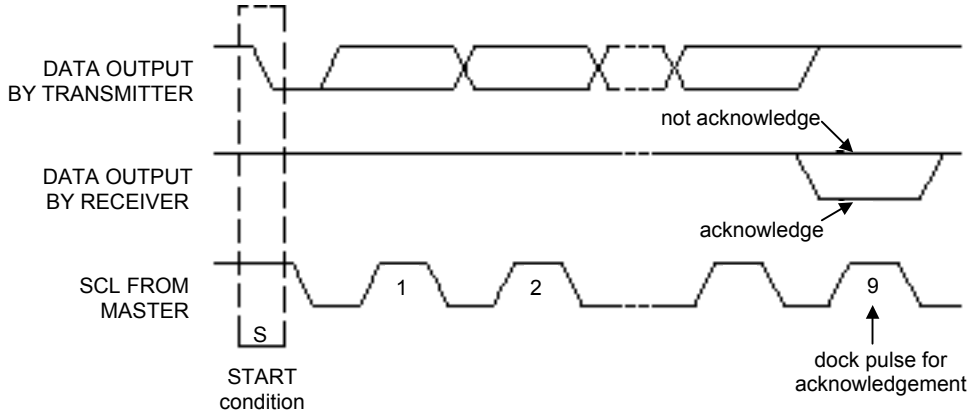


Example of an I²C-bus configuration using two microcontrollers

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the interface bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. In addition, a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a stop condition.



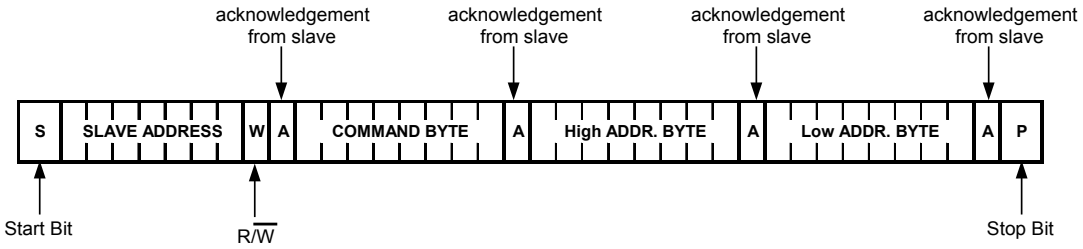
Acknowledge on the I²C-bus

10.5. I²C PROTOCOL

Since the I2C protocol allows multiple devices on the bus, each device must have an address. This address is known as a "Slave Address". A Slave Address consists of 7 bits, followed by a single bit that indicates the direction of data flow. This single bit is 1 for a Write cycle, which indicates the data is being sent from the current bus master to the device being addressed. This single bit is a 0 for a Read cycle, which indicates that the data is being sent from the device being addressed to the current bus master. For example, the valid Slave Addresses for the ISD5100-Series device, for both Write and Read cycles, are shown in section 7.3.1 on page 13 of this datasheet.

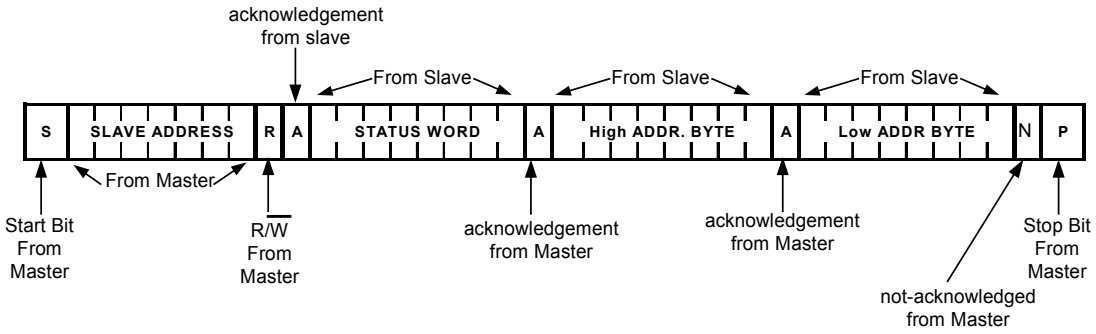
Before any data is transmitted on the I2C interface, the current bus master must address the slave it wishes to transfer data to or from. The Slave Address is always sent out as the 1st byte following the Start Condition sequence. An example of a Master transmitting an address to a ISD5100-Series slave is shown below. In this case, the Master is writing data to the slave and the R/W bit is "0", i.e. a Write cycle. All the bits transferred are from the Master to the Slave, except for the indicated Acknowledge bits. The following example details the transfer explained in section 7.3.1-2-3 on pages 13-20 of this datasheet.

Master Transmits to Slave Receiver (Write) Mode



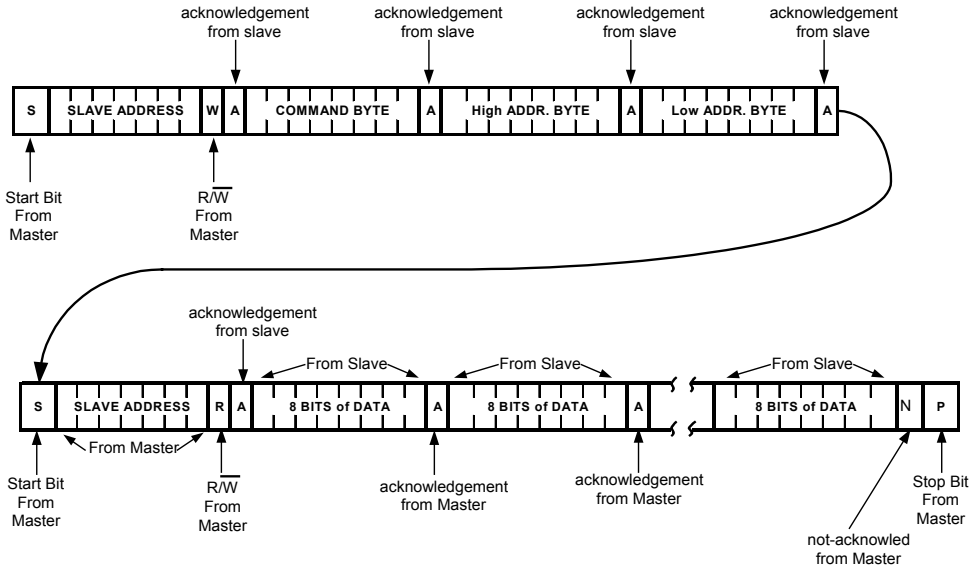
A common procedure in the ISD5100-Series is the reading of the Status Bytes. The Read Status condition in the ISD5100-Series is triggered when the Master addresses the chip with its proper Slave Address, immediately followed by the R/W bit set to a "0" and without the Command Byte being sent. This is an example of the Master sending to the Slave, immediately followed by the Slave sending data back to the Master. The "N" not-acknowledge cycle from the Master ends the transfer of data from the Slave. The following example details the transfer explained in section 7.3.1 on page 13 of this datasheet.

Master Reads from Slave immediately after first byte (Read Mode)



Another common operation in the ISD5100-Series is the reading of digital data from the chip's memory array at a specific address. This requires the I^2C interface Master to first send an address to the ISD5100-Series Slave device, and then receive data from the Slave in a single I^2C operation. To accomplish this, the data direction R/W bit must be changed in the middle of the command. The following example shows the Master sending the Slave address, then sending a Command Byte and 2 bytes of address data to the ISD5100-Series, and then immediately changing the data direction and reading some number of bytes from the chip's digital array. An unlimited number of bytes can be read in this operation. The "N" not-acknowledge cycle from the Master forces the end of the data transfer from the Slave. The following example details the transfer explained in section 7.5.4 on page 47 of this datasheet.

Master Reads from the Slave after setting data address in Slave (Write data address, READ Data)



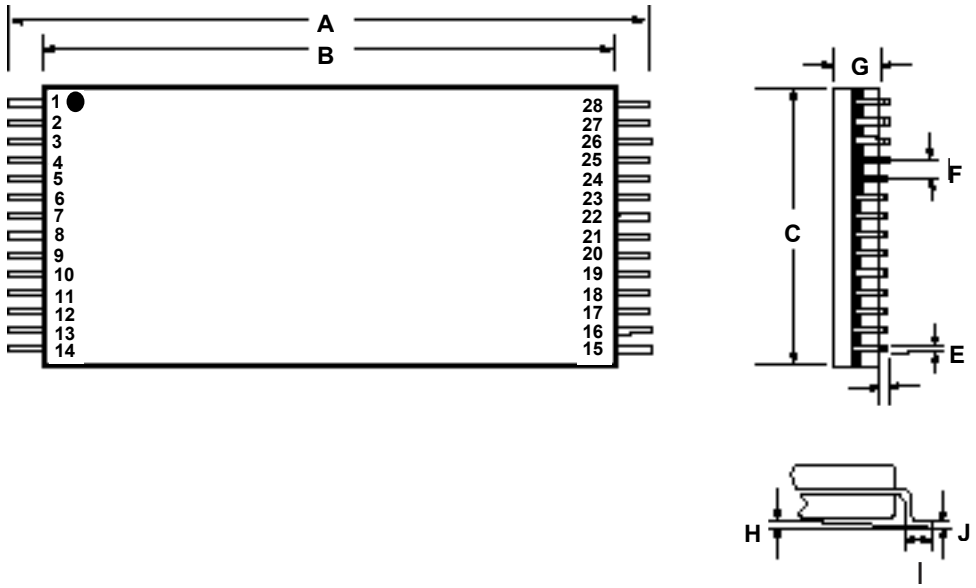
11. TYPICAL APPLICATION CIRCUIT

< To Be Determined >

Please see web site www.winbond-usa.com for updates.

12. PACKAGE SPECIFICATION

12.1. PLASTIC THIN SMALL OUTLINE PACKAGE (TSOP) TYPE 1 DIMENSIONS

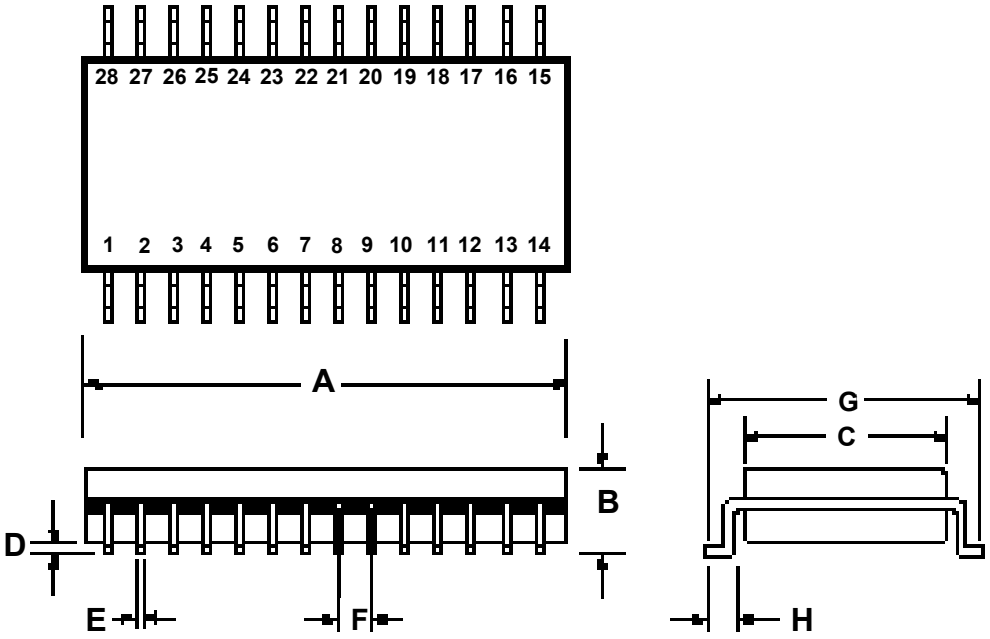


Plastic Thin Small Outline Package (TSOP) Type 1 Dimensions

	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	0.520	0.528	0.535	13.20	13.40	13.60
B	0.461	0.465	0.469	11.70	11.80	11.90
C	0.311	0.315	0.319	7.90	8.00	8.10
D	0.002		0.006	0.05		0.15
E	0.007	0.009	0.011	0.17	0.22	0.27
F		0.0217			0.55	
G	0.037	0.039	0.041	0.95	1.00	1.05
H	0^0	3^0	6^0	0^0	3^0	6^0
I	0.020	0.022	0.028	0.50	0.55	0.70
J	0.004		0.008	0.10		0.21

Note: *Lead coplanarity to be within 0.004 inches.*

12.2. PLASTIC SMALL OUTLINE INTEGRATED CIRCUIT (SOIC) DIMENSIONS

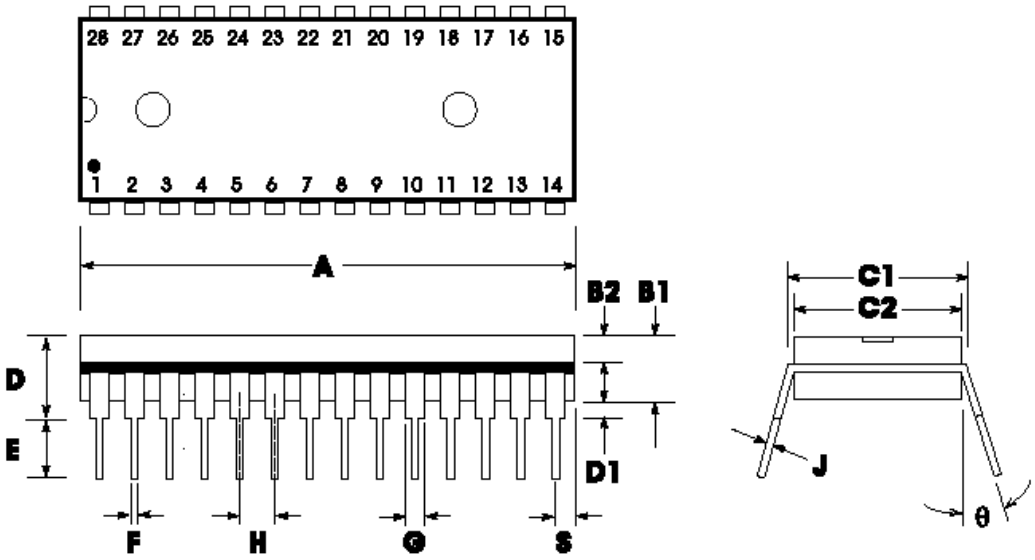


Plastic Small Outline Integrated Circuit (SOIC) Dimensions

	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	0.701	0.706	0.711	17.81	17.93	18.06
B	0.097	0.101	0.104	2.46	2.56	2.64
C	0.292	0.296	0.299	7.42	7.52	7.59
D	0.005	0.009	0.0115	0.127	0.22	0.29
E	0.014	0.016	0.019	0.35	0.41	0.48
F		0.050			1.27	
G	0.400	0.406	0.410	10.16	10.31	10.41
H	0.024	0.032	0.040	0.61	0.81	1.02

Note: *Lead coplanarity to be within 0.004 inches.*

12.3. PLASTIC DUAL INLINE PACKAGE (PDIP) DIMENSIONS



Plastic Dual Inline Package (PDIP) (P) Dimensions

	INCHES			MILLIMETERS		
	Min	Nom	Max	Min	Nom	Max
A	1.445	1.450	1.455	36.70	36.83	36.96
B1		0.150			3.81	
B2	0.065	0.070	0.075	1.65	1.78	1.91
C1	0.600		0.625	15.24		15.88
C2	0.530	0.540	0.550	13.46	13.72	13.97
D			0.19			4.83
D1	0.015			0.38		
E	0.125		0.135	3.18		3.43
F	0.015	0.018	0.022	0.38	0.46	0.56
G	0.055	0.060	0.065	1.40	1.52	1.65
H		0.100			2.54	
J	0.008	0.010	0.012	0.20	0.25	0.30
S	0.070	0.075	0.080	1.78	1.91	2.03
0	0°		15°	0°		15°

12.4 ISD5116 DIE BONDING PHYSICAL LAYOUT

ISD5116 DEVICE PIN/PAD LOCATIONS WITH RESPECT TO DIE CENTER IN MICRON (μm)

PIN	Pin Name	X Axis	Y Axis
V_{SSA}	V_{SS} Analog Ground	1879.45	3848.65
$\overline{RAC}$	Row Address Clock	1536.20	3848.65
$\overline{INT}$	Interrupt	787.40	3848.65
XCLK	External Clock Input	475.60	3848.65
V_{CCD}	V_{CC} Digital Supply Voltage	288.60	3848.65
V_{CCD}	V_{CC} Digital Supply Voltage	73.20	3848.65
SCL	Serial Clock Line	-201.40	3848.65
A1	Address 1	-560.90	3848.65
SDA	Serial Data Address	-818.20	3848.65
A0	Address 0	-1369.40	3848.65
V_{SSD}	V_{SS} Digital Ground	-1671.30	3848.65
V_{SSD}	V_{SS} Digital Ground	-1842.90	3848.65
V_{SSA}	V_{SS} Analog Ground	-1948.00	-3841.60
MIC+	Non-inverting Microphone Input	-1742.20	-3841.60
MIC-	Inverting Microphone Input	-1509.70	-3841.60
ANA OUT+	Non-inverting Analog Output	-1248.00	-3841.60
ANA OUT-	Inverting Analog Output	-913.80	-3841.60
ACAP	AGC/AutoMute Cap	-626.50	-3841.60
SP-	Speaker Negative	-130.70	-3841.60
V_{SSA}	V_{SS} Analog Ground	202.90	-3841.60
SP+	Speaker Positive	626.50	-3841.60
V_{CCA}	V_{CC} Analog Supply Voltage	960.10	-3841.60
ANA IN	Analog Input	1257.40	-3841.60
AUX IN	Auxiliary Input	1523.00	-3841.60
AUX OUT	Auxiliary Output	1767.20	-3841.60

12.5 ISD5108 DIE BONDING PHYSICAL LAYOUT

ISD5108 DEVICE PIN/PAD LOCATIONS WITH RESPECT TO DIE CENTER IN MICRON (μm)

PIN	Pin Name	X Axis	Y Axis
V_{SSA}	V_{SS} Analog Ground	1882.40	2820.65
$\overline{RAC}$	Row Address Clock	1539.15	2820.65
$\overline{INT}$	Interrupt	790.35	2820.65
XCLK	External Clock Input	478.55	2820.65
V_{CCD}	V_{CC} Digital Supply Voltage	291.55	2820.65
V_{CCD}	V_{CC} Digital Supply Voltage	76.15	2820.65
SCL	Serial Clock Line	-198.45	2820.65
A1	Address 1	-557.95	2820.65
SDA	Serial Data Address	-815.25	2820.65
A0	Address 0	-1366.45	2820.65
V_{SSD}	V_{SS} Digital Ground	-1668.35	2820.65
V_{SSD}	V_{SS} Digital Ground	-1839.95	2820.65
V_{SSA}	V_{SS} Analog Ground	-1945.05	-2821.60
MIC+	Non-inverting Microphone Input	-1739.25	-2821.60
MIC-	Inverting Microphone Input	-1506.75	-2821.60
ANA OUT+	Non-inverting Analog Output	-1245.05	-2821.60
ANA OUT-	Inverting Analog Output	-910.85	-2821.60
ACAP	AGC/AutoMute Cap	-623.55	-2821.60
SP-	Speaker Negative	-127.75	-2821.60
V_{SSA}	V_{SS} Analog Ground	205.85	-2821.60
V_{SSA}	V_{SS} Analog Ground	295.85	-2821.60
SP+	Speaker Positive	629.45	-2821.60
V_{CCA}	V_{CC} Analog Supply Voltage	963.05	-2821.60
V_{CCA}	V_{CC} Analog Supply Voltage	1053.05	-2821.60
ANA IN	Analog Input	1260.35	-2821.60
AUX IN	Auxiliary Input	1525.95	-2821.60
AUX OUT	Auxiliary Output	1770.15	-2821.60

12.6 ISD5104 DIE BONDING PHYSICAL LAYOUT

ISD5104 DEVICE PIN/PAD LOCATIONS WITH RESPECT TO DIE CENTER IN MICRON (μm)

PIN	Pin Name	X Axis	Y Axis
V_{SSA}	V_{SS} Analog Ground	TBD	TBD
$\overline{RAC}$	Row Address Clock	TBD	TBD
$\overline{INT}$	Interrupt	TBD	TBD
XCLK	External Clock Input	TBD	TBD
V_{CCD}	V_{CC} Digital Supply Voltage	TBD	TBD
V_{CCD}	V_{CC} Digital Supply Voltage	TBD	TBD
SCL	Serial Clock Line	TBD	TBD
A1	Address 1	TBD	TBD
SDA	Serial Data Address	TBD	TBD
A0	Address 0	TBD	TBD
V_{SSD}	V_{SS} Digital Ground	TBD	TBD
V_{SSD}	V_{SS} Digital Ground	TBD	TBD
V_{SSA}	V_{SS} Analog Ground	TBD	TBD
MIC+	Non-inverting Microphone Input	TBD	TBD
MIC-	Inverting Microphone Input	TBD	TBD
ANA OUT+	Non-inverting Analog Output	TBD	TBD
ANA OUT-	Inverting Analog Output	TBD	TBD
ACAP	AGC/AutoMute Cap	TBD	TBD
SP-	Speaker Negative	TBD	TBD
V_{SSA}	V_{SS} Analog Ground	TBD	TBD
SP+	Speaker Positive	TBD	TBD
V_{CCA}	V_{CC} Analog Supply Voltage	TBD	TBD
ANA IN	Analog Input	TBD	TBD
AUX IN	Auxiliary Input	TBD	TBD
AUX OUT	Auxiliary Output	TBD	TBD

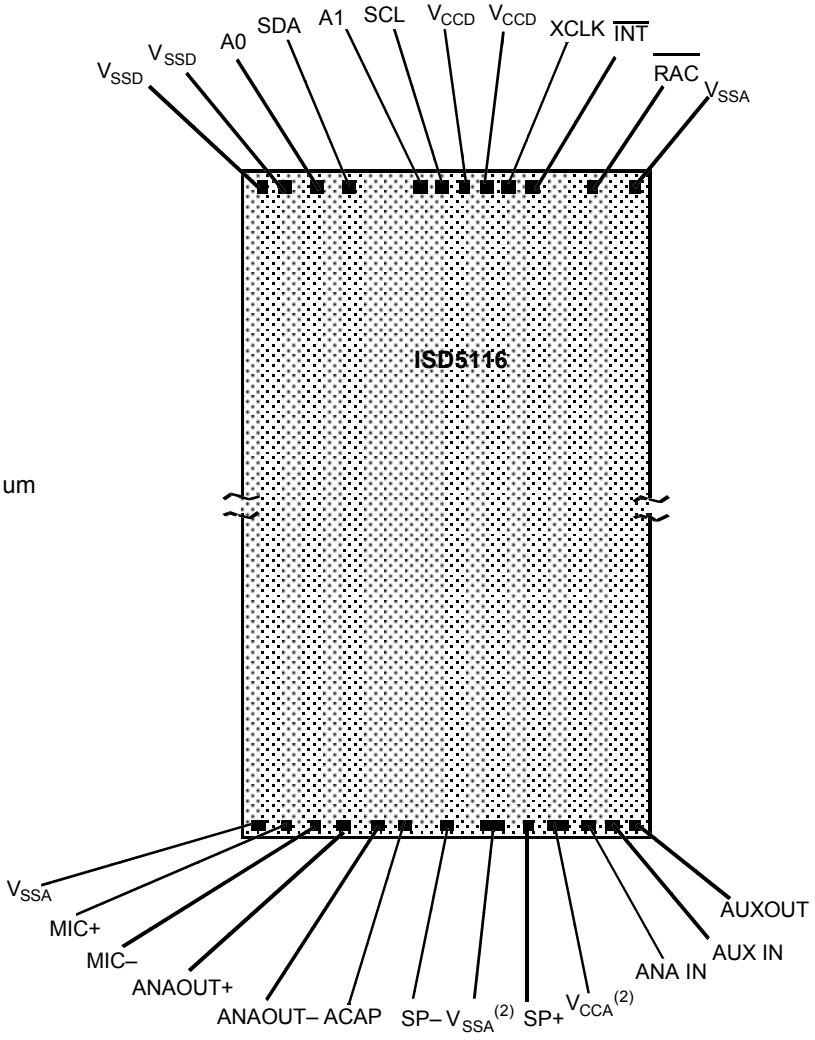
ISD5116 DEVICE BONDING PHYSICAL LAYOUT (1) (UNPACKAGED DIE)

ISD5116 Device

Die Dimensions
X: 4125 um
Y: 8030 um

Die Thickness(3)
292.1 um ± 12.7 um

Pad Opening (min)
90 x 90 microns
3.5 x 3.5 mils



Notes

1. The backside of die is internally connected to Vss. It MUST NOT be connected to any other potential or damage may occur.
2. Double bond recommended.
3. This figure reflects the current die thickness. Please contact Winbond as this thickness may change in the future.

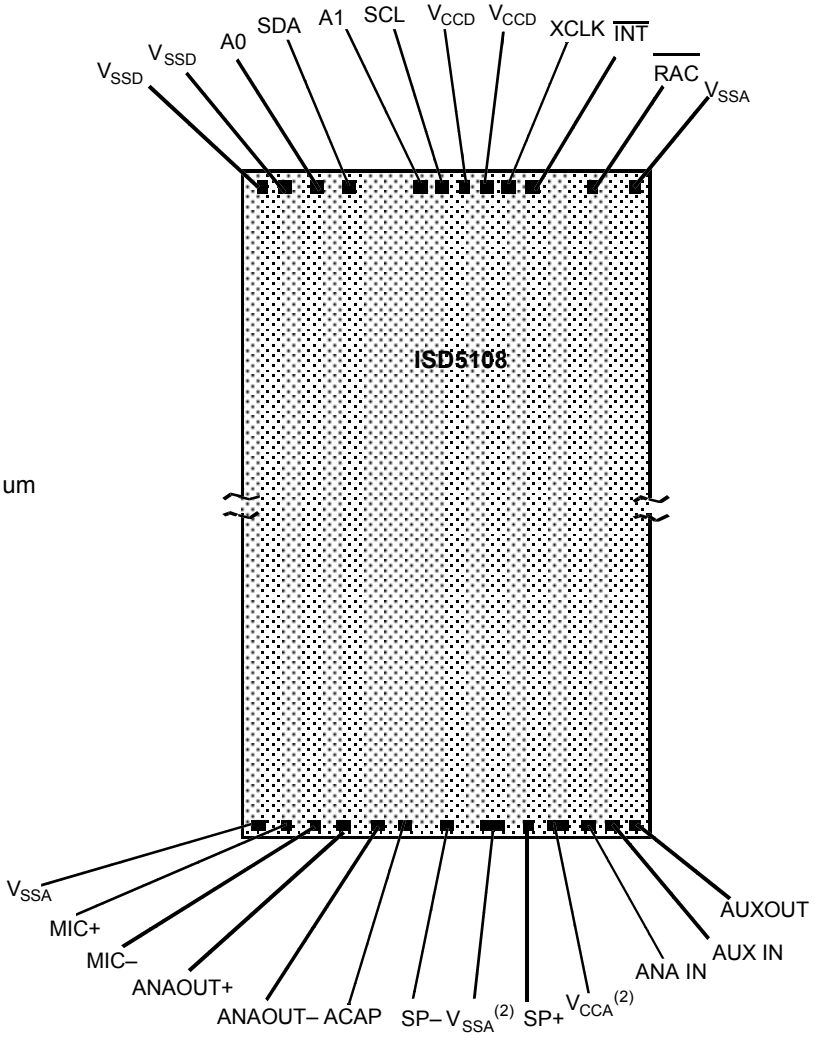
ISD5108 DEVICE BONDING PHYSICAL LAYOUT [1] (UNPACKAGED DIE)

ISD5108 Device

Die Dimensions
X: 4230 um
Y: 6090 um

Die Thickness[3]
292.1 um ± 12.7 um

Pad Opening (min)
90 x 90 microns
3.5 x 3.5 mils



Notes

1. The backside of die is internally connected to Vss. It MUST NOT be connected to any other potential or damage may occur.
2. Double bond recommended.
3. This figure reflects the current die thickness. Please contact Winbond as this thickness may change in the future.

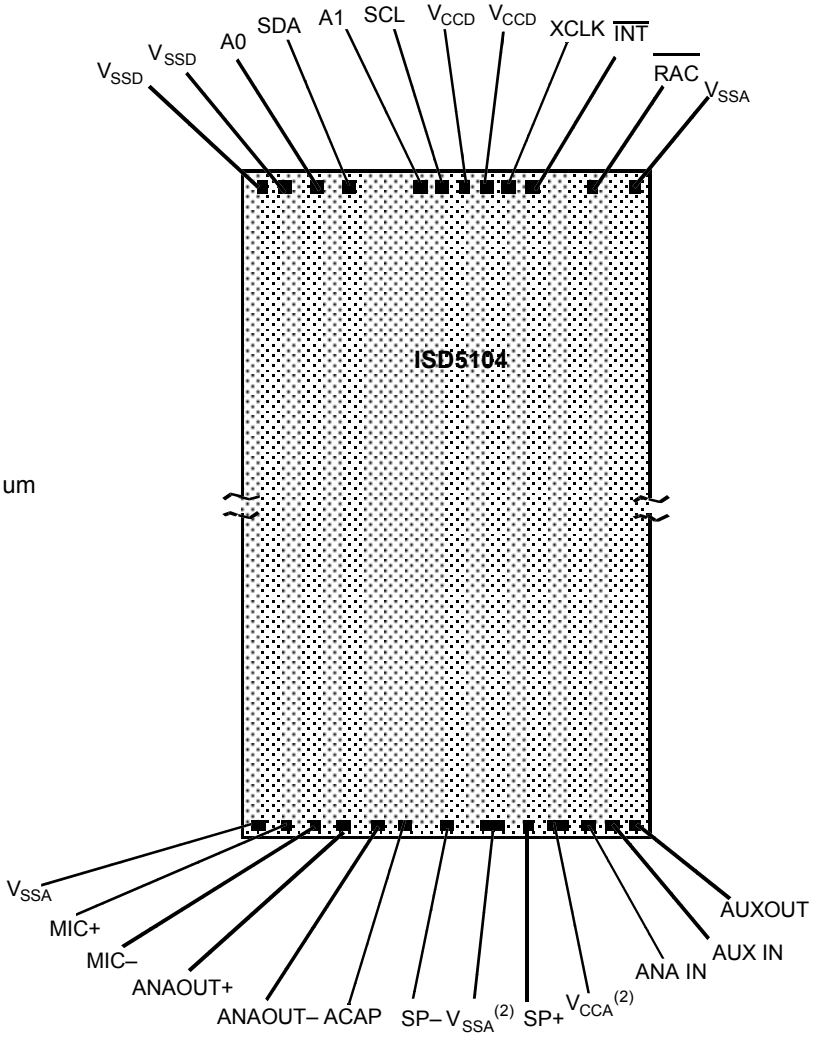
ISD5104 DEVICE BONDING PHYSICAL LAYOUT (1) (UNPACKAGED DIE)

ISD5104 Device

Die Dimensions
X: TBD
Y: TBD

Die Thickness(3)
292.1 um ± 12.7 um

Pad Opening (min)
90 x 90 microns
3.5 x 3.5 mils

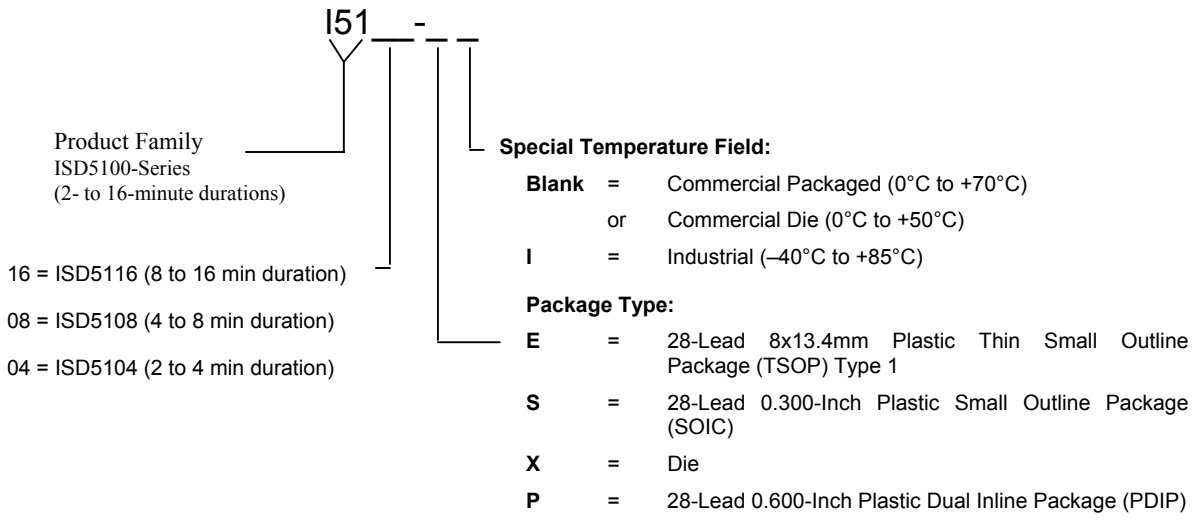


Notes

1. The backside of die is internally connected to Vss. It MUST NOT be connected to any other potential or damage may occur.
2. Double bond recommended.
3. This figure reflects the current die thickness. Please contact Winbond as this thickness may change in the future.

13. ORDERING INFORMATION

Winbond Part Number Description



When ordering ISD5100-Series devices, please refer to the following valid part numbers.

Part Number		
I5116E	I5108E	I5104E
I5116EI	I5108EI	I5104EI
I5116S	I5108S	N/A
I5116SI	I5108SI	N/A
I5116X	I5108X	I5104X
I5116P	N/A	N/A

For the latest product information, access Winbond's worldwide website at
http://www.winbond-usa.com

14. VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
0.1	Mar 2003		New data sheet for the ISD5100-Series

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Headquarters
No. 4, Creation Rd. III
Science-Based Industrial Park,
Hsinchu, Taiwan
TEL: 886-3-5770066
FAX: 886-3-5665577
http://www.winbond.com.tw/

Winbond Electronics Corporation America
2727 North First Street, San Jose,
CA 95134, U.S.A.
TEL: 1-408-9436666
FAX: 1-408-5441798
http://www.winbond-usa.com/

Winbond Electronics (Shanghai) Ltd.
27F, 299 Yan An W. Rd. Shanghai,
200336 China
TEL: 86-21-62365999
FAX: 86-21-62356998

Taipei Office
9F, No. 480, Pueiguang Rd.
Neihu District,
Taipei, 114, Taiwan
TEL: 886-2-81777168
FAX: 886-2-87153579

Winbond Electronics Corporation Japan
7F Daini-ueno BLDG, 3-7-18
Shinyokohama Kohoku-ku,
Yokohama, 222-0033
TEL: 81-45-4781881
FAX: 81-45-4781800

Winbond Electronics (H.K.) Ltd.
Unit 9-15, 22F, Millennium City,
No. 378 Kwun Tong Rd.,
Kowloon, Hong Kong
TEL: 852-27513100
FAX: 852-27552064