19-1100; Rev 0; 6/96

EVALUATION KIT AVAILABLE

MAXIM

8-Bit, 300Msps Flash ADC

General Description

The MAX1125 is a monolithic, flash analog-to-digital converter (ADC) capable of digitizing a 2V analog input signal into 8-bit digital words at a typical 300Msps update rate.

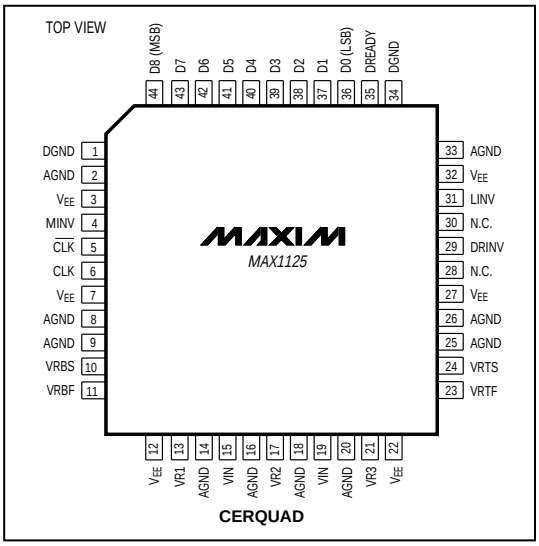
For most applications, no external sample-and-hold is required for accurate conversion due to the device's narrow aperture time, wide bandwidth, and low input capacitance. A single standard -5.2V power supply is required to operate the MAX1125, with nominal 2.2W power dissipation. A special decoding scheme reduces metastable errors to 1LSB.

The part is packaged in a 42-pin ceramic sidebraze that is pin compatible with the CX20116 and CX41396D. The surface-mount 44-pin CERQUAD package allows access to additional reference ladder taps, an overrange bit, and a data-ready output. The pin-compatible 150Msps MAX1114 is also available.

Applications

Digital Oscilloscopes
Transient Capture
Radar, EW, ECM
Direct RF Down-Conversion
Medical Electronics
Ultrasound, CAT Instrumentation

Pin Configurations



CERQUAD

Features

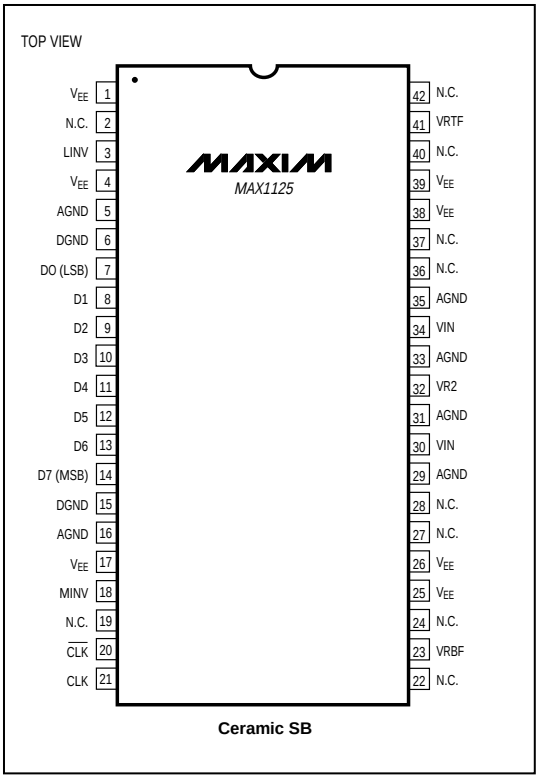
- ♦ **Metastable Errors Reduced to 1LSB**
- ♦ **10pF Input Capacitance**
- ♦ **210MHz Input Bandwidth**
- ♦ **300Msps Conversion Rate**
- ♦ **2.2W Typical Power Dissipation**
- ♦ **Single -5.2V Supply**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSBs)
MAX1125AIDO	-20°C to +85°C	42 Ceramic SB	±0.75
MAX1125BIDO	-20°C to +85°C	42 Ceramic SB	±1
MAX1125AIBH	-20°C to +85°C	44 CERQUAD	±0.75
MAX1125BIBH	-20°C to +85°C	44 CERQUAD	±1

Functional Diagram appears at end of data sheet.

Pin Configurations (continued)



Ceramic SB

ABSOLUTE MAXIMUM RATINGS

Negative Supply Voltage (V_{EE} TO GND) .....-7.0V to +0.5V
Ground Voltage Differential.....-0.5V to +0.5V
Analog Input Voltage .....V_{EE} to +0.5V
Reference Input Voltage.....V_{EE} to +0.5V
Digital Input Voltage .....V_{EE} to +0.5V
Reference Current V_{RTF} to V_{RBF}.....25mA
Digital Output Current .....0mA to -30mA
Operating Temperature Range .....-25°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec). .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, R_{SOURCE} = 50Ω, VRBF = -2.00V, VR2 = -1.00V, VRTF = 0.00V, f_{CLK} = 150MHz, 50% Duty Cycle, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	TEST LEVEL	MAX1125A			MAX1125B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
DC ACCURACY									
Integral Linearity		VI	-0.75	±0.60	+0.75	-0.95	±0.80	+0.95	LSB
Differential Linearity		VI	-0.75		+0.75	-0.95		+0.95	LSB
No Missing Codes			Guaranteed			Guaranteed			
ANALOG INPUT									
Offset Error V_{RT}		IV	-30		+30	-30		+30	mV
Offset Error V_{RB}		IV	-30		+30	-30		+30	mV
Input Voltage Range		VI	-2.0		0.0	-2.0		0.0	V
Input Capacitance	Over full input range	V		10			10		pF
Input Resistance		V		15			15		kΩ
Input Current		VI		250	500		250	500	µA
Input Slew Rate		V		1,000			1,000		V/µs
Large Signal Bandwidth	VIN = full scale	V		210			210		MHz
Small Signal Bandwidth	IN = 500mVp-p	V		335			335		MHz
REFERENCE INPUT									
Ladder Resistance		VI	100	200	300	100	200	300	Ω
Reference Bandwidth		V		10			10		MHz
TIMING CHARACTERISTICS									
Maximum Sample Rate		VI	250	300		250	300		Msps
Clock to Data Delay		V		2.4			2.4		ns
Output Delay TEMPCO		V		2			2		ps/°C
CLK-to-Data Ready Delay (t_D)		V		2.0			2.0		ns
Aperture Jitter		V		5			5		ps
Acquisition Time		V		1.5			1.5		ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{EE} = -5.2V, R_{SOURCE} = 50Ω, VRBF = -2.00V, VR2 = -1.00V, VRTF = 0.00V, f_{CLK} = 150MHz, 50% Duty Cycle, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	TEST LEVEL	MAX1114A MIN	MAX1114A TYP	MAX1114A MAX	MAX1114B MIN	MAX1114B TYP	MAX1114B MAX	UNITS
DYNAMIC PERFORMANCE									
Signal-to-Noise Ratio	F_{IN} = 3.58MHz	VI	45	47		44	46		dB
	F_{IN} = 100MHz	VI	39	42		38	41		
Total Harmonic Distortion	F_{IN} = 3.58MHz	VI	-48	-52		-46	-50		dB
	F_{IN} = 100MHz	VI	-40	-43		-39	-42		
Signal-to-Noise and Distortion (SINAD)	F_{IN} = 3.58MHz	VI	44	46		42	44		dB
	F_{IN} = 100MHz	VI	37	39		35	37		
DIGITAL INPUTS									
Digital Input High Voltage (MINV, LINV)		VI	-1.1		-0.7	-1.1		-0.7	V
Digital Input Low Voltage (MINV, LINV)		VI	-2.0		-1.5	-2.0		-1.5	V
Clock Synchronous Input Currents		V		40			40		µA
Clock Low Width, T_{PWL}		VI	2	1.8		2	1.8		ns
Clock High Width, T_{PWH}		VI	2	1.8		2	1.8		ns
DIGITAL OUTPUTS									
Digital Output High Voltage	50Ω to -2V	VI	-1.1			-1.1			V
Digital Output Low Voltage	50Ω to -2V	VI			-1.5			-1.5	V
POWER-SUPPLY REQUIREMENTS									
Supply Current	T_A = +25 °C	I		425	550		425	550	mA
Power Dissipation	T_A = +25 °C	I		2.2	2.9		2.2	2.9	W

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

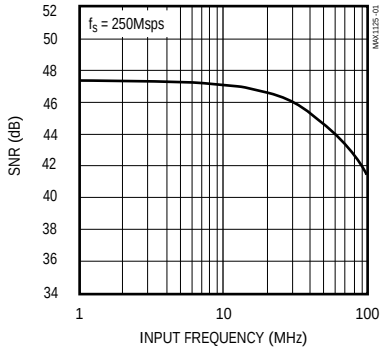
All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed; therefore, T_j = T_C = T_A.

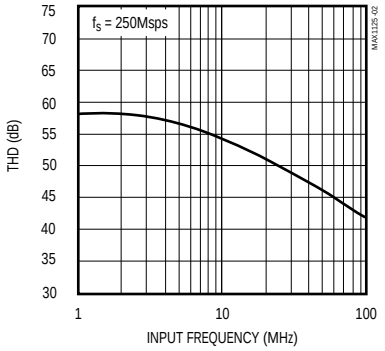
TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = +25°C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = +25°C. Parameter is guaranteed over specified temperature range.

Typical Operating Characteristics

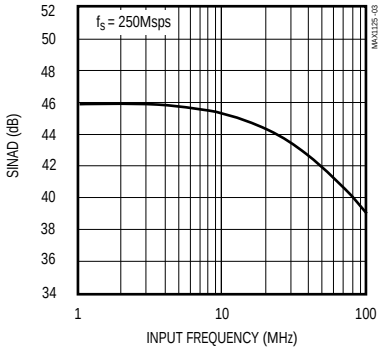
SIGNAL-TO-NOISE RATIO vs. INPUT FREQUENCY



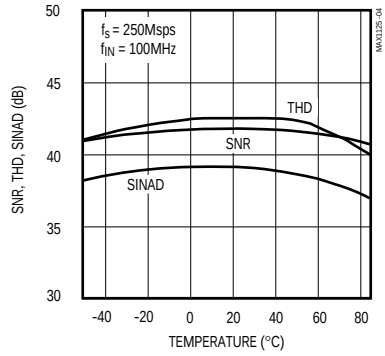
TOTAL HARMONIC DISTORTION vs. INPUT FREQUENCY



SIGNAL-TO-NOISE AND DISTORTION vs. INPUT FREQUENCY



SNR, THD, SINAD vs. TEMPERATURE



Pin Description

PIN		NAME	FUNCTION
Ceramic SB	CERQUAD		
1, 4, 17, 25, 26, 38, 39	3, 7, 12, 22, 27, 32	V_{EE}	Negative Analog Supply (nominally -5.2V)
2, 19, 22, 24, 27, 28, 36, 37, 40, 42	28, 30	N.C.	No Connect. Not internally connected.
3	31	LINV	D0–D6 Output Inversion Control
5, 16, 29, 31, 33, 35	2, 8, 9, 14, 16, 18, 20, 25, 26, 33	AGND	Analog Ground
6, 15	1, 34	DGND	Digital Ground
7	36	D0	Digital Data Output (LSB)
8–13	37–42	D1–D6	Digital Data Output
14	43	D7	Digital Data Output (MSB)
18	4	MINV	D7 Output Inversion Control
—	44	D8	Overrange Output
20	5	$\overline{CLK}$	Inverse ECL Clock Input Pin
21	6	CLK	ECL Clock Input Pin
—	10	VRBS	Reference Voltage Bottom, Sense
23	11	VRBF	Reference Voltage Bottom, Force
30, 34	15, 19	VIN	Analog Input. Can be connected to the input signal or used as a sense.
—	13	VR1	Reference Voltage Tap 1 (typically -1.5V)
32	17	VR2	Reference Voltage Tap 2 (typically -1V)
—	21	VR3	Reference Voltage Tap 3 (typically -0.5V)
41	23	VRTF	Reference Voltage Top, Force
—	24	VRTS	Reference Voltage Top, Sense
—	29	DRINV	Data-Ready Inverse
—	35	DREADY	Data-Ready Output

Detailed Description

The MAX1125 is a 300Msps, monolithic, 8-bit parallel flash analog-to-digital converter (ADC) with an analog bandwidth of over 200MHz. A major advance over previous flash converters is the inclusion of 256 input preamplifiers between the reference ladder and input comparators. (See *Functional Diagram*.) This feature not only reduces clock-transient kickback to the input and reference ladder due to a low AC beta, but also reduces the effect of the dynamic state of the input signal on the latching characteristics of the input comparators. The preamplifiers act as buffers and stabilize the input capacitance so it remains constant for varying input voltages and frequencies, making the part easier to drive than previous flash converters. The MAX1125 incorporates a special decoding scheme that reduces metastable errors (sparkle codes or flyers) to a maximum of 1LSB.

The MAX1125 has true differential analog and digital data paths from the preamplifiers to the output buffers (Current-Mode Logic) for reducing potential missing codes while rejecting common-mode noise.

Careful layout of the analog circuitry reduces signature errors. Every comparator also has a clock buffer to reduce differential delays and to improve signal-to-noise ratio. The output-drive capability of the device can provide full ECL swings into 50Ω loads.

Typical Interface Circuit

Figure 1 shows the typical interface circuit. The MAX1125 is relatively easy to apply depending on the accuracy needed. Wire-wrap may be employed with careful point-to-point ground connections if desired, but a double-sided PC board with a ground plane on the component side, separated into digital and analog sections, gives the best performance. The converter is bonded-out to place the digital pins on the left side of the package and the analog pins on the right side. Additionally, an RF bead connection through a single point from the analog to digital ground planes reduces ground noise pickup.

Figure 2 (CERQUAD package only) shows the most elaborate method of achieving the least error by correcting for integral nonlinearity, input induced distortion, and power-supply/ground noise. It uses external reference ladder tap connections, an input buffer, and supply decoupling. The function of each pin and external connections to other components is as follows:

V_{EE}, AGND, DGND

V_{EE} is the supply pin with AGND as ground for the device. The power-supply pins should be bypassed as close to the device as possible with at least a 0.01µF ceramic capacitor. A 1µF tantalum should also be used for low-frequency suppression. DGND is the ground for the ECL outputs and should be referenced to the output pulldown voltage and bypassed as shown in Figure 1.

Analog Input VIN

There are two analog input pins that are tied to the same point internally. Either one may be used as an analog input sense and the other for input force. This is convenient for testing the source signal to see if there is sufficient drive capability. The pins can also be tied together and driven by the same source. The MAX1125 is superior to similar devices due to a preamplifier stage before the comparators (Figure 4). This makes the device easier to drive because it has constant capacitance and induces less slew-rate distortion. An optional input buffer may be used.

Clock Inputs CLK, $\overline{CLK}$

The clock inputs are designed to be driven differentially with ECL levels. Because $\overline{CLK}$ is internally biased to -1.3V, the clock may be driven single-ended (Figure 5). $\overline{CLK}$ may be left open, but a 0.01µF bypass capacitor from $\overline{CLK}$ to AGND is recommended. NOTE: System performance may be degraded due to increased noise or jitter.

Output Logic Control MINV, LINV

These are ECL-compatible digital controls for changing the output code from straight binary to two's complement, etc. (Table 1 and Figure 4). Both MINV and LINV are in the logic low (0) state when left open. The high state can be obtained by tying to AGND through a diode or 3.9kΩ resistor.

Table 1. Output Coding

MINV	0	0	1	1
LINV	0	1	0	1
0V	111...11	100...00	011...11	000...00
.	111...10	100...01	011...10	000...01
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
V_{IN} .	100...00	111...11	000...00	011...11
.	011...11	000...00	111...11	100...00
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
.	000...01	011...10	100...01	111...10
-2V	000...00	011...11	100...00	111...11

1: V_{IH}, V_{OH} 0: V_{IL}, V_{OL}

Digital Outputs D0 to D7

The digital outputs can drive ECL levels into 50Ω when pulled down to -2V. When pulled down to -5.2V, the outputs can drive 150Ω to 1kΩ loads.

Reference Inputs VRBF, VR2, VRTF

There are two reference inputs and one external reference voltage tap. These are -2V (VRBF), mid-tap (VR2) and AGND (VRTF). The reference pins can be driven as shown in Figure 1. VR2 should be bypassed to AGND for further noise suppression.

Reference Inputs VRBF, VRBS, VR1, VR2, VR3, VRTF, VRTS (CERQUAD package only)

These are five external reference voltage taps from -2V (VRBF) to AGND (VRTF) that can be used to control integral linearity over temperature. The taps can be driven by

op amps (Figure 2). These voltage level inputs can be bypassed to AGND for further noise suppression, if so desired. VRB and VRT have force and sense pins for monitoring the top and bottom voltage references.

Not Connected (N.C.)

All N.C. pins should be tied to DGND on the left side of the package and to AGND on the right side of the package.

Data Ready and Data Ready Inverse DREADY, DRINV (CERQUAD package only)

The data-ready pin is a flag that goes high or low at the output when data is valid or ready to be received. It is essentially a delay line that accounts for the time necessary for information to be clocked through the MAX1125's decoders and latches. This function is useful for interfacing with high-speed memory. Using the data-ready output to latch the output data ensures minimum setup and hold times. DRINV is a data-ready inverse control pin (Figure 3).

Overrange Input D8 (CERQUAD package only)

When the MAX1125 is in an overrange state, D8 goes high, and all data outputs go high as well. This makes it possible to include the MAX1125 in higher resolution systems.

Operation

The MAX1125 has 256 preamp/comparator pairs that are each supplied with the voltage from VRTF to VRBF divided equally by the resistive ladder as shown in the *Functional Diagram*. This voltage is applied to the positive input of each preamplifier/comparator pair. An analog input voltage applied at VIN is connected to the negative inputs of each preamplifier/comparator pair. The comparator states are then clocked through each comparator's individual clock buffer. When CLK is low, the comparators' master, or input stage, compares the analog input voltage to the respective reference voltage. When CLK changes from low to high, the comparators are latched to the state prior to the clock transition and output logic codes in sequence from the top comparators, closest to VRTF (0V), down to the point where the magnitude of the input signal changes sign (thermometer code). The output of each comparator is then registered into four 64-to-6 bit decoders when CLK changes from high to low. At the output of the decoders is a set of four 7-bit latches that are enabled (track) when CLK changes from high to low. From here, the outputs of the latches are coded into 6 LSBs from 4 columns and 4 columns are coded into 2 MSBs. Next are the MINV and LINV controls for output inversions that consist of a set of eight XOR gates. Finally, 8 ECL output latches and buffers are used to drive the external loads. The conversion takes one clock cycle from the input to the data outputs.

Evaluation Boards

The MAX1114/MAX1125 evaluation kit (EV kit) demonstrates the full performance of the MAX1125. This board includes a voltage reference circuit, clock driver circuit, output data latches and an on-board reconstruction of the digital data. A separate data sheet describing the operation of this board is also available. Contact the factory for price and delivery.

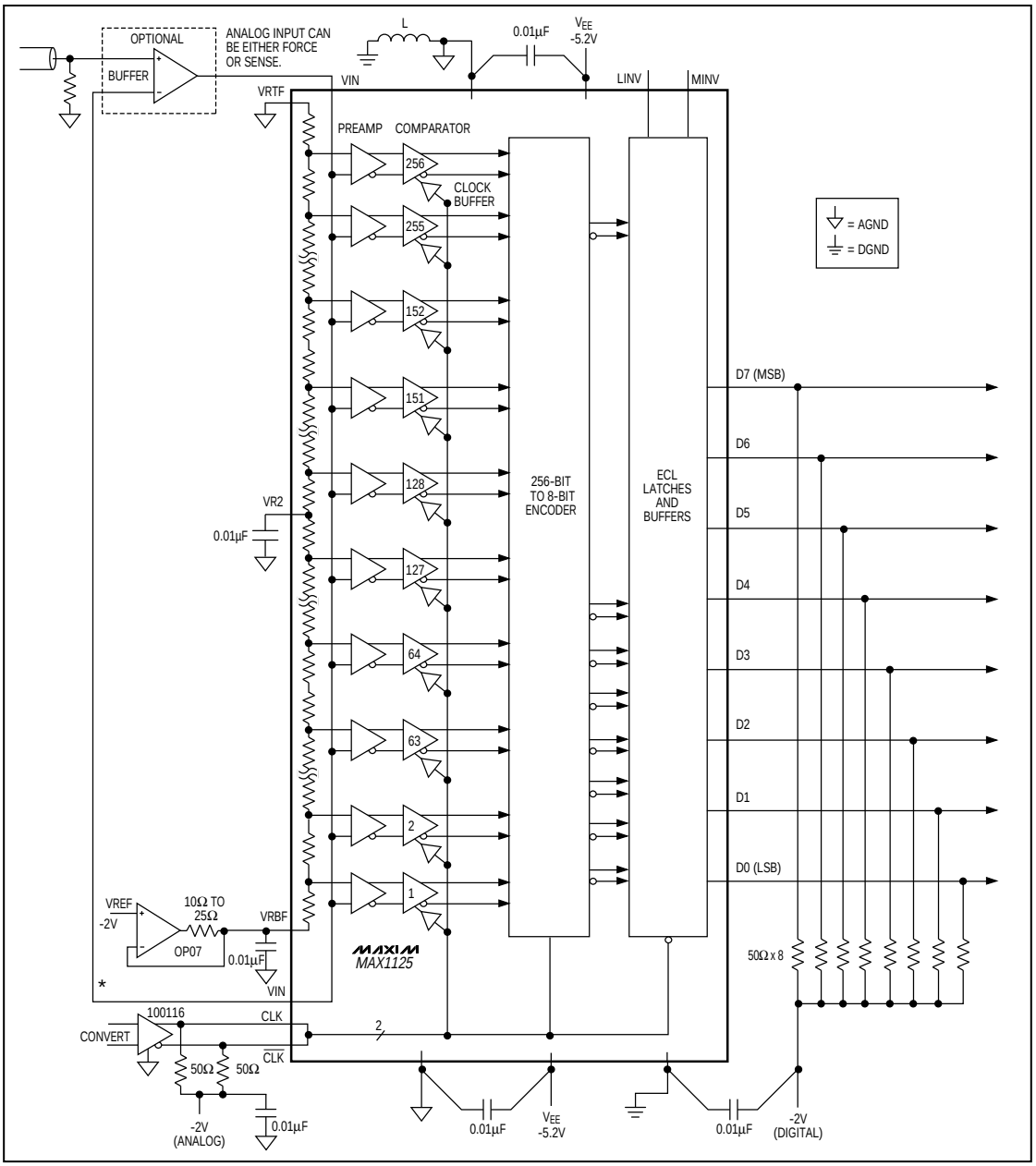


Figure 1. Typical Interface Circuit 1

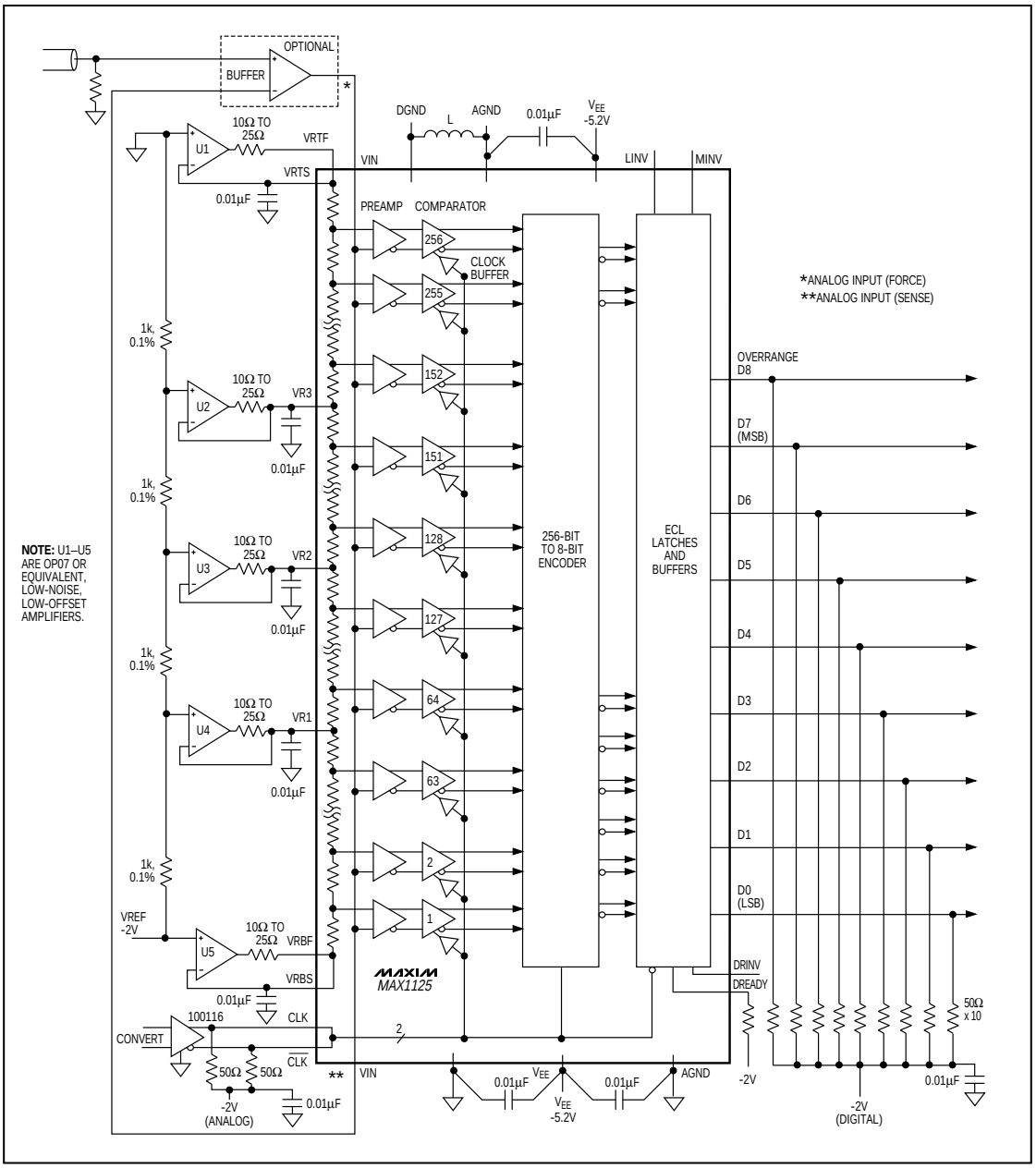


Figure 2. Typical Interface Circuit 2 (CERQUAD package only)

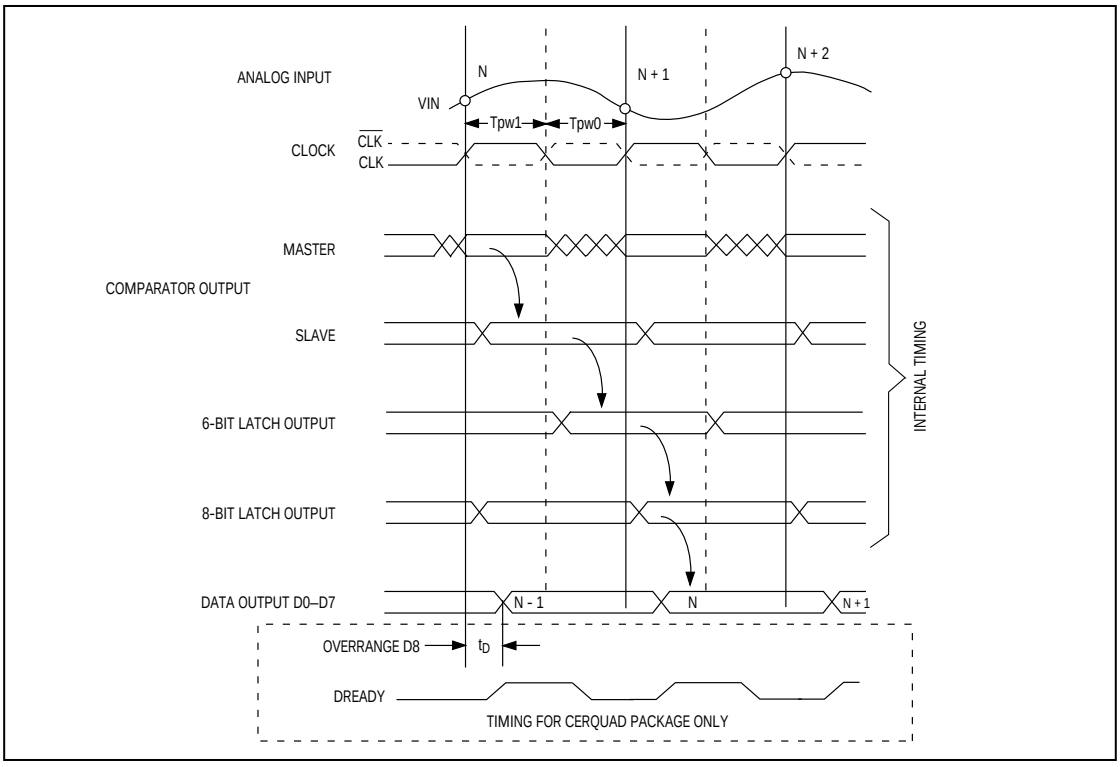


Figure 3. Timing Diagram

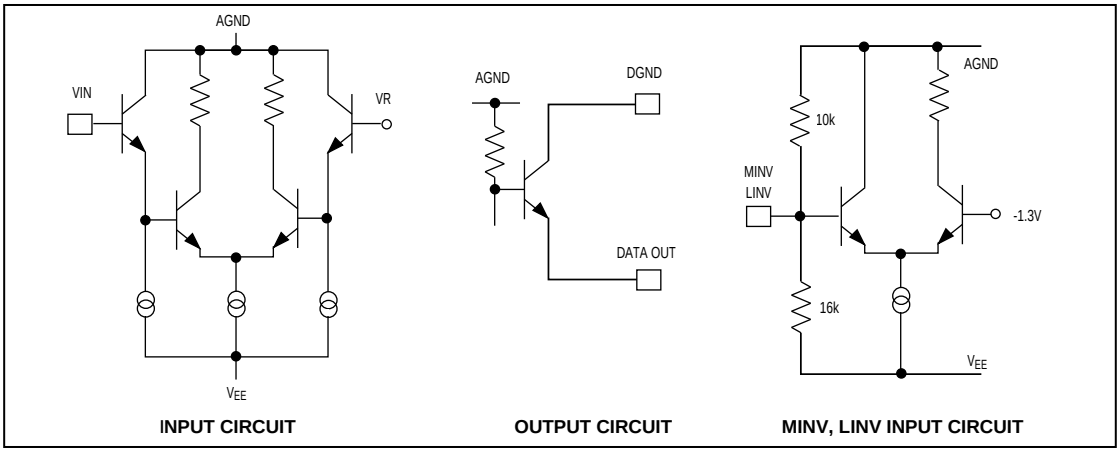


Figure 4. Subcircuit Schematics

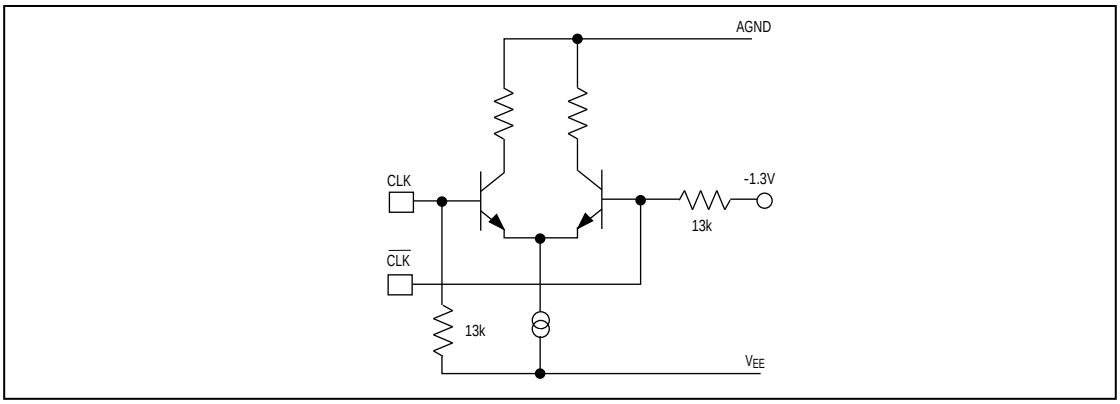


Figure 5. Clock Input

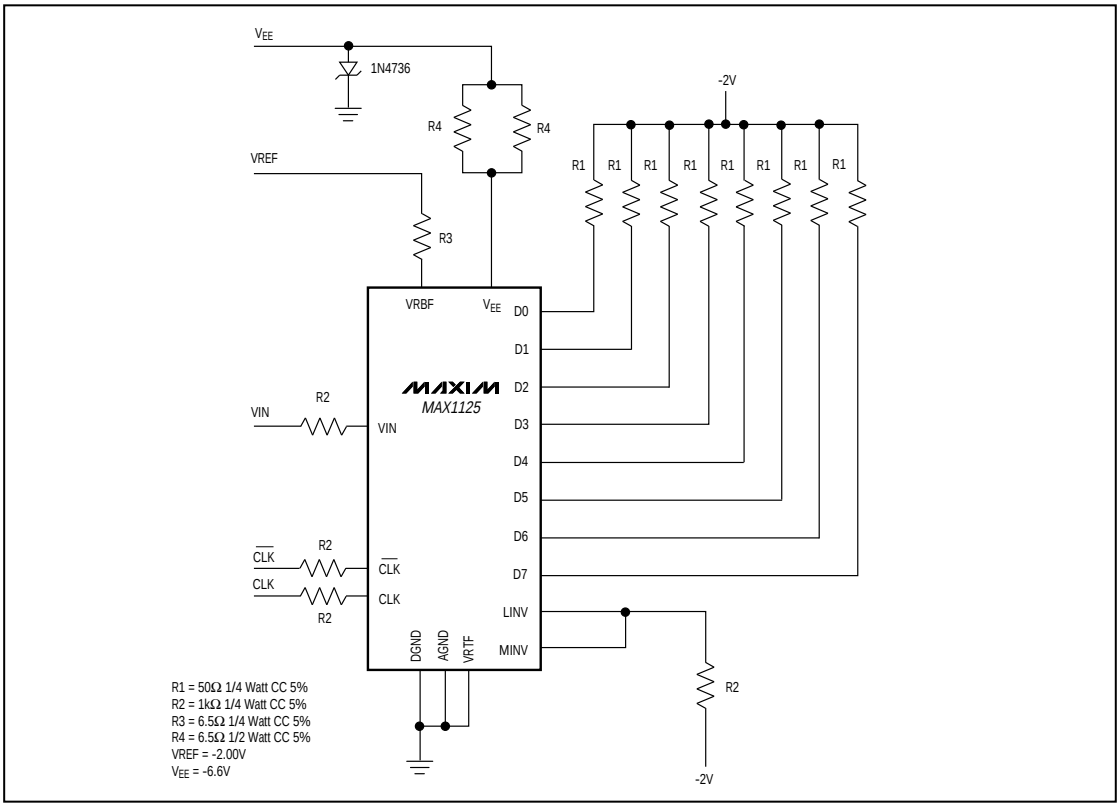


Figure 6. Burn-In Circuit (Ceramic SB package only)

8-Bit, 300Msps Flash ADC

Functional Diagram