MN85560

MPEG2 Video Encoder

■ Overview

The MN85560 is an MPEG2 video encoder that outputs encoded data that conform to the ISO/IEC 1318-2 (MPEG2 video) Main Profile@Main Level and ISO/IEC 1172-2 (MPEG1 video) standards.

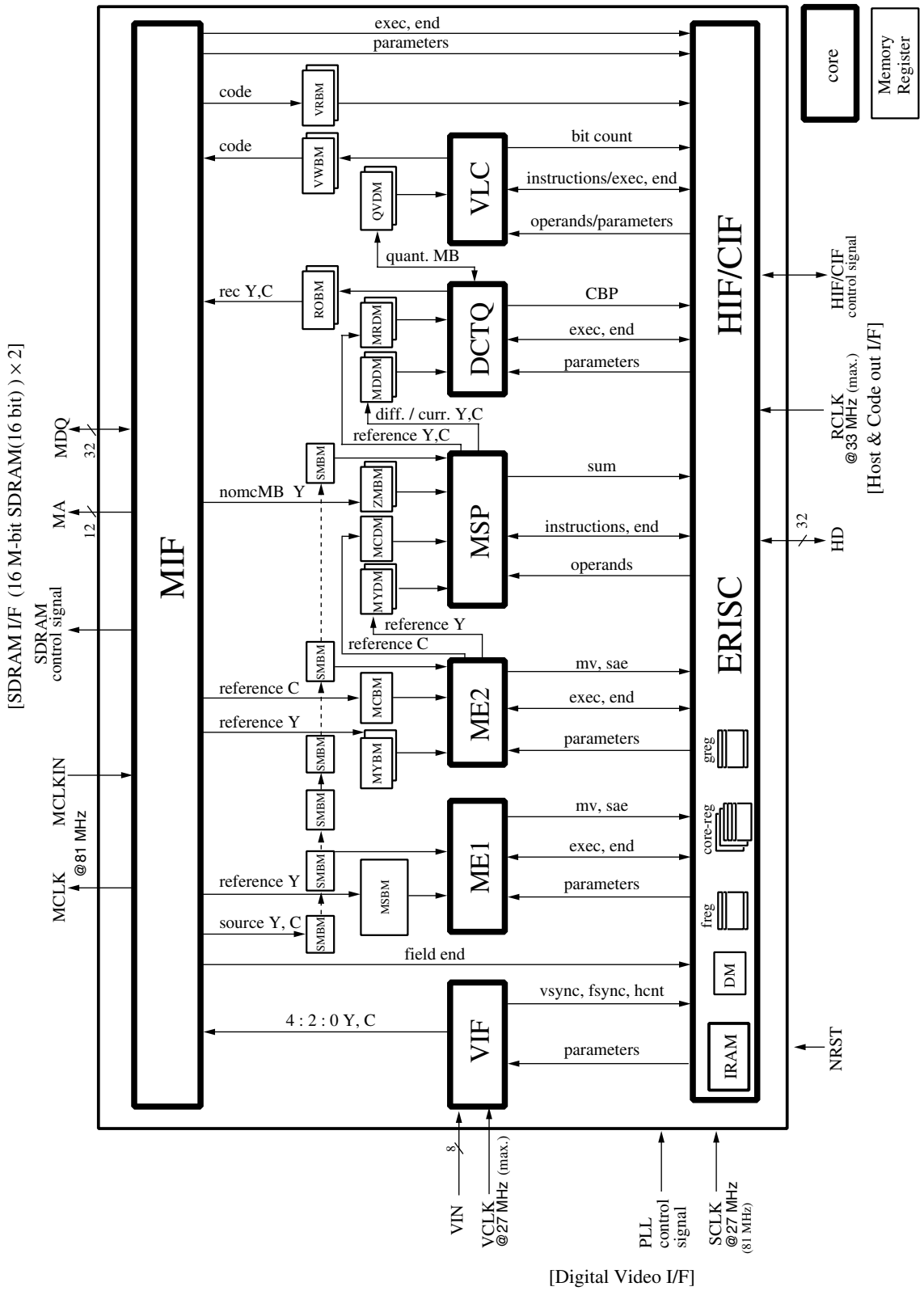
■ Features

- Incorporates the image input filters used for front-end processing.
- Supports PAL size images with just two external 16M synchronous DRAMs (SDRAM).
- The back-end code output buffer is allocated in SDRAM and can be controlled from microcode.
- Provides image quality improvement functions:
  - Multiple-mode high-performance motion vector detection
  - Original rate control techniques implemented in microcode
- Intra-slice functions for low delay modes and PES output to reduce the system encoding load
- Clock input
  - Three clocks: system clock SCLK (27 MHz), video input clock VCLK, and code output clock RCLK.
  - An internal PLL circuit is used to generate an 81 MHz clock from SCLK (27 MHz). This clock is used for internal circuits and the synchronous DRAM.
- Supply voltages: 3.3 V (I/O supply voltage and internal PLL circuit supply voltage)
  1.8 V (internal circuit supply voltage)

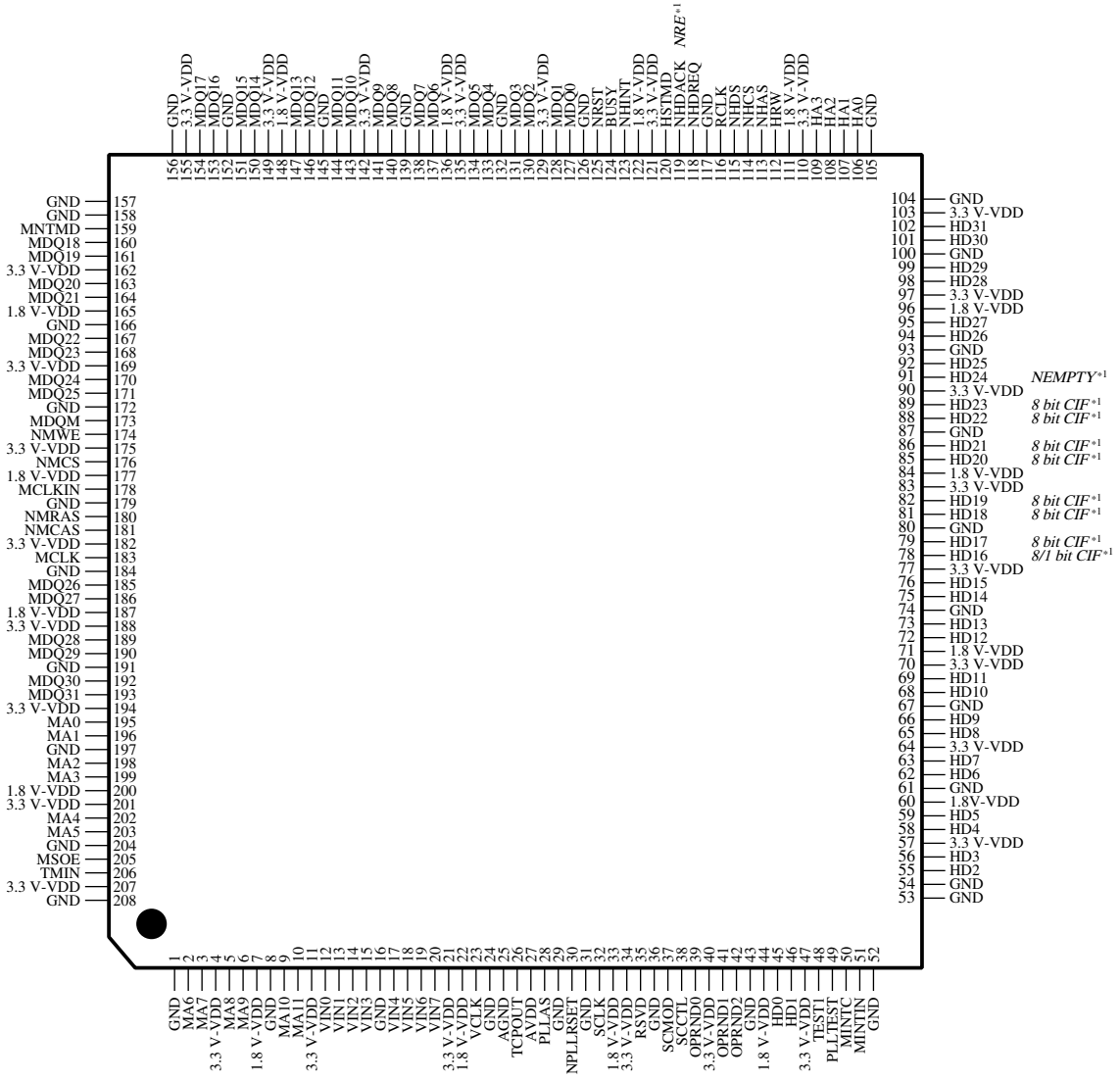
■ Applications

- DVD recorders, multimedia personal computers, MPEG2 cameras etc.

■ Block Diagram



■ Pin Assignment



(TOP VIEW)

Note) *1: Pins names shown in italic refer to CIF serial mode pins.

■ Pin Functions

Pin No.	I/O	Output at reset	Number	Function
SCLK	I	—	1	System clock
VCLK	I	—	1	Video input clock
RCLK	I	—	1	Code output clock (Used in single-bus parallel mode and serial mode.)
NRST	I	—	1	Chip initialization reset input signal
VIN[7 : 0]	I	—	8	Video input
MCLK	O	*clock*[*3]	1	Clock output[*1] for external memory (SDRAM)
MCLKIN	I	—	1	Transfer clock input[*1] between external memory/MN85560
NMCS	O	*"H"* [*3]	1	Chip select output for external memory (SDRAM)
NMRAS	O	*"H"* [*3]	1	RAS output for external memory (SDRAM)
NMCAS	O	*"H"* [*3]	1	CAS output for external memory (SDRAM)
NMWE	O	*"H"* [*3]	1	Write enable output for external memory (SDRAM)
MDQM	O	*"H"* [*3]	1	Data I/O buffer control for external memory (SDRAM)
MA[11 : 0]	O	*all "L"* [*3]	12	Address output for external memory (SDRAM)
MDQ[31 : 0][*4]	I/O	*all "H"* [*3]	32	Data I/O for external memory (SDRAM)
MSOE	I	—	1	OE control for external memory (SDRAM) (0: MDQ (I/O) are set to input mode and the SDRAM output pins are set to the high-impedance state.)
HA[3 : 0]	I	—	4	Host interface address signals
HRW	I	—	1	Host interface read/write signal
NHAS	I	—	1	Host interface address strobe
NHCS	I	—	1	Host interface chip select signal
NHDS	I	—	1	Host interface data strobe
NHDREQ	O	"H"	1	DMA transfer request signal
NHDACK	I	—	1	Code output enable signal
NHINT	O	"H"	1	Host interface interrupt generation notification signal
HSTMD	I	—	1	Host interface mode (1 : 32-bit hostmode, 0 : 16-bit hostmode)
HD[15 : 0]	**I**[*2]/O	—	16	Host interface data I/O
HD[31 : 16]	**I**[*2]/O	—	16	At HSTMD = 1: HD[31:16] function in input mode
	O[*2]	all "L"		At HSTMD = 0: HD[31:16] function in output mode) (At reset, HD16 functions as the 1-bit CIF output, and HD24: empty)

Note) *1: MCLK and MCLKIN should be connected externally with a delay of 1 ns or less.

*2: The bold notation in the HD pin I/O column indicates the I/O state immediately following a chip reset.

*3: Items in italic indicate values immediately after a chip reset when MSOE is high.

*4: The MD[31:0] values (all high) immediately following a chip reset are due to these lines being pulled up internally in the IC. Therefore, no problems will occur if the SDRAM is driving MD[31:0].

■ Pin Functions (continued)

Pin No.	I/O	Output at reset	Number	Function
OPRND[2 : 0]	O	—	3	open
SCMOD	I	—	1	Must be held low.
SCCTL	I	—	1	Must be held low.
BUSY	O	"L"	1	Chip status output signal
TEST1	I	—	1	Must be held low.
MNTMD	I	—	1	Must be held low.
TMIN	I	—	1	Must be held low.
MINTC	I	—	1	Must be held low.
MINTIN	I	—	1	Must be held low.
RSVD	I	—	1	Must be held low.
PLLAS	I	—	1	PLL assert input signal (1: The PLL circuit operates. 0: The PLL circuit is stopped.)
NPLLRSET	I	—	1	PLL reset input signal
TCPOUT	O	—	1	open
PLLTEST	I	—	1	Must be held low.
AVDD	I	—	1	PLL power supply
AGND	I	—	1	PLL ground

■ Architecture

• Chip State Transitions

The MN85560 has three internal states: run, hold, and slave. In the run state, the MN85560 executes microcode, in the hold state, it does not execute microcode, and in the slave state, it does not execute microcode and allows all of its internal resources to be accessed. The registers that are mapped to direct addresses can be read or written in any of these states. Resources that are mapped to indirect addresses can only be accessed when the MN85560 is in the slave state. The only exception to this is hifreg0 to hifreg5, which can be accessed in the run state. The indirectly addressed resources cannot be accessed in the hold state.

In addition to the above three states, the chip also has a reset state which is a chip initialization state. There are two techniques for switching the MN85560 to the reset state: hardware reset using the NRST pin, and software reset using the direct address registers. During a hardware reset, none of the internal resources can be read or written. During a software reset, only the CHIPCTL0 direct address register can be written. Figure 1 shows the MN85560 chip state transition diagram.

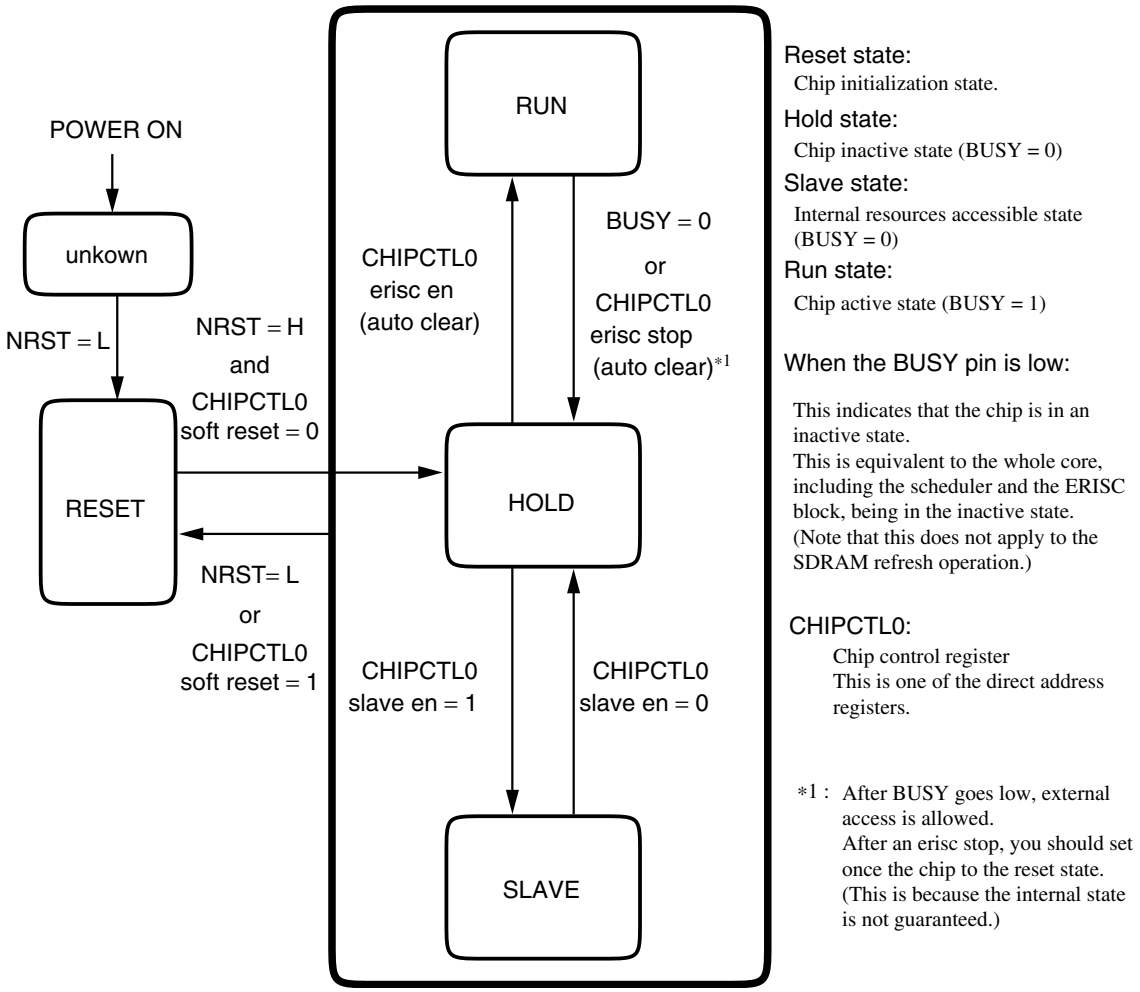


Figure 1. Chip State Transition Diagram

■ Architecture (continued)

• Chip State Transitions (continued)

The slave state is a state in which the external circuit can read and write instruction memory (IRAM), data memory (DM), and the global registers. This state is mainly used for downloading microcode, encoding parameters, and other data. After reading out instruction memory (IRAM), for example to verify program download, you should reset the MN85560. In particular, you should switch the MN85560 from the slave to the hold state and then set it to the reset state. Then you should return the MN85560 to the hold state.

After applying power, supplying the clock, and starting the PLL oscillator with the prescribed procedure, the MN85560 can be set to the reset state by asserting the NRST pin (hardware reset). Alternatively, you may switch the MN85560 from the hold state to the reset state by setting the direct address register CHIPCTL0[0] (soft reset) to 1 (software reset). Note that the contents of direct address register CHIPCTL0 are not reset after a software reset.

After a hardware reset, the MN85560 is switched from the reset state to the hold state by negating the NRST pin. After a software reset, this is performed by setting direct address register CHIPCTL0[0] (soft reset) to 0.

The MN85560 is switched from the hold state to the slave state by setting direct address register CHIPCTL0[1] (slave en) to 1.

You should perform the following register initializations when the MN85560 is in the slave state.

Indirect address resource initreg0 ($1309A) = $0000

Indirect address resource initreg1 ($1309B) = $00c0

Note that these values return to the default values when the MN85560 switches to the reset state. This means that they must be set back to the above values.

The MN85560 is switched from the slave state to the hold state by setting direct address register CHIPCTL0[1] (slave en) to 0.

The MN85560 is switched from the hold state to the run state by setting direct address register CHIPCTL0[4] (erisc en) to 1. Note that erisc en is automatically cleared to 0 immediately after it is set.

The transition from the run state to the hold state occurs automatically when microcode execution completes and operation of all MN85560 blocks (see the block diagram) terminates except for SDRAM refresh operations. At this point the BUSY pin will go to the low level. Alternatively, the MN85560 can be forcibly switched from the run state to the hold state by setting direct address register CHIPCTL0[5] (erisc stop) to 1. In this case, after the processing being performed by all blocks that were executing when CHIPCTL0[5] (erisc stop) was set to 1 completes, the BUSY pin goes low and the MN85560 switches to the hold state. Note that erisc stop is automatically cleared to 0 immediately after it is set to 1. If the MN85560 is forcibly switched to the hold state, we recommend that you set the MN85560 to the reset state, and then set it to the slave state and once again download the microcode, encoding parameters, and other settings before executing another encode operation. This is because the states of the internal resources cannot be guaranteed in this case.

SDRAM refresh is started by executing the startup sequence using microcode. After that, the MN85560 continues to manage the number refresh operations regardless of whether it is in the run, hold or slave state. Since refresh operations are stopped in the reset state, you should restart the refresh operation by running the microcode that starts the refresh operation again.

■ Electrical Characteristics

1. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Unit
Supply voltage 1	V_{DD}	– 0.3 to +4.6	V
Supply voltage 2	V_{DDI}	– 0.3 to +3.6	V
Supply voltage 3	AV_{DD}	– 0.3 to +4.6	V
Input voltage	V_I	– 0.3 to V_{DD} + 0.3 (Upper limit: 4.6)	V
Output voltage	V_O	– 0.3 to V_{DD} + 0.3 (Upper limit: 4.6)	V
Average output current	I_O	±24	mA
Power dissipation	P_D	3.3 (layer 4)	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	–40 to +125	°C

Note) 1. The absolute maximum ratings are limiting values under which the chip will not be destroyed. Operation is not guaranteed within these ranges.

2. All of the V_{DD} and V_{SS} pins must directly connected to the power supply or ground, respectively.

3. Insert bypass capacitors of at least 0.1 µF between the V_{DD} and V_{SS} pins as close as possible to the IC itself.

4. Power should be applied in the order first the 3.3 V system (V_{DD} and AV_{DD}) and then the 1.8 V system (V_{DDI}). Power should be turned off in the order first the 1.8 V system (V_{DDI}) and the 3.3 V system (V_{DD} and AV_{DD}).

2. Recommended Operating Conditions at T_a = 0°C to 70°C, V_{SS} = 0 V, AV_{SS} = 0 V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage 1	V_{DD}		3.0	3.3	3.6	V
Supply voltage 2	V_{DDI}		1.65	1.80	1.95	V
Supply voltage 3	AV_{DD}		3.0	3.3	3.6	V
Ambient temperature	T_a		0	—	70	°C
System clock frequency	SCLK	V_{DD} = 3.0 V to 3.6 V AV_{DD} = 3.0 V to 3.6 V DUTY : 50% ± 10%	—	—	27.0	MHz
System clock frequency	VCLK	V_{DD} = 3.0 V to 3.6 V DUTY : 50% ± 10%	—	—	27.0	MHz
System clock frequency	RCLK	V_{DD} = 3.0 V to 3.6 V DUTY : 50% ± 10%	—	—	33.0	MHz

■ Electrical Characteristics (continued)

3. DC Characteristics at T_a = 0°C to 70°C, V_{SS} = 0 V, AV_{SS} = 0 V, V_{DD} = 3.0 V to 3.6 V, V_{DDI} = 1.65 V to 1.95 V, AV_{DD} = 3.0 V to 3.6 V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating current drain	I_{DDO}	$V_I = V_{DD}$ or V_{SS} SCLK = 27.0 MHz VCLK = 27.0 MHz RCLK = 40.5 MHz With output pins open.	—	—	V_{DDI} 750 V_{DD} 90	mA mA
Input pins (TTL level) : SCLK, VCLK, RCLK, NRST, VIN7 to VIN0, MCLKIN, MSOE, HA3 to HA0, HRW, NHAS, NHCS, NHDS, NHDACK, HSTMD, SCMOD, SCCTL, TEST1, MNTMD, MINTC, MINTIN, PLLAS, NPLLRSET, PLLTEST, RSVD						
High-level input voltage	V_{IH}		2.0	—	V_{DD}	V
Low-level input voltage	V_{IL}		0	—	0.8	V
Input leakage current	I_{LI}	$V_I = V_{DD}$ or V_{SS} V_{DD} = 3.3 V ± 0.3 V	–5	—	5	µA
Input pins (LVCMOS) : TMIN						
High-level input voltage	V_{IH}		$V_{DD}\times0.7$	—	V_{DD}	V
Low-level input voltage	V_{IL}		0	—	$V_{DD}\times0.3$	V
Input leakage current	I_{LI}	$V_I = V_{SS}$	–10	—	10	mA
Pull-down resistance	R_{IL}	$V_I = V_{DD}$	10	30	90	kΩ
Input pins (LVCMOS) : MINTC, MINTIN						
High-level input voltage	V_{IH}		$V_{DD}\times0.7$	—	V_{DD}	V
Low-level input voltage	V_{IL}		0	—	$V_{DD}\times0.3$	V
Input leakage current	I_{LI}	$V_I = V_{DD}$ or V_{SS}	–5	—	5	µA
Output pins (LVTTL) : MCLK, NMCS, NMRAS, NMCAS, NMWE, MDQM, MA11 to MA0, NHDREQ, NHINT, OPRND2 to OPRND0, BUSY						
High-level output voltage	V_{OH}	I_O = –8.0 mA	2.4	—	—	V
Low-level output voltage	V_{OL}	I_O = 8.0 mA	—	—	0.4	V
Output leakage current	I_{OZ}	V_O: high-impedance state $V_O = V_{DD}$ or V_{SS}	–5	—	5	mA
I/O pins (LVTTL) : MDQ31 to MDQ0						
High-level input voltage	V_{IH}		2.0	—	V_{DD}	V
Low-level input voltage	V_{IL}		0	—	0.8	V
High-level output voltage	V_{OH}	I_O = –8.0 mA	2.4	—	—	V
Low-level output voltage	V_{OL}	I_O = 8.0 mA	—	—	0.4	V
Output leakage current	I_{OZ}	V_O: high-impedance state $V_O = V_{DD}$	–10	—	10	µA
Pull-up resistance	R_{IH}	$V_I = V_{SS}$	10	30	90	kΩ

■ Electrical Characteristics (continued)

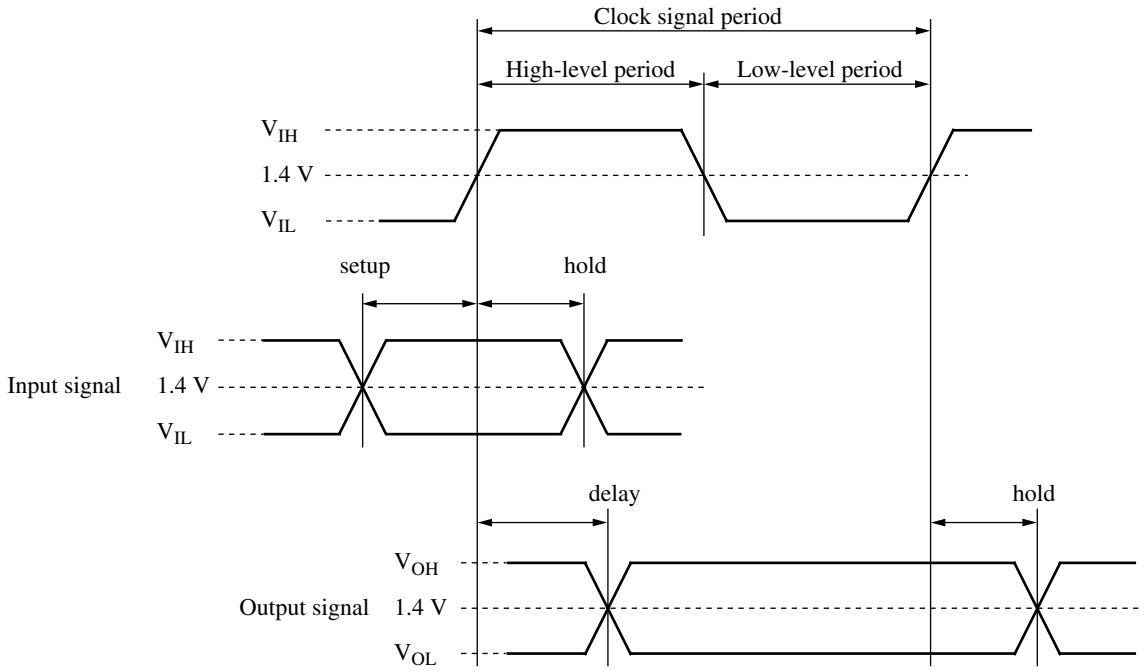
3. DC Characteristics at T_a = 0°C to 70°C, V_{SS} = 0 V, AV_{SS} = 0 V, V_{DD} = 3.0 V to 3.6 V, V_{DDI} = 1.65 V to 1.95 V, AV_{DD} = 3.0 V to 3.6 V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input pins (LVTTL) : HD31 to HD0						
High-level input voltage	V_{IH}		2.0	—	V_{DD}	V
Low-level input voltage	V_{IL}		0	—	0.8	V
High-level output voltage	V_{OH}	I_O = −8.0 mA	2.4	—	—	V
Low-level output voltage	V_{OL}	I_O = 8.0 mA	—	—	0.4	V
Output leakage current	I_{OZ}	V_O: high-impedance state $V_O = V_{DD}$ or V_{SS}	−5	—	5	µA

■ Electrical Characteristics (continued)

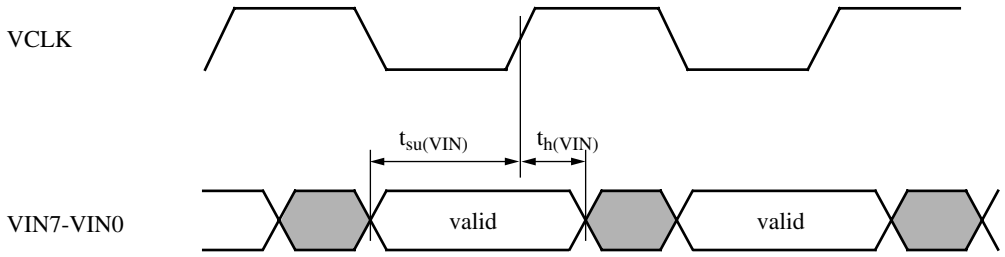
4. AC Characteristics

The signal reference level for AC characteristics measurement is 1.4 V as shown in the figure.



Note) The AC characteristics are values for the case where the internal PLL circuit is used to supply a 27 MHz clock signal to the SCLK pin, and to provide 27 MHz and 33 MHz signals to the VCLK and RCLK pins, respectively.
Note that the AC characteristics values may differ when this IC is used under conditions other than those described above.

• Timing Charts



Parameter	Symbol	Min	Typ	Max	Unit
VIN7:0 setup time to the VCLK rising edge	$t_{su(VIN)}$	10.0	—	—	ns
VIN7:0 hold time to the VCLK rising edge	$t_{h(VIN)}$	1.0	—	—	ns

■ Electrical Characteristics (continued)

4. AC Characteristics (continued)

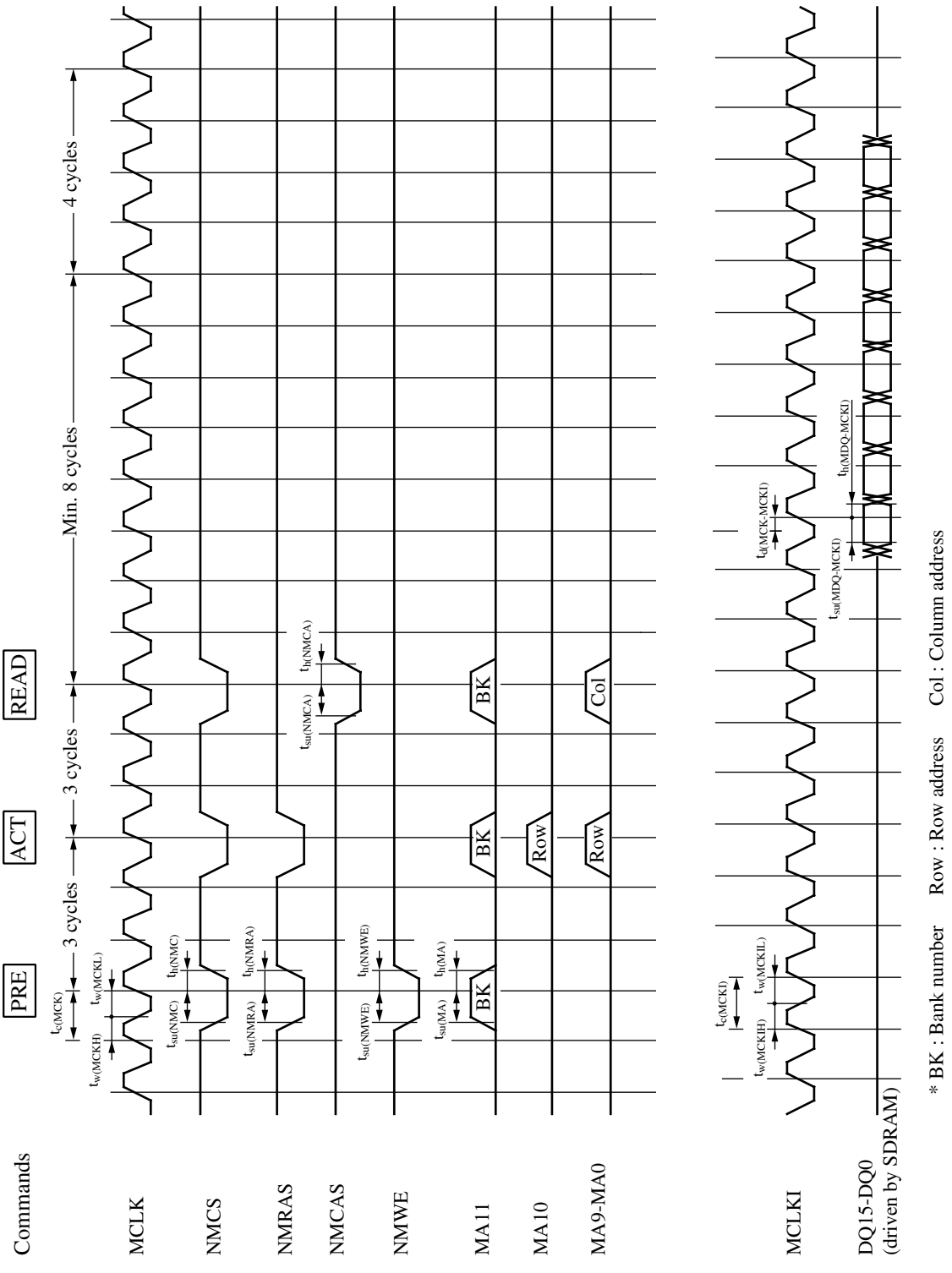
Parameter	Symbol	Min	Typ	Max	Unit
MCLK cycle time	$t_{c(MCK)}$	—	12.3	—	ns
MCLK high-level pulse width	$t_{w(MCKH)}$	3.5	—	—	ns
MCLK low-level pulse width	$t_{w(MCKL)}$	3.5	—	—	ns
NMCS setup time to the MCLK rising edge	$t_{su(NMC)}$	3.0	—	—	ns
NMCS hold time from the MCLK rising edge	$t_{h(NMC)}$	2.0	—	—	ns
NMRAS setup time to the MCLK rising edge	$t_{su(NMRA)}$	3.0	—	—	ns
NMRAS hold time from the MCLK rising edge	$t_{h(NMRA)}$	2.0	—	—	ns
NMCAS setup time to the MCLK rising edge	$t_{su(NMCA)}$	3.0	—	—	ns
NMCAS hold time from the MCLK rising edge	$t_{h(NMCA)}$	2.0	—	—	ns
NMWE setup time to the MCLK rising edge	$t_{su(NMWE)}$	3.0	—	—	ns
NMWE hold time from the MCLK rising edge	$t_{h(NMWE)}$	2.0	—	—	ns
MA11-0 setup time to the MCLK rising edge	$t_{su(MA)}$	3.0	—	—	ns
MA11-0 hold time from the MCLK rising edge	$t_{h(MA)}$	2.0	—	—	ns
MDQM setup time to the MCLK rising edge	$t_{su(MDQM)}$	3.0	—	—	ns
MDQM hold time from the MCLK rising edge	$t_{h(MDQM)}$	2.0	—	—	ns
MDQ31-0 setup time to the MCLK rising edge	$t_{su(MDQ-MCK)}$	3.0	—	—	ns
MDQ31-0 hold time from the MCLK rising edge	$t_{h(MDQ-MCK)}$	2.0	—	—	ns
MCLKIN cycle time	$t_{c(MCKI)}$	—	12.3	—	ns
MCLKIN high-level pulse width	$t_{w(MCKIH)}$	3.5	—	—	ns
MCLKIN low-level pulse width	$t_{w(MCKIL)}$	3.5	—	—	ns
MCLKIN rising edge delay from the MCLK rising edge	$t_{d(MCK-MCKI)}$	0	—	1.0	ns
MDQ31:0 setup time to the MCLK rising edge	$t_{su(MDQ-MCKI)}$	2.0	—	—	ns
MDQ31:0 hold time from the MCLK rising edge	$t_{h(MDQ-MCKI)}$	2.0	—	—	ns

Note) The allowable values of the MCLK and MCLKIN cycle times are listed in the "Typ" column. This is because the MN85560 directly inputs the clock output from MCLK to MCLKIN.

■ Electrical Characteristics (continued)

4. AC Characteristics (continued)

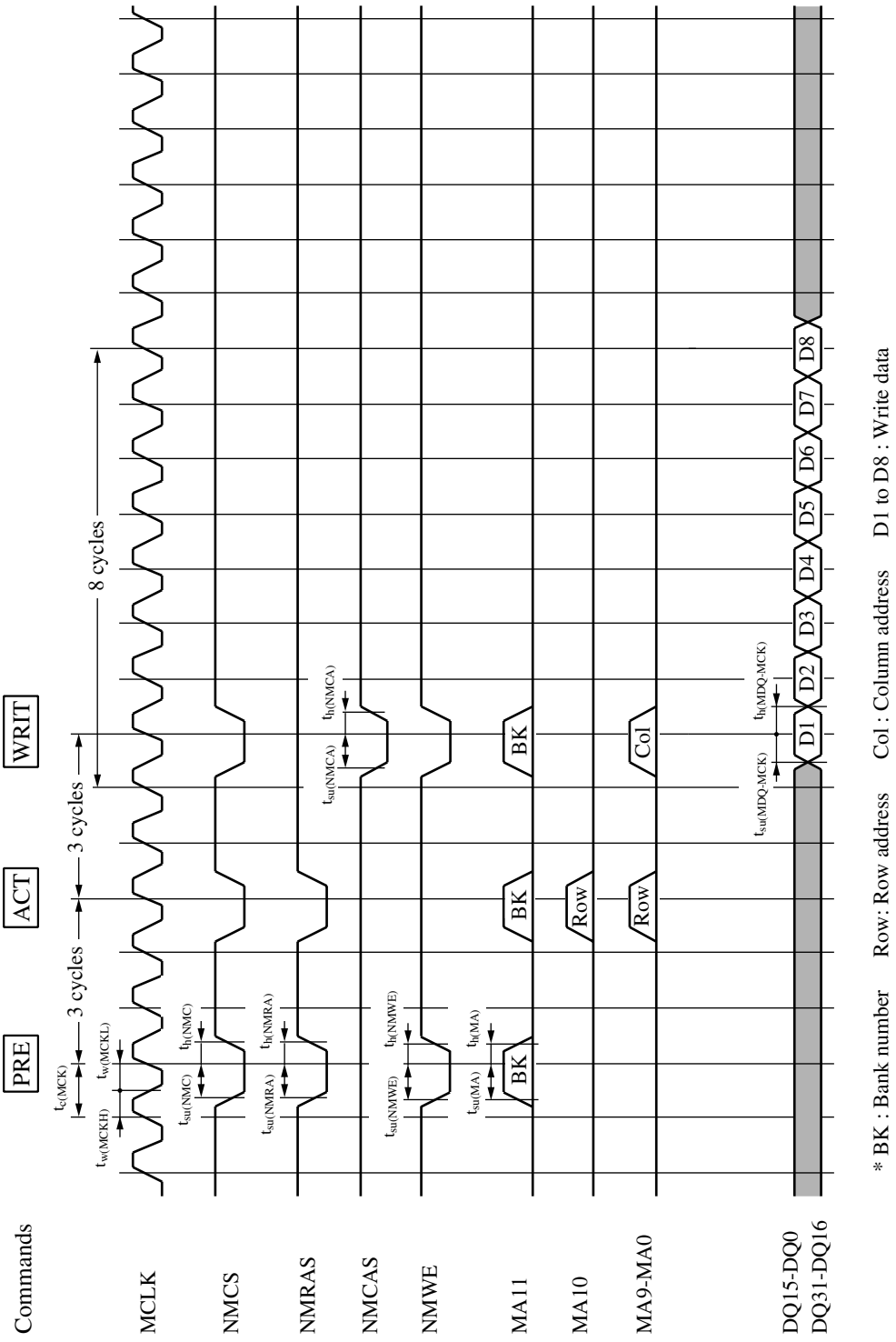
• Timing Charts (Basic burst read operation)



■ Electrical Characteristics (continued)

4. AC Characteristics (continued)

• Timing Charts (Basic burst write operation)



■ Electrical Characteristics (continued)

4. AC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Unit
Serial mode					
HD24 (NEMPTY) fall time from the RCLK rising edge	$t_{h(NEMPTY)}$	3	—	—	ns
NHDACK (NRE) setup time to the RCLK rising edge	$t_{su(NHDACK)}$	3	—	—	ns
NHDACK (NRE) hold time from the RCLK rising edge	$t_{h(NHDACK)}$	4	—	—	ns
HD16 (HD23:16) data setup time to the RCLK rising edge	$t_{v(HD)}$	—	—	25	ns
HD16 (HD23:16) data hold time from the RCLK rising edge	$t_{h(HD)}$	3	—	—	ns
Parallel mode (single bus cycle mode)					
NHDACK setup time to the RCLK rising edge	$t_{su(NHDACK-RCLK)}$	10	—	—	ns
NHDACK hold time from the RCLK rising edge	$t_{h(NHDACK-RCLK)}$	10	—	—	ns
HD31:0 drive time from the NHDACK falling edge	$t_{d(HD-NHDACK)}$	1	—	—	ns
HD31:0 data setup time to the RCLK rising edge	$t_{v(HD-RCLK)}$	—	—	20	ns
HD31:0 data hold time from the NHDACK rising edge	$t_{h(HD-NHDACK)}$	1	—	—	ns
Parallel mode (two bus cycle mode)					
HA3:0 setup time to the NHAS falling edge	$t_{su(HA-NHAS)}$	15	—	—	ns
HA3:0 hold time from the NHAS rising edge	$t_{h(HA-NHAS)}$	15	—	—	ns
NHAS pulse width	$t_{w(NHAS)}$	30	—	—	ns
NHAS setup time to the NHDS falling edge	$t_{su(NHAS-NHDS)}$	15	—	—	ns
NHCS setup time to the NHDS falling edge	$t_{su(NHCS-NHDS)}$	15	—	—	ns
NHCS hold time from the NHDS rising edge	$t_{h(NHCS-NHDS)}$	15	—	—	ns
NHDS pulse width	$t_{w(NHDS)}$	100	—	—	ns
HRW setup time to the NHDS falling edge	$t_{su(HRW-NHDS)}$	15	—	—	ns
HRW hold time from the NHDS rising edge	$t_{h(HRW-NHDS)}$	15	—	—	ns

■ Electrical Characteristics (continued)

4. AC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Unit
Parallel mode (two bus cycle mode) (continued)					
HD31:0 drive time from the NHCS falling edge	$t_{d(HD-NHCS)}$	1	—	—	ns
HD31:0 drive time from HWR transitions	$t_{d(HD-HRW)}$	1	—	—	ns
HD31:0 data setup time to the NHDS falling edge	$t_{v(HD-NHDS)}$	—	—	100	ns
HD31:0 data hold time from the NHCS rising edge	$t_{h(HD-NHCS)}$	1	—	—	ns
HD31:0 data hold time from HWR transitions	$t_{h(HD-HRW)}$	1	—	—	ns
NHDS recovery time	t_r	40	—	—	ns

■ Electrical Characteristics (continued)

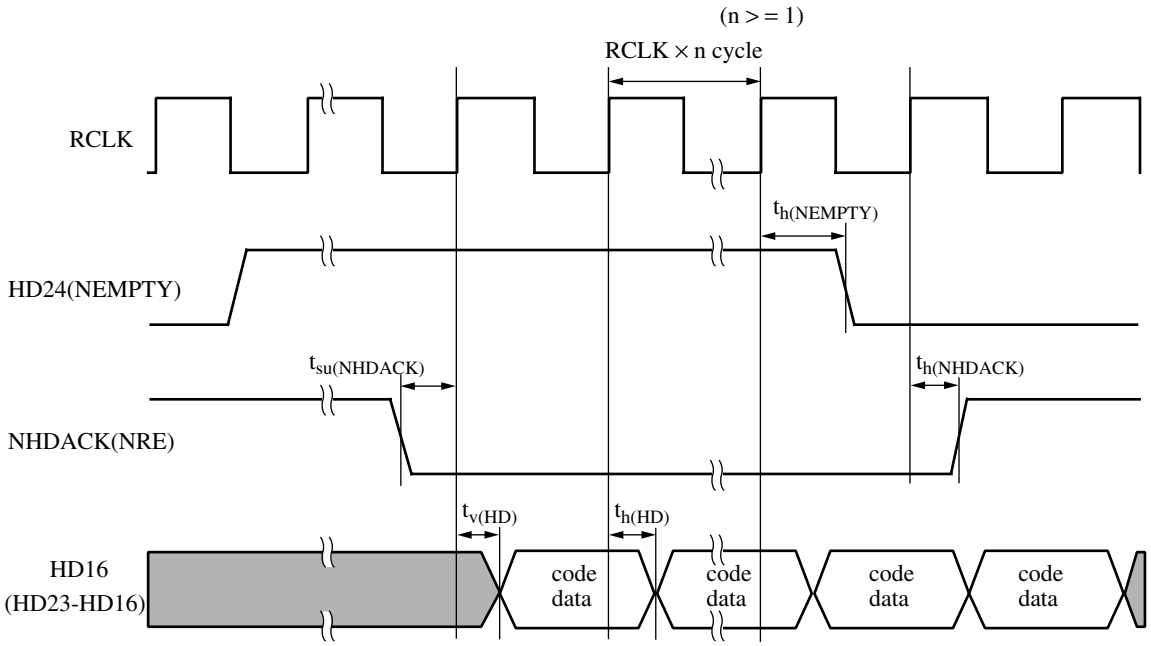
4. AC Characteristics (continued)

• Interface operation timing (Serial mode)

The only difference between the 1-bit mode and the 8-bit mode is the bit width: the operation timing is identical. In 1-bit mode, code is output from HD16, and in 8-bit mode code is output from HD23:16.

1. HD24 (NEMPTY) goes high at $t_{v(NEMPTY)}$ after the RCLK rising edge.
2. When HD24 (NEMPTY) is high, NHDACK (NRE) should be set low $t_{su(NHDACK)}$ before the RCLK rising edge.
3. Code data is output at the point $t_{v(HD)}$ after the first RCLK rising edge after NHDACK (NRE) was set low. The code data is held for just the period $t_{h(HD)}$ from at the next RCLK rising edge. The next code data is output after that.
4. Following NHDACK (NRE) being set low, code data is output continuously in synchronization with RCLK.
5. When HD24 (NEMPTY) goes low, we recommend that you hold NHDACK (NRE) low until after $t_{h(NHDACK)}$ has elapsed from the next RCLK rising edge and then set it high. Code data output stops on the next RCLK cycle after that. (This is not valid code data, rather the pin merely remains in the driving state.) However, note that HD24 (NEMPTY) goes low at $t_{h(NEMPTY)}$ after the RCLK rising edge.

• Timing Chart (Serial mode)



■ Electrical Characteristics (continued)

4. AC Characteristics (continued)

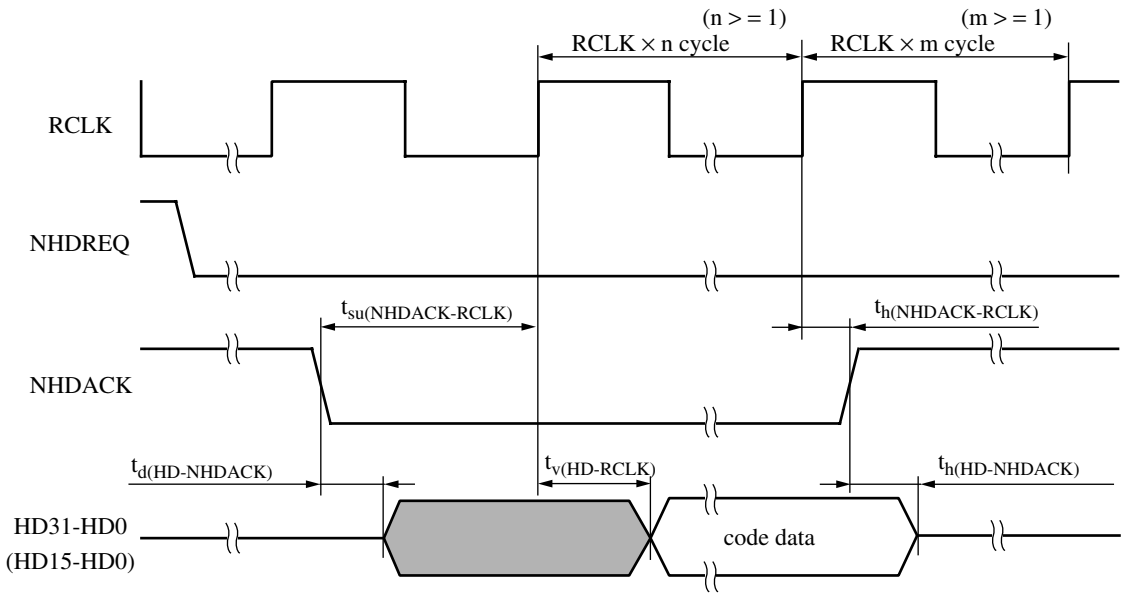
• Interface operation timing (Parallel mode)

<Single bus cycle mode>

While the following describes 32-bit mode, 16-bit mode only differs in the bit width: the operation timing is identical.

1. When NHDREQ is low, NHDACK should be set low at $t_{su(NHDACK-RCLK)}$ before the RCLK rising edge. The MN85560 starts drive of the HD31:0 pins at $t_{d(HD-NHDACK)}$ after NHDACK is set low.
2. After NHDACK is set low, code data is output at $t_{v(HD-RCLK)}$ after the first RCLK rising edge.
3. NHDACK should be held low for one complete RCLK cycle. You should hold NHDACK low until after $t_{h(NHDACK-RCLK)}$ from the RCLK rising edge, and then set NHDACK high.
4. After setting NHDACK high, the code data is held just the period $t_{h(HD-NHDACK)}$. After that, HD31:0 go to the high-impedance state.
5. After that, NHDACK should be held high for at least one complete RCLK cycle.

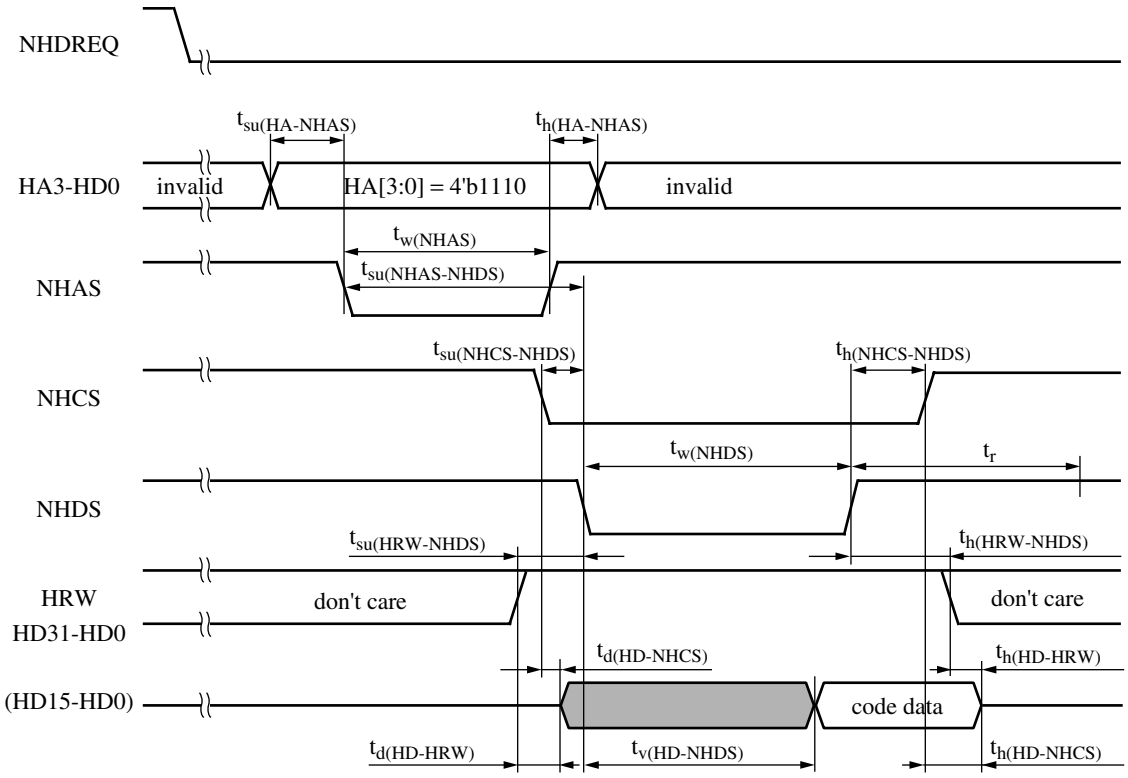
• Timing Chart (Parallel mode: single bus cycle mode)



■ Electrical Characteristics (continued)

4. AC Characteristics (continued)

• Timing Chart (Parallel mode: two bus cycle mode)



■ Electrical Characteristics (continued)

4. AC Characteristics (continued)

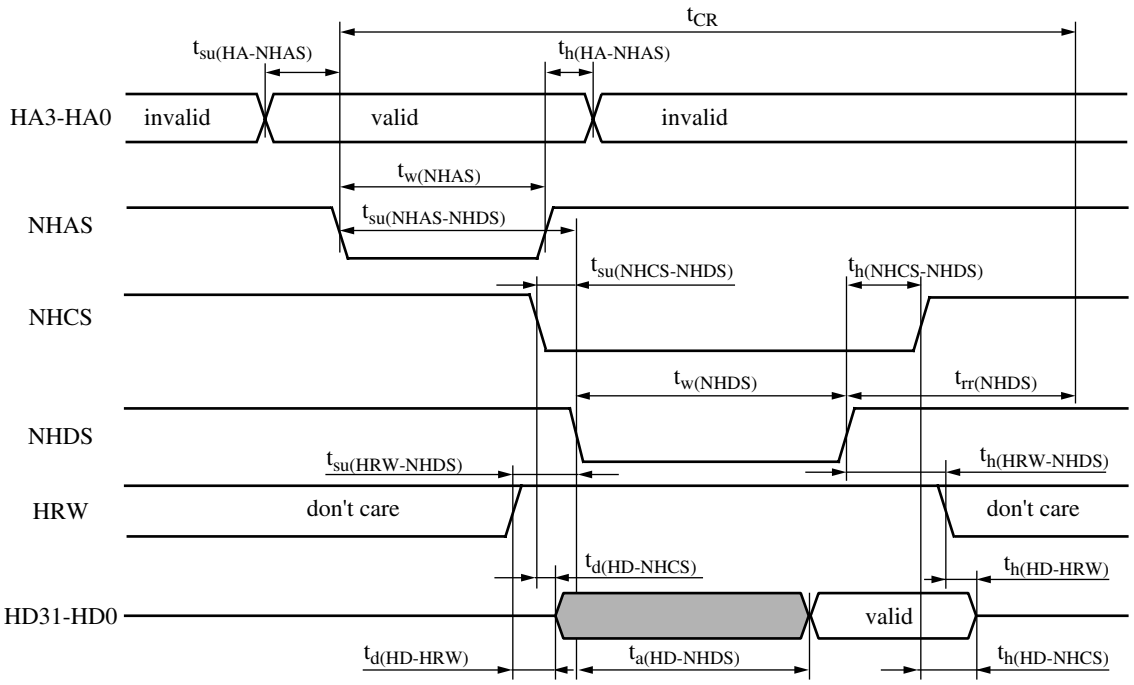
Parameter	Symbol	Min	Typ	Max	Unit
Read operations					
H3:0 setup time to the NHAS falling edge	$t_{su(HA-NHAS)}$	15	—	—	ns
H3:0 hold time from the NHAS rising edge	$t_{h(HA-NHAS)}$	15	—	—	ns
NHAS pulse width	$t_{w(NHAS)}$	30	—	—	ns
NHAS setup time to the NHDS falling edge	$t_{su(NHAS-NHDS)}$	15	—	—	ns
NHCS setup time to the NHDS falling edge	$t_{su(NHCS-NHDS)}$	15	—	—	ns
NHCS hold time from the NHDS rising edge	$t_{h(NHCS-NHDS)}$	15	—	—	ns
NHDS pulse width	$t_{w(NHDS)}$	200	—	—	ns
HRW setup time to the NHDS falling edge	$t_{su(HRW-NHDS)}$	15	—	—	ns
HRW hold time from the NHDS rising edge	$t_{h(HRW-NHDS)}$	15	—	—	ns
HD31:0 drive time from the NHCS falling edge	$t_{d(HD-NHCS)}$	1	—	—	ns
HD31:0 drive time from HRW transitions	$t_{d(HD-HRW)}$	1	—	—	ns
Read access time from the NHDS falling edge	$t_{a(HD-NHDS)}$	—	—	200	ns
HD31:0 hold time from the NHCS rising edge	$t_{h(HD-NHCS)}$	1	—	—	ns
HD31:0 hold time from HRW transitions	$t_{h(HD-HRW)}$	1	—	—	ns
NHDS recovery time	$t_{rr(NHDS)}$	40	—	—	ns
Read cycle time	t_{CR}	255	—	—	ns
Write operations					
HA3:0 setup time to the NHAS falling edge	$t_{su(HA-NHAS)}$	15	—	—	ns
HA3:0 hold time from the NHAS rising edge	$t_{h(HA-NHAS)}$	15	—	—	ns
NHAS pulse width	$t_{w(NHAS)}$	30	—	—	ns
NHAS setup time to the NHDS falling edge	$t_{su(NHAS-NHDS)}$	15	—	—	ns

■ Electrical Characteristics (continued)

4. AC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Unit
Write operations (continued)					
NHCS setup time to the NHDS falling edge	$t_{su(NHCS-NHDS)}$	15	—	—	ns
NHCS hold time from the NHDS rising edge	$t_{h(NHCS-NHDS)}$	15	—	—	ns
NHDS pulse width	$t_{w(NHDS)}$	100	—	—	ns
HRW setup time to the NHDS falling edge	$t_{su(HRW-NHDS)}$	15	—	—	ns
HRW hold time from the NHDS rising edge	$t_{h(HRW-NHDS)}$	15	—	—	ns
HD31:0 setup time to the NHDS rising edge	$t_{su(HD-NHDS)}$	20	—	—	ns
HD31:0 hold time from the NHDS rising edge	$t_{h(HD-NHDS)}$	20	—	—	ns
NHDS recovery time	$t_{rw(NHDS)}$	90	—	—	ns
Write cycle time	t_{CW}	205	—	—	ns

• Timing Chart (Read operation)



■ Electrical Characteristics (continued)

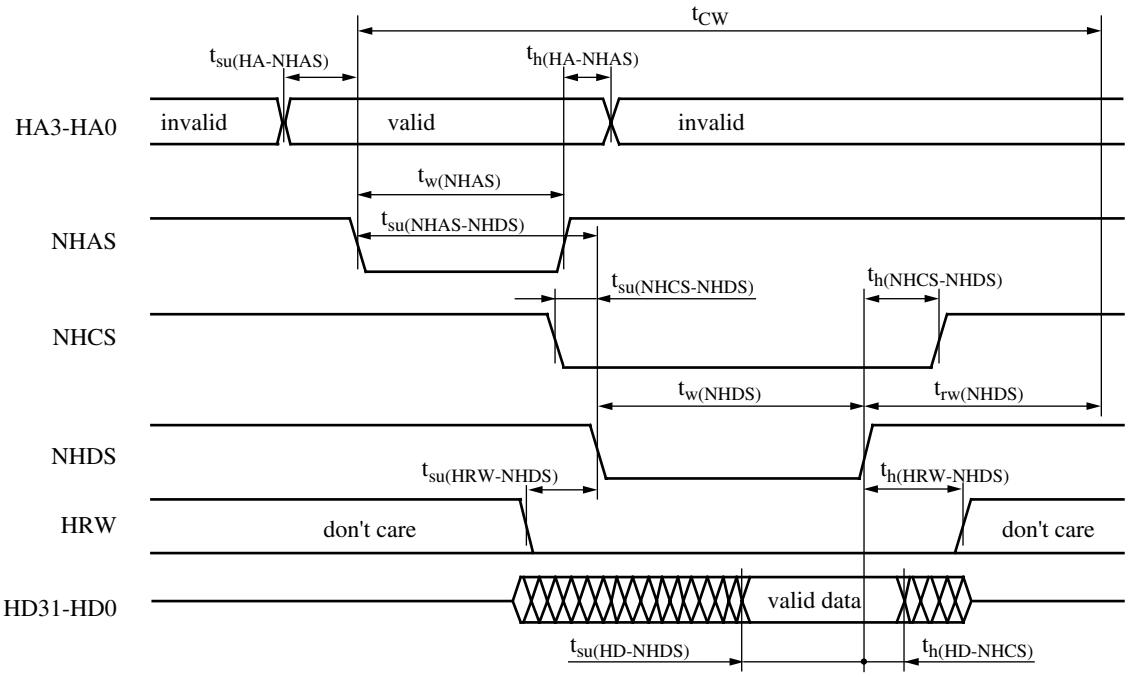
4. AC Characteristics (continued)

• Write Operation

The operation timing is as follows:

1. The value of the address to be written in HA3:0 must be set up before setting NHAS low. However, NHAS must be set low at $t_{su(NHAS-NHDS)}$ before NHDS is set low.
2. Hold NHAS low for the period $t_{w(NHAS)}$. After that, NHAS may be set high. However, HA3:0 must be fixed within the period $t_{h(HA-NHAS)}$ from the point NHAS is set high.
3. Set NHCS low at $t_{su(NHCS-NHDS)}$ before NHDS is set low. Also, HRW must be set low at $t_{SU(HRW-NHDS)}$ before NHDS is set low. HD31:0 will remain in the high-impedance state in case of setting HRW low even if NHCS is low.
4. Hold NHDS low for the period $t_{w(NHDS)}$. Set up the value of the data to be written in HD31:0 before setting NHDS high.
5. Set NHDS high. Hold HD31:0 fixed for the period $t_{h(HD-NHDS)}$ after setting NHDS high. After setting NHDS high, hold NHDS fixed at the high level for the period $t_{rw(NHDS)}$ until the next read or write operation.
6. After setting NHDS high and at least the time $t_{h(NHCS-NHDS)}$ has elapsed, set NHCS high. Note that HRW may be changed when at least the time $t_{h(HRW-NHDS)}$ has passed after NHDS was set high.

• Timing Chart (Write operation)



■ Electrical Characteristics (continued)

4. AC Characteristics (continued)

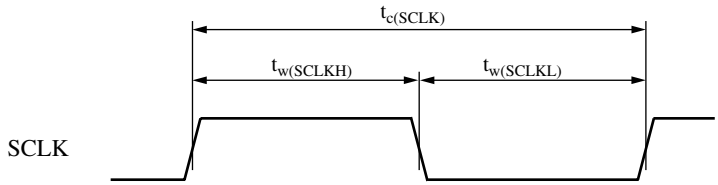
Parameter	Symbol	Min	Typ	Max	Unit
SCLK cycle time	$t_{c(SCLK)}$	—	37.0	—	ns
SCLK high-level pulse width	$t_{w(SCLKH)}$	14.0	—	—	ns
SCLK low-level pulse width	$t_{w(SCLKL)}$	14.0	—	—	ns
VCLK cycle time	$t_{c(VCLK)}$	37.0	—	—	ns
VCLK high-level pulse width	$t_{w(VCLKH)}$	14.0	—	—	ns
VCLK low-level pulse width	$t_{w(VCLKL)}$	14.0	—	—	ns
RCLK cycle time	$t_{c(RCLK)}$	30.0	—	—	ns
RCLK high-level pulse width	$t_{w(RCLKH)}$	12.0	—	—	ns
RCLK low-level pulse width	$t_{w(RCLKL)}$	12.0	—	—	ns

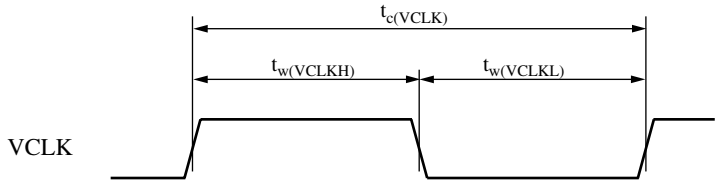
Note) The reason the allowable value of the SCLK cycle time is listed in the "Typ" column is to indicate that the MN85560 only has the SCLK cycle time specification of 37.0 ns (27.0 MHz). Thus, a frequency of over 27 MHz cannot be used. Furthermore, note that use of a frequency of less than 27 MHz involves changes to certain of the AC characteristics, and such specifications cannot be guaranteed for this product.

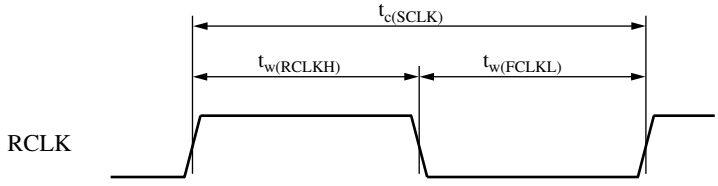
• Clock Signal Timing Chart

This section presents the timing of the clock signal input to the clock input pin.

A fixed value can be input to the code output clock RCLK, but only when the code output mode is set to parallel mode two bus cycle DMA transfer mode.







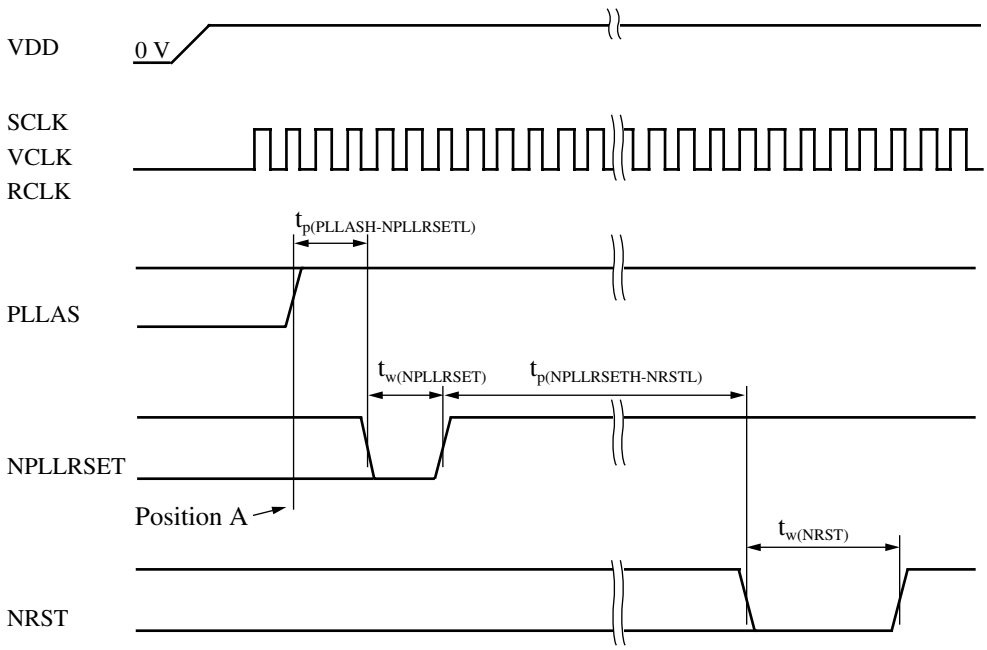
■ Electrical Characteristics (continued)

4. AC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Unit
PLL initialization operation wait time	$t_{p(PLLASH-NPLLRSETL)}$	50.0	—	—	ns
NPLLRSET low-level pulse width	$t_{w(NPLLRSET)}$	50.0	—	—	ns
Chip hardware reset wait time	$t_{p(NPLLRSETH-NRSTL)}$	100	—	—	µs
NRST low-level pulse width	$t_{w(NRST)}$	15	—	—	cycle*

Note) *: A number of clock cycles for the clock with the lowest frequency of the SCLK, VCLK, and RCLK clocks. (However, this does not apply for code output in parallel mode two bus cycle mode.)

• Timing Chart



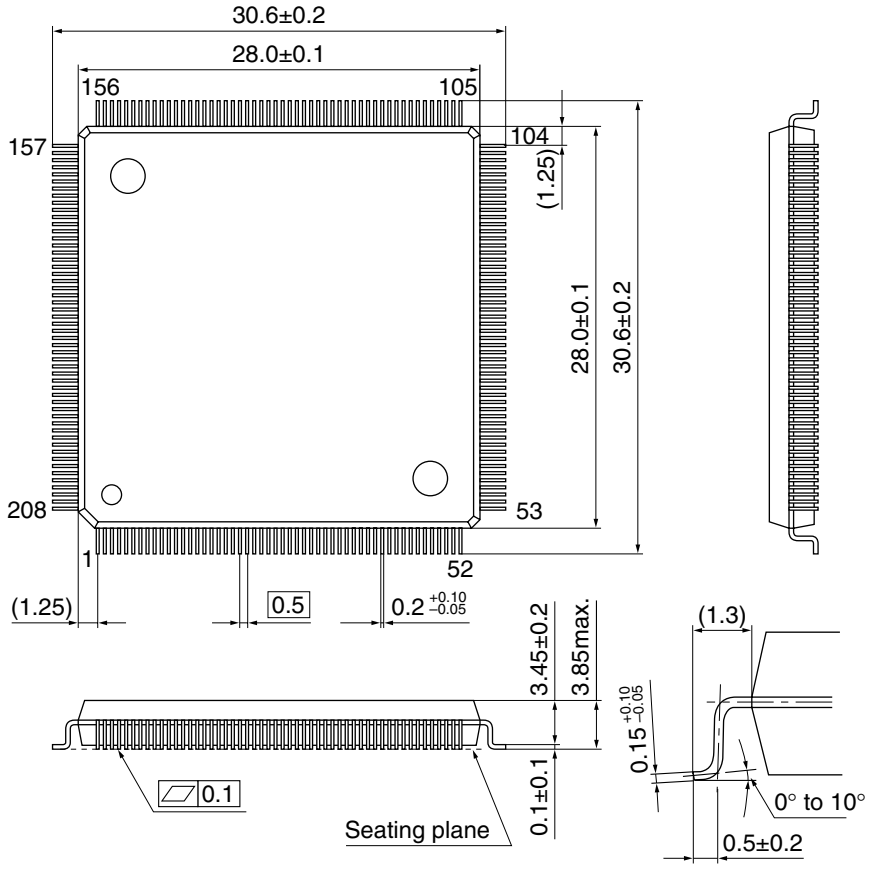
The MN85560 takes a 27 MHz signal input as the SCKL system clock and uses a PLL circuit to multiply that to 81 MHz. Therefore when powering up, the hardware reset signal must be asserted after the PLL oscillator has stabilized.

The pins used to start PLL operation are the PLL assert pin (PLLAS) and the PLL reset input pin (NPLLRSET). Note that the signal that performs the chip hardware reset is the chip initialization reset input pin (NRST).

The period that NRTS must be asserted is 15 cycles of the slowest of the SCLK, VCLK, and RCLK signals (for code output in parallel mode two bus cycle mode, the SCLK and VCLK signals). Stabilized signals must be provided to all input pins before asserting PLLAS (position A in the figure).

■ Package Dimensions (Unit: mm)

• QFP208-P-2828A



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