MN863831EFG

160-Output STN Segment Driver

■ Overview

The MN863831EFG is a 160-output segment driver IC for dot matrix (4-bit or 8-bit data input) STN LCD panels. It latches 4-bit or 8-bit parallel data transferred from an LCD controller and generates the LCD drive signals.

In combination with an LCD common driver IC, MN86372 series, this IC is optimal for implementing low-power LCD modules. Since this IC also provides an LCD drive voltage compensation function, it can implement high-quality LCD display modules with minimal crosstalk. It supports both color and monochrome displays.

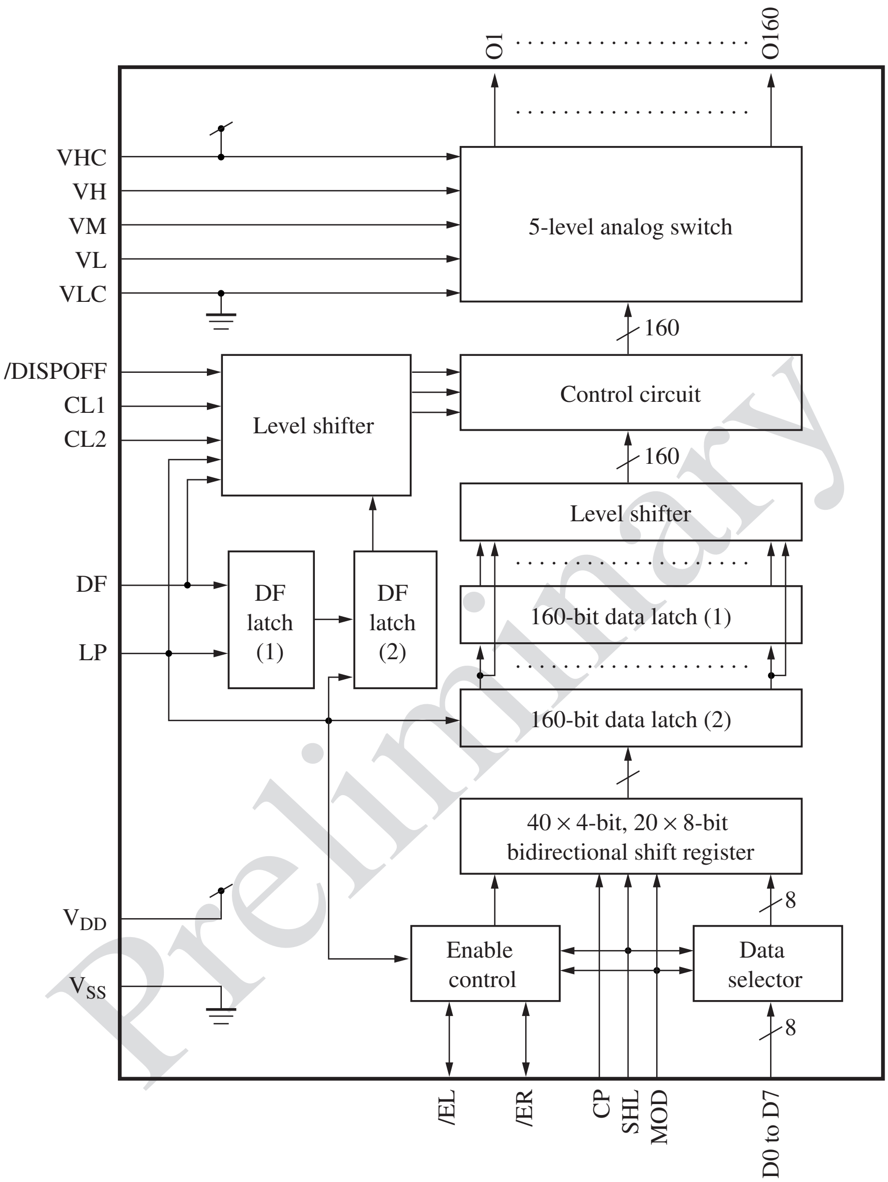
■ Features

- Supports LCD drive voltages up to 6.0 V.
- Provides 160 LCD drive outputs.
- Provides an LCD drive voltage compensation function to implement high-quality LCD display modules with minimal crosstalk.
- Inverts the LCD drive voltage by signal alternation.
- Provides 5 LCD drive voltage input pins: VHC, VH, VM, VL, and VLC
- Built-in voltage conversion block (level shifter) allows interfacing with LCD controllers with supply voltages in the range from 3.0 V to 5.5 V.
- Built-in bidirectional shift register allows arbitrary direction of the output data transfer and allows easy mounting in large-screen applications.
- Supports multistage cascade connection to drive high-resolution LCD panels.
- Supports both 4-bit and 8-bit parallel input mode.
- The 4-bit and 8-bit parallel input modes allow data rates 1/4 or 1/8 of those required with conventional serial transfer devices for lower power consumption.
- Provides a power saving function, in which all but one driver are set to standby mode and disable to input display data, for even lower power consumption in LCD modules with multistage cascade connection.

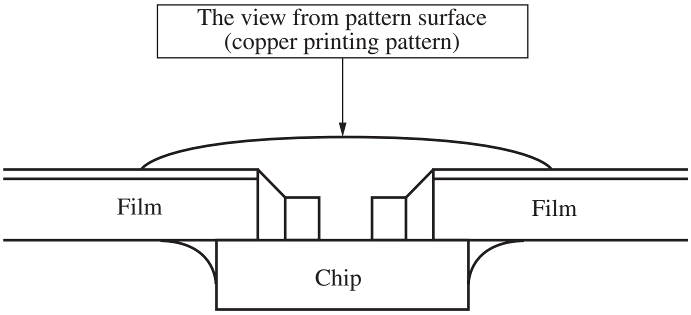
■ Applications

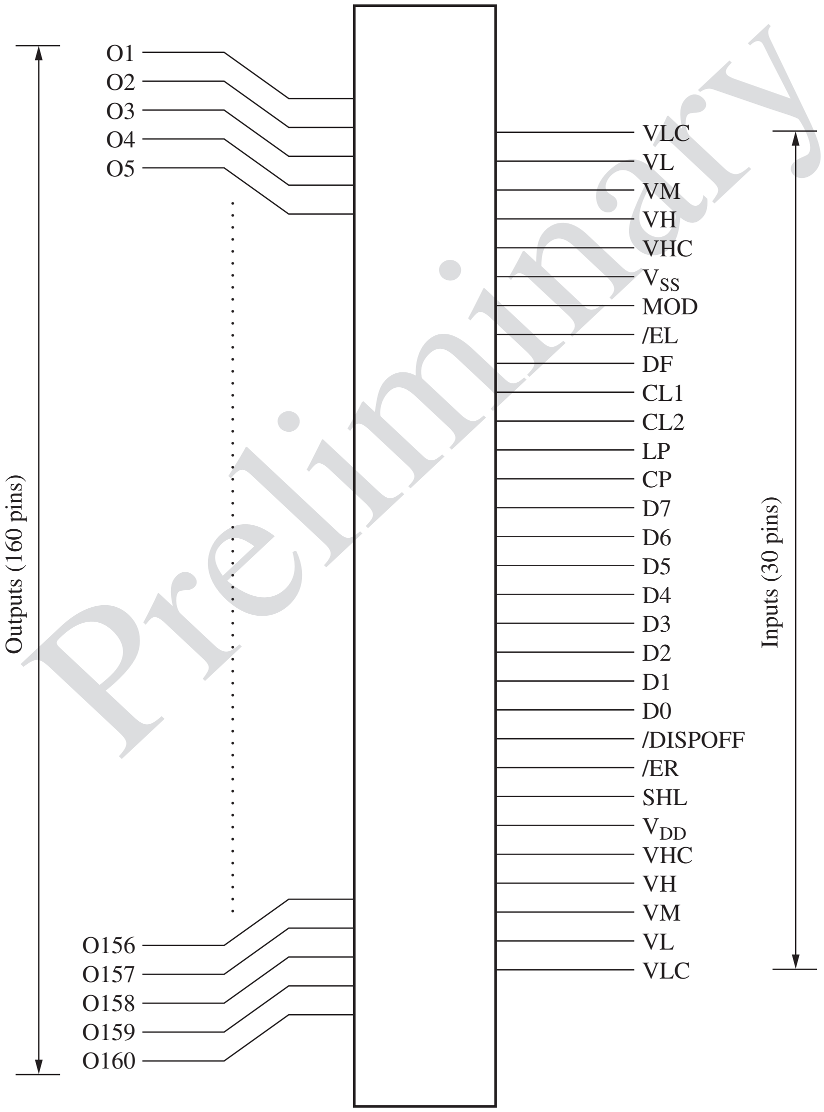
- Word processors, PDAs, and other portable information terminals

■ Block Diagram



■ Pin Arrangement





■ Pin Descriptions

Pin No.	I/O	Function	Description
D0 to D7	I	Display data inputs (8 bits)	Parallel input of display data in 4-bit or 8-bit units. • In 4-bit parallel input mode, the 4 pins D0 to D3 are used for data input. The 4 pins D4 to D7 should be tied to V_{DD} or V_{SS}. • In 8-bit parallel input mode, the 8 pins D0 to D7 are used for data input.
O1 to O160	O	LCD drive outputs	These pins output the LCD drive voltages.
SHL	I	Shift direction selection	Switches the shift register data shift direction, and the /ER and /EL pin I/O mode.
CP	I	Shift clock input	The shift register transfer clock input. The shift register operates on the falling edge of this signal.
LP	I	Latch signal input	The DF signal and the shift register data are latched on the falling edge of this signal, and the latched data is output.
/DISPOFF	I	Display off input	The LCD drive outputs output the VM level regardless of the data while this pin is low.
CL1	I	LCD compensation voltage (VHC and VLC) control	Controls the period for the LCD compensation voltage (VHC and VLC) output to the LCD drive output pins according to the display data.
CL2	I	LCD compensation voltage (VM) control	Controls the period for the LCD compensation voltage (VM) output to the LCD drive output pins according to the display data.
DF	I	Alternation signal input	Performs signal alternation for the LCD drive voltage.
V_{DD}	Power supply	Logic system power supply	Power supply used for the logic circuits
V_{SS}	Power supply	GND	GND
VH (2 pins)	Power supply	Drive power supply	LCD drive power supply
VL (2 pins)	Power supply	Drive power supply	LCD drive power supply
VM (2 pins)	Power supply	Drive power supply	LCD drive power supply, (LCD compensation power supply)
VHC (2 pins)	Power supply	Drive power supply	LCD drive power supply, (LCD compensation power supply) Used as the power supply for the LCD drive circuit.
VLC (2 pins)	Power supply	Drive power supply	LCD drive power supply, (LCD compensation power supply) Connected internally to the V_{SS} pin.
/EL	I/O	Enable signal input and output	Data input/output for the chip enable signal
/ER	I/O	Enable signal input and output	Data input/output for the chip enable signal
MOD	I	Mode selection (with a pull-up resistor)	(see table below)

MOD	
Low	4-bit parallel input
High	8-bit parallel input

■ Function Descriptions

1. Control circuit for bidirectional shift register

This IC includes two circuits, an enable control circuit and a data selector, that control the built-in bidirectional shift register.

1.1 Enable control circuit

This circuit consists of a base-40 counter circuit (for 4-bit parallel input mode), a base-20 counter circuit (for 8-bit parallel input mode), and a control circuit for the chip enable I/O circuit.

This counter counts clock pulses and outputs a carry on the falling edge of the 40th clock cycle (in 4-bit parallel input mode) or the 20th clock cycle (in 8-bit parallel input mode). This corresponds to the completion of the shift register data shift operation. This carry stops the data shift clock internally to the IC, and places the counter and the shift register in the stopped state. When LP signal goes high, the base-40 and base-20 counters are reset and set to the counter wait state (standby state).

The standby state is not cleared until the chip enable I/O signal (/EL and /ER) that corresponds to shift direction goes low. When that chip enable signal goes low, the data shift clock and counter start operating again.

When this IC is connected in the serial cascade form, the counter carry signal is used as the chip enable signal for the driver IC in the next stage. The result of this operation is that at the completion of each 40 clock cycles (in 4-bit parallel input mode) or 20 clock cycles (in 8-bit parallel input mode), the next driver IC in sequence goes to the active state and the total power consumption of the whole LCD panel is reduced.

1.2 Data selector circuit

This circuit determines, based on the state of the SHL pin, the data shift direction of the internal shift register and the I/O mode of the chip enable I/O pin as shown in tables 1-a and 1-b.

2. 40 × 4-bit (4-bit parallel input mode)/20 × 8-bit (8-bit parallel input mode) bidirectional shift register

The IC internal 4-bit parallel 40-stage and 8-bit parallel 20-stage bidirectional shift registers operate on the falling edge of the clock pulse.

In 4-bit parallel input mode, since the input data is divided into 4-bit parallel units, the shifting of the 160 output units of data requires 40 clock cycles. (See Timing Charts 1 and 3.)

In 8-bit parallel input mode, since the input data is divided into 8-bit parallel units, the shifting of the 160 output units of data requires 20 clock cycles. (See Timing Charts 2 and 4.)

The shift direction is selected by the SHL pin as shown in tables 1-a and 1-b.

3. 160-bit data latch (2)

The 160-bit data latch (2) holds the 160 bits of data acquired by the shift register for a single horizontal scan period (1H).

Data is latched on the falling edge of the LP signal, which is the start pulse for the horizontal scan period, held for 1H, and the next data is latched on the next falling edge on the LP signal.

Timing Chart 3 shows the shift register and latch operation for the first stage segment driver when multiple driver ICs are connected in series and operated in 4-bit parallel mode.

Also, Timing Chart 4 shows the shift register and latch operation for the first stage segment driver when multiple driver ICs are connected in series and operated in 8-bit parallel mode.

■ Function Descriptions (continued)

4. Level shifters

The level shifters convert levels from the logic circuit signal levels (V_{DD} = high, V_{SS} = low) to the signal levels (VHC = high, VLC = V_{SS} = low) used by the LCD drive circuits, such as the analog switches. The IC includes two types of level shifters, one is for 160 bits display data and the other is for control signals.

5. 160-bit data latch (1)

The 160-bit data latch (1) holds the 160 bits of display data acquired by the 160-bit data latch (2) for an additional 1H. Thus the 160-bit data latch (1) holds the data for the previous line from the display data currently being scanned.

Data is latched on the falling edge of the LP signal, held for 1H, and the next data is latched on the next falling edge on the LP signal.

6. 5-level analog switch

The 5-level analog switch is controlled by the control circuit and selects one of the 5 drive voltages (VHC, VH, VM, VL, and VLC), and outputs the selected levels to the 160 LCD drive output pins.

7. DF latch (1)

The DF latch (1) holds the DF data for a single horizontal scan period (1H).

Data is latched on the rising edge of the LP signal, which is the start pulse for the horizontal scan period, held for 1H, and the next data is latched on the next rising edge on the LP signal.

8. DF latch (2)

The DF latch (2) latches the data acquired by the DF latch (1) on the falling edge of the LP signal, holds that data for 1H, and latches the next data on the next falling edge of the LP signal.

(Timing Charts 3 and 4 show this latch operation.)

9. Control circuit

The voltage selected by the 5-level analog switch is determined by the 160-bit data latch (1), the 160-bit data latch (2), the /DISPOFF signal, the CL1 signal, the CL2·$\overline{\text{LP}}$ signal, the DF input, and DF latch (2).

When the /DISPOFF signal is low, the VM level of the LCD drive voltage is selected, regardless of the values of the data latches (1) and (2) outputs, the DF input, the DF latch (2) output, and the high/low state of the CL1 and CL2·$\overline{\text{LP}}$ signals. When the /DISPOFF signal is low, the VM level is output from the common driver, and the voltage applied to all of the dots becomes 0 V, since the same voltage is applied. This results in a completely blank display.

When either the CL1 or CL2·$\overline{\text{LP}}$ signal is high, the IC switches the LCD drive voltage and the LCD compensation voltage by comparing the data latch (1) and (2) outputs with the DF input and the DF latch (2) output.

Table 2 lists the LCD drive output pin output voltage levels according to the data latch (1) output (Qn-1), the data latch (2) output (Qn), the CL1 and CL2·$\overline{\text{LP}}$ signals, the DF input, the DF latch (2) output (DFn-1), and the /DISPOFF signal.

Figure 1 presents examples of the LCD drive output pin waveform as driven according to table 2, which appears later. Two examples are presented, one with the DF pin held high, and the other with an LCD alternation signal input to the DF pin.

■ Function Descriptions (continued)

Table 1-a. Data shift control — In 4-bit parallel input mode (MOD = low)

SHL	/ER	/EL			Shift clock						
					1	2	···	n	···	39	40
Low	Input	Output	D3	→	O160	O156	···	O4(40–n)+4	···	O8	O4
			D2	→	O159	O155	···	O4(40–n)+3	···	O7	O3
			D1	→	O158	O154	···	O4(40–n)+2	···	O6	O2
			D0	→	O157	O153	···	O4(40–n)+1	···	O5	O1
High	Output	Input	D3	→	O1	O5	···	O4n–3	···	O153	O157
			D2	→	O2	O6	···	O4n–2	···	O154	O158
			D1	→	O3	O7	···	O4n–1	···	O155	O159
			D0	→	O4	O8	···	O4n	···	O156	O160

Table 1-b. Data shift control — In 8-bit parallel input mode (MOD = high)

SHL	/ER	/EL			Shift clock						
					1	2	···	n	···	19	20
Low	Input	Output	D7	→	O160	O152	···	O8(20–n)+8	···	O16	O8
			D6	→	O159	O151	···	O8(20–n)+7	···	O15	O7
			D5	→	O158	O150	···	O8(20–n)+6	···	O14	O6
			D4	→	O157	O149	···	O8(20–n)+5	···	O13	O5
			D3	→	O156	O148	···	O8(20–n)+4	···	O12	O4
			D2	→	O155	O147	···	O8(20–n)+3	···	O11	O3
			D1	→	O154	O146	···	O8(20–n)+2	···	O10	O2
			D0	→	O153	O145	···	O8(20–n)+1	···	O9	O1
High	Output	Input	D7	→	O1	O9	···	O8n–7	···	O145	O153
			D6	→	O2	O10	···	O8n–6	···	O146	O154
			D5	→	O3	O11	···	O8n–5	···	O147	O155
			D4	→	O4	O12	···	O8n–4	···	O148	O156
			D3	→	O5	O13	···	O8n–3	···	O149	O157
			D2	→	O6	O14	···	O8n–2	···	O150	O158
			D1	→	O7	O15	···	O8n–1	···	O151	O159
			D0	→	O8	O16	···	O8n	···	O152	O160

■ Function Descriptions (continued)

Table 2. LCD drive output pin output voltage

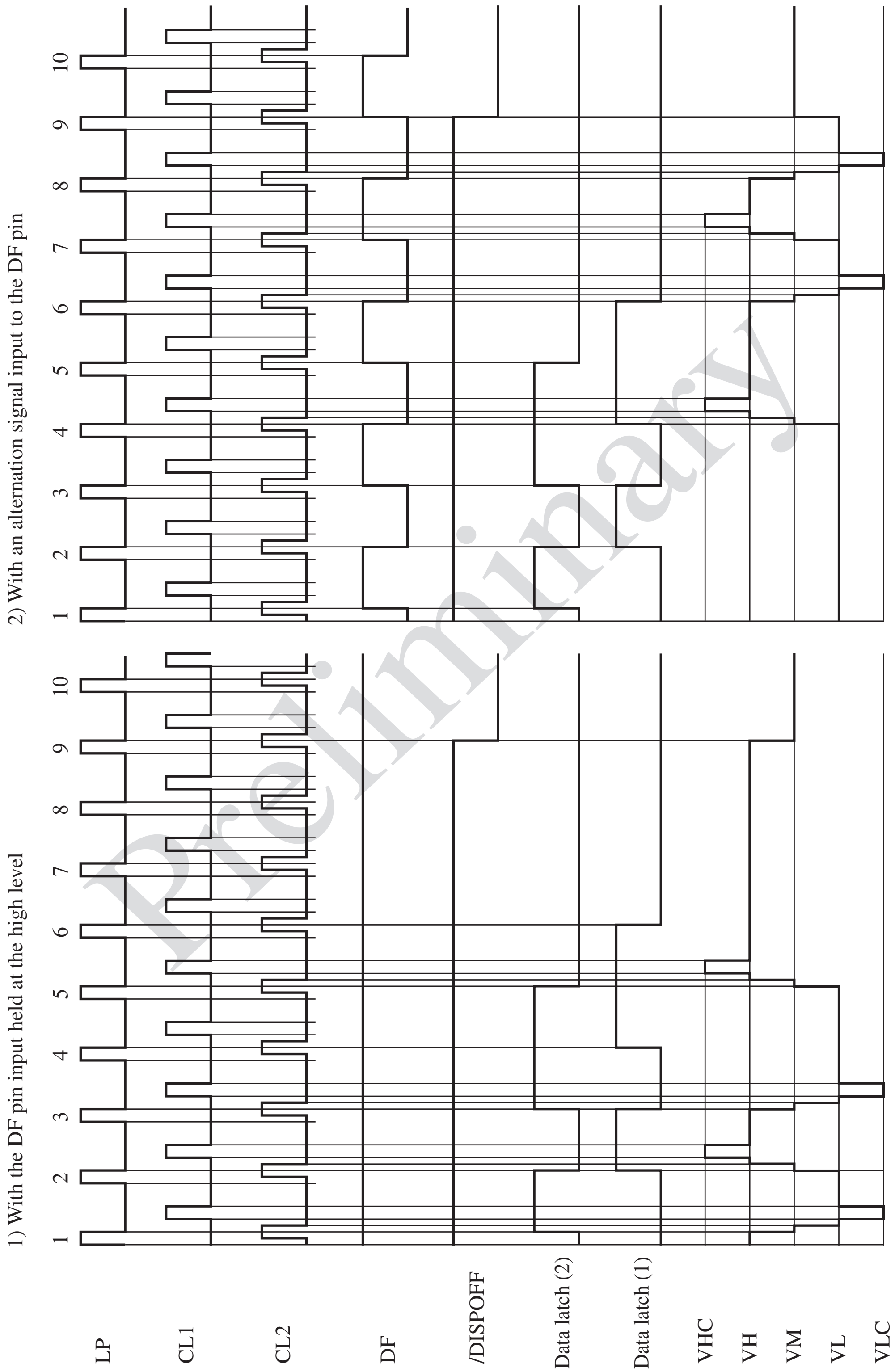
/DISPOFF	CL1	CL2 · $\overline{LP}$	DF latch (2) output DFn-1	DF input	Data latch (1) output Qn-1	Data latch (2) output Qn	LCD drive output O1 to O160
High	High	Low	High	High	High	High	VL
						Low	VHC
					Low	High	VLC
						Low	VH
				Low	High	High	VHC
						Low	VL
					Low	High	VH
						Low	VLC
			Low	High	High	High	VLC
						Low	VH
					Low	High	VL
						Low	VHC
				Low	High	High	VH
						Low	VLC
					Low	High	VHC
						Low	VL
	Low	High	High	High	High	High	VL
						Low	VM
					Low	High	VM
						Low	VH
				Low	High	High	VM
						Low	VL
					Low	High	VH
						Low	VM
			Low	High	High	High	VM
						Low	VH
					Low	High	VL
						Low	VM
				Low	High	High	VH
						Low	VM
					Low	High	VM
						Low	VL
		Low	*	High	*	High	VL
						Low	VH
				Low		High	VH
						Low	VL
Low	*	*	*	*	*	*	VM

Note) 1. *: Don't care

2. The timing charts for the IC blocks are presented on the following pages.
3. The IC is specified to operate as follows: when the DF input is high, the output is inverted with respect to the actual input data.
4. To provide correct display, either the input data must be inverted, or an input to the DF pin that is inverted with respect to that of the common driver must be provided.

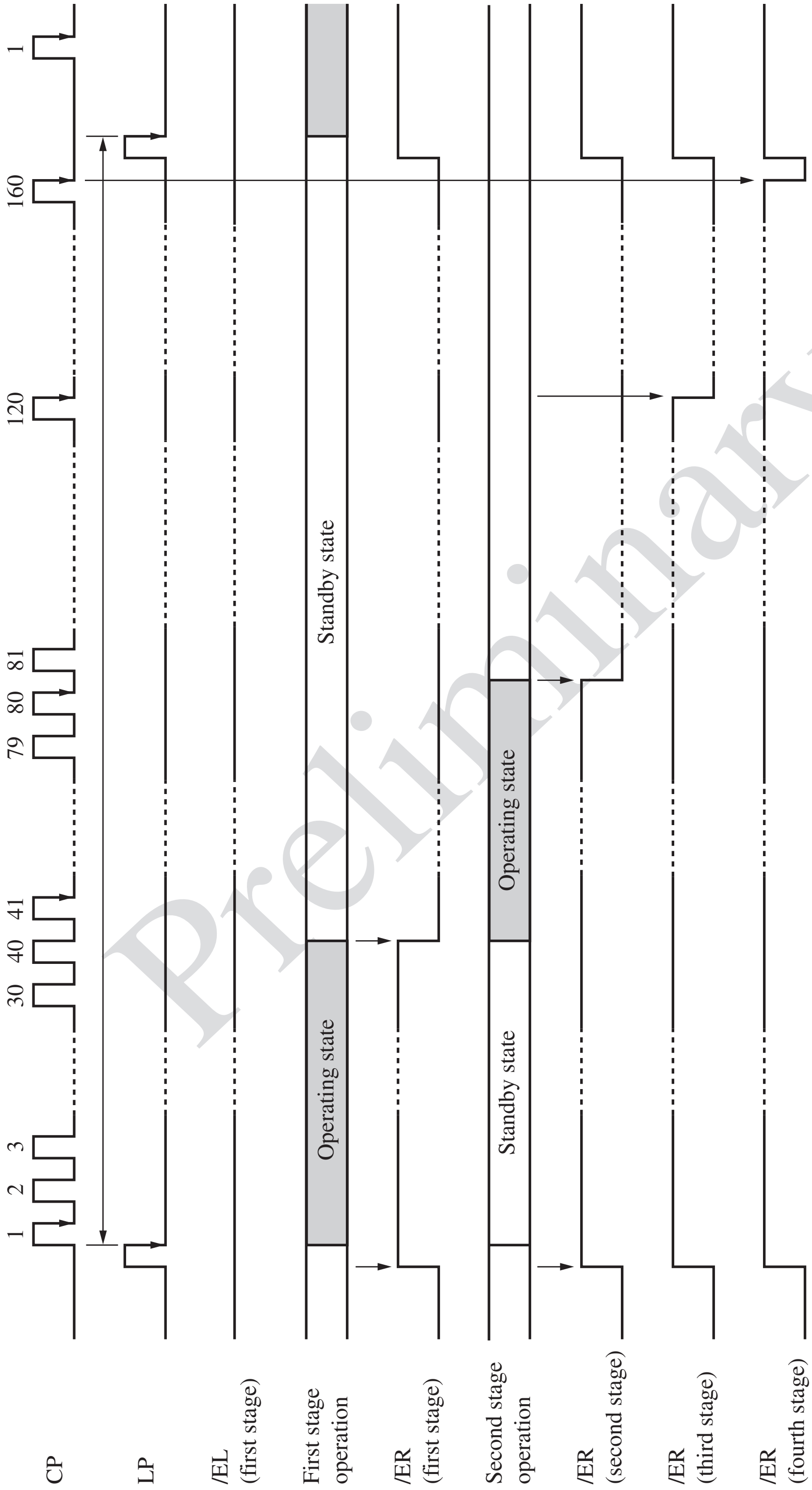
■ Function Descriptions (continued)

Figure 1. LCD drive output waveform examples



■ Timing Charts

1. Counter and chip enable pins (4-bit parallel input mode)



Note) 1. When 4 ICs are connected in serial cascade form (VGA monochrome display panel)

2. $f_{LP} = f_{CP} /160$

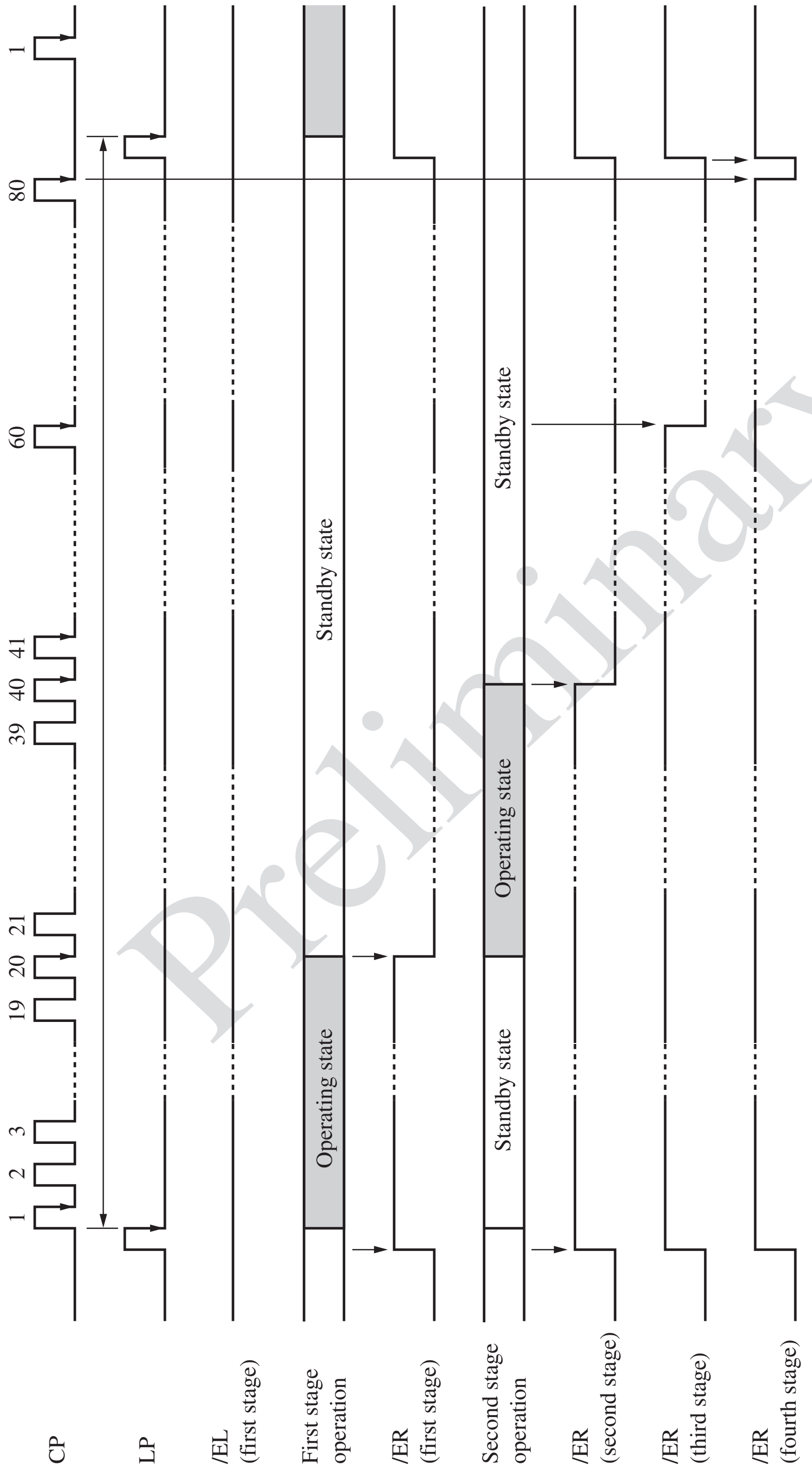
3. SHL = high

Note that when SHL is low, the only difference is that the /ER and /EL in input and output will be reversed. In the above timing chart, /EL becomes /ER and /ER becomes /EL.

4. MOD = low

■ Timing Charts (continued)

2. Counter and chip enable pins (8-bit parallel input mode)



Note) 1. When 4 ICs are connected in serial cascade form (VGA monochrome display panel)

2. $f_{LP} = f_{CP}$ /80

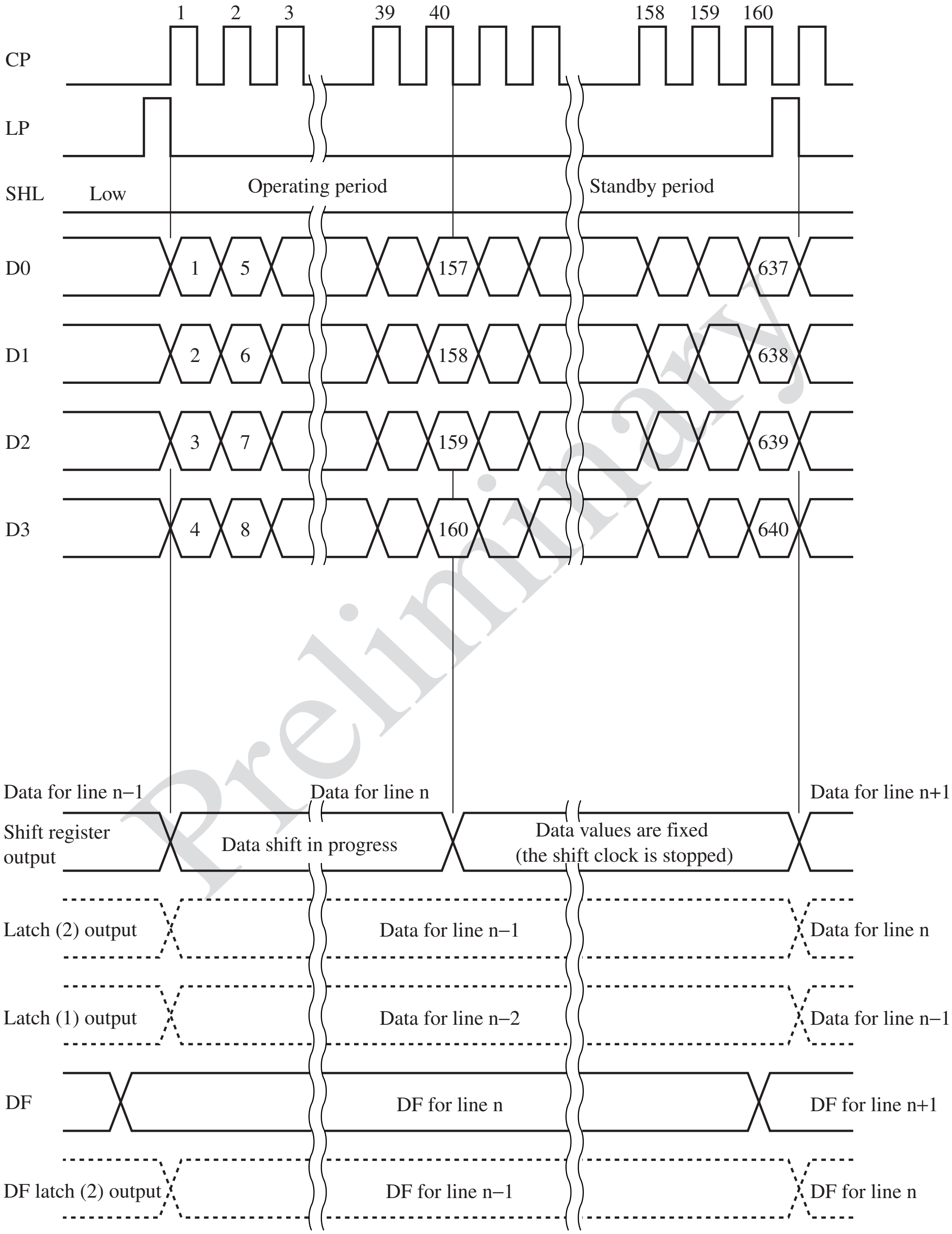
3. SHL = high

Note that when SHL is low, the only difference is that the /ER and /EL in input and output will be reversed. In the above timing chart, /EL becomes /ER and /ER becomes /EL.

4. MOD = high

■ Timing Charts (continued)

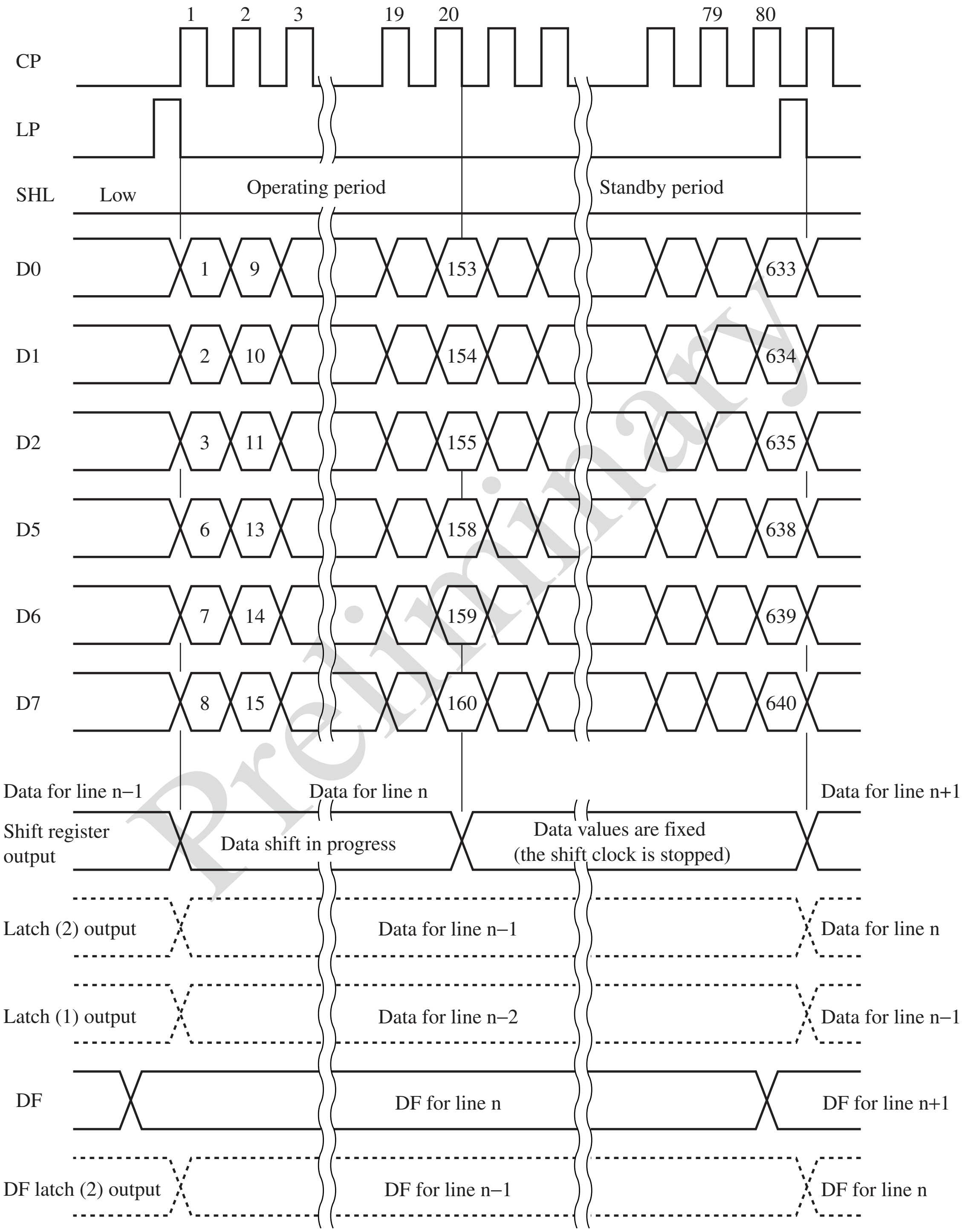
3. Shift register and latch operation (VGA monochrome display panel)



Note) $f_{LP} = f_{CP} /160$

■ Timing Charts (continued)

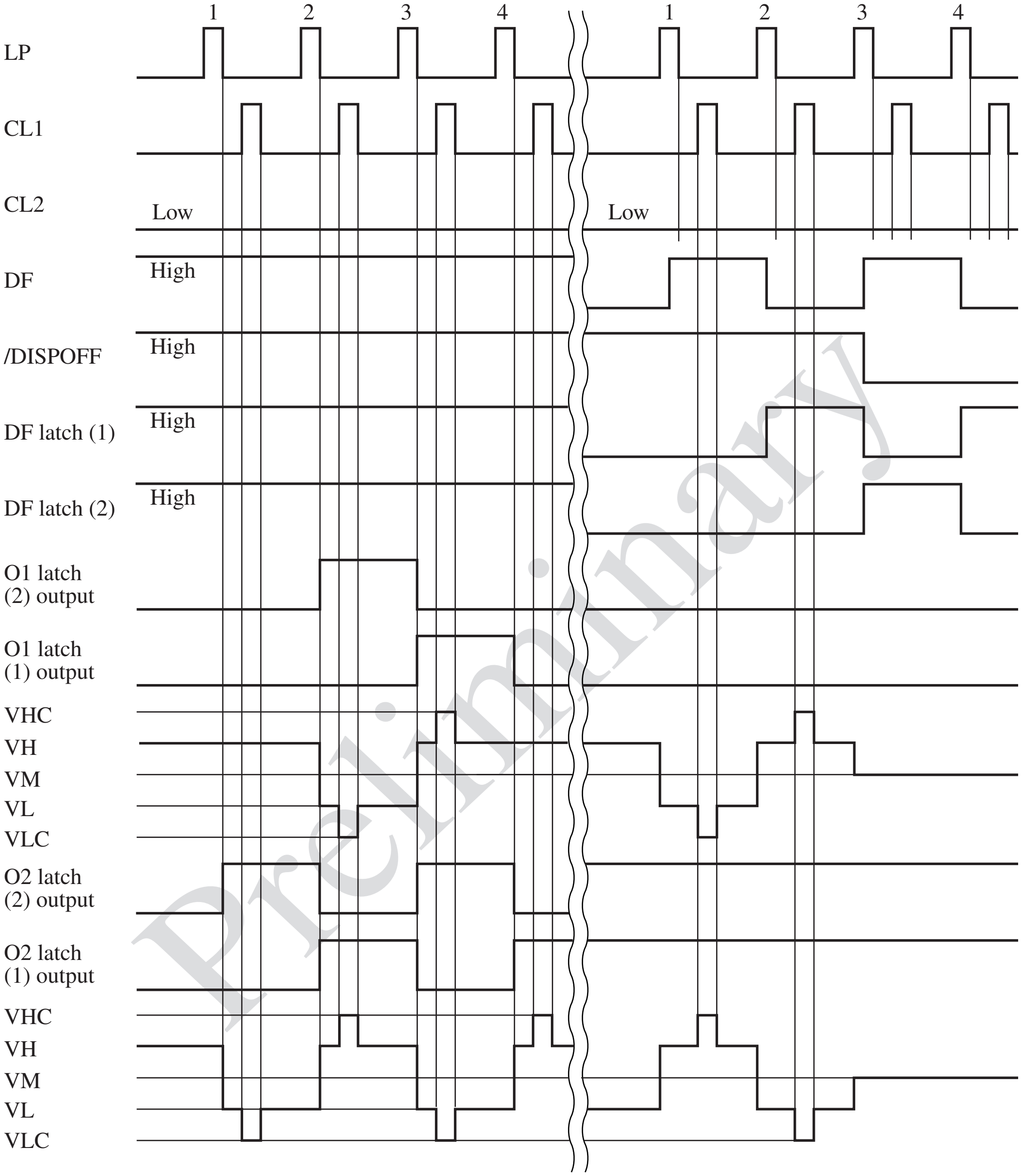
4. Shift register and latch operation (VGA monochrome display panel)



Note) $f_{LP} = f_{CP}/80$

■ Timing Charts (continued)

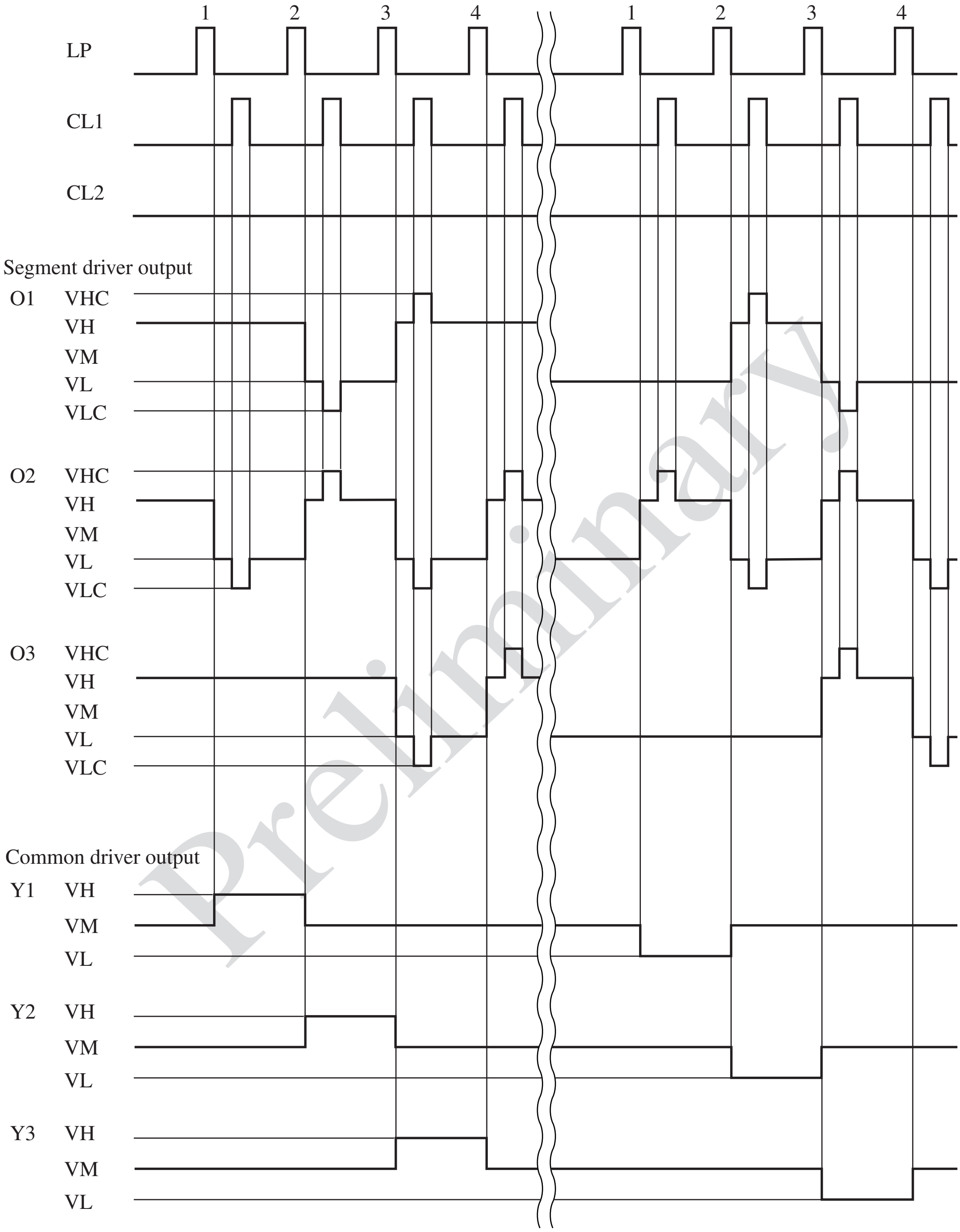
5. Segment driver LCD output



Note) The figure above shows the correspondence between the latch (1) and latch (2) data (DF latch (1) and DF latch (2)); the O1 and O2 drive voltages.

■ Timing Charts (continued)

6. Segment and common driver LCD output waveforms (when /DISPOFF is high)



■ Timing Charts (continued)

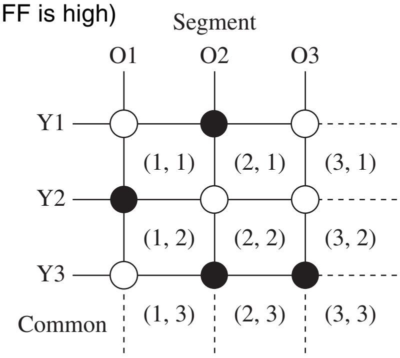
7. LCD display and LCD applied voltage waveforms (when /DISPOFF is high)

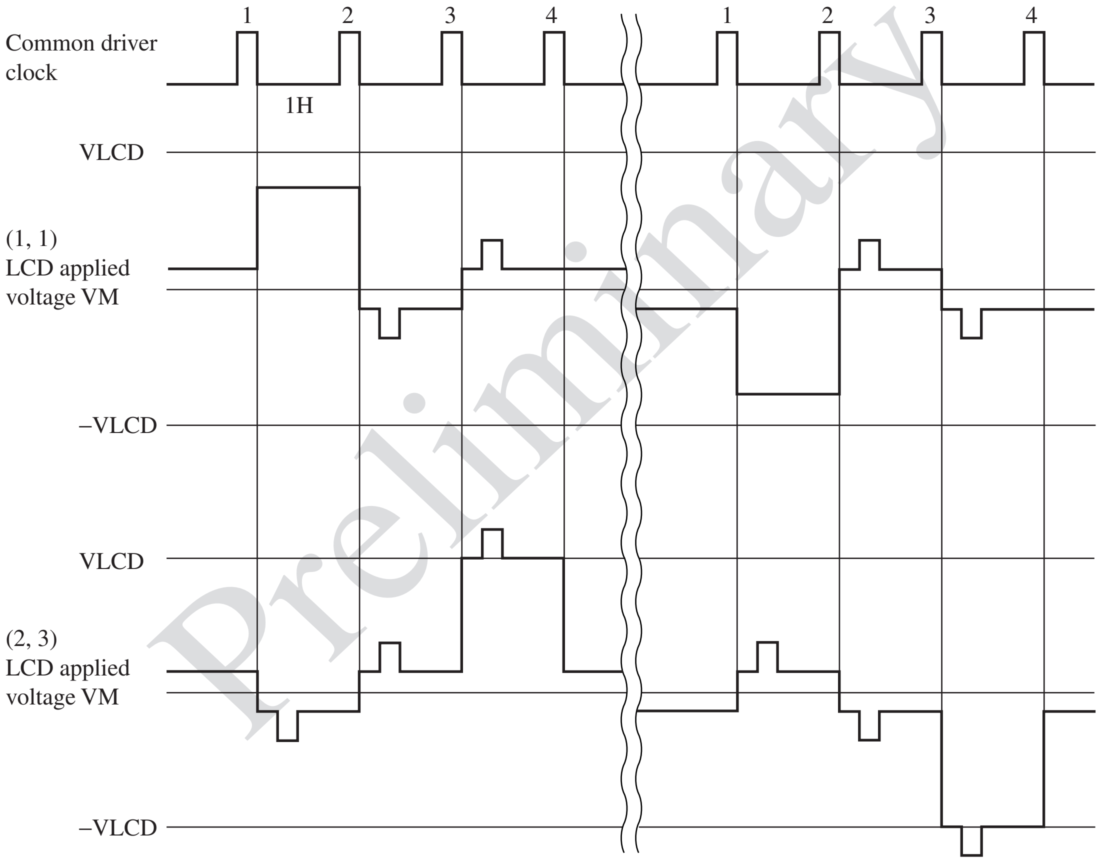
When the drive outputs shown in section 6 are applied, if the display is normally white, the display will be shown in the right figure.

If the display is normally black, then the display will be set up for black/white reversed display. The waveforms of the voltages applied to (1,1) and (2,3) dots in the right figure are shown below.

Note that the applied voltages are referenced to the common side drive voltage VM, and therefore displayed as $V_{COM}-V_{SEG}$.

$VLCD = V_{COM}-V_{SEG}$



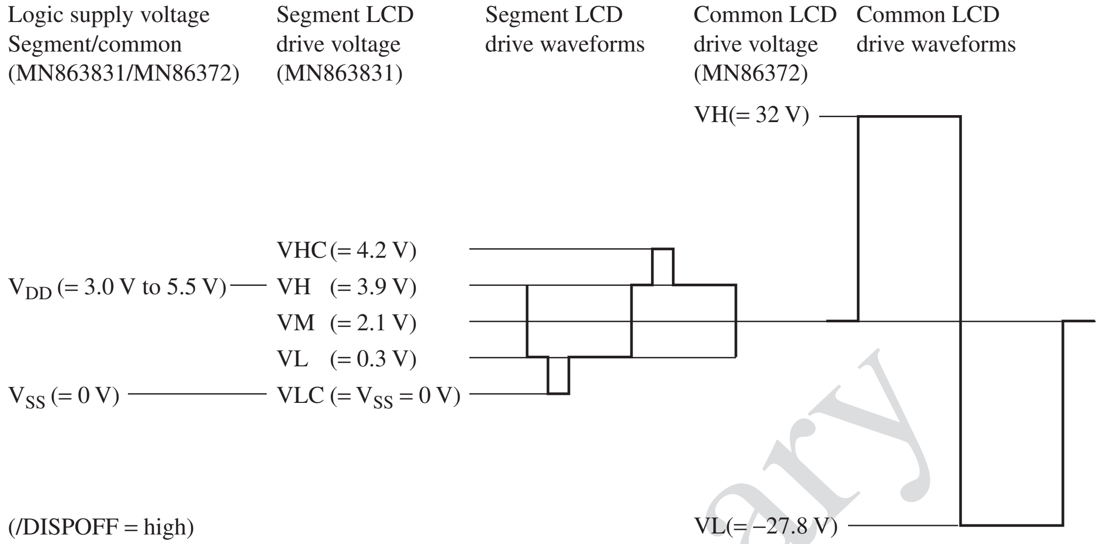


Note) 1. When the LCD voltage applied to a dot is ±VLCD, it will be displayed as black in normally white mode and as white in normally black mode.

2. Since the drive waveform is dulled at the segment drive waveform transition and the actual voltage drops, this IC applies the compensation voltage at the drive waveform transition to compensate the actual voltage.

■ LCD Drive Voltage Names and Relationships (Reference)

The figure presents the LCD drive voltage provided by this IC and the MN86372 series common drivers, and the relationships between those voltages.



■ Electrical Characteristics

1. Absolute Maximum Ratings at V_{SS} = 0 V, T_a = 25°C

Parameter	Symbol	Rating	Unit
Supply voltage 1	V_{DD}	– 0.3 to +7.0	V
Supply voltage 2	VHC	– 0.3 to +7.0	V
Drive voltage	V_n	– 0.3 to VHC+0.3	V
Input voltage	VIN	– 0.3 to V_{DD}+0.3	V
Operating temperature	T_{opr}	–20 to +75	°C
Storage temperature	T_{stg}	–40 to +125	°C

Note) 1. The absolute maximum ratings are limiting values for applied stresses below which the chip will not be destroyed. Operation is not guaranteed within these ranges.
2. These ratings are guarantees that apply when the standard Matsushita packages are used.
3. The term V_n above refers to VHC, VH, VM, VL, and VLC. These must be set up so that the following conditions hold: VHC≥VH≥VM≥VL≥VLC=V_{SS}.
4. When power is first applied, certain voltage application sequences may result in large currents flowing in this IC and permanent damage to the IC. To prevent this, always apply the logic system power supply levels (V_{DD} and V_{SS}) first, and only after those levels are established apply the LCD drive system power supply levels. Note that the conditions in note 3 above must be met at all times during this process.

2. Operating Conditions at V_{SS} = 0 V, T_a = –20°C to 75°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}		3.0	3.3	5.5	V
Drive voltage	VHC		3.0	4.2	6.0	V
Drive voltage	VH		VHC–0.7	VHC–0.3	VHC	V
Drive voltage	VM		VL	—	VH	V
Drive voltage	VL		0	0.3	0.7	V

■ Electrical Characteristics (continued)

2. Operating Conditions at V_{SS} = 0 V, T_a = –20°C to 75°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Clock frequency	f_{cp}		—	—	30	MHz
Digital signal input pin capacitance †1	C_{in}	At 1 MHz	—	6	—	pF
Rise and fall time for CP, LP, and D0 to D7	t_r, t_f		—	—	4 †2	ns

Note) 1. †1: CP, D0 to D7

†2: The following condition must be met: t_r, $t_f \leq 1/2(1/f-2t_w)$

Here, f is the frequency used and t_w is the minimum pulse width.

2. The VLC drive voltage is shorted to V_{SS} internally to the IC. Thus VLC = V_{SS}.
3. Connect directly each of the multiple drive supply pins of VHC, VH, VM, VL, and VLC.

3. DC Characteristics at V_{SS} = 0 V, V_{DD} = 3.0 V to 5.5 V, T_a = –20°C to +75°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating supply current	I_{DD}	f_{CP} = 20 MHz f_{Dn} = 10 MHz f_{LP} = 36 kHz	—	2	6	mA
Quiescent supply current (8-bit parallel input mode)	I_{SS1}	In the clock stopped state with MOD = open	—	—	100	µA
Quiescent supply current (4-bit parallel input mode)	I_{SS2}	In the clock stopped state with MOD = low	—	—	500	µA
1) Input Pins (SHL, CP, LP, CL1, CL2, DF, D0 to D7, /DISPOFF)						
High-level input voltage	V_{IH1}		$0.7 \times V_{DD}$	—	V_{DD}	V
Low-level input voltage	V_{IL1}		0	—	$0.3 \times V_{DD}$	V
Input leakage current	I_{LI1}		–10	—	10	µA
2) Input with Pull-up Resistor Pins (MOD)						
High-level input voltage	V_{IH2}		$0.7 \times V_{DD}$	—	V_{DD}	V
Low-level input voltage	V_{IL2}		0	—	$0.3 \times V_{DD}$	V
Pull-up resistance	R_{PU2}	V_{DD} = 3.3 V, MOD = 0 V	30	100	300	KΩ
3) I/O Pins (/ER, /EL)						
High-level input voltage	V_{IH3}		$0.7 \times V_{DD}$	—	V_{DD}	V
Low-level input voltage	V_{IL3}		0	—	$0.3 \times V_{DD}$	V
Input leakage current	I_{LI3}		–10	—	10	µA
High-level output voltage	V_{OH3}	I_{OH} = – 0.5 mA	V_{DD}– 0.5	—	—	V
Low-level output voltage	V_{OL3}	I_{OL} = 0.5 mA		—	0.5	V
Output leakage current	I_{LO3}		–10	—	10	µA

■ Electrical Characteristics (continued)

3. DC Characteristics at V_{SS} = 0 V, V_{DD} = 3.0 V to 5.5 V, T_a = –20°C to +75°C (continued)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
4) LCD Drive Outputs (O1 to O160)		V_{SS} = 0 V, V_{DD} = 3.0 V, T_a = –20°C to +75°C					
Output on resistance	R_{ON}	VHC = 4.2 V	VHC	—	450	900	Ω
		VH = 3.9 V	VH	—	450	900	
		VM = 2.1 V	VM	—	450	900	
		VL = 0.3 V	VL	—	450	900	
		VLC = 0.0 V V_n–V_O = 0.5 V V_O: Applied voltage of O1 to O160	VLC	—	450	900	
Output on resistance Variations between drive voltages	R_{ON1}	VHC = 4.2 V VH = 3.9 V		—	—	200	Ω
Output on resistance Variations between pins	R_{ON2}	VM = 2.1 V VL = 0.3 V VLC = 0.0 V		—	—	200	Ω

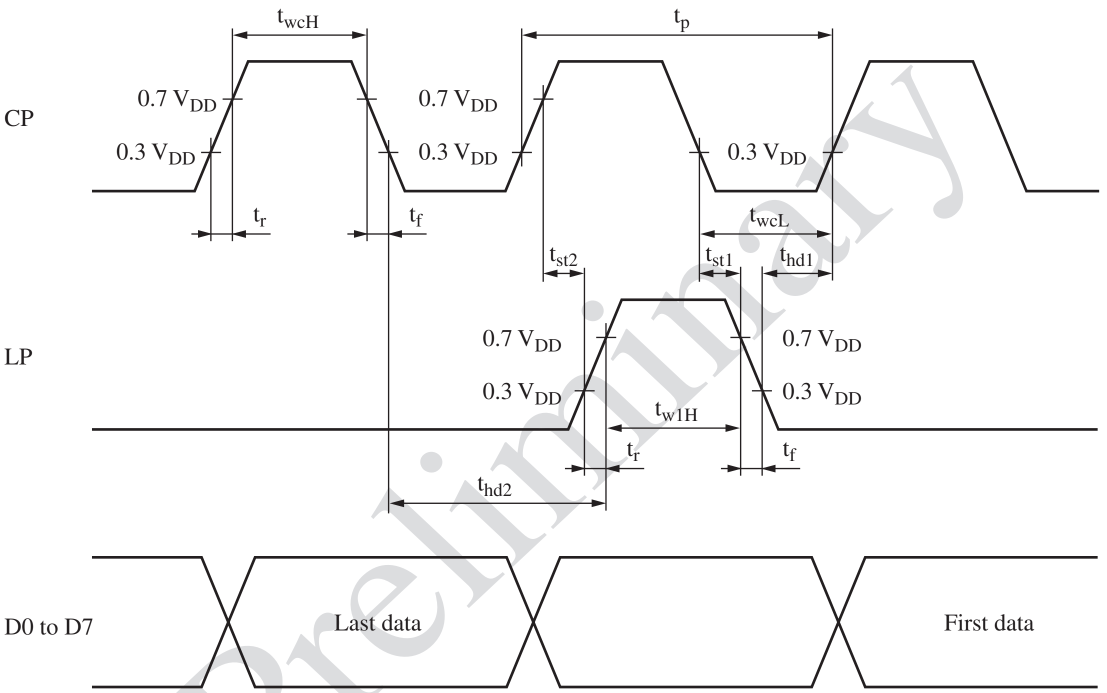
4. AC Characteristics at V_{SS} = 0 V, V_{DD} = 3.0 V to 5.5 V, T_a = –20°C to +75°C

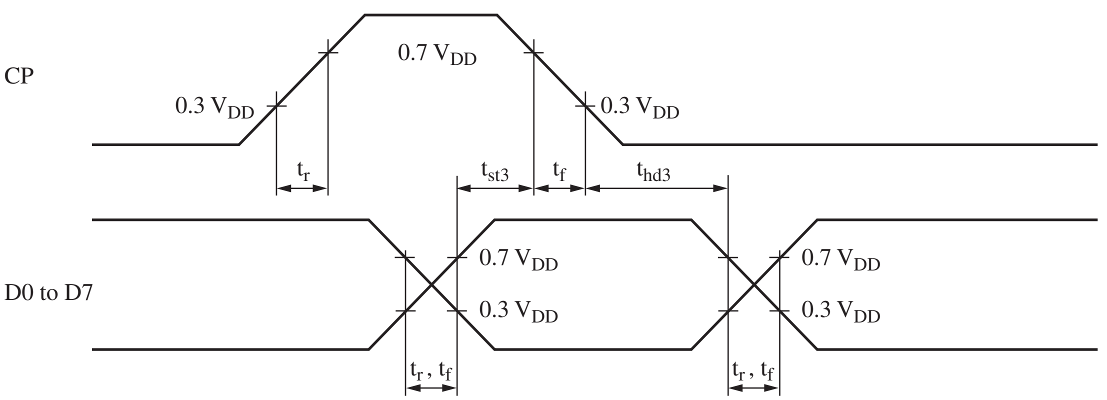
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
CP cycle time	t_p		33.3	—	—	ns
CP high-level period	t_{wcH}		10	—	—	ns
CP low-level period	t_{wcL}		10	—	—	ns
LP high-level period	t_{wlH}		40	—	—	ns
LP setup time 1	t_{st1}	CP-LP	15	—	—	ns
LP setup time 2	t_{st2}	CP-LP	10	—	—	ns
LP hold time 1	t_{hd1}	CP-LP	15	—	—	ns
LP hold time 2	t_{hd2}	CP-LP	50	—	—	ns
Data setup time	t_{st3}	CP-Dx	10	—	—	ns
Data hold time	t_{hd3}	CP-Dx	10			ns
Carry signal setup time	t_{st4}		12	—	—	ns
Carry signal output delay time	t_{d1}		—	—	21	ns
LP rising edge to CL2 rising edge time	t_{lc1}		18	—	—	ns
CL2 rising edge to LP falling edge time	t_{cl1}		18	—	—	ns
CL2 falling edge to CL1 rising edge time	t_{cc}		2	—	—	µs
LP rising edge to DF rising edge time, DF falling edge time	t_{ld}		40	—	—	ns

■ Electrical Characteristics (continued)

4. AC Characteristics at V_{SS} = 0 V, V_{DD} = 3.0 V to 5.5 V, T_a = –20°C to +75°C (continued)

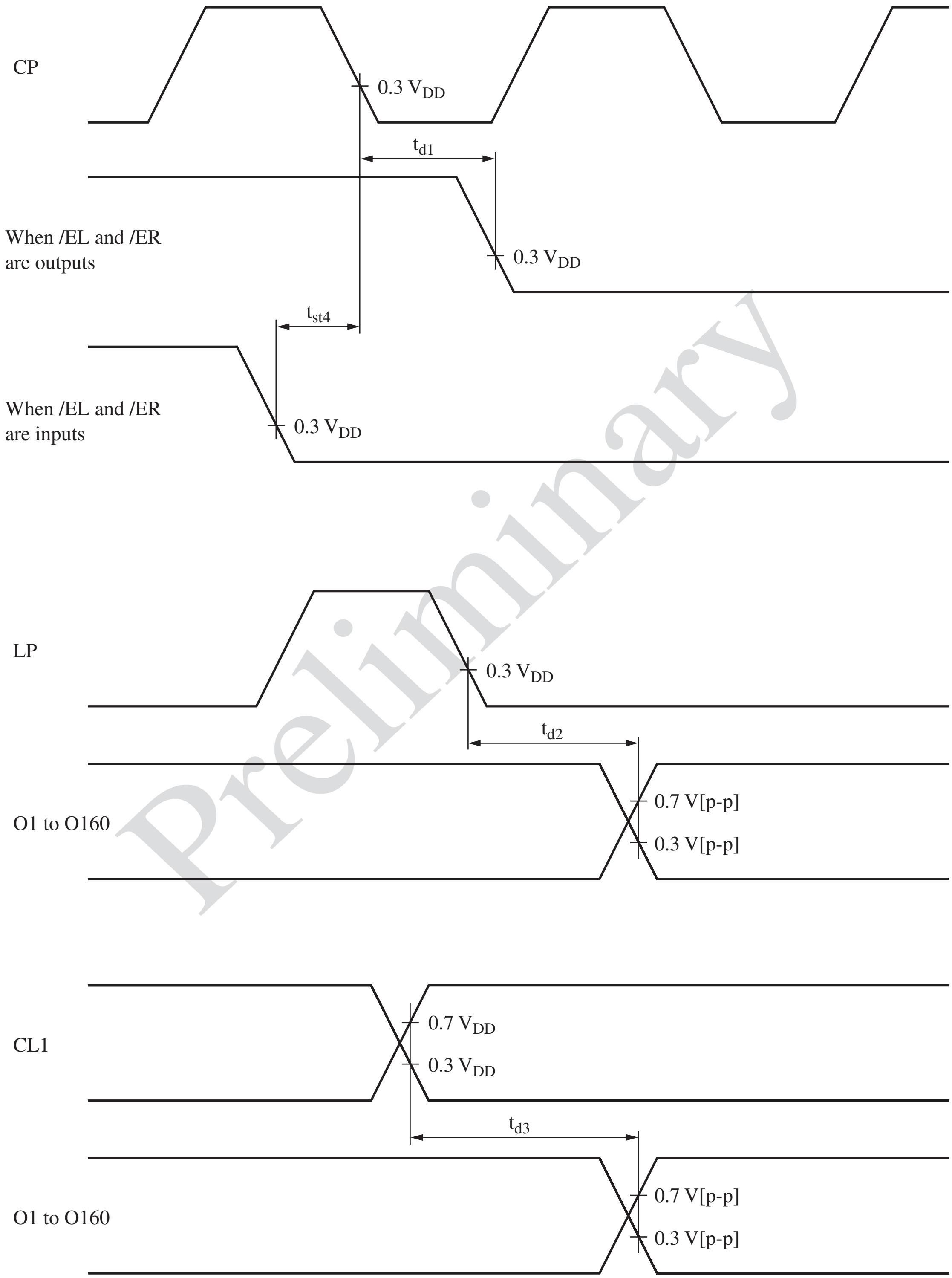
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
LCD drive signal output delay time 1	t_{d2}	LP→O_n	—	—	250	ns
LCD drive signal output delay time 2	t_{d3}	CL1→O_n	—	—	250	ns
LCD drive signal output delay time 3	t_{d4}	CL2→O_n	—	—	250	ns
LCD drive signal output delay time 4	t_{d5}	DF→O_n	—	—	250	ns
LCD drive signal output delay time 5	t_{d6}	/DISPOFF→O_n	—	—	250	ns





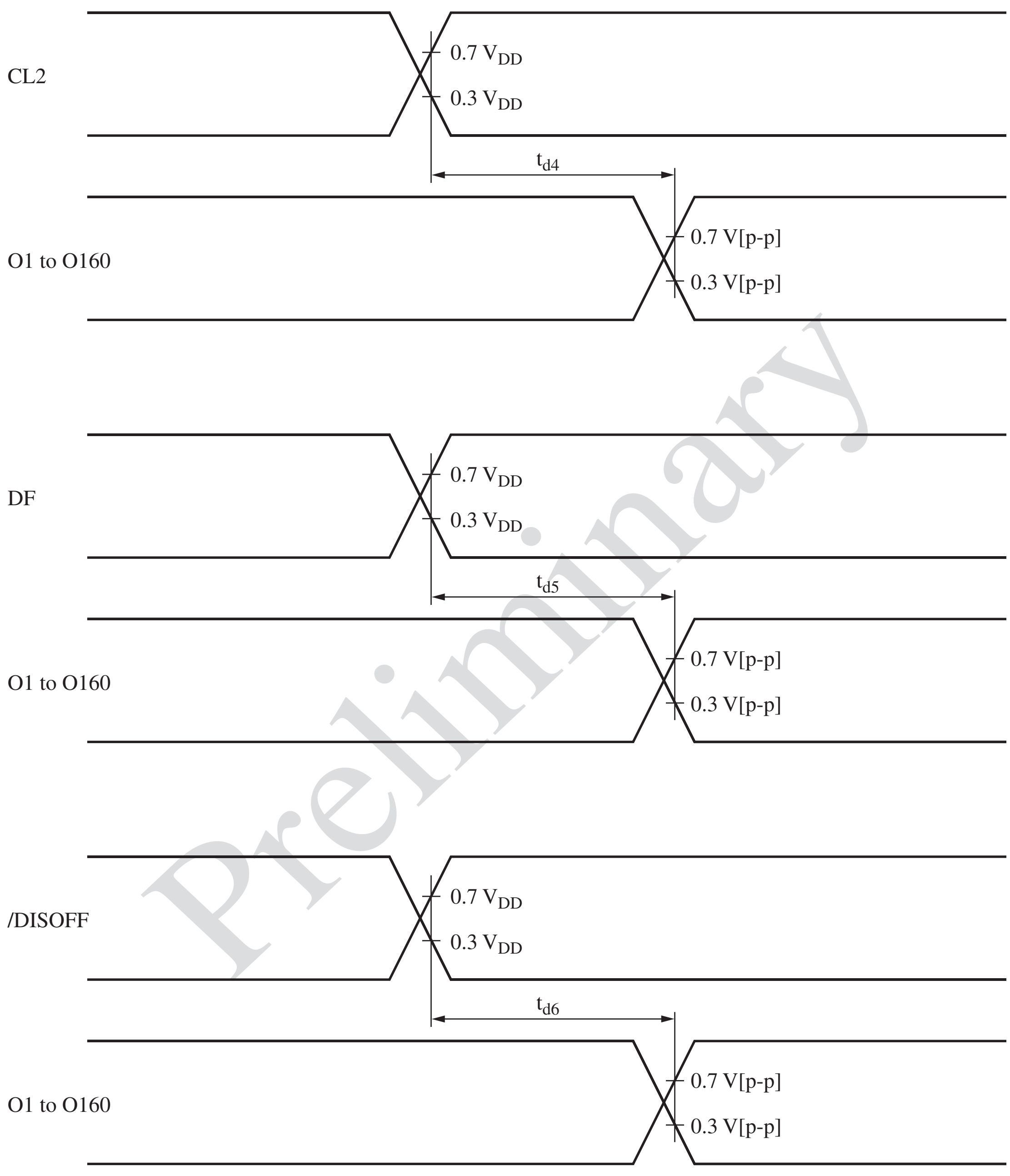
■ Electrical Characteristics (continued)

4. AC Characteristics (continued)



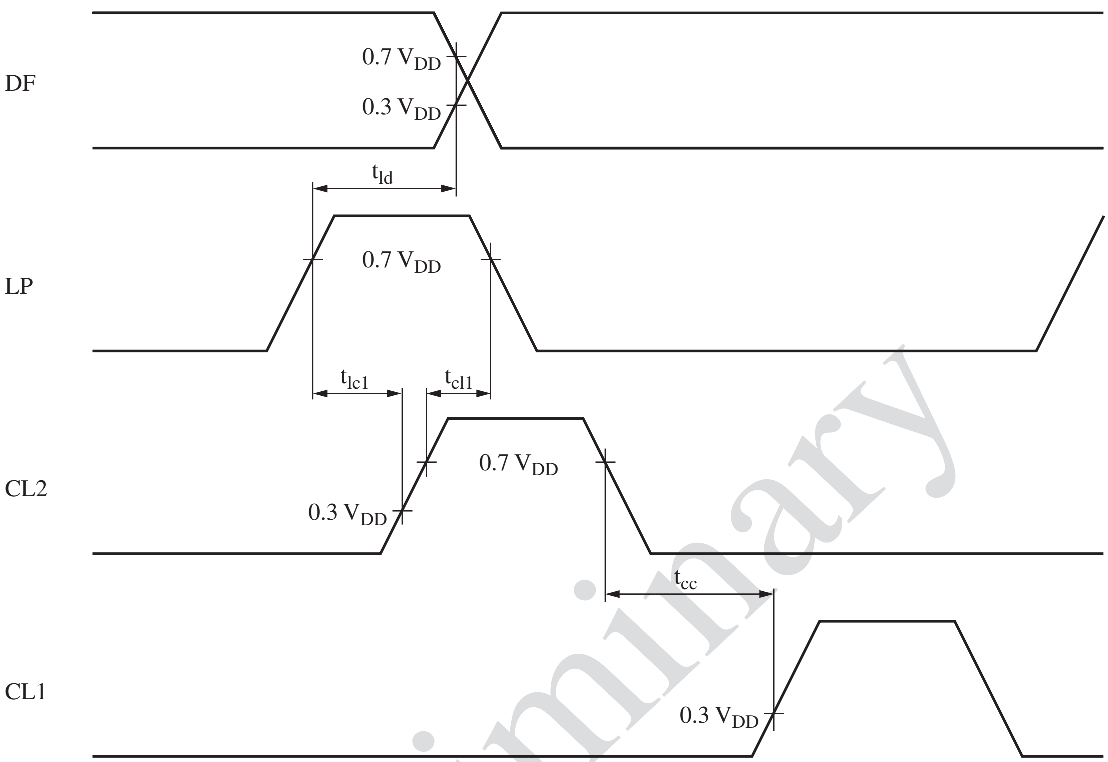
■ Electrical Characteristics (continued)

4. AC Characteristics (continued)



■ Electrical Characteristics (continued)

4. AC Characteristics (continued)



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