MN88831

PCM Audio Decoder LSI for Satellite Broadcasting Tuners (Includes Built-In Digital Filter and D/A Converter)

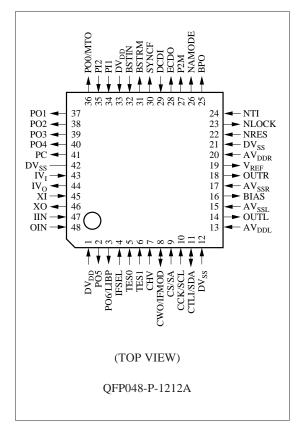
Overview

The MN88831 greatly streamlines set design by incorporating a satellite broadcasting PCM audio decoder, a switched capacitor D/A converter, and analog post filter to a single chip.

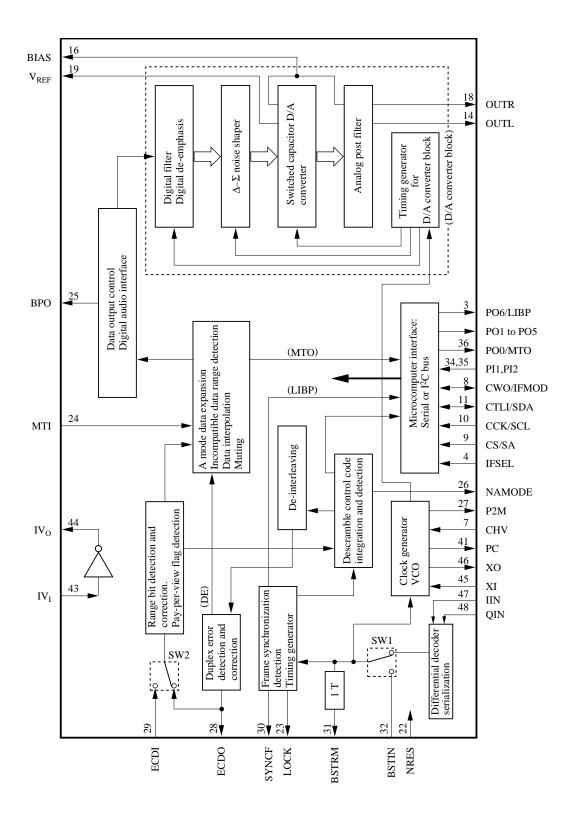
Features

- Built-in digital filter using 8-fold oversampling
- Built-in tertiary Δ - Σ noise shaping D/A converter
- Reduced jitter noise through use of switched capacitor configuration
- Built-in analog post filter
- Built-in digital de-emphasis circuit
- Choice of microcomputer interfaces with selector pin: 3-wired serial interface or I²C interface
- Muting function supporting following settings
 - Pay-per-view flag detection
 - Error frequency detection
 - Detection of control code bit-7
- Built-in general-purpose microcomputer I/O port
- Bit stream input pin supporting 0.4 V_{P-P} input
- Applications
- Satellite broadcasting tuners (BS, CS)

Pin Assignment



Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Power supply voltage	V _{DD}	– 0.3 to 7.0	V
Input voltage	VI	-0.3 to V _{DD} +0.3	V
Output voltage	Vo	-0.3 to V _{DD} +0.3	V
Output current	I _O	25	mA
Power dissipation	P _D	480	mW
Operating temperature	T _{opr}	-20 to +70	°C
Storage temperature	T _{stg}	-55 to +125	°C

Notes:

1. The above ratings represent the maximum values that may be applied without damaging the chip, not the limits for guaranteed operation.

2. If the chip is to be used in the presence of strong electric fields—under a CRT tube, for example—apply shielding to the package surface to ensure roper operation.

- 3. The power dissipation is for an ambient temperature (Ta) of 70°C.
- 4. The voltages applied to the pins CCK/SCL, CTLI/SDA, CWO/IFMOD, PO0/MTO, PO1–PO5, and PO6/LIBP must be within the range between –0.3V and 5.5V when the power is off.

Operating Conditions	DV _{SS} =	AV _{SS} =0V				
Parameter	Symbol	Test Conditions	min	typ	max	Unit
Power supply voltage for	DV _{DD}	(*1)	4.5	5.0	5.5	V
digital circuits						
Power supply voltage for	AV _{DD}	(*2)	4.5	5.0	5.5	V
analog circuits						
XI clock frequency	f _{XI}	CHV="H" (256fs mode)		12.288		MHz
XI clock frequency	f _{XI}	CHV="L" (384fs mode)		18.432		MHz
XI clock input amplitude	_	C cut input	0.8		3.0	V _{P-P}
BSTIN input amplitude		C cut input	0.35	0.5		V _{P-P}
Ambient temperature during	Та		-20		+70	°C
operation						

Notes:

1. *1 & *2:

For the logic portions of the microcomputer interface, DV_{DD} min = 4.0V.

 $\mathrm{AV}_{\mathrm{DD}}$ covers both $\mathrm{AV}_{\mathrm{DDL}}$ and $\mathrm{AV}_{\mathrm{DDR}}$.

 AV_{SS} covers both AV_{SSL} and AV_{SSR} .

Analog characteristics are only guaranteed for $DV_{DD} = AV_{DD} = 5.0V$.

- 2. Always use low-impedance external connections for V_{DD} and V_{SS} . Always connect the two through a bypass capacitor of at least 0.01 μF to ensure proper operation.
- Keep the NRES pin (pin No. 22) at "L" level to prevent operation error of the CTLI/SDA pin in the I²C interface at voltages lower than the guaranteed operating power supply voltage.

Electrical Characteristics

(1) DC characteristics

 $AV_{DD}=DV_{DD}=4.5$ to 5.5V, $AV_{SS}=DV_{SS}=0V$, Ta=-20 to $+70^{\circ}C$

boad, V_{DD} =5.5V boad, V_{DD} =5.5V s	$0.7 \times DV_{DD}$ DV_{SS}	56	80 80 DV _{DD}	mA mA V
		56	DV _{DD}	
				V
				V
	DV _{SS}			
			$0.3 \times DV_{DD}$	V
	$0.8 \times \mathrm{DV}_\mathrm{DD}$		DV _{DD}	V
	DV _{SS}		$0.2 \times DV_{DD}$	V
			i	
= -1mA	$DV_{DD}-0.8$			V
=+1mA			0.5	V
=+1mA			0.5	V
High-impedance state			+10	
OV to DV _{DD}			±10	μA
=+1mA			0.5	V
OV to DV _{DD}			+50	μΑ
ES = 0V to 0.5V			±30	
		$0.45 \times AV_{DD}$		V
		$0.5 \times AV_{DD}$		V
	0.5	$\times \mathrm{DV}_\mathrm{DD} \pm 0$	V	
	=+1mA =+1mA High-impedance state DV to DV _{DD} =+1mA DV to DV _{DD}	DV_{SS} $= -1mA$ $DV_{DD} - 0.8$ $= +1mA$ $Iigh-impedance state$ $DV to DV_{DD}$ $= +1mA$ $DV to DV_{DD}$ $= -1mA$ $DV to DV_{DD}$ $= -1mA$ $DV to DV_{DD}$ $= -1mA$	$\begin{array}{c c c c c c c c c c c c c c c c c c c $	DV_{SS} $0.2 \times DV_{DD}$ = -1mA $DV_{DD} - 0.8$ =+1mA 0.5 =+1mA 0.5 High-impedance state ± 10 $V \text{ to } DV_{DD}$ ± 10 =+1mA 0.5 $\psi \text{ to } DV_{DD}$ ± 10 $\psi \text{ to } DV_{DD}$ ± 50

Notes:

*1: IFSEL, TES0, TES1, CHV, MTI, ECDI, PI1, PI2, IIN, QIN, CWO/IFMOD (C3, C4 only), IVI (C5 only)

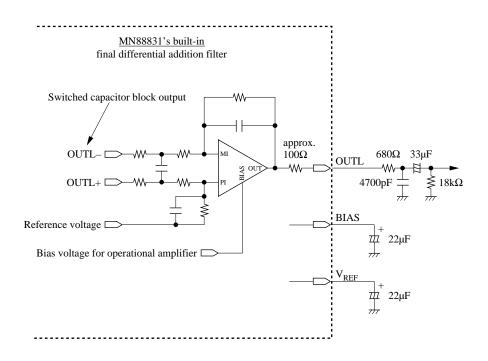
*2: CS/SA, CCK/SCL, NRES, CTLI/SDA (C6, C7 only)

*3: NLOCK, BPO, NAMODE, P2M, ECDO, SYNCF, BSTRM, PC

*4: PO0/MTO, PO1 to PO6, CWO/IFMOD, PC (C12 only)

*5: CTLI/SDA

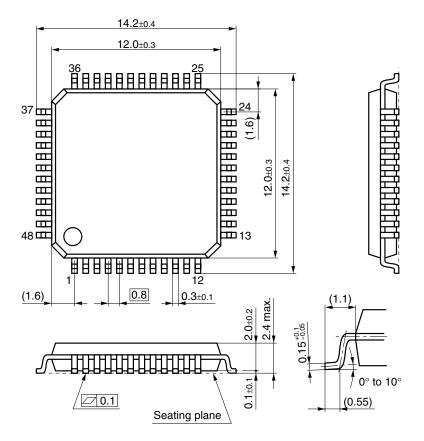
Application Circuit Example



Structure of Analog Post Filter and Sample Analog Connections

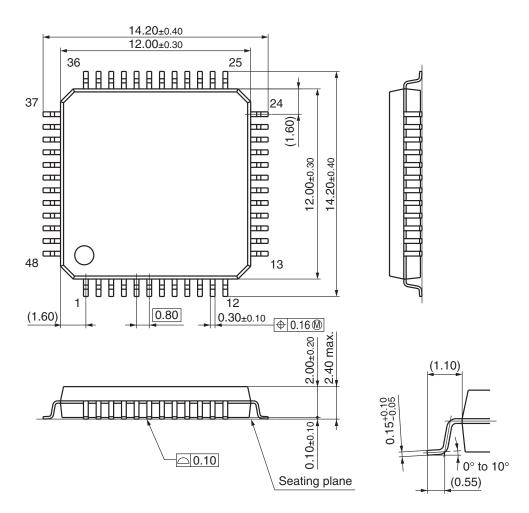
Package Dimensions (Unit: mm)

QFP048-P-1212A



Note) The package of this product will be changed to the following lead-free type (QFP048-P-1212D).

- New Package Dimensions (Unit: mm)
- QFP048-P-1212D (Lead-free package)



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