OKI semiconductor

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MSM5832 MICROPROCESSOR REAL-TIME CLOCK/CALENDAR

GENERAL DESCRIPTION

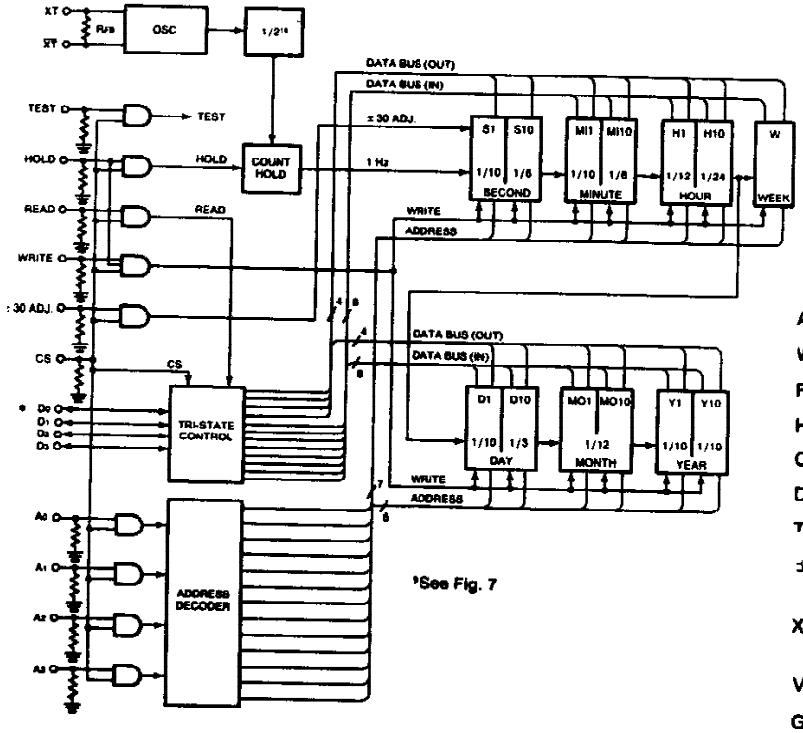
The MSM5832 is a monolithic, metal-gate CMOS integrated circuit that functions as a real time clock/calendar for use in bus-oriented microprocessor applications. The on-chip 32,768 Hz crystal controlled oscillator time base is counted down to provide addressable 4-bit I/O data of SECONDS, MINUTES, HOURS, DAY-OF-WEEK, DATE, MONTH, and YEAR. Data access is controlled by 4-bit address, chip select, read, write and hold inputs. Other functions include 12H/24H format selection, leap year identification and manual ±30 second correction.

The MSM5832 normally operates from a 5 volt ±5% supply. Battery back-up operation down to 2.2 volts allows continuation of time keeping when main power is off. One test input facilitates rapid testing of the time keeping operations. The MSM5832 is offered in an 18-lead dual-in-line plastic (RS suffix) package.

FEATURES

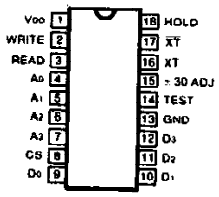
- Microprocessor bus-oriented
TIME	MONTH	DATE	YEAR	DAY OF WEEK
23:59:59	12	31	99	7
- 4-BIT DATA BUS
- 4-BIT ADDRESS
- Read, Write, Hold, Chip select inputs
- Interrupt signal outputs—1024, 1, 1/60, 1/3600 Hz
- 32.768 KHz crystal controlled operation
- Leap year register bit
- 12 or 24 hour format
- ±30 second error correction
- Single 5 volt power supply
- Back-up battery operation to V_{DD} = 2.2 V
- Low Power Dissipation
  90 μw Max. at V_{DD} = 3 V
  2.5 mw Max. at V_{DD} = 5 V
- High Density 300 mil 18-Pin Package

FUNCTIONAL BLOCK DIAGRAM



*See Fig. 7

PIN CONFIGURATION



A0 to A3: Address Inputs

WRITE: Write Enable

READ: Read Enable

HOLD: Count Hold Enable

CS: Chip Select

D0 to D3: Data Input/Output

TEST: Test Input

±30 ADJ: ±30 Second Correction Input

XT & $\overline{XT}$: xtal oscillator connections

V_{DD}: +5 V Supply

GND: Ground

FUNCTION TABLE

FIGURE 1

ADDRESS INPUTS				INTERNAL COUNTER	DATA I/O				DATA LIMITS	NOTES
A_0	A_1	A_2	A_3		D_0	D_1	D_2	D_3		
0	0	0	0	S 1	*	*	*	*	0 ~ 9	S_1 or S_{10} are reset to zero irrespective of input data D_0~D_3 when write instruction is executed with address selection
1	0	0	0	S 10	*	*	*		0 ~ 5	
0	1	0	0	MI 1	*	*	*	*	0 ~ 9	
1	1	0	0	MI 10	*	*	*		0 ~ 5	
0	0	1	0	H 1	*	*	*	*	0 ~ 9	
1	0	1	0	H 10	*	*	†	†	0~1 / 0~2	D_2="1" for PM D_3="1" for 24 hour format D_2="0" for AM D_3="0" for 12 hour format
0	1	1	0	W	*	*	*		0 ~ 6	
1	1	1	0	D 1	*	*	*	*	0 ~ 9	
0	0	0	1	D 10	*	*	†		0 ~ 3	D_2 ="1" for 29 days in month 2 D_2 ="0" for 28 days in month 2 (2)
1	0	0	1	MO 1	*	*	*	*	0 ~ 9	
0	1	0	1	MO 10	*				0 ~ 1	
1	1	0	1	Y 1	*	*	*	*	0 ~ 9	
0	0	1	1	Y 10	*	*	*	*	0 ~ 9	

(1) *data valid as "0" or "1"
blank does not exist (unrecognized during a write and held at "0" during a read)
†data bits used for AM/PM, 12/24 HOUR and leap year must be masked from the H10 and D10 registers for correct time to be read.
(2) If D_2 previously set to "1", upon completion of month 2 day 29, Q_2 will be internally reset to "0"

TYPICAL CHARACTERISTICS—Oscillator Frequency Deviations

Frequency Deviation *vs* Temperature

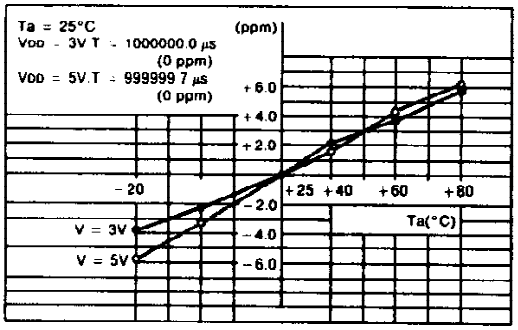


FIGURE 2

Frequency Deviation *vs* Supply Voltage

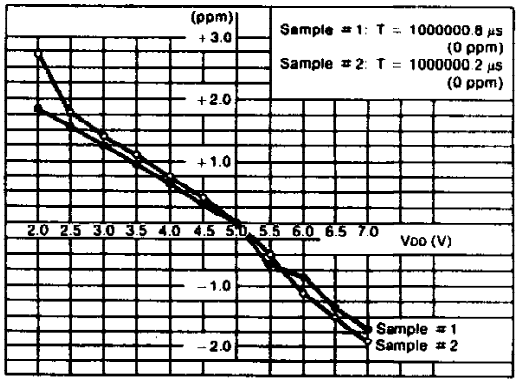


FIGURE 3

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	−0.3 ~ 7.0	V
Input Voltage	V_{IN}	−0.3 ~ V_{DD} +0.3	V
Data I/O Voltage	V_D	−0.3 ~ V_{DD} +0.3	V
Storage Temperature	T_{stg}	−55 ~ 150	°C

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V_{DD}	4.75	5	5.25	V	5V ± 5%
Standby Supply Voltage	V_{DDS}	2.2	5	7	V	
Input Signal Level	V_{IH}	3.6	5	V_{DD}	V	V_{DD} = 5V ± 5% Respect to Gnd
	V_{IL}	−0.3	0	0.8	V	
Crystal Oscillator Freq.	f(XT)		32.768	65.536*	KHz	
Operating Temperature	Ta	−30		+85	°C	

*Device will run at 2× speed when operating at 65.536KHz f(XT)

DC CHARACTERISTICS

(V_{DD} = 5V ± 5%; T_A = −30 to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input Current (1)	I_{TH}	10	25	50	μA	V_{IN} = 5V
	I_{IL}	−1		1	μA	V_{IN} = 0V
Data I/O Leakage Current	I_{LD}	−1		1	μA	$V_{I/O}$ = 0 to V_{DD}, CS = "0"
Output Low Voltage	V_{OL}			0.4	V	Io = 1.6 ma, CS = "1", READ = "1"
Output Low Current	I_{OL}	1.6			mA	Vo = 0.4V, CS = "1", READ = "1"
Output High Voltage	V_{OH}	Open Drain n-MOS Output; Depends on value of Pull-up Resistor				See Fig. 7
Output High Current	I_{OH}					
Operating Supply Current	I_{DDS}			30	μA	V_{DD} = 3V, Ta = 25°C
	I_{DD}			500	μA	V_{DD} = 5V, Ta = 25°C

(1) XT, $\overline{XT}$ and D0~D3 excluded.

AC CHARACTERISTICS

CAPACITANCE

T_A = 25°C, f = 1 MHz

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input/Output Capacitance	$C_{I/O}$			8	pF
Input Capacitance	C_{IN}			5	pF

Note: This parameter is periodically sampled and not 100% tested.

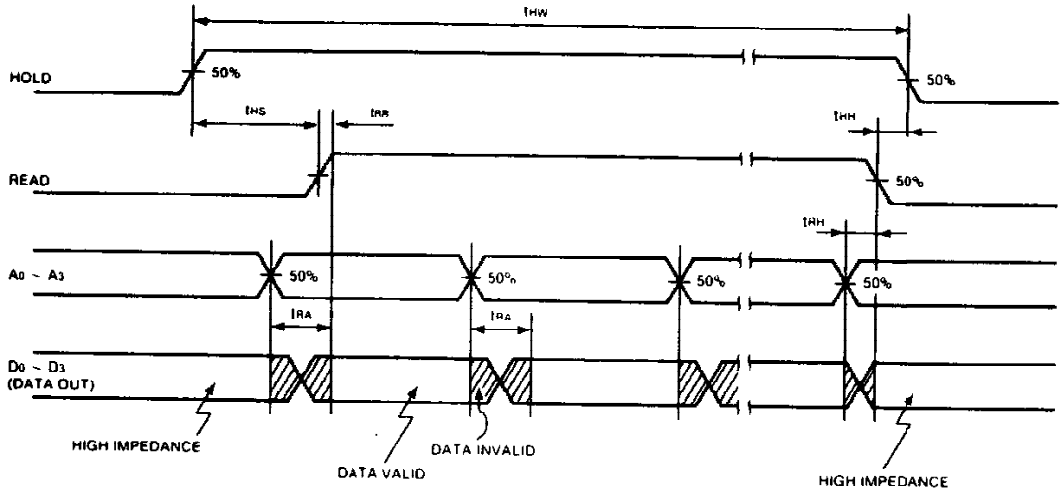
READ CYCLE

(V_{DD} = 5V ± 5%; Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
HOLD Set-up Time	t_{HS}	150			μS
HOLD Hold Time	t_{HH}	0			μS
HOLD Pulse Width	t_{HW}			1	SEC
READ Hold Time	t_{RH}	0			μS
ADDRESS Access Time	t_{RA}			6	μS
READ Access Time	t_{RR}		.3	.6	μS

READ CYCLE

FIGURE 4



Notes: 1. A Read occurs during the overlap of a high CS and a high READ
2. Output Load: 1 TTL Gate, C_L = 50 pf and R_L = 4.7 KΩ
3. CS may be a permanent "1", or may be coincident with HOLD pulse

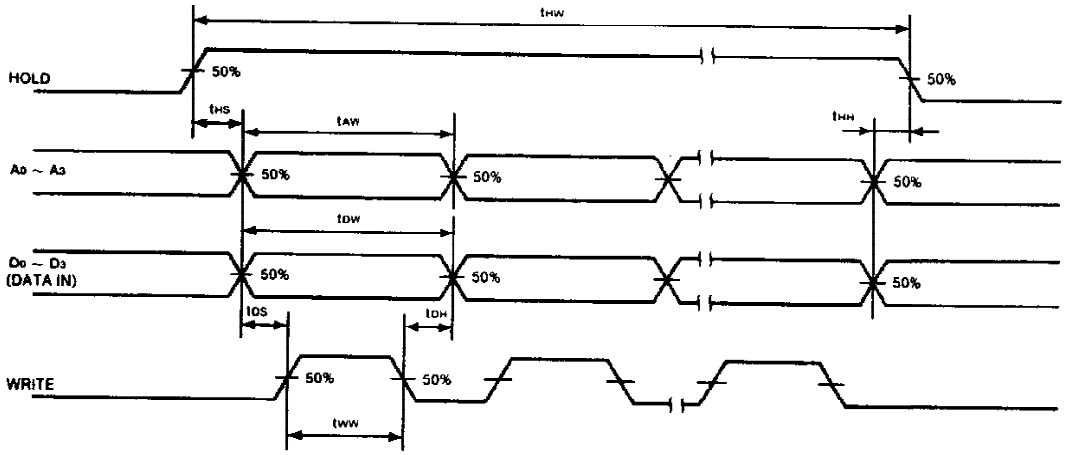
WRITE CYCLE

(V_{DD} = 5V ± 5%; Ta = 25°C)

Parameter	Symbol	Min.	Max.	Unit
HOLD Set-up Time	t_{HS}	150		μS
HOLD Hold Time	t_{HH}	0		μS
HOLD Pulse Width	t_{HW}		1	SEC
ADDRESS Pulse Width	t_{AW}	1.7		μS
DATA Pulse Width	t_{DW}	1.7		μS
DATA Set-up Time	t_{DS}	0.5		μS
DATA Hold Time	t_{DH}	0.2		μS
WRITE Pulse Width	t_{WW}	1.0		μS

WRITE CYCLE

FIGURE 5



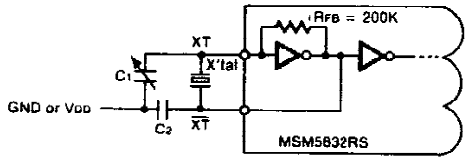
Notes: 1. A WRITE occurs during the overlap of a high CS, a high HOLD and a high WRITE
2. CS may be a permanent "1", or may be coincident with HOLD pulse

FUNCTIONAL DESCRIPTION

A block diagram of the MSM5832 microprocessor real-time clock/calendar and a package connection diagram are shown on the first page. Figure 9 illustrates a method of interfacing between the clock/calendar circuit and a micro processor. Figures 9, 10 and 11 illustrate alternative standby power supply circuits. A function table listing relationships between address inputs, data input/output and internal counter selection is shown in Figure 1. Unless otherwise indicated, the following descriptions are based on the block diagram.

32.768 K Hz OSCILLATOR (pins 16 and 17): An internal inverting amplifier with feedback resistor, R_{FB}, is connected with a crystal and two capacitors *as shown in Figure 6* to form a stable, accurate oscillator—which serves as the precision time base of the circuit. Capacitors C1 and C2 in series provide the parallel load capacitance required for precise tuning of the quartz crystal. Typical oscillator performance as a function of ambient temperature and supply voltage is shown in Figures 2 and 3 respectively.

OSCILLATOR CIRCUIT — FIGURE 6



$C_1 = C_2 = 15 \sim 30$ pF

CHIP SELECT (pin 8): Connecting CS input to V_{DD} enables all inputs and outputs. Unconnected—pull-down to GND is provided by an internal resistor—or connecting CS to GND will disable HOLD, WRITE, READ, ±30 ADJ, $D_0 \sim D_3$, $A_0 \sim D_3$ and TEST.
As shown in Figure 9 CS can be used to detect system power failure by connecting system power (+5V) to CS. so that when system power is *on*, all inputs and outputs will be enabled, and when system power is *off*, all inputs and outputs will be disabled. The threshold voltage of CS is higher than all other inputs to insure correct operation of this function.

HOLD (pin 18): Switching this input to V_{CC} inhibits the internal 1Hz clock to the S1 counter. After the specified HOLD set-up time (150 μs), all counters will be in a static state, thus allowing error-free read or write operations. So long as the HOLD pulse width is less than 1 second, accuracy of the real time will be undisturbed. Pull-down to GND is provided by an internal resistor.

READ (pin 3): Read function *as shown in Figure 4* is enabled when READ is switched to V_{DD}. Pull-down to GND is provided by an internal resistor.

WRITE (pin 2): Write function *as shown in Figure 5* is enabled when WRITE is switched to V_{DD}. Pull-down to GND is provided by an internal resistor.

±30 ADJ (Pin 15): Momentarily connecting this input to V_{CC} (>31.25 ms) will reset seconds (S1, S10 counters and $2^{11} \sim 2^{15}$ frequency dividers) to 00; if seconds were 30 or more, one minute is added to the minutes (MI 1 counter) and if seconds were less than 30, the minutes are unchanged. Pull-down to GND is provided by an internal resistor.

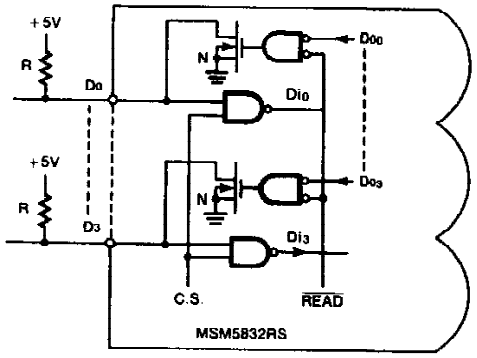
$A_0 \sim A_3$ (pins 4 ~ 7): Address inputs, used to select internal counters for read/write operations (see function table—*Figure 1*). A "1" is defined as V_{DD}; a "0" is GND. Pull-down to GND is provided by internal resistors.

$D_0 \sim D_3$ (pins 9 ~ 12): Data Inputs/Outputs, two-way bus lines controlled by READ and WRITE inputs. *As shown in Figure 7 external pull-up resistors of 4.7K or higher are required by the open-drain N-channel MOS outputs.* D_3 is the MSB; D_0 is the LSB.

TEST (pin 14): Normally this input is unconnected—pull-down to GND is provided by an internal resistor—or connected to GND. With CS at V_{DD}, pulses to V_{DD} on the TEST input will directly clock the S1, MI10, W, D1 and Y1 counters, depending on which counter is addressed (W and D1 are selected by D1 address in this mode only). Roll-over to next counter is enabled in this mode.

Max. Input Freq = 10KHz

DATA I/O CIRCUIT — FIGURE 7



REFERENCE SIGNAL OUTPUT
Reference signals are available as outputs on $D_0 \sim D_3$ if CS, READ and $A_0 \sim A_3$ are at V_{DD}. Refer to *Figure 8* for specifics. *As shown in Figure 9* these signals may be used to generate interrupts for the microprocessor.

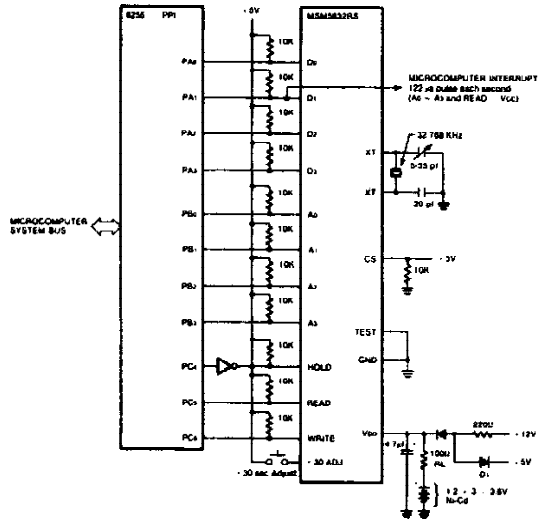
REFERENCE SIGNAL OUTPUTS — FIGURE 8

CONDITIONS	OUTPUT	REFERENCE FREQUENCY	PULSE WIDTH
HOLD = L	D_0 (1)	1024 Hz	duty 50 %
READ = H	D_1 (2)	1 Hz	122.1 μs
C.S. = H	D_2 (2)	1/60 Hz	122.1 μs
$A_0 \sim A_3$ = H	D_3 (3)	1/3600 Hz	122.1 μs

(1) 1024 Hz signal at D_0 not dependent on HOLD input level. Use this signal for trimming the quartz oscillator. Probe capacitance will load the oscillator if a probe is placed on XT or $\overline{XT}$ causing erroneous readings. Trim to 976.5625 μs ± .0015 μs
(2) Negative Pulse, Negative True
(3) Positive Pulse, Positive True

TYPICAL APPLICATION—Use with Programmable Peripheral Interface (PPI)

FIGURE 9



Suggested XTAL Sources:
1.) Statek CX-IV-32.768

NOTE A:
This circuit combines battery charging with switching logic to power the 5832/58321 from the battery when system power fails. RL is a current limit to protect the battery if VDD is accidentally shorted. Since Diode D1's cathode is at the system power supply (+5V), D1 and D2's anodes will be one diode drop positive from system power and the cathode of D2 will also track the system power supply. VCHG and RCHG are chosen to trickle charge the batteries. VCHG need not be a regulated voltage and the unregulated voltage into the system +5V supply is ideal. When system power fails, D1 and D2 prevent the battery from trying to power the system. VDD will be the battery voltage whenever VCHG is less than the battery voltage.

TYPICAL APPLICATIONS—Alternative Standby Power Supply Circuits

FIGURE 10

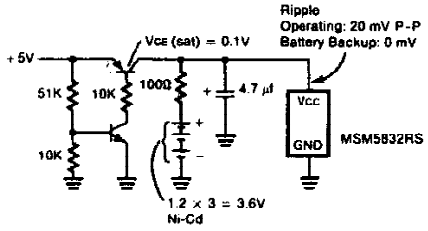
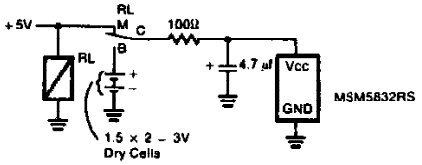
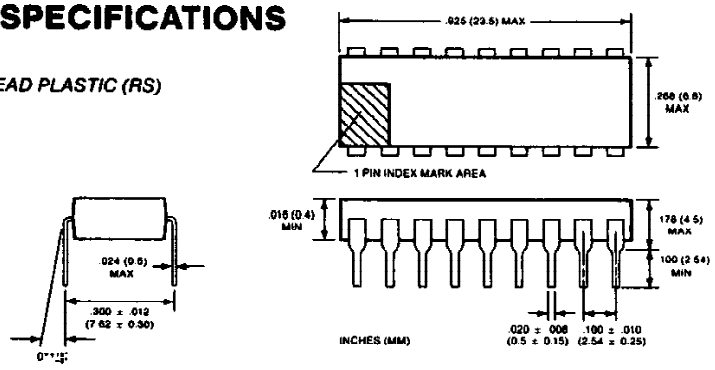


FIGURE 11



PACKAGE SPECIFICATIONS

18 LEAD PLASTIC (RS)



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