TOSHIBA

TOSHIBA Original CMOS 16-Bit Microcontroller

TLCS-900/L Series

TMP93CF76
TMP93CF77
TMP93CW76
TMP93CU76
TMP93CT76

TOSHIBA CORPORATION

Preface

Thank you very much for making use of Toshiba microcomputer LSIs.
Before use this LSI, refer the section, “Points of Note and Restrictions”.
Especially, take care below cautions.

CAUTION
How to release the HALT mode

Usually, interrupts can release all halts status. However, the interrupts = (INT0, INT1), which can release the HALT mode may not be able to do so if they are input during the period CPU is shifting to the HALT mode (for about 3 clocks of fc or fs) with IDLE1 or STOP mode (IDLE2 is not applicable to this case). (In this case, an interrupt request is kept on hold internally.)

If another interrupt is generated after it has shifted to HALT mode completely, halt status can be released without difficultly. The priority of this interrupt is compare with that of the interrupt kept on hold internally, and the interrupt with higher priority is handled first followed by the other interrupt.

CMOS 16-Bit Microcontroller

TMP93CF76/CF77/CW76/CU76/CT76

1. Outline and Feature

TMP93CF76/CF77/CW76/CU76/CT76 are a high-speed advanced 16-bit microcontroller developed for application with VCR system control, software servo motor control, VFT driver and timer control.

In addition to basics such as I/O ports, the TMP93CF76/CF77/CW76/CU76/CT76 have high-speed/high-precision signal measuring circuit, PWM (Pulse-Width-Modulator) and high-precision real timing pulse generator.

The device characteristics are as follows:

(1) Original 16-bit CPU (900/L CPU)

- TLCS-90 instruction mnemonic upward compatible
- 16 Mbyte linear address space
- General-purpose registers and register bank system
- 16-bit multiplication/division and bit transfer/arithmetic instructions
- High-speed micro DMA: 4 channels (2 μs/2 byte at 16 MHz)

(2) Minimum instruction execution time: 250 ns at 16 MHz

(3) Internal ROM:

TMP93CF76	192 KB
TMP93CF77	160 KB
TMP93CW76	128 KB
TMP93CU76	96 KB
TMP93CT76	72 KB

(4) Internal RAM:

TMP93CF76	4.0 KB
TMP93CF77	4.0 KB
TMP93CW76	2.5 KB
TMP93CU76	2.5 KB
TMP93CT76	2.0 KB

(5) 20-bit time-base-counter (TBC)
- Free running counter
- Accuracy: 125 ns (at fc = 16 MHz)
- Overflow: 131 ms (at fc = 16 MHz)

(6) 8-bit timer (TC0): 1 channel
- For CTL linear time counter

(7) 16-bit timer (TC1 to 5): 5 channels
- C.sync count, capstan FG count, general: 3 channels

(8) Timing pulse generator (TPG): 2 channels
- (16-bit timing data + 6-bit output data) with 8-stages FIFO : 1 channel
- (16-bit timing data + 4-bit output data) : 1 channel
- Accuracy: 500 ns (at 16 MHz)

(9) Pulse width modulation outputs (PWM)
- 14-bit PWM: 3 channels (for controlling capstan, drum and tuner)
- 8-bit PWM: 1 channel (for controlling volume)
- Carrier frequency: 31.25 kHz (at 16 MHz)

(10) 24-bit time base counter capture circuit (Capture 0)
- (18-bit timing data + 6 bit trigger data) with 8-stages FIFO: 1 channel
- Capture input sources: Remote-control-input (RMTIN), V.sync, CTL, Drum-PG, general (1 channel)
- Accuracy: 500 ns (at 16 MHz)

(11) 17-bit time base counter capture circuit (Capture 1/2)
- (16-bit timing data + 1-bit trigger data): 2 channels
- Capture input sources: Drum-FG, Capstan-FG
- Accuracy: 125 ns (at 16 MHz)

(12) VISS/VASS detection circuit (VISS/VASS)
- CTL duty detection
- VASS data 16-bit latch

(13) Composite-sync-signal (C.sync) input
- Vertical-sync-signal (V.sync) separation
- Horizontal-sync-signal (H.sync) separation

(14) Head Amp switch/Color Rotary control (HA/CR)

(15) Pseudo-V/H generator (PV/PH)

(16) 8-bit AD converter (ADC): 10 channels
- Conversion speed: 95 states (11.8 μs at 16 MHz)

(17) Serial Channel (SIO): 1channel

(18) Serial bus I/F
- I^2C bus with 8-stages FIFO: 1 channel/2 ports

(19) Watch dog timer (WDT)

(20) Interrupt controller (INTC)

- CPU: 8 sources → SWI instruction and illegal instruction
- Internal: 17 sources
- External: 5 sources

7-level priority can be set.

(21) I/O ports

- 67 I/O ports (multiplexed functional pins.)
  High Break Down Voltage PortE, F are Included: 14 I/O ports
- 8 input ports (P40/AIN2 to P47/AIN9)
- 10 output ports
  PC0/G0 to PC7/G7, PD0/G8 to PD1/G9: High Break Down Voltage

(22) Standby function: 4 halt modes (RUN, IDLE2, IDLE1, STOP)

(23) System clock function

- Dual clock operation 16 MHz (High-speed: normal)/32 kHz (Low-speed:slow)
  … 17-bit Real Time Counter built in

(24) Operating Voltage

- Vcc = 2.7 to 5.5 V (at 32 kHz)
- Vcc = 4.5 to 5.5 V (at 16 MHz)

(25) Package

- 100 pin QFP 14 mm × 20 mm (Pin pitch: 0.65 mm)
- Product name: P-QFP100-1420-0.65A

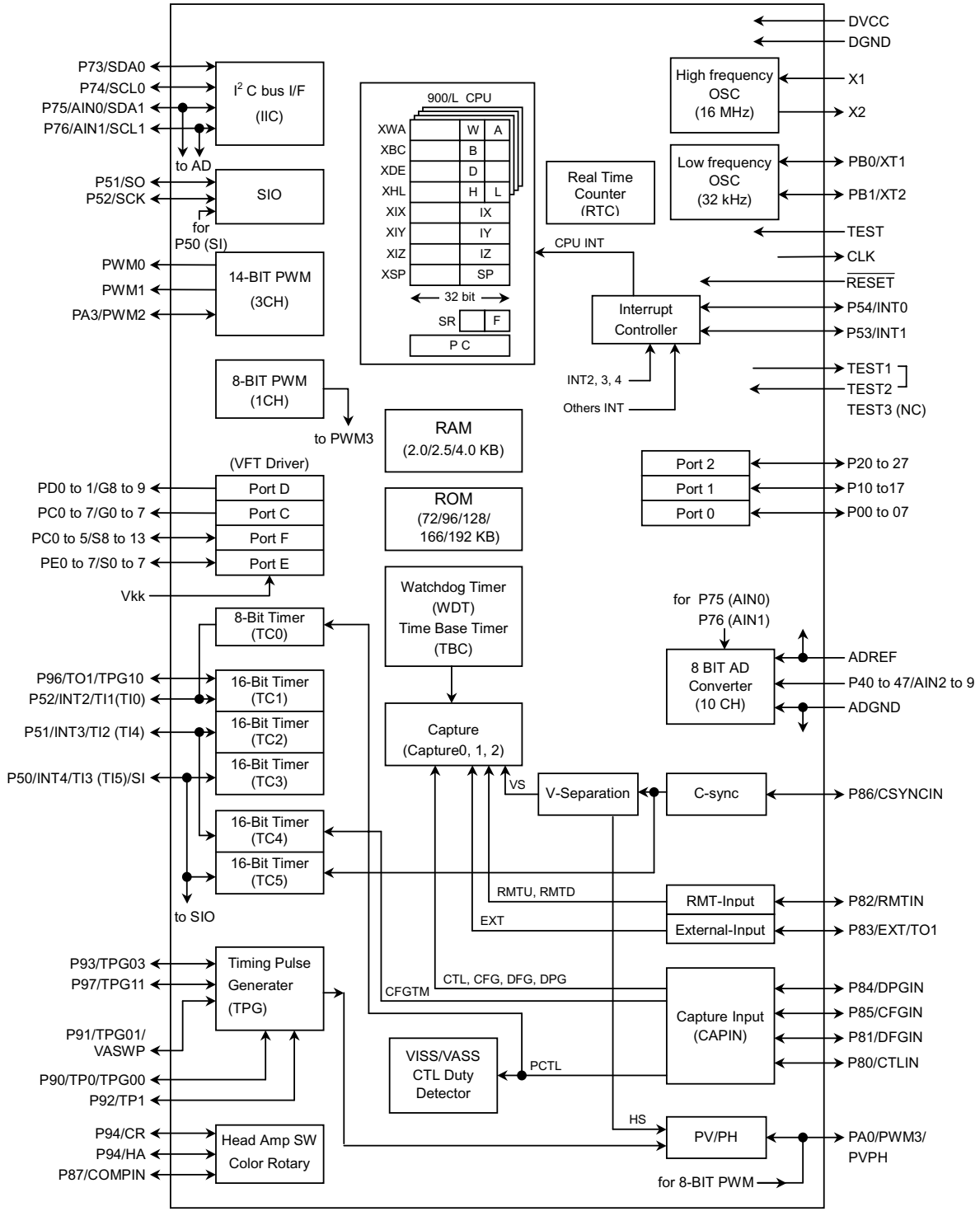


Figure 1.1 TMP93CF76/CF77/CW76/CU76/CT76 block diagram

2. Pin Assignment and Functions

The assignment of input and output pins for the TMP93CF76/CF77/CW76/CU76/CT76, their names and functions are described below.

2.1 Pin Assignment

Figure 2.1.1 shows pin assignment of the TMP93CF76/CF77/CW76/CU76/CT76.

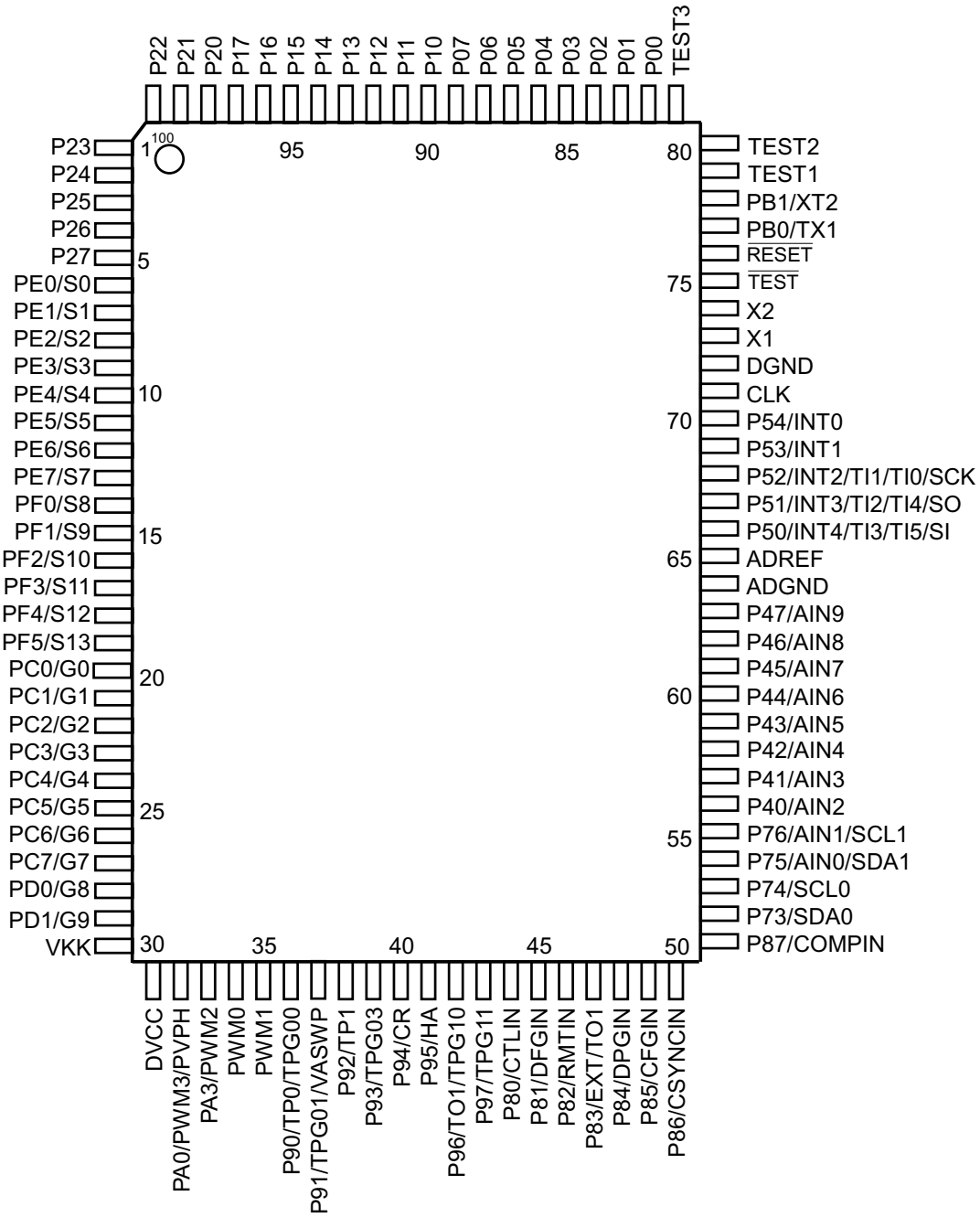


Figure 2.1.1 Pin assignment (100-pin QFP)

2.2 Pin Names and Functions

The names of input/output pins and their functions are described below.

Table 2.2.1 Pin names and function (1/3)

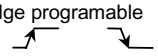
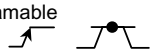
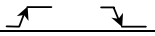
Pin name	Number of pins	I/O	Functions
P00 to P07	8	I/O	port0: I/O ports
P10 to P17	8	I/O	port1: I/O ports
P20 to P27	8	I/O	port2: I/O ports
P40 to P47	8	Input	port4: Input ports
AIN2 to AIN9		Input	Analog input: Input to AD converter
P50	1	I/O	Port50: I/O port (schmitt input)
INT4		Input	External Interrupt request input 4: Rising edge/Falling edge programable
TI3		Input	16-bit timer3 (TC3) Input 3 
TI5		Input	16-bit timer5 (TC5) input 5
SI		Input	SIO received data
P51	1	I/O	Port51: I/O port (schmitt input)
INT3		Input	External Interrupt request input 3: Rising edge/Falling edge programable
TI2		Input	16-bit timer2 (TC2): Input 2 
TI4		Input	16-bit timer4 (TC4): input 4
SO		Output	SIO sending data
P52	1	I/O	Port52: I/O port (schmitt input)
INT2		Input	External Interrupt request input 2: Rising edge/Falling edge programable
TI1		Input	16-bit timer1 (TC1) Input 1 
TI0		Input	8-bit Timer0 (TC0) Input 0
SCK		I/O	SIO clock line
P53	1	I/O	Port53: I/O port (schmitt input)
INT1		Input	External Interrupt request pin1: Rising edge/Level programable 
P54	1	I/O	Port54: I/O port (schmitt input)
INT0		Input	External Interrupt request pin0: Rising edge/Falling edge programable 
P73	1	I/O	Port73: I/O port (schmitt input, Push-pull or open-drain output selectable)
SDA0		I/O	I^2C bus SDA0 line
P74	1	I/O	Port74: I/O port (schmitt input, Push-pull or open-drain output selectable)
SCL0		I/O	I^2C bus SCL0 line
P75	1	I/O	Port75: I/O port (schmitt input, Push-pull or open-drain output selectable)
SDA1		I/O	I^2C bus SDA1 line
AIN0		Input	Analog input 0: Analog input signal for AD converter
P76	1	I/O	Port76: Input port (schmitt input, Push-pull or open-drain output selectable)
SCL1		I/O	I^2C bus SCL1 line
AIN1		Input	Analog input 1: Analog input signal for AD converter
P80	1	I/O	Port80: I/O port (schmitt input)
CTLIN		Input	CTL Capture input (Capture 0)
P81	1	I/O	Port81: I/O port (schmitt input)
DFGIN		Input	DFG Capture input (Capture 1)

Table 2.2.1 Pin names and function (2/3)

Pin name	Number of pins	I/O	Functions
P82	1	I/O	Port82: I/O port (schmitt input)
RMTIN		Input	Remote Control Signal Capture input
P83	1	I/O	Port83: I/O port (schmitt input)
EXT		Input	External Capture input (Capture 0)
TO1		Output	Timer Out 1
P84	1	I/O	Port84: I/O port (schmitt input)
DPGIN		Input	DPG Capture input (Capture 0)
P85	1	I/O	Port85: I/O port (schmitt input)
CFGIN		Input	CFG Capture input (Capture 2)
P86	1	I/O	Port86: I/O port (schmitt input)
CSYNCIN		Input	C.sync Capture input
P87	1	I/O	Port87: I/O port (schmitt input)
COMPIN		Input	Envelope Comparate Input (to HA/CR)
P90	1	I/O	Port90: I/O port (Push-pull or open-drain output selectable)
TP0		Output	Timing Pulse output 0
TPG00		Output	TPG00: TPG0 output
P91	1	I/O	Port91: I/O port (Push-pull or open-drain output selectable)
VASWP		Output	Video/Audio head switching control signal output
TPG01		Output	TPG01: TPG0 output
P92	1	I/O	Port92: I/O port (Push-pull or open-drain output selectable)
TP1		Output	Timing Pulse output 1
P93	1	I/O	Port93: I/O port (Push-pull or open-drain output selectable)
TPG03		Output	TPG03: TPG0 output
P94	1	I/O	Port94: I/O port (Push-pull or open-drain output selectable)
CR		Output	Color Rotary Output
P95	1	I/O	Port95: I/O port (Push-pull or open-drain output selectable)
HA		Output	Head Amp Switching Control Output
P96	1	I/O	Port96: I/O port (Push-pull or open-drain output selectable)
TO1		Output	Timer Out 1
TPG10		Output	TPG10: TPG1 output
P97	1	I/O	Port97: I/O port (Push-pull or open-drain output selectable)
TPG11		Output	TPG11: TPG1 output
PA0	1	I/O	PortA0: I/O port
PVPH		Output	PVPH 3-state Output
PWM3		Output	PWM(8 bits) output 3
PA3	1	I/O	PortA3: I/O port (Push-pull or open-drain output selectable)
PWM2		Output	PWM(14 bits) output 2

Table 2.2.1 Pin names and function (3/3)

Pin name	Number of pins	I/O	Functions
PWM0	1	Output	PWM(14 bits) output 0 (Push-pull or open-drain output selectable)
PWM1	1	Output	PWM(14 bits) output 1 (Push-pull or open-drain output selectable)
PB0 XT1	1	I/O Input	PortB0: I/O port (Open-drain Output) Low Frequency Oscillator connecting pin
PB1 XT2	1	I/O Output	PortB1: I/O port (Open-drain Output) Low Frequency Oscillator connecting pin
PC0 to PC7 G0 to G7	8	Output Output	PortC: Output (High break down voltage outputs with pull-down resistor) Grid Drivers
PD0,1 G8, 9	2	Output Output	PortD: Output (High break down voltage outputs with pull-down resistor) Grid Drivers
PE0 to PE7 S0 to S7	8	I/O Output	PortE: I/O ports (High break down voltage outputs with pull-down resistor) Segment Drivers
PF0 to PF5 S8 to S13	6	I/O Output	PortF: I/O ports (High break down voltage outputs with pull-down resistor) Segment Drivers
TEST1	1	Output	TEST1 should be connected with TEST2 pin.
TEST2	1	Input	
TEST3(NC)	1	Output	TEST3 should be open connection.
CLK	1	Output	Clock output: Output (System Clock ÷ 2) clock. Pulled-up during reset. Can be set to output disable for reducing noise. (Initial Disable)
$\overline{\text{TEST}}$	1	Input	Test pin: Always set to “Vcc” level
$\overline{\text{RESET}}$	1	Input	Reset: Initializes LSI. (with pull-up resistor)
X1	1	Input	High Frequency Oscillator connecting pins (16 MHz)
X2	1	Output	High Frequency Oscillator connecting pins (16 MHz)
VKK	1		VFT Driver power supply pin
DVCC	1		Power supply pin
DGND	1		GND pin (0 V)
ADREF	1		Reference voltage input for AD converter
ADGND	1		GND pin for AD converter

3. Operation

This section describes the functions and basic operational blocks of TMP93CF76/CF77/CW76/CU76/CT76 devices.

See the "7. Points of Concern and Restrictions" for the using notice and restrictions for each block.

3.1 CPU

TMP93CF76/CF77/CW76/CU76/CT76 devices have a built-in high-performance 16-bit CPU (900/L CPU). (For CPU operation, see TLCS-900/L CPU in the previous section).

This section describes CPU functions unique to the TMP93CF76/CF77/CW76/CU76/CT76 that are not described in the previous section.

3.1.1 Reset

To reset the TMP93CF76/CF77/CW76/CU76/CT76, the RESET input must be kept at 0 for at least 10 system clocks. (1.25 μs at 16 MHz) within the operating voltage range and with a stable oscillation.

When reset is accepted, the CPU sets as follows:

- Program Counter (PC) according to Reset Vector that is stored FFFF00H to FFFF02H.

  PC (7:0) ← stored data in location FFFF00H
  PC (15:8) ← stored data in location FFFF01H
  PC (23:16) ← stored data in location FFFF02H
- Stack pointer (XSP) for system mode to 100H.
- IFF2 to 0 bits of status register to 111. (Sets mask register to interrupt level 7.)
- MAX bit of status register to 1. (Sets to maximum mode)
- Bits RFP2 to 0 of status register to 000. (Sets register banks to 0.)

When reset is released, instruction execution starts from PC (reset vector). CPU internal registers other than the above are not changed.

When reset is accepted, processing for built-in I/Os, ports, and other pins is as follows

- Initializes built-in I/O registers as per specifications.
- Sets port pins (including pins also used as built-in I/Os) to general-purpose input/output port mode.

Note: By resetting, register in the CPU except program counter (PC), status register (SR) and stack pointer (XSP) and the data in internal RAM are not changed.

3.2 Memory Map

Figure 3.2.1 is a memory map of the TMP93CF76/CF77/CW76/CU76/CT76.

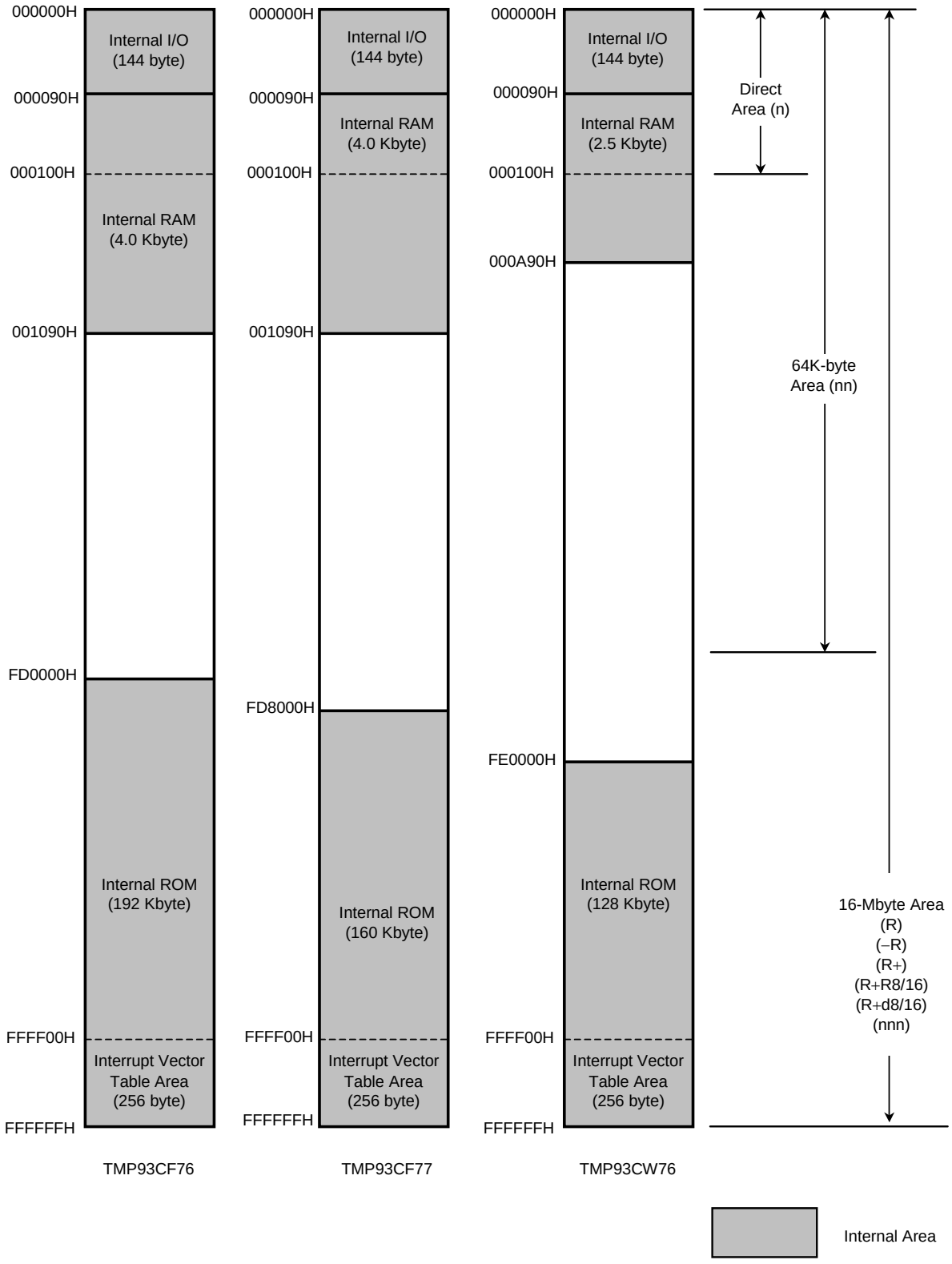


Figure 3.2.1 Memory map (1/2)

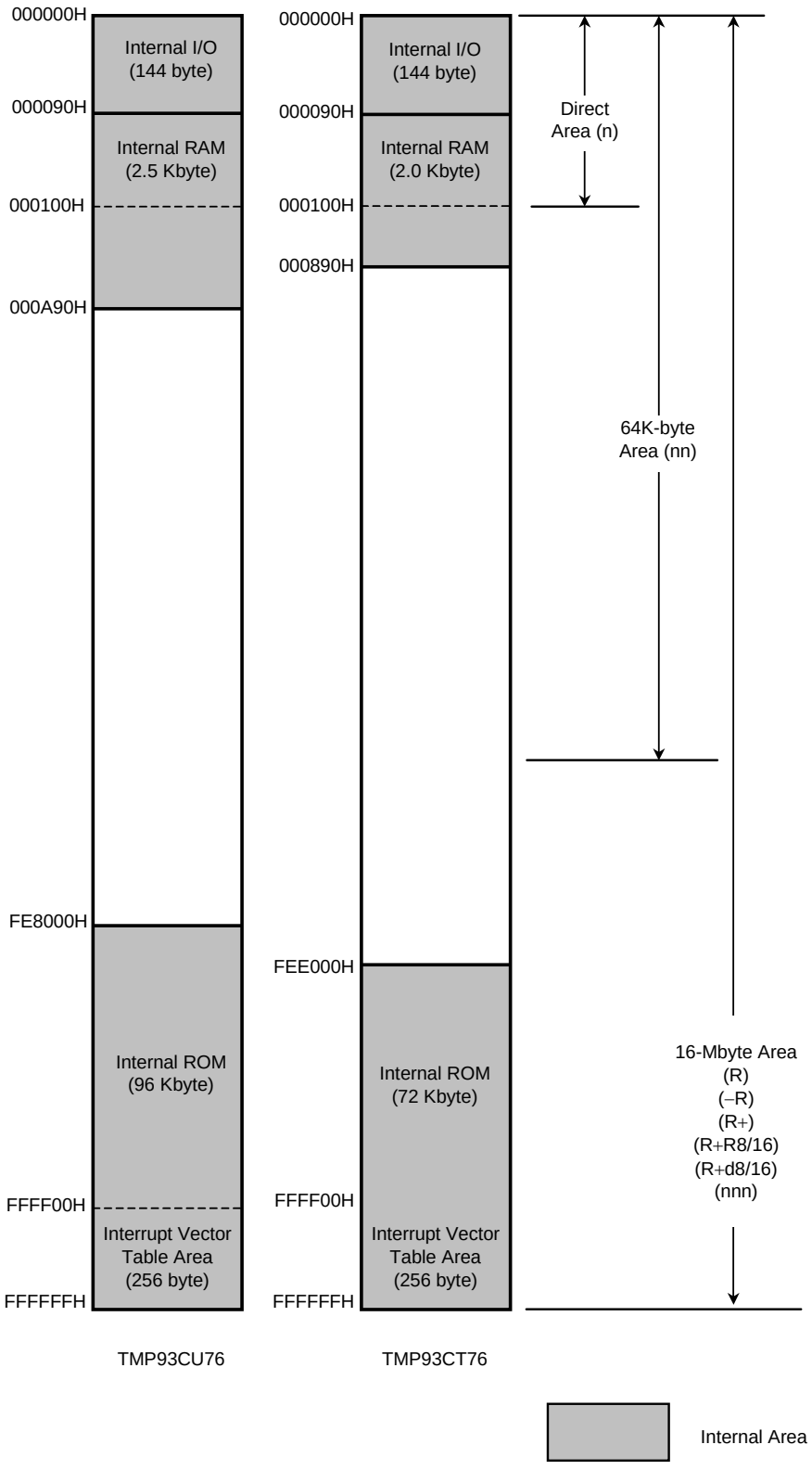


Figure 3.2.1 Memory map (2/2)

4. Electrical Characteristics

4.1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Power Supply Voltage	Vcc	−0.5 to 6.5	V
Input Voltage	V_{IN}	−0.5 to Vcc+0.5	
Output Voltage (except PC, PD, PE, PF)	V_{OUT1}	−0.5 to Vcc+0.5	
Output Voltage (PC, PD, PE, PF)	V_{OUT2}	Vcc−40	
Output Current (except PC, PD, PE, PF) (per 1 pin)	I_{OH1}	−3.2	mA
Output Current (PC, PD) (per 1 pin)	I_{OH2}	−25	
Output Current (PE, PF) (per 1 pin)	I_{OH3}	−15	
Output Current (per 1 pin)	I_{OL}	3.2	
Output Current (total except PC, PD, PE, PF)	ΣI_{OH1}	−40	
Output Current (total of PC, PD, PE, PF)	ΣI_{OH2}	−120	
Output Current (total)	ΣI_{OL}	120	
Power Dissipation (Ta = 70°C)	PD	600	mW
Soldering Temperature	Tsolder	260	°C
Storage Temperature	Tstg	−65 to 150	
Operating Temperrature	Topr	−20 to 70	

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

4.2 DC Characteristics (1/2)

Ta = −20 to 70°C

Parameter		Symbol	Condition	Min	Typ.	Max	Unit
Power Supply Voltage		Vcc	fc = 4 to 16 MHz	4.5		5.5	V
			fs = 30 to 34 kHz	2.7			
Input Low Voltage	P0, P1, P2, P4, P9, PA, PB, PE, PF	V_{IL1} (CMOS)	Vcc = 2.7 to 5.5 V	−0.3		0.3 Vcc	V
	$\overline{RESET}$, P5, P7, P8	V_{IL2} (Schmitt)				0.25 Vcc	
	$\overline{TEST}$	V_{IL3} (Fixed)				0.3	
	X1	V_{IL4} (Xtal)				0.2 Vcc	
Input High Voltage	P0, P1, P2, P4, P9, PA, PB, PE, PF	V_{IH1} (CMOS)		0.7 Vcc		Vcc + 0.3	
	$\overline{RESET}$, P5, P7, P8	V_{IH2} (Schmitt)		0.75 Vcc			
	$\overline{TEST}$	V_{IH3} (Fixed)		Vcc − 0.3			
	X1	V_{IH4} (Xtal)		0.8 Vcc			

4.2 DC Characteristics (2/2)

Ta = −20 to 70°C

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Output Low Voltage	V_{OL}	IOL = 1.6 mA (Vcc = 2.7 to 5.5 V)			0.45	V
Output High Voltage	V_{OH}	IOH = −400 μA (Vcc = 2.7 to 5.5 V)	2.4			V
	V_{OH1}	IOH = −700 μA (Vcc = 4.5 to 5.5 V)	4.1			
PE, PF	I_{OH}	Vcc = 4.5 V VOH = 2.4 V	−5			mA
PC, PD			−15			
Input Leakage Current	I_{LI}	0.0 ≦ Vin ≦ V_{CC}		0.02	±5	μA
Output Leakage Current	I_{LO}	0.2 ≦ Vin ≦ V_{CC} -0.2		0.05	±10	
Power Down Voltage	V_{STOP}	VIL2 = 0.2 V_{CC}, VIH2 = 0.8 V_{CC}	2.0		6.0	V
$\overline{RESET}$ Pull Up Resistor	R_{RST}	Vcc = 5 V ± 10%	50		150	kΩ
		Vcc = 3 V ± 10%	80		200	
Pin Capacitance	C_{IO}	osc = 1 MHz/100 mVp-p			10	pF
Schmitt Width $\overline{RESET}$, P5,P7,P8	V_{TH}			1.0		V
NORMAL	Icc	Vcc = 5 V ± 10% fc = 16 MHz		30	50	mA
RUN				18	28	
IDLE2				15	25	
IDLE1				5	8	
SLOW		Vcc = 3 V ± 10% fs = 32.768 kHz (typ: V_{CC} = 3.0 V)		50	80	μA
RUN				30	45	
IDLE2				25	40	
IDLE1				12	25	
STOP		Vcc = 2.7 to 5.5 V		0.2	10	

Note 1: Typical value are for Ta = 25°C and Vcc = 5 V unless otherwise noted.

Note 2: Icc measurement conditions (NORMAL,SLOW).
Only CPU is operational;output pins are open and input pins are fixed.

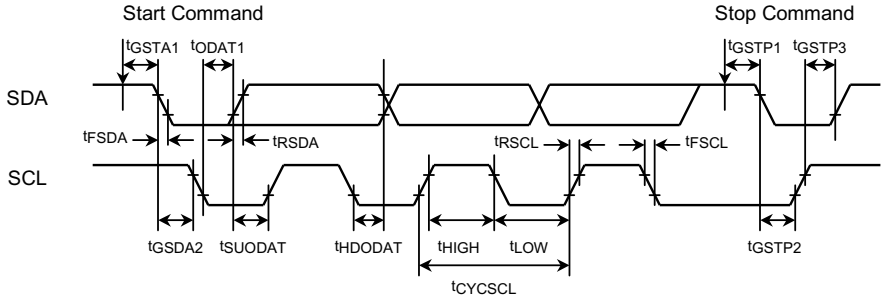
4.3 AD Conversion Characteristics

Ta = −20 to 70°C, V_{CC} = 4.5 to 5.5 V

Parameter	Symbol	Min	Typ.	Max	Unit
Analog Reference Voltage Supply	ADREF	Vcc − 1.5	Vcc	Vcc	V
	ADGND	Vss	Vss	Vss	V
Analog Input Voltage Range	V_{AIN}	ADGND	—	ADREF	V
Analog Current for ADREF	I_{REF}	—	1.0	1.5	mA
Total tolerance (excludes quantization error) (Ta = 25°C, Vcc = ADREF = 5 V)	E_T	—	—	±3	LSB

4.4 Serial Bus Interface Timing

(1) I²C bus Logic Timing



Parameter	Symbol	Min	Typ.	Max	Unit
SCL cycle	t_{CYCSCL}	2^N/fc	—	—	s
SCL low pulse width	t_{LOW}	—	2^{N-1}/fc	—	s
SCL High pulse width	t_{HIGH}	2^{N-1}/fc	—	—	s
SDA Rising Time (Note 1)	t_{RSDA}	—	—	—	s
SDA Falling Time (Note 1)	t_{FSDA}	—	—	—	s
SCL Rising Time (Note 1)	t_{RSCL}	—	—		s
SCL Falling Time (Note 1)	t_{FSCL}	—	—		s
The time from start command write to start sheecense	t_{GSTA1}	—	—	2^N/fc	s
Start condition hold time, start generation of the first clock after this	t_{GSTA2}	—	2^{N-1}/fc		s
Delay time from SCL falling to data output (Note 2)	t_{ODAT1}	—	—	5/fc	s
Set up time of data output for SCL rising (Note 2)	t_{SUODAT}	0	—	—	s
The time of holding data for SCL rising (Note 3)	t_{HODAT}	4/fc	—	—	s
The time from stop command write to starting stop sheecense	t_{GSTP1}	—	—	2^{N-1}/fc	s
The time from SDA falling to SCL rising (during stop sheecense)	t_{GSTP2}	2^{N-2}/fc	—	—	s
Stop condition set up time	t_{GSTP3}	2^{N-1}/fc	—	—	s

Note 1: The time of rising/falling depend on the feature of bus interface.

Note 2: The worst case is at the first bit of slave address.

Note 3: The worst case is at the acknowledge bit.

Note 4: N: dividing value set by I2CCR1 <SCK 2:0>.

SCK	N
000	6
001	7
010	8
011	9
100	10
101	11
110	12
111	reserved

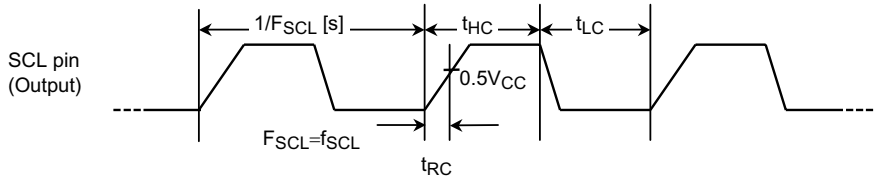
(2) Master SCL output timing

The I2CCR1 <SCK 2:0> are used to select a maximum transfer frequency directed from the SCL pin in the master mode.When rising time of the output clock (t_{RC}) is at least 8/fc [s], a high-level time of the output clock (t_{HC}) is t_{SCL}.

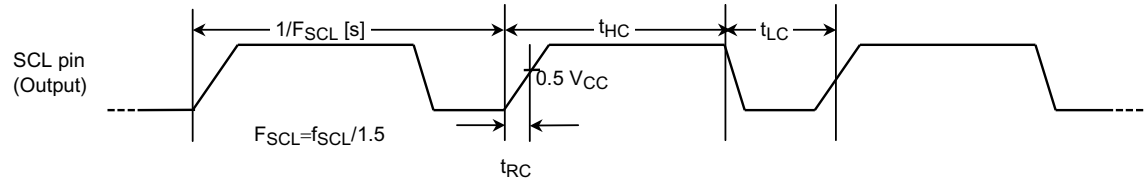
While the SCL line is fixed to low-level by a slave device,the output clock stops.

The first clock (t_{HC} [s]) after restart is $(t_{SCL}/2) \leq t_{HC} \leq t_{SCL}$.

(a) In case of $t_{RC} < (8/fc)$ [s] $t_{HC} = t_{LC} = t_{SCL}/2$ [s] ($t_{SCL} = 1/f_{SCL}$ [s])



(b) In case of $t_{RC} \geq (8/fc)$ [s] $t_{HC} = t_{SCL}$ [s] , $t_{LC} = t_{SCL}/2$ [s]



(3) Clock Syncro 8 bit SIO mode

1. SCK Input mode

Parameter	Symbol	Expression		Unit
		Min	Max	
SCK cycle	t_{SCY2}	2^5X		s
SCK falling→Latch output data	t_{OHS2}	6X		s
Enable output data→SCK raising	t_{OSS2}		$t_{SCY2} - 16X$	s
SCK raising→Latch input data	t_{HSR2}	6X		ns
Enable input data→SCK raising	t_{ISS2}	0		ns

Note: $X=1/f_c$

2. SCK Output mode

Parameter	Symbol	Expression		Unit
		Min	Max	
SCK cycle	t_{SCY2}	2^5X	$2^{11}X$	s
SCK falling→Latch output data	t_{OHS2}	2X		s
Enable output data→SCK raising	t_{OSS2}		$t_{SCY2} - 2X$	s
SCK raising→Latch input data	t_{HSR2}	2X		s
Enable input data→SCK raising	t_{ISS2}	0		ns

Note: $X=1/f_c$