DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD78042A, 78043A, 78044A, 78045A

8-BIT SINGLE-CHIP MICROCOMPUTER

DESCRIPTION

The μPD78042A, μPD78043A, μPD78044A, and μPD78045A are 8-bit single-chip microcomputers that incorporate many hardware peripherals such as an FIP® controller/driver, 8-bit resolution A/D converter, timer, serial interface, and interrupt controller.

In addition to these standard mask ROM models, one-time PROM models that can operate in the same voltage range, EPROM models, and various development tools are being developed.

The functions of these microcomputers are described in detail in the following User's Manual. Be sure to read this manual when you design a system using any of these microcomputers.

μPD78044A Sub-Series User's Manual : IEU-1394
78K/0 Series User's Manual, Instruction: IEU-1372

FEATURES

- High-capacity ROM and RAM

Item / Product name	Program memory (ROM)	Data memory		
		Internal high-speed RAM	Buffer RAM	FIP display RAM
μPD78042A	16K bytes	512 bytes	64 bytes	48 bytes
μPD78043A	24K bytes			
μPD78044A	32K bytes	1024 bytes		
μPD78045A	40K bytes			

- Wide range of instruction execution time
  - from high-speed (0.4 μs) to ultra low-speed (122 μs)
- I/O ports: 68
- FIP controller/driver: total display outputs: 34
- 8-bit resolution A/D converter: 8 channels
- Serial interface: 2 channels
- Timer: 6 channels
- Power supply voltage: V_{DD} = 2.7 to 6.0 V

APPLICATIONS

VCRs, audio systems, etc.

ORDERING INFORMATION

Part number	Package
μPD78042AGF-xxx-3B9	80-pin plastic QFP (14 x 20 mm)
μPD78043AGF-xxx-3B9	80-pin plastic QFP (14 x 20 mm)
μPD78044AGF-xxx-3B9	80-pin plastic QFP (14 x 20 mm)
μPD78045AGF-xxx-3B9	80-pin plastic QFP (14 x 20 mm)

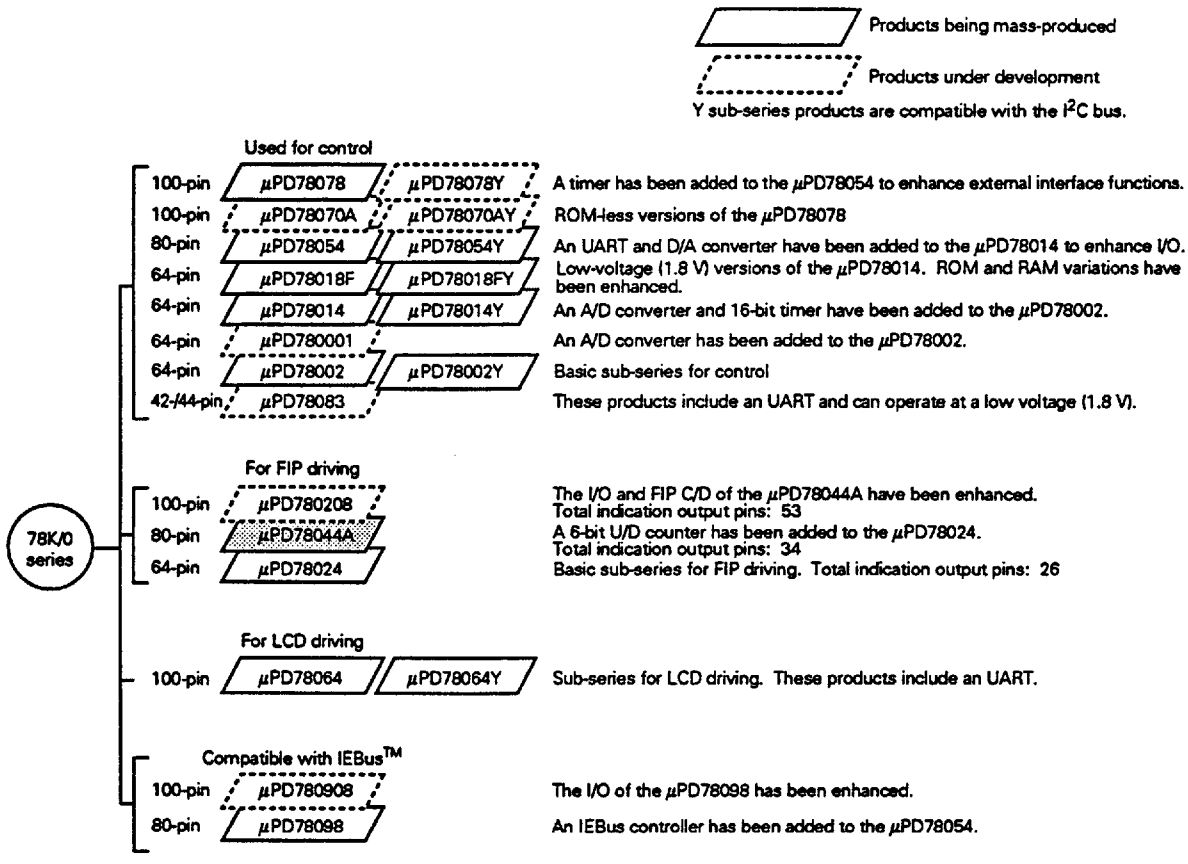
Remark "xxx" indicates ROM code number.

Document No. IC-3317A
(O. D. No. IC-8834A)
Date Published June 1995 P
Printed in Japan

Major changes in this revision are indicated by stars (★) in the margins.

★ 78K/0 SERIES PRODUCT DEVELOPMENT

The 78K/0 series products were developed as shown below. The sub-series names are indicated in frames.



The table below shows the main differences between sub-series.

Sub-series name		Function: ROM capacity	Timer: 8-bit	Timer: 16-bit	Timer: Watch	Timer: WDT	8-bit A/D	8-bit D/A	Serial interface	I/O	Minimum V_{DD}	External expansion
For control	μPD78078	32K-60K	4ch	1ch	1ch	1ch	8ch	2ch	3ch (UART:1ch)	88 pins	1.8 V	○
	μPD78070A	—								61 pins	2.7 V	
	μPD78054	16K-60K	2ch							69 pins	2.0 V	
	μPD78018F	8K-48K						—	2ch	53 pins	1.8 V	
	μPD78014	8K-32K									2.7 V	
	μPD780001	8K		—	—				1ch	39 pins		—
	μPD78002	8K-16K			1ch		—			53 pins		○
	μPD78083	8K-16K			—		8ch		1ch (UART:1ch)	33 pins	1.8 V	—
For FIP driving	μPD780208	32K-40K	2ch	1ch	1ch	1ch	8ch	—	2ch	74 pins	2.7 V	—
	μPD78044A	16K-40K								68 pins		
	μPD78024	24K-32K								54 pins		
For LCD driving	μPD78064	16K-32K	2ch	1ch	1ch	1ch	8ch	—	2ch (UART:1ch)	57 pins	2.0 V	—
Compatible with IEBus	μPD780908	60K	2ch	1ch	1ch	1ch	8ch	2ch	3ch (UART:1ch)	88 pins	2.7 V	○
	μPD78098	32K-60K								69 pins		

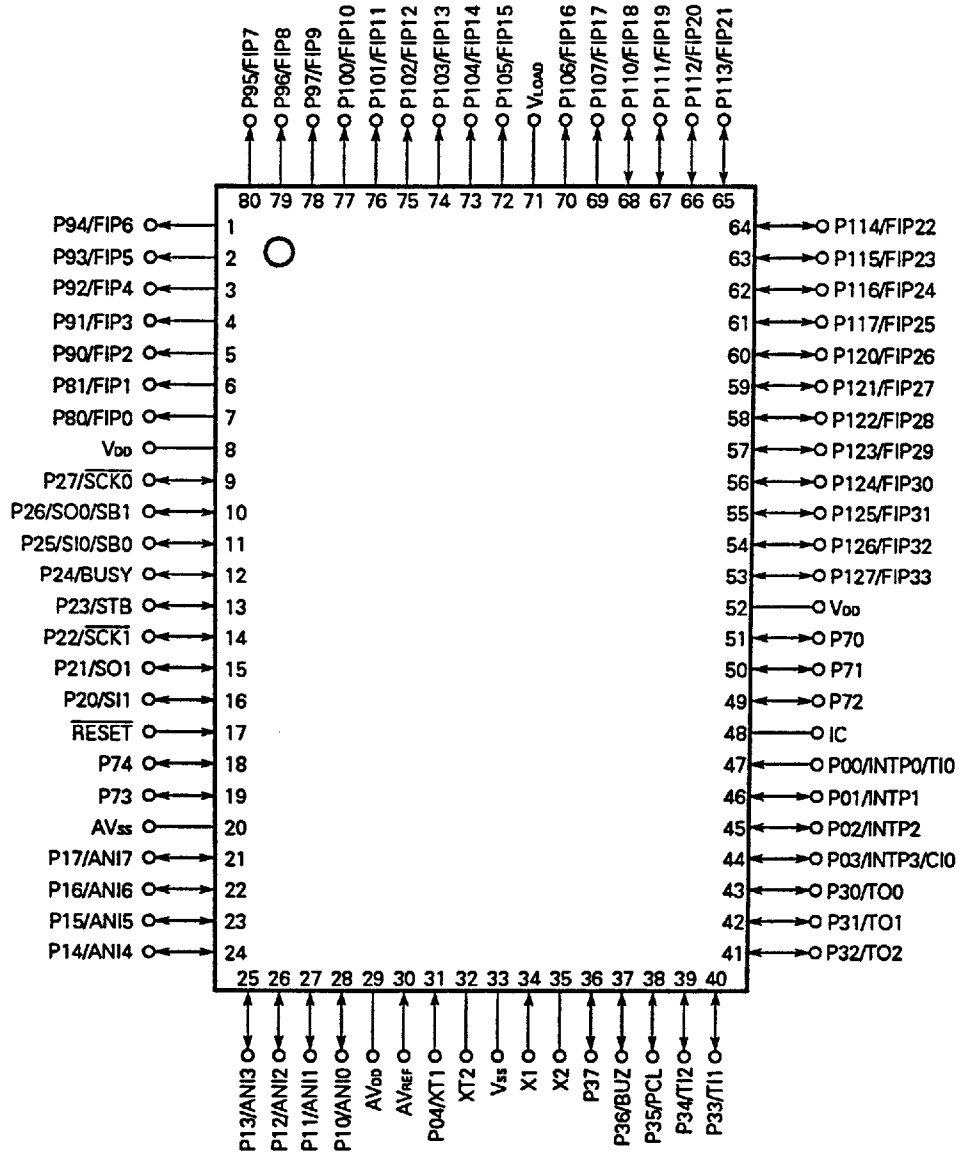
FUNCTIONAL OUTLINE

Item \ Product name		μPD78042A	μPD78043A	μPD78044A	μPD78045A
Internal memory	ROM	16K bytes	24K bytes	32K bytes	40 K bytes
	Internal high-speed RAM	512 bytes		1024 bytes	
	Buffer RAM	64 bytes			
	FIP display RAM	48 bytes			
General registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)			
Instruction cycle		Variable instruction execution time			
	For main system clock	0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs (at 5.0 MHz)			
	For subsystem clock	122 μs (at 32.768 kHz)			
Instruction set		• Multiplication/division (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit (set, reset, test, Boolean algebra)			
I/O ports (including those multiplexed with FIP pins)		Total : 68 lines • CMOS input : 2 lines • CMOS I/O : 27 lines • N-ch open-drain : 5 lines • P-ch open-drain I/O : 16 lines • P-ch open-drain output : 18 lines			
FIP controller/driver		Total : 34 lines • Segments : 9 to 24 lines • Digits : 2 to 16 lines			
A/D converter		• 8-bit resolution × 8 channels • Power supply voltage: V_{DD} = 4.0 to 6.0 V			
Serial interface		• 3-line/SBI/2-line mode selectable : 1 channel • 3-line mode (with automatic transmission/reception function of up to 64 bytes) : 1 channel			
Timer		• 16-bit timer/event counter : 1 channel • 8-bit timer/event counter : 2 channels • Watch timer : 1 channel • Watchdog timer : 1 channel • 6 bit up/down counter : 1 channel			
Timer output		3 lines (one for 14-bit PWM output)			
Clock output		19.5 kHz, 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz (at main system clock of 5.0 MHz) 32.768 kHz (at subsystem clock of 32.768 kHz)			
Buzzer output		1.2 kHz, 2.4 kHz, 4.9 kHz (at 5.0 MHz: main system clock)			
Vectored interrupt	Maskable interrupt	Internal 10 lines, external 4 lines			
	Non-maskable interrupt	Internal 1 line			
	Software interrupt	Internal 1 line			
Text input		Internal 1 line			
Power supply voltage		V_{DD} = 2.7 to 6.0 V			
Package		80-pin plastic QFP (14 × 20 mm)			

CONTENTS

1. PIN CONFIGURATION (TOP VIEW)

- 80-pin plastic QFP (14 x 20 mm)
  μPD78042AGF-xxx-3B9, μPD78043AGF-xxx-3B9
  μPD78044AGF-xxx-3B9, μPD78045AGF-xxx-3B9



Cautions 1. Connect the IC (Internally Connected) pins directly to the Vss.

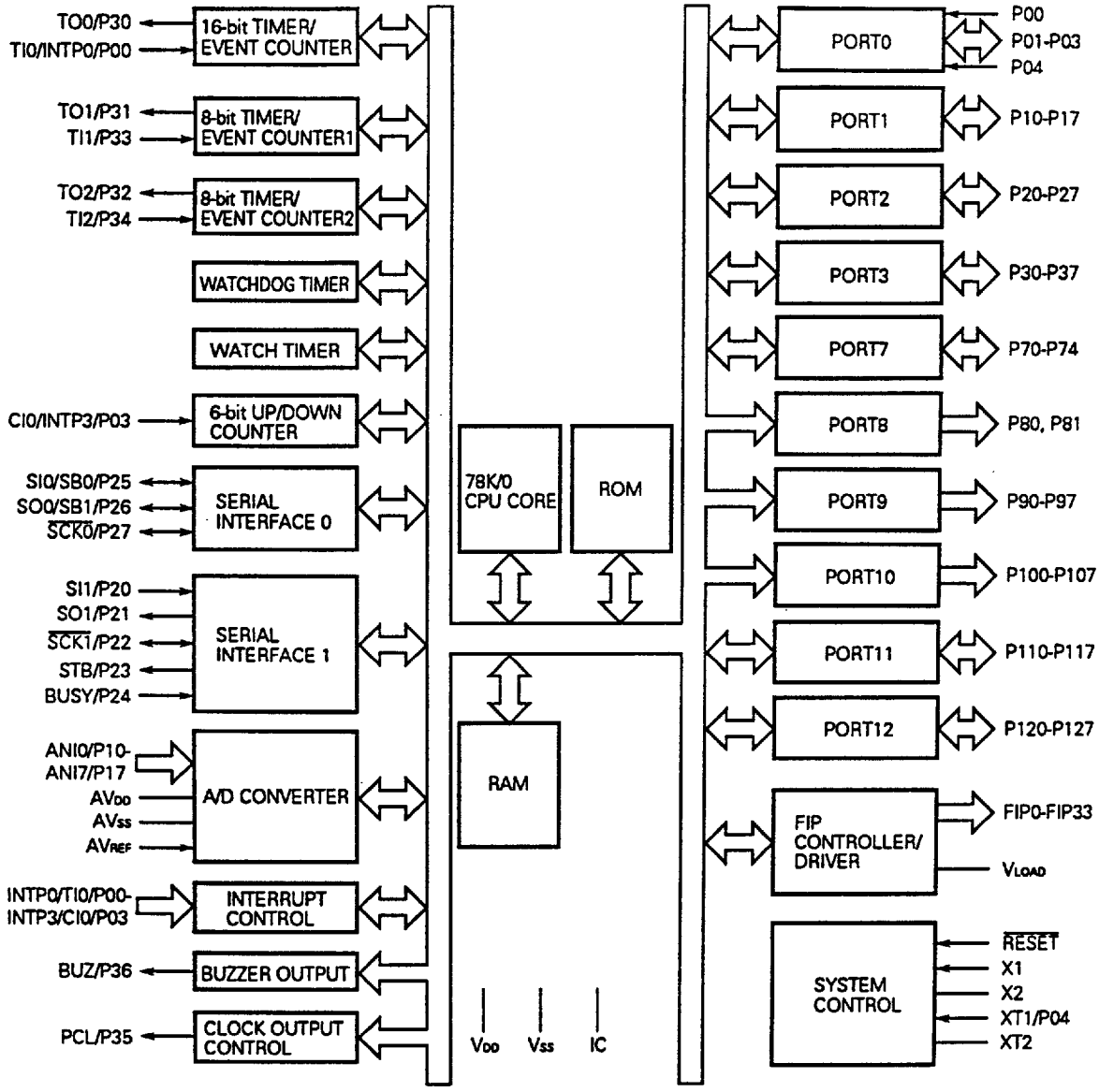
2. Connect the AVDD pin to the VDD pin.

3. Connect the AVss pin to the Vss pin.

P00-P04 : Port0
P10-P17 : Port1
P20-P27 : Port2
P30-P37 : Port3
P70-P74 : Port7
P80,P81 : Port8
P90-P97 : Port9
P100-P107 : Port10
P110-P117 : Port11
P120-P127 : Port12
INTP0-INTP3 : Interrupt From Peripherals
TI0-TI2 : Timer Input
TO0-TO2 : Timer Output
CIO : Counter Input
SB0,SB1 : Serial Bus
SI0,SI1 : Serial Input
SO0,SO1 : Serial Output

$\overline{SCK0}$,$\overline{SCK1}$: Serial Clock
PCL : Programmable Clock
BUZ : Buzzer Clock
STB : Strobe
BUSY : Busy
FIP0-FIP33 : Fluorescent Indicator Panel
V_{LOAD} : Negative Power Supply
X1,X2 : Crystal (Main System Clock)
XT1,XT2 : Crystal (Subsystem Clock)
$\overline{RESET}$: Reset
ANI0-ANI7 : Analog Input
AV_{DD} : Analog Power Supply
AVss : Analog Ground
AV_{REF} : Analog Reference Voltage
V_{DD} : Power Supply
Vss : Ground
IC : Internally Connected

2. BLOCK DIAGRAM



Remark The capacities of the internal ROM and RAM differ depending on the product.

3. PINS FUNCTIONS

3.1 PORT PINS (1/2)

Pin name	I/O	Function		On reset	Shared by:
P00	Input	Port 0 5-bit I/O port	Input only	Input	INTP0/TI0
P01	I/O		Can be specified for input or output in 1-bit units. When used as an input port pin, a pull-up resistor can be connected through software.	Input	INTP1
P02					INTP2
P03					INTP3/CI0
P04[Note 1]	Input		Input only	Input	XT1
P10-P17	I/O	Port 1 8-bit I/O port Can be specified for input or output in 1-bit units. When used as an input port pin, a pull-up resistor can be connected through software.[Note 2]		Input	ANI0-ANI7
P20	I/O	Port 2 8-bit I/O port Can be specified for input or output in 1-bit units. When used as an input port pin, a pull-up resistor can be connected through software.		Input	SI1
P21					SO1
P22					$\overline{SCK1}$
P23					STB
P24					BUSY
P25					SI0/SB0
P26					SO0/SB1
P27					$\overline{SCK0}$
P30	I/O	Port 3 8-bit I/O port Can be specified for input or output in 1-bit units. Can directly drive LEDs. When used as an input port pin, a pull-up resistor can be connected through software. A pull-down resistor can be connected in 1-bit units by the mask option.		Input	TO0
P31					TO1
P32					TO2
P33					TI1
P34					TI2
P35					PCL
P36					BUZ
P37					—

Notes 1. When the P04/XT1 pins is used as an input port pin, bit 6 (FRC) of the processor clock control register must be set to 1. At this time, do not use the feedback resistor of the subsystem clock oscillator circuit.

2. When the P10/ANI0 through P17/ANI7 pins are used as the analog input lines of the A/D converter, be sure to place the port 1 in the input mode. In this case, the pull-up resistors are automatically unused.

3.1 PORT PINS (2/2)

Pin name	I/O	Function	On reset	Shared by:
P70-P74	I/O	Port 7 5-bit N-ch open-drain I/O port Can be specified for input or output in 1-bit units. Can directly drive LEDs. A pull-up resistor can be connected in 1-bit units by the mask option.	Input	—
P80, P81	Output	Port 8 2-bit P-ch open-drain high-voltage output port. Can directly drive LEDs. A pull-down resistor can be connected in 1-bit units by the mask option (whether V_{LOAD} or V_{SS} is connected can be specified in bit units).	Output	FIP0, FIP1
P90-P97	Output	Port 9 8-bit P-ch open-drain high-voltage output port. Can directly drive LEDs. A pull-down resistor can be connected in 1-bit units by the mask option (whether V_{LOAD} or V_{SS} is connected can be specified in 4-bit units).	Output	FIP2-FIP9
P100-P107	Output	Port 10 8-bit P-ch open-drain high-voltage output port. Can directly drive LEDs. A pull-down resistor can be connected in 1-bit units by the mask option (whether V_{LOAD} or Vss is connected can be specified in 4-bit units).	Output	FIP10-FIP17
P110-P117	I/O	Port 11 8-bit P-ch open-drain high-voltage I/O port. Can directly drive LEDs. Can be specified for input or output in 1-bit units. A pull-down resistor can be connected in 1-bit units by the mask option (whether V_{LOAD} or V_{SS} is connected can be specified in 4-bit units).	Input	FIP18-FIP25
P120-P127	I/O	Port 12 8-bit P-ch open-drain high-voltage I/O port Can directly drive LEDs. Can be specified for input or output in 1-bit units. A pull-down resistor can be connected in 1-bit units by the mask option (whether V_{LOAD} or V_{SS} is connected can be specified in 4-bit units).	Input	FIP26-FIP33

3.2 PINS OTHER THAN PORT PINS (1/2)

Pin name	I/O	Function	On reset	Shared by:
INTP0	Input	Valid edge (rising, falling, or both rising and falling edges) can be specified. External interrupt input	Input	P00/TI0
INTP1				P01
INTP2				P02
INTP3		Falling edge-active external interrupt input	Input	P03/CI0
SI0	Input	Serial data input lines of serial interface	Input	P25/SB0
SI1				P20
SO0	Output	Serial data output lines of serial interface	Input	P26/SB1
SO1				P21
SB0	I/O	Serial data I/O lines of serial interface	Input	P25/SI0
SB1				P26/SO0
$\overline{SCK0}$	I/O	Serial clock I/O lines of serial interface	Input	P27
$\overline{SCK1}$				P22
STB	Output	Automatic transmission/reception strobe output line of serial interface	Input	P23
BUSY	Input	Automatic transmission/reception busy input line of serial interface	Input	P24
TI0	Input	External count clock input to 16-bit timer (TM0)	Input	P00/INTP0
TI1		External count clock input to 8-bit timer (TM1)		P33
TI2		External count clock input to 8-bit timer (TM2)		P34
TO0	Output	16-bit timer output (multiplexed with 14-bit PWM output)	Input	P30
TO1		8-bit timer output		P31
TO2				P32
CI0	Input	Clock input to up/down counter	Input	P03/INTP3
PCL	Output	Clock output (for trimming main system clock and subsystem clock)	Input	P35
BUZ	Output	Buzzer output	Input	P36
FIP0, FIP1	Output	High-voltage, high-current digit/segment output of FIP controller/driver	Output	P80, P81
FIP2-FIP9				P90-P97
FIP10-FIP15	Output	High-voltage, high-current digit/segment output of FIP controller/driver	Output	P100-P105
FIP16, FIP17	Output	High-voltage segment output of FIP controller/driver	Output	P106, P107
FIP18-FIP25			Input	P110-P117
FIP26-FIP33				P120-P127
V_{LOAD}	—	Connects pull-down resistor to FIP controller/driver	—	—

3.2 PINS OTHER THAN PORT PINS (2/2)

Pin name	I/O	Function	On reset	Shared by:
ANI0-ANI7	Input	A/D converter analog input lines	Input	P10-P17
AV_{REF}	Input	A/D converter reference voltage input line	—	—
AV_{DD}	—	Analog power supply to A/D converter. Connected to the V_{DD} pin.	—	—
AV_{SS}	—	A/D converter ground line. Connected to the Vss pin.	—	—
$\overline{\text{RESET}}$	Input	System reset input	—	—
X1	Input	Connect crystal for main system clock oscillation	—	—
X2	—		—	—
XT1	Input	Connect crystal for subsystem clock oscillation	Input	P04
XT2	—		—	—
V_{DD}	—	Positive power supply	—	—
V_{SS}	—	Ground potential	—	—
IC	—	Internal connection. Connected directly to the Vss pin.	—	—

3.3 PIN I/O CIRCUITS AND PROCESSING OF UNUSED PINS

Table 3-1 shows the I/O circuit type of each pin and the processing of unused pins.
For the configuration of the I/O circuit of each type, refer to Fig. 3-1.

Table 3-1 I/O Circuit Type

Pin name	I/O Circuit type	I/O	Recommended connections when unused
P00/INTP0/TI0	2	Input	Connected to V_{SS}.
P01/INTP1	8-A	I/O	Individually connected to V_{SS} with a resistor.
P02/INTP2			
P03/INTP3/CI0			
P04/XT1	16	Input	Connected to V_{DD} or V_{SS}. ★
P10/ANI0-P17/ANI7	11	I/O	Individually connected to V_{DD} or V_{SS} with a resistor.
P20/SI1	8-A		
P21/SO1	5-A		
P22/$\overline{SCK1}$	8-A		
P23/STB	5-A		
P24/BUSY	8-A		
P25/SI0/SB0	10-A		
P26/SO0/SB1			
P27/$\overline{SCK0}$			
P30/TO0	5-C		
P31/TO1			
P32/TO2			
P33/TI1	8-B		
P34/TI2			
P35/PCL	5-C		
P36/BUZ			
P37			
P70-P74	13-B		★
P80/FIP0, P81/FIP1	14-A	Output	Open
P90/FIP2-P97/FIP9			
P100/FIP10-P107/FIP17			
P110/FIP18-P117/FIP25	15-C	I/O	Individually connected to V_{DD} or V_{SS} with a resistor. ★
P120/FIP26-P127/FIP33			
$\overline{RESET}$	2	Input	—
XT2	16	—	Open
AV_{REF}	—		Connected to V_{SS}.
AV_{DD}			Connected to V_{DD}.
AV_{SS}			Connected to V_{SS}.
V_{LOAD}			
IC			Connected directly to V_{SS}.

Fig. 3-1 Pin I/O Circuits (1/2)

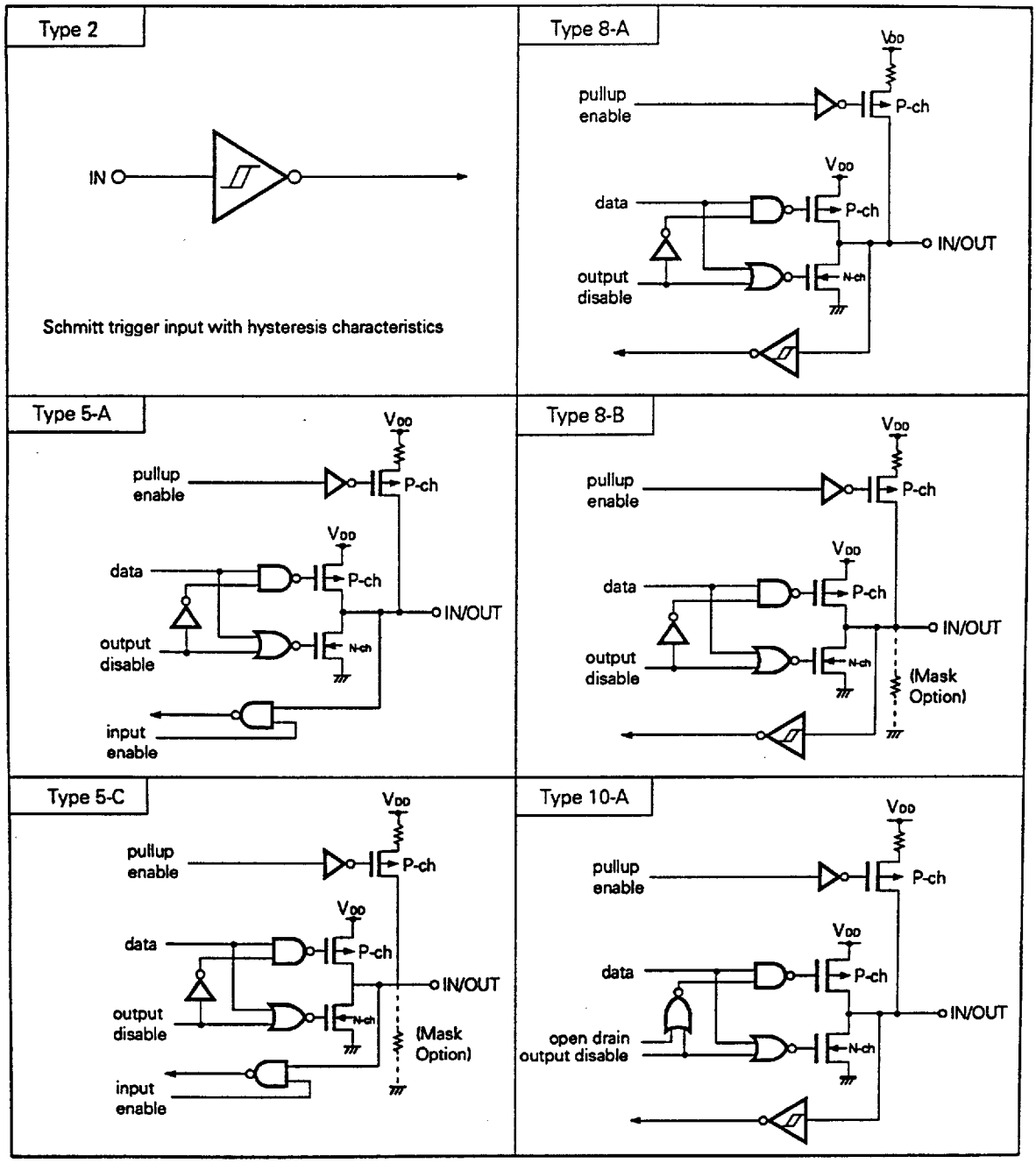
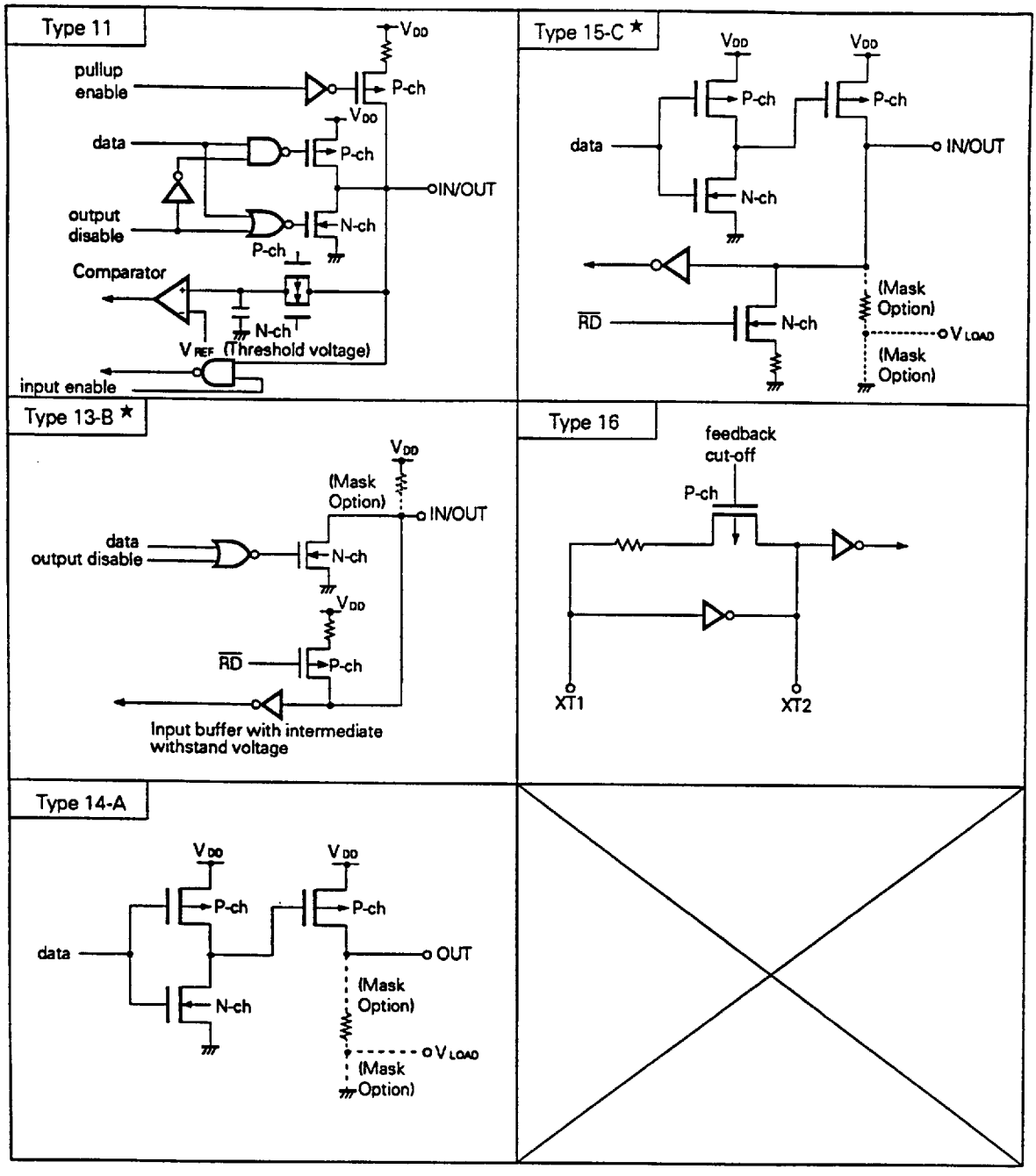


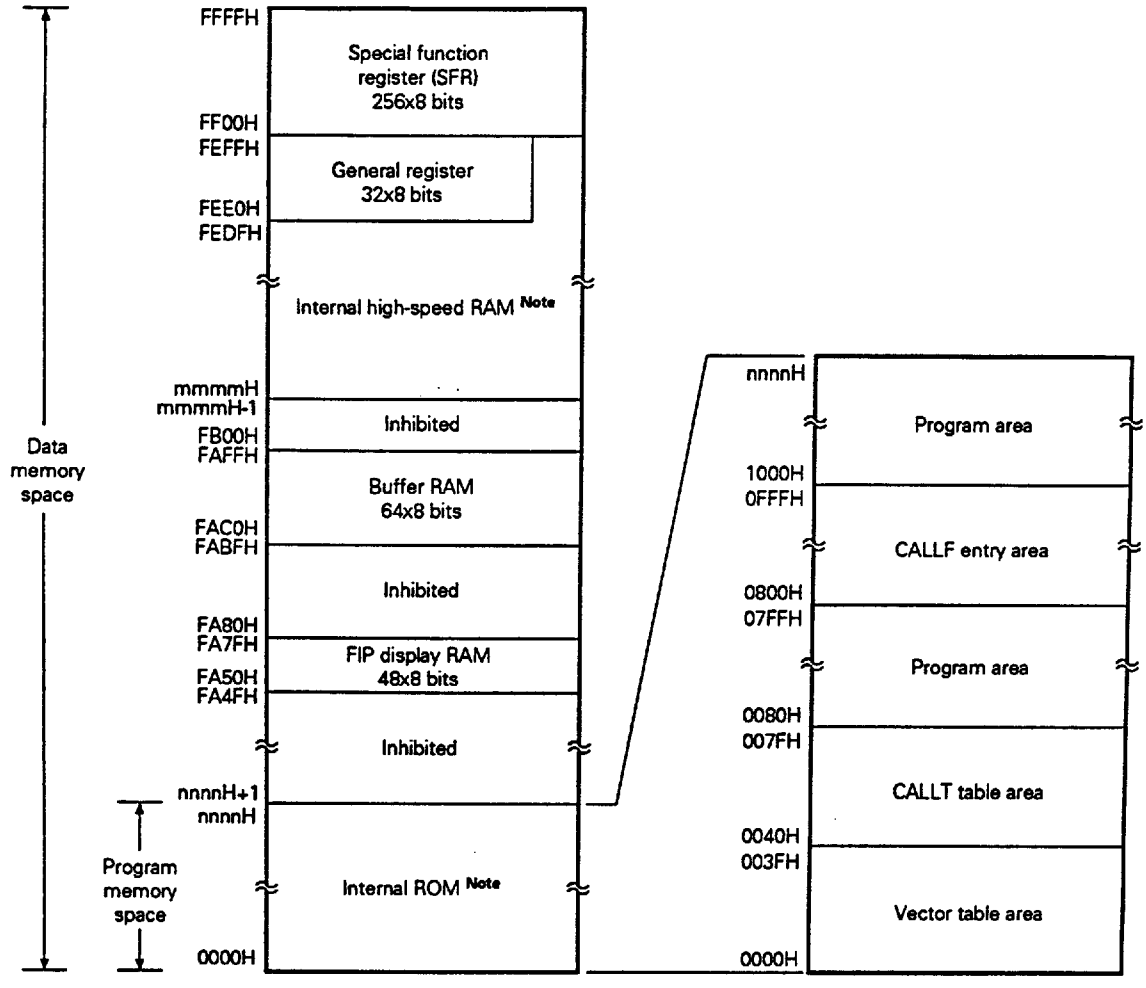
Fig. 3-1 Pin I/O Circuits (2/2)



4. MEMORY SPACE

Fig. 4-1 shows the memory map for μPD78042A, μPD78043A, μPD78044A, and μPD78045A.

Fig. 4-1 Memory Map



Note The internal ROM and internal high-speed RAM capacities vary depending on the product. (Refer to the table below.)

Product name	Last Address of Internal ROM nnnnH	First address of internal high-speed RAM mmmmH
μPD78042A	3FFFH	FD00H
μPD78043A	5FFFH	
μPD78044A	7FFFH	FB00H
μPD78045A	9FFFH	

5. PERIPHERAL HARDWARE FUNCTIONS

5.1 PORTS

I/O ports are classified into the following 5 kinds:

- CMOS input (P00, P04) : 2
- CMOS input/output (P01 - P03, ports 1 - 3) : 27
- N-ch open-drain input/output (port 7) : 5
- P-ch open-drain output (ports 8 - 10) : 18
- P-ch open-drain input/output (ports 11 and 12) : 16

Total : 68

Table 5-1 Port Function

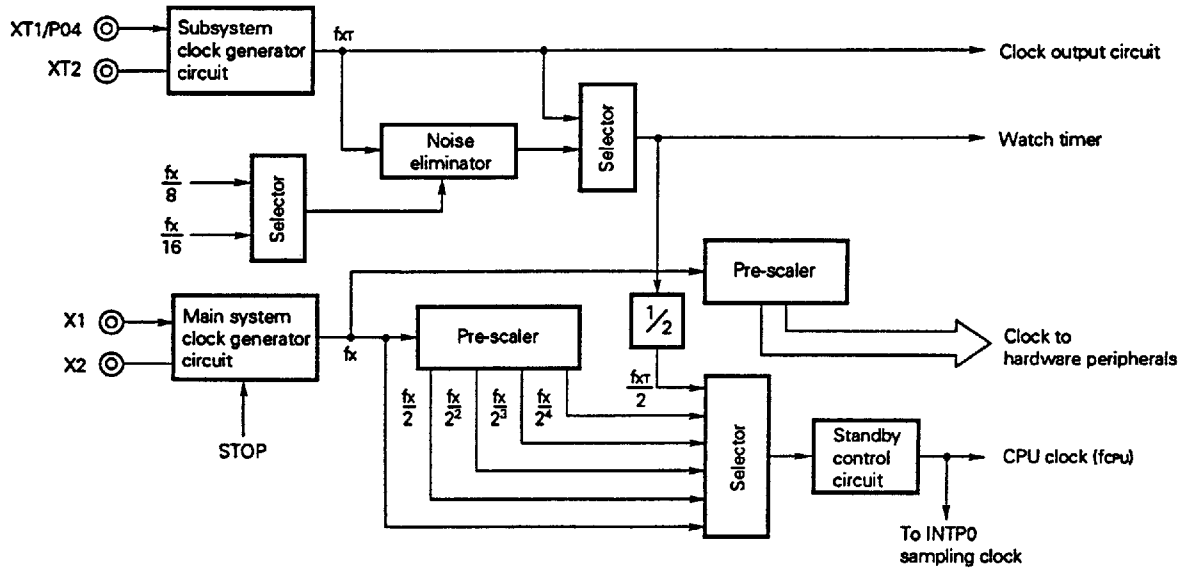
Product	Pin	Function
Port 0	P00, P04	Input port
	P01-P03	I/O port. Can be specified for input or output in 1-bit units. When used as input port, internal pull-up resistor can be connected through software.
Port 1	P10-P17	I/O port. Can be specified for input or output in 1-bit units. When used as input port, internal pull-up resistor can be connected through software.
Port 2	P20-P27	I/O port. Can be specified for input or output in 1-bit units. When used as input port, internal pull-up resistor can be connected through software.
Port 3	P30-P37	I/O port. Can be specified for input or output in 1-bit units. When used as input port, internal pull-up resistor can be connected through software. Pull-down resistor can be connected in 1-bit units by the mask option. Can directly drive LED.
Port 7	P70-P74	N-ch open-drain I/O port. Can be specified for input or output in 1-bit units. Pull-up resistor can be connected in 1-bit units by the mask option. Can directly drive LED.
Port 8	P80, P81	P-ch open-drain high-voltage output port. Pull-down resistor can be connected in 2-bit units by the mask option (connection to V_{LOAD} or V_{SS} can be specified in 2-bit units). Can directly drive LED.
Port 9	P90-P97	P-ch open-drain high-voltage output port. Pull-down resistor can be connected in 1-bit units by the mask option (connection to V_{LOAD} or V_{SS} can be specified in 4-bit units). Can directly drive LED.
Port 10	P100-P107	P-ch open-drain high-voltage output port. Pull-down resistor can be connected in 1-bit units by the mask option (connection to V_{LOAD} or V_{SS} can be specified in 4-bit units). Can directly drive LED.
Port 11	P110-P117	P-ch open-drain high-voltage I/O port. Can be specified for input or output in 1-bit units. Pull-down resistor can be connected in 1-bit units by the mask option (connection to V_{LOAD} or V_{SS} can be specified in 4-bit units). Can directly drive LED.
Port 12	P120-P127	P-ch open-drain high-voltage I/O port. Can be specified for input or output in 1-bit units. Pull-down resistor can be connected in 1-bit units by the mask option (connection to V_{LOAD} or V_{SS} can be specified in 4-bit units). Can directly drive LED.

5.2 CLOCK GENERATOR CIRCUIT

The clock generator circuit has two kinds of generator circuits: the main system clock and subsystem clock. The instruction time can be changed.

- 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs (with main system clock: 5.0 MHz)
- 122 μs (with subsystem clock: 32.768 kHz)

★ **Fig. 5-1 Clock Generator Circuit Block Diagram**



5.3 TIMER/EVENT COUNTER

Six channels of timer/event counters are provided.

- 16-bit timer/event counter : 1 channel
- 8-bit timer/event counter : 2 channels
- Watch timer : 1 channel
- Watchdog timer : 1 channel
- 6-bit up/down counter : 1 channel

Table 5-2 Timer/Event Counter Groups and Configurations

		16-bit timer/ event counter	8-bit timer/ event counter	Watch timer	Watchdog timer	6-bit up/ down counter
Group	Interval timer	1 channel	2 channels	1 channel	1 channel	—
	External event counter	1 channel	2 channels	—	—	1 channel
Function	Timer output	1 output	2 outputs	—	—	—
	PWM output	1 output	—	—	—	—
	Pulse width measurement	1 input	—	—	—	—
	Square wave output	1 output	2 outputs	—	—	—
	Interrupt Request	1	2	1	1	1
★	Test input	—	—	1 input	—	—

Fig. 5-2 16-Bit Timer/Event Counter Block Diagram

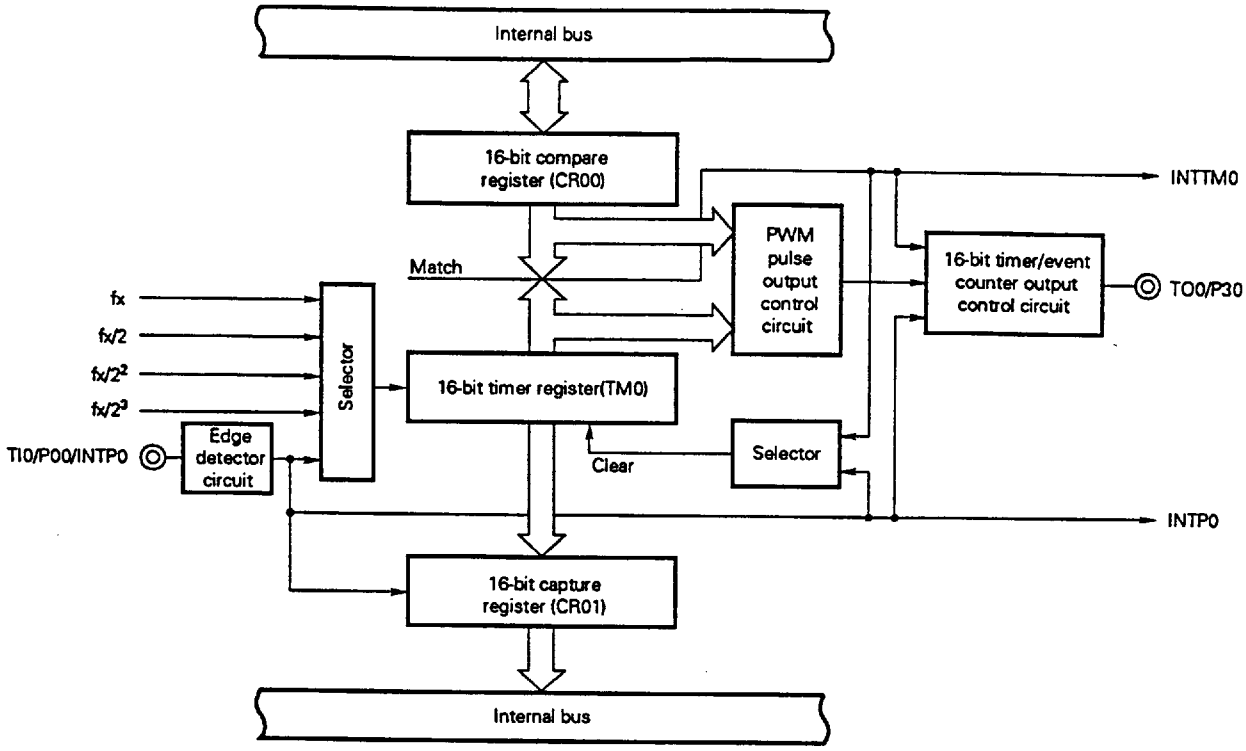


Fig. 5-3 8-Bit Timer/Event Counter Block Diagram

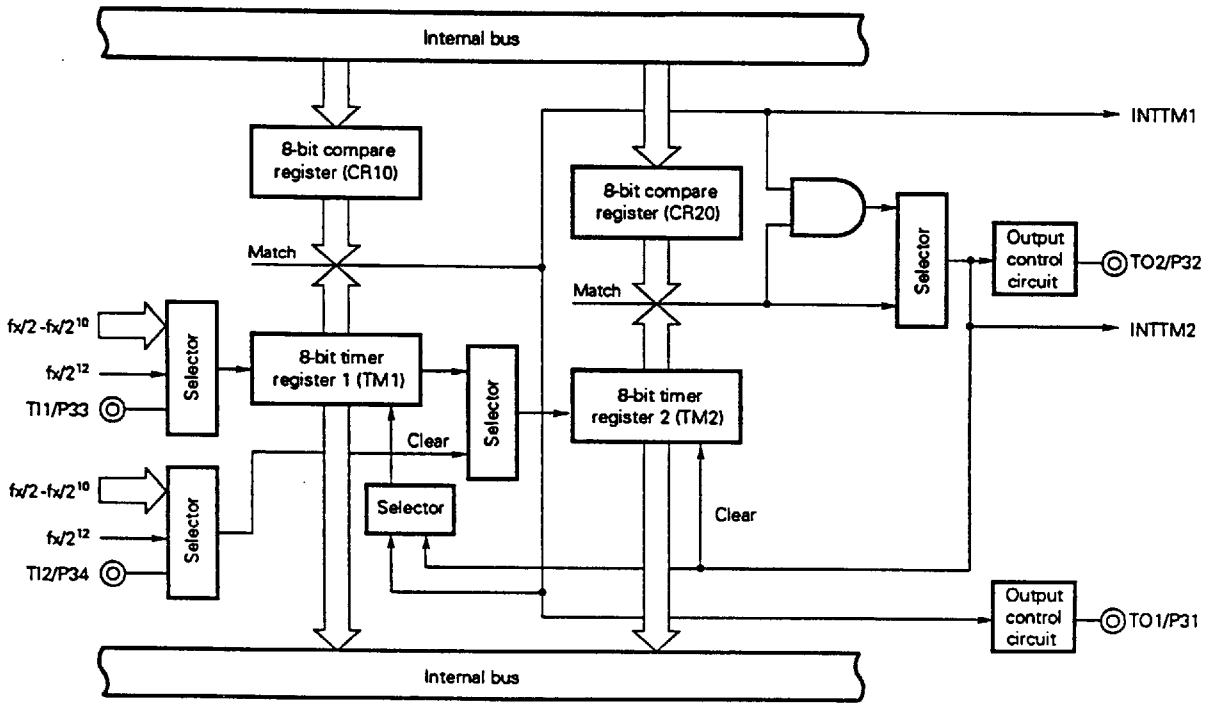


Fig. 5-4 Watch Timer Block Diagram

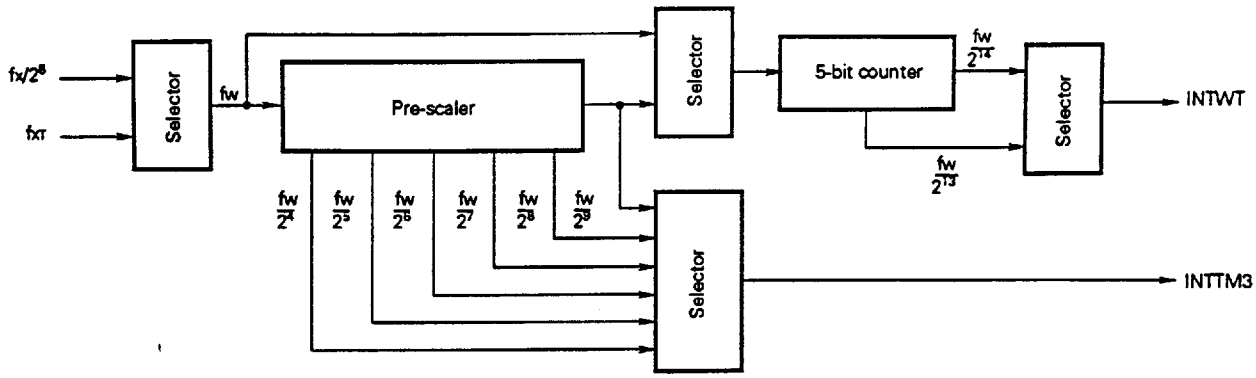


Fig. 5-5 Watchdog Timer Block Diagram

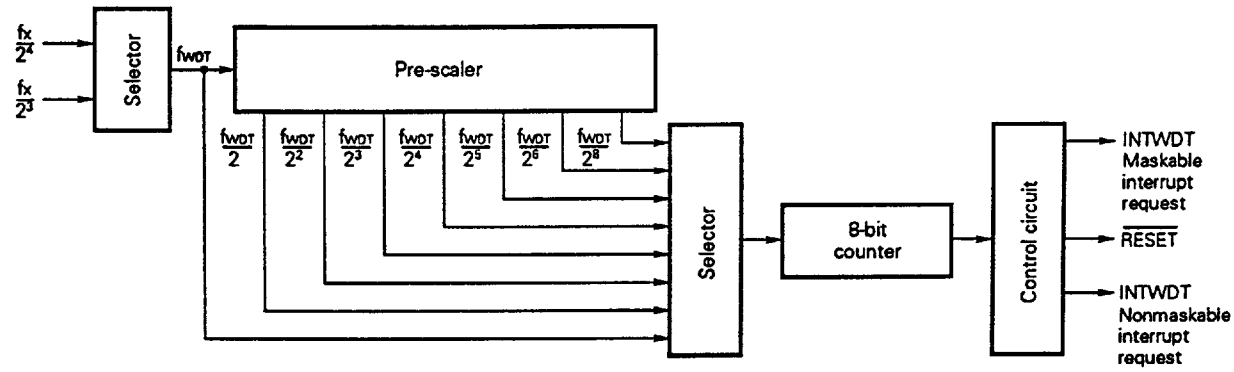
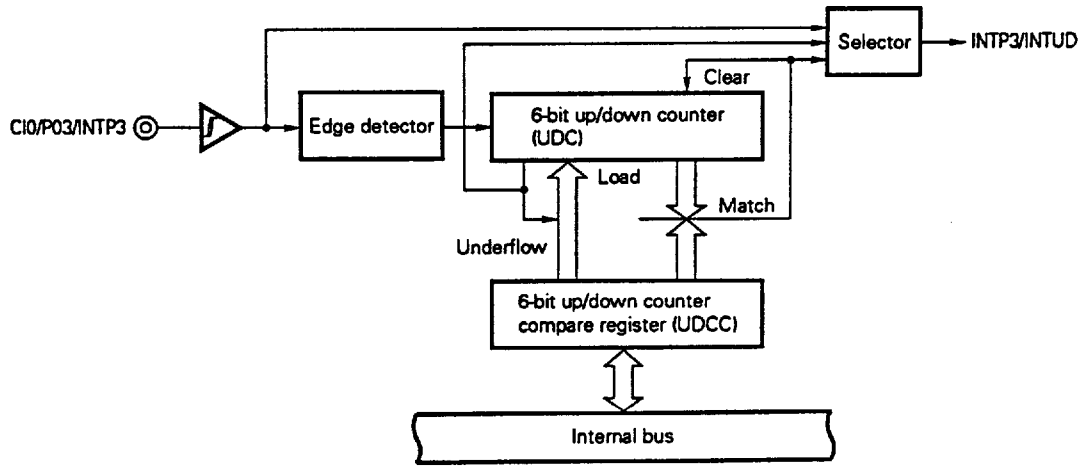


Fig. 5-6 6-Bit Up/Down Counter Block Diagram



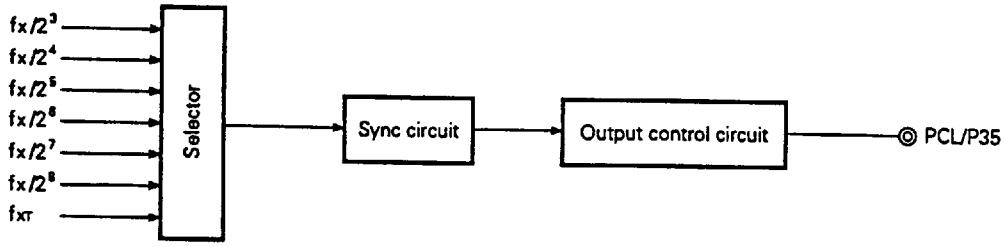
Caution When using the 6-bit up/down counter, set the CI0/P03/INTP3 pin in the input mode (set bit 3 of port mode register 0 (PM03) to 1).

5.4 CLOCK OUTPUT CONTROL CIRCUIT

Clocks of the following frequencies can be output to the clock:

- 19.5 kHz/39.1 kHz/78.1 kHz/156 kHz/313 kHz/625 kHz (with main system clock: 5.0 MHz)
- 32.768 kHz (with subsystem clock: 32.768 kHz)

Fig. 5-7 Clock Output Control Circuit Block Diagram

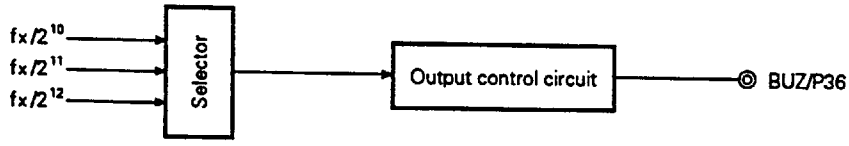


5.5 BUZZER OUTPUT CONTROL CIRCUIT

Clocks of the following frequencies can be output to the buzzer:

- 1.2 kHz/2.4 kHz/4.9 kHz (with main system clock: 5.0 MHz)

Fig. 5-8 Buzzer Output Control Circuit Block Diagram



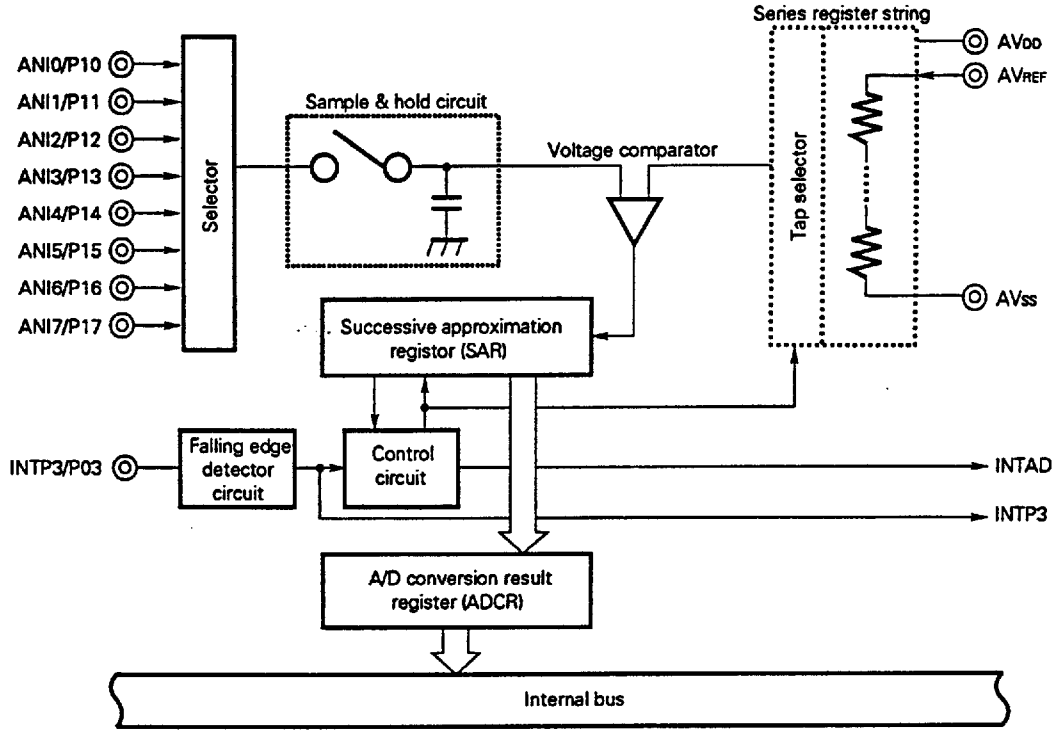
5.6 A/D CONVERTER

An 8-bit resolution 8-channel A/D converter is provided.

This A/D converter can be started in the following two modes:

- Hardware start
- Software start

Fig. 5-9 A/D Converter Block Diagram



5.7 SERIAL INTERFACE

Two channels of clocked serial interfaces are provided.

- Serial interface channel 0
- Serial interface channel 1

Table 5-3 Serial Interface Groups and Functions

Function	Serial interface channel 0	Serial interface channel 1
3-line serial I/O mode	• (MSB/LSB first selectable)	• (MSB/LSB first selectable)
SBI (serial bus interface) mode	• (MSB first)	—
2-line serial I/O mode	• (MSB first)	—
3-wire serial I/O mode with automatic transmission/ reception function	—	• (MSB/LSB first selectable)

Fig. 5-10 Serial Interface Channel 0 Block Diagram

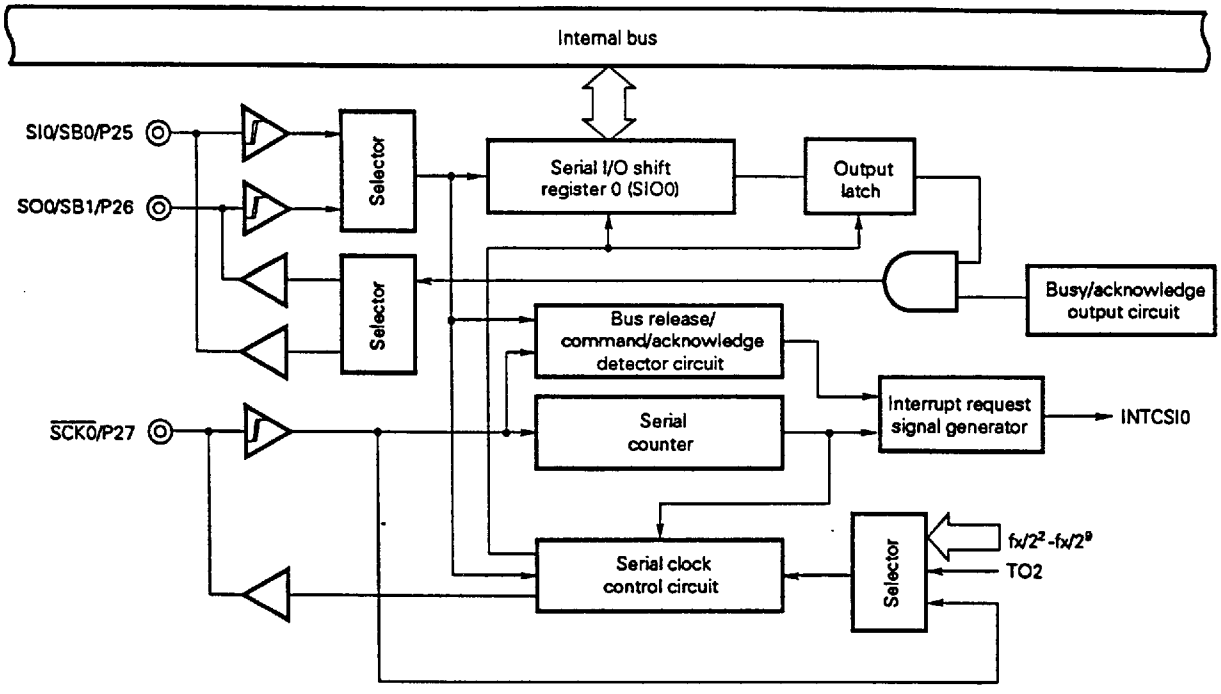
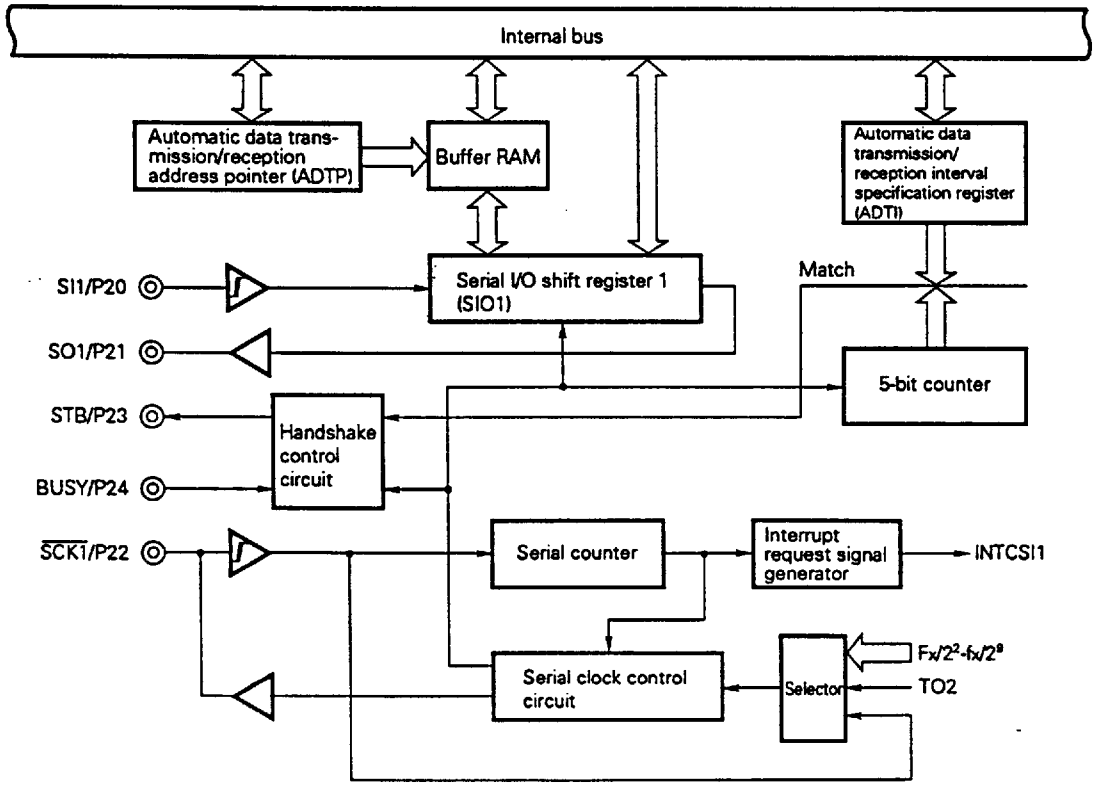


Fig. 5-11 Serial Interface Channel 1 Block Diagram

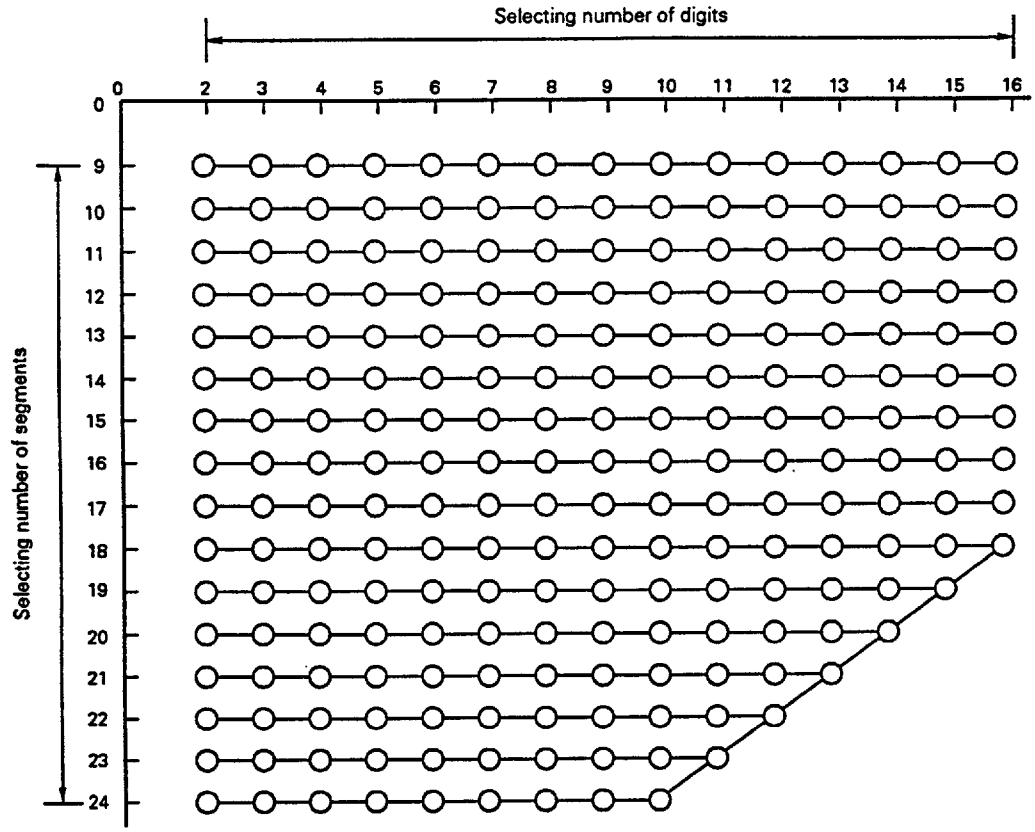


5.8 FIP CONTROLLER/DRIVER

An FIP controller/driver having the following features is provided:

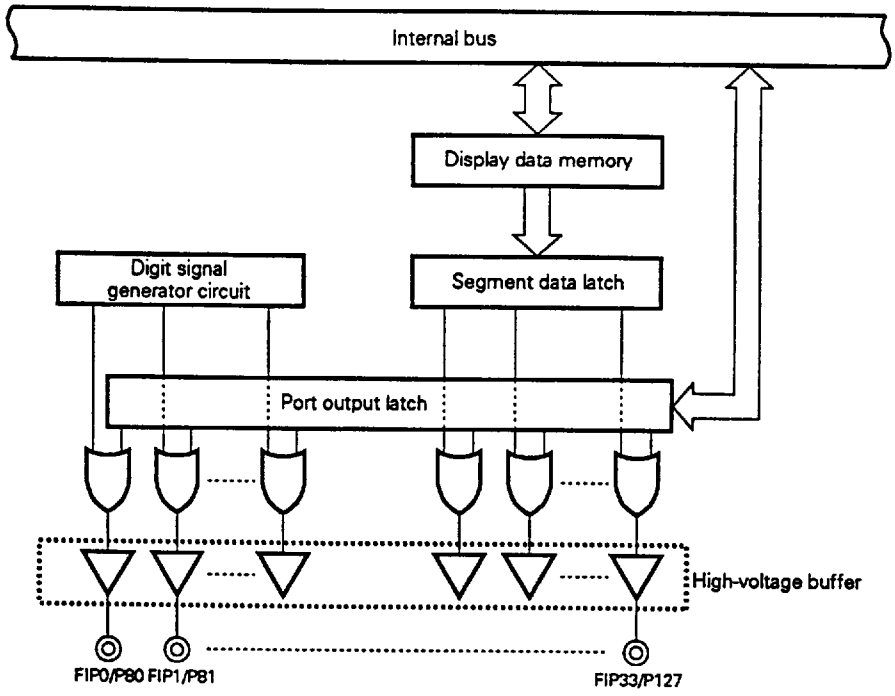
(a) Automatic output of segment signals (DMA operation) and digit signals by automatically reading display data
(b) Display mode registers (DSPM0 and DSPM1) that can control an FIP of 9 to 24 segments and 2 to 16 digits
(c) Port pins not used for FIP display can be used as output port or I/O port pins.
(d) Display mode register (DSPM1) can adjust luminance in eight steps.
(e) Hardware suitable for key scan application using segment pins
(f) High-voltage output buffer (FIP driver) that can directly drive an FIP
(g) Display output pins can be connected to a pull-down resistor by the mask option.

Fig. 5-12 Selecting Display Modes



Caution If the total number of digits and segments exceeds 34, the specified number of digits takes precedence.

Fig. 5-13 FIP Controller/Driver Block Diagram



6. INTERRUPT FUNCTION AND TEST FUNCTION

6.1 INTERRUPT FUNCTION

The following three types of interrupt functions are available:

- Non-maskable interrupt : 1
- Maskable interrupt : 13
- Software interrupt : 1

Table 6-1 Interrupt Source List

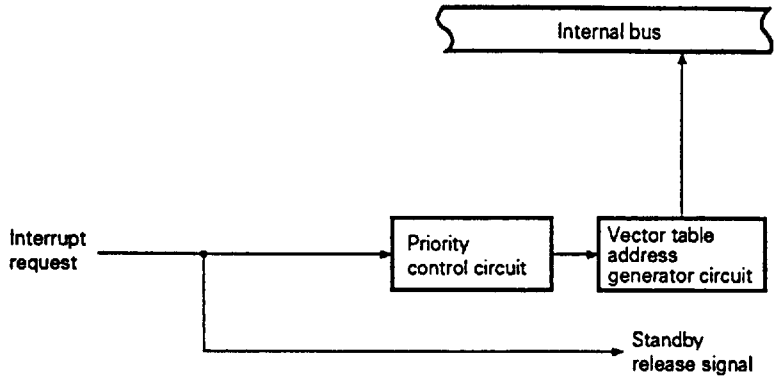
Interrupt type	Default priority (Note 1)	Interrupt source		Internal/ external	Vector table address	Basic configuration type (Note 2)
		Name	Trigger			
Non-maskable	—	INTWDT	Watchdog timer overflow (with watchdog timer mode 1 selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (with interval timer mode selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	(D)
	3	INTP2			000AH	
	4	INTP3			000CH	
		INTUD	Up/down counter match signal generation	Internal		(B)
	5	INTCSI0	End of serial interface channel 0 transfer	Internal	000EH	(B)
	6	INTCSI1	End of serial interface channel 1 transfer		0010H	
	7	INTTM3	Reference time interval signal from watch timer		0012H	
	8	INTTM0	16-bit timer/event counter match signal generation		0014H	
	9	INTTM1	8-bit timer/event counter 1 match signal generation		0016H	
	10	INTTM2	8-bit timer/event counter 2 match signal generation		0018H	
	11	INTAD	End of A/D converter conversion		001AH	
	12	INTKS	Key scan timing from FIP controller/driver		001CH	
Software	—	BRK	Execution of BRK instruction	Internal	003EH	(E)

Notes 1. Default priority is the priority order when several maskable interrupts are generated at the same time. 0 is the highest order and the 12 is the lowest order.

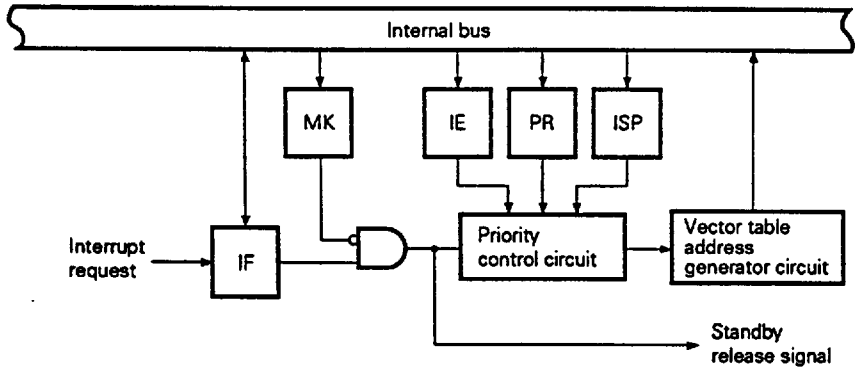
2. Basic configuration types (A) to (E) correspond to (A) to (E) in Fig. 6-1.

Fig. 6-1 Basic Configuration of Interrupt Function (1/2)

(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt (INTP0)

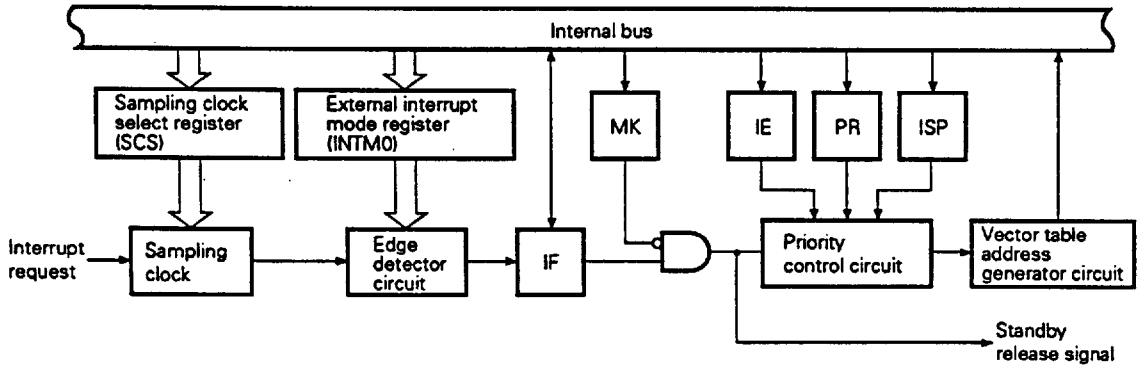
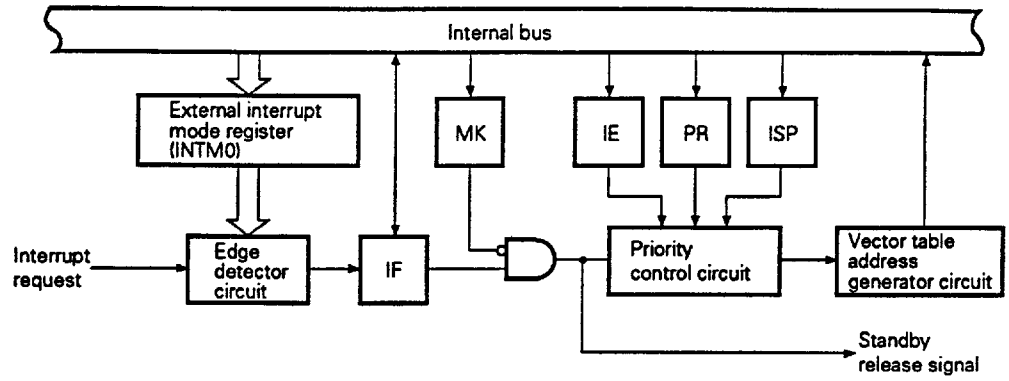
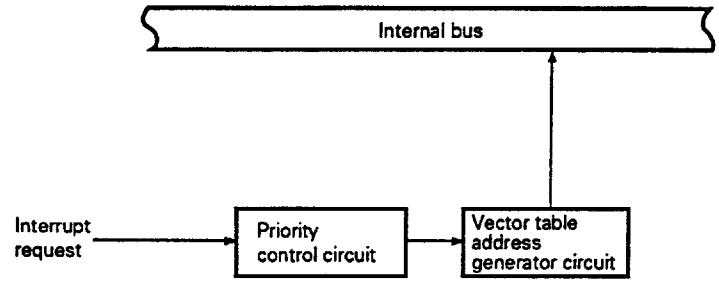


Fig. 6-1 Basic Configuration of Interrupt Function (2/2)

(D) External maskable interrupt (except INTP0)



(E) Software interrupt



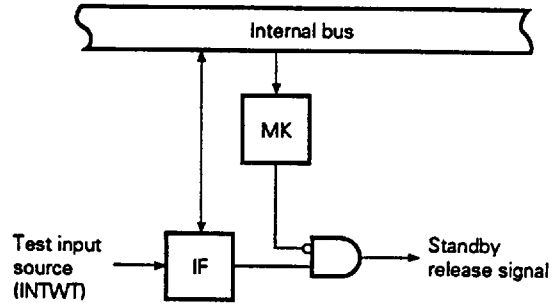
IF : Interrupt request flag
IE : Interrupt enable flag
ISP : In-service priority flag
MK : Interrupt mask flag
PR : Priority specification flag

6.2 TEST FUNCTION

The following test function is available.

Test input source		Internal/external
Name	Trigger	
INTWT	Overflow of watch timer	Internal

Fig. 6-2 Basic Configuration of Test Function



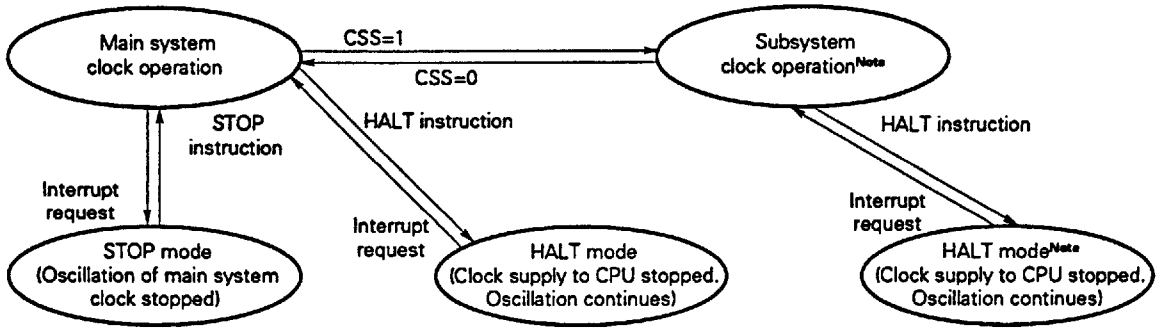
IF : Test request flag
MK : Test mask flag

7. STANDBY FUNCTION

The standby function is to reduce the current dissipation of the system and can be effected in the following two modes:

- HALT mode: In this mode, the operating clock of the CPU is stopped. By using this mode in combination with the normal operation mode, the system can be operated intermittently, so that the average current dissipation can be reduced.
- STOP mode: Oscillation of the main system clock is stopped. All the operations on the main system clock are stopped, and therefore, the current dissipation of the system can be minimized with only the subsystem clock oscillating.

Fig. 7-1 Standby Function



Note By stopping the main system clock, the current dissipation can be reduced. When the CPU operates on the subsystem clock, stop the main system clock by setting the MCC. The STOP instruction cannot be used.

Caution When the main system clock is stopped and the subsystem clock is operating, to switch again from the subsystem clock to the main system clock, allow sufficient time for the oscillation to settle before switching, by coding the program accordingly.

8. RESET FUNCTION

The system can be reset in the following two modes:

- External reset by $\overline{\text{RESET}}$ pin
- Internal reset by watchdog timer that detects hang up

9. INSTRUCTION SET

(1) 8-bit instruction

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

First operand \ Second operand	#byte	A	r Note	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL + byte] [HL + B] [HL + C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
rl											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											ROR4 ROL4
[HL + byte] [HL + B] [HL + C]		MOV											
X													MULU
C													DIVUW

Note Except for r=A

(2) 16-bit instruction

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

First operand \ Second operand	#word	AX	rp[Note]	sfrp	saddrp	laddr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW[Note]						INCW DECW PUSH POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
laddr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp=BC, DE, HL

(3) Bit manipulation instruction

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

First operand \ Second operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	Saddr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call/Branch instruction

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

Second operand / First operand	AX	!addr16	!addr11	[addr5]	$addr16
Basic operation	BR	CALL BR	CALLF	CALLT	BR BC BNC BZ BNZ
Compound operation					BT BF BTCLR DBNZ

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

10. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

	Parameter	Symbol	Conditions		Rating	Unit
	Power supply voltage	V_{DD}			−0.3 to +7.0	V
		V_{LOAD}			V_{DD} − 40 to V_{DD} + 0.3	V
		AV_{DD}			−0.3 to V_{DD} + 0.3	V
		AV_{REF}			−0.3 to V_{DD} + 0.3	V
		AV_{SS}			−0.3 to +0.3	V
	Input voltage	V_{I1}	P00-P04, P10-P17 (except when used as analog input pins), P20-P27, P30-P37, X1, X2, XT2, $\overline{RESET}$		−0.3 to V_{DD} + 0.3	V
★		V_{I2}	P70-P74	N-ch open drain	−0.3 to +16 Note 1	V
		V_{I3}	P110-P117, P120-P127	P-ch open drain	V_{DD} − 40 to V_{DD} + 0.3	V
	Output voltage	V_{O1}	P01-P03, P10-P17, P20-P27, P30-P37		−0.3 to V_{DD} + 0.3	V
★		V_{O2}	P70-P74		−0.3 to +16 Note 1	V
		V_{O3}	P80, P81, P90-P97, P100-P107, P110-P117, P120-P127		V_{DD} − 40 to V_{DD} + 0.3	V
	Analog input voltage	V_{AN}	ANI0-ANI7	Analog input pin	AV_{SS} − 0.3 to AV_{REF} + 0.3	V
	Output current, high	I_{OH}	P01-P03, P10-P17, P20-P27, P30-P37 per pin		−10	mA
			P01-P03, P10-P17, P20-P27, P30-P37 total		−30	mA
			P80, P81, P90-P97, P100-P107, P110-P117, P120-P127 per pin		−30	mA
			P80, P81, P90-P97, P100-P107, P110-P117, P120-P127 total		−120	mA
	Output current, low	I_{OL}	P01-P03, P10-P17, P20-P27, P30-P37, P70-P74 per pin	Peak value	30	mA
				rms value	15 Note 2	mA
			P70-P74 total	Peak value	100	mA
				rms value	60 Note 2	mA
			P01-P03, P10-P17, P20-P27, P30-P37 total	Peak value	50	mA
				rms value	20 Note 2	mA
	Total power dissipation	P_T Note 3	T_A = −40 to +60 °C		800	mW
					600	mW
	Operating ambient temperature	T_A			−40 to +85	°C
	Storage temperature	T_{stg}			−65 to +150	°C

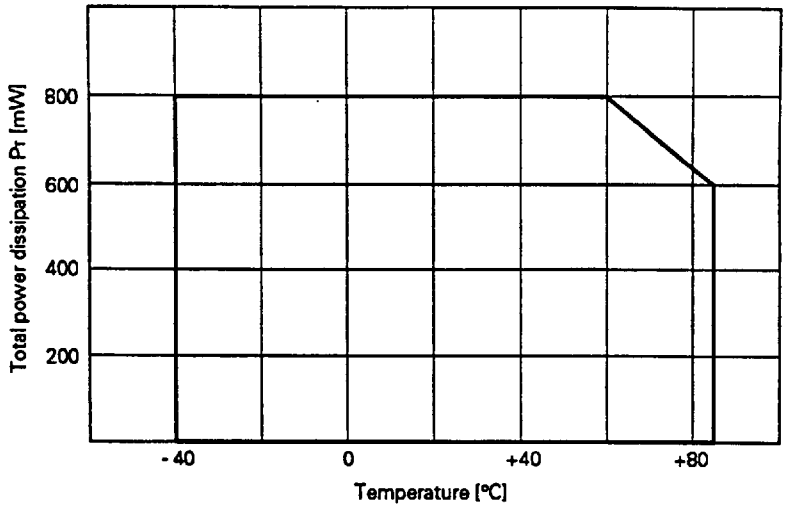
Caution Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The parameters apply independently. The device should be operated within the limits specified under DC and AC Characteristics.

Remark Unless otherwise specified, the characteristics of a shared pin are the same as those of a port pin.

Notes 1. For pins to which pull-up resistors are connected by the mask option, the rating is -0.3 to V_{DD} + 0.3.

2. To obtain the rms value, calculate [rms value] = [peak value] × $\sqrt{duty}$.

Notes 3. Permissible total power dissipation differs depending on the temperature (see the following figure).



How to calculate total power dissipation

The following three power dissipation are available for the μPD78042A, μPD78043A, μPD78044A and μPD78045A. The sum of the three power dissipation should be less than the total power dissipation P_T (80 % or less of ratings is recommended).

① CPU power dissipation: calculate V_{DD} (MAX.) × I_{DD1} (MAX.).
② Output pin power dissipation: Normal output and display output are available. Power dissipation when maximum current flows into each output pin is added.
③ Pull-down resistor power dissipation: Power dissipation by pull-down resistor connected to display output pin by the mask option.

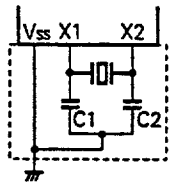
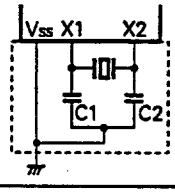
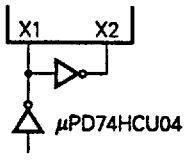
Example 9 segments × 11 digits, 4LED outputs, V_{DD} = 5 V ±10 %, 5.0 MHz oscillation
13 mA (MAX.) flows into segment pin and timing pin. 10 mA (MAX.) flows into LED output pin. The voltage of the FIP (voltage of V_{LOAD}) is −30 V.
Other output power dissipation is considered to be small.

① CPU power dissipation : 5.5 V × 21.6 mA = 118.8 mW
② Pin power dissipation : Segment pin ..... 2 V × 13 mA × 9 lines = 234 mW
Timing pin ..... 2 V × 13 mA = 26 mW
LED output ..... $\left[\frac{10}{15} \times 2\ \text{V}\right] \times 10\ \text{mA} \times 4\ \text{lines} = 53.3\ \text{mW}$
③ Pull-down resistor power dissipation: $\left[\frac{(30 + 5.5\ \text{V})^2}{25\ \text{k}\Omega}\right] \times 7\ \text{lines} = 352.9\ \text{mW}$

The total power dissipation = ① + ② + ③ = 785 mW (< P_T = 800 mW)

In this example, if the temperature range is T_A = −40 °C to +60 °C, the permissible total power dissipation is 800 mW from the graph above, so there is no problem in power dissipation of 785 mW. However, when the total power dissipation exceeds the rating of the permissible total power dissipation, it is necessary to lower the power dissipation.
Lowering the power dissipation can be realized by reducing the number of internal pull-down resistors.

MAIN SYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T_A = −40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

Resonator	Recommended circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)Note 1		1		5	MHz
		Oscillation stabilization timeNote 2				4	ms
Crystal resonator		Oscillation frequency (f_X)Note 1		1	4.19	5	MHz
		Oscillation stabilization timeNote 2	V_{DD} = 4.5 to 6.0 V			10	ms
						30	
External clock		X1 input frequency (f_X)Note 1		1		5	MHz
		X1 input high, low-level width (t_{XH}, t_{XL})		100		500	ns

Notes 1. It indicates only the oscillator characteristics. For the instruction execution time, see the AC Characteristics.

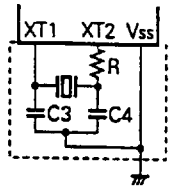
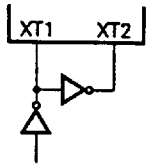
2. Time required until oscillation becomes stable after V_{DD} is applied or the STOP mode is disabled.

Cautions 1. If the main system clock oscillator is to be used, wire the area inside the broken line square as follows to avoid influence of wiring capacitance:

- **Make wiring as short as possible.**
- **Do not cross other signal lines.**
- **Do not get close to lines with fluctuating large current.**
- **Make sure that the connecting points of the capacitor of the oscillator always have the same electric potential as Vss.**
- **Do not connect the oscillator to a ground pattern that conducts a large current.**
- **Do not take out signal from the oscillator.**

2. When switching to the main system clock again after the subsystem clock has been used with the main system clock stopped, be sure to set the program to provide enough time for the oscillation to stabilize.

SUBSYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T_A = −40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

Resonator	Recommended circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})Note 1		32	32.768	35	kHz
		Oscillation stabilization timeNote 2	V_{DD} = 4.5 to 6.0 V		1.2	2	s
						10	
External clock		XT1 input frequency (f_{XT})Note 1		32		50	kHz
		XT1 input high, low-level width (t_{XTH}, t_{XTL})		10		15	μs

Notes 1. It indicates only the oscillator characteristics. For the instruction execution time, see the AC Characteristics.

2. Time required until oscillation becomes stable after V_{DD} reaching MIN. of oscillation voltage range.

Cautions 1. If the subsystem clock oscillator is to be used, wire the area inside the broken line square as follows to avoid influence of wiring capacitance:

- **Make wiring as short as possible.**
- **Do not cross other signal lines.**
- **Do not get close to lines with fluctuating large current.**
- **Make sure that the connecting points of the capacitor of the oscillator always have the same electric potential as Vss.**
- **Do not connect the oscillator to a ground pattern that conducts a large current.**
- **Do not take out signal from the oscillator.**

2. The subsystem clock oscillator is more likely to have malfunctions due to noise than the main system clock oscillator because gain for the subsystem clock oscillator is made lower to reduce current consumption. When using the subsystem clock, be careful about how to connect wires.

RECOMMENDED OSCILLATOR CONSTANT

Main system clock: Ceramic resonator (T_A = −40 to +85 °C)

Manufacturer	Part number	Frequency (MHz)	Recommended circuit constant		Oscillation voltage range		Remark	
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)		
Murata Mfg.	CSA5.00MG	5.00	30	30	2.7	6.0		
	CST5.00MGW	5.00	—	—	2.7	6.0	Capacitor contained	
Matsushita Electronic Parts	EFOEN5004A (T)	5.00	33	33	2.7	6.0		★
	EFOEC5004A	5.00	—	—	2.7	6.0	Capacitor contained	★

Subsystem clock: Crystal (T_A = −40 to +85 °C)

Manufacturer	Part number	Frequency (kHz)	Recommended circuit constant			Oscillation voltage range	
			C3 (pF)	C4 (pF)	R (kΩ)	MIN. (V)	MAX. (V)
Kyocera	KF-38G-12P0200	32.768	15	22	220	2.7	6.0

CAPACITANCE (T_A = 25 °C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V				15	pF
Output capacitance	C_{OUT}	f = 1 MHz Unmeasured pins returned to 0 V				35	pF
Input/output capacitance	C_{IO}	f = 1 MHz Unmeasured pins returned to 0 V	P01-P03, P10-P17, P20-P27, P30-P37			15	pF
			P70-P74			20	pF
			P110-P117, P120-P127			35	pF

Remark Unless otherwise specified, the characteristics of the shared pin are the same as the characteristics of the port pin.

POWER SUPPLY VOLTAGE (T_A = −40 to +85 °C)

Parameter	Conditions	MIN.	TYP.	MAX.	Unit
CPU[Note 1]		2.7[Note 2]		6.0	V
Display controller		4.5		6.0	V
PWM mode of 16-bit timer/event counter (TM0)		4.5		6.0	V
A/D converter		4.0		6.0	V
Other hardware		2.7		6.0	V

Notes 1. Except for system clock oscillator, display controller, and PWM.

2. Operating power supply voltage range differs depending on the cycle time. See the AC Characteristics.

DC CHARACTERISTICS (T_A = −40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IH1}	P21, P23		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P00-P03, P20, P22, P24-P27, P33, P34, $\overline{RESET}$		0.8V_{DD}		V_{DD}	V
	V_{IH3}	P70-P74	N-ch open drain	0.7V_{DD}		15[Note 1]	V ★
	V_{IH4}	X1, X2[Note 2]		V_{DD} − 0.5		V_{DD}	V
	V_{IH5}	XT1/P04, XT2[Note 2]	V_{DD} = 4.5 to 6.0 V	V_{DD} − 0.5		V_{DD}	V
				V_{DD} − 0.3		V_{DD}	V
	V_{IH6}	P10-P17, P30-P32, P35-P37	V_{DD} = 4.5 to 6.0 V	0.65V_{DD}		V_{DD}	V
				0.7V_{DD}		V_{DD}	V
	V_{IH7}	P110-P117, P120-P127	V_{DD} = 4.5 to 6.0 V	0.7V_{DD}		V_{DD}	V
				V_{DD} − 0.5		V_{DD}	V
Low-level input voltage	V_{IL1}	P21-P23		0		0.3V_{DD}	V
	V_{IL2}	P00-P03, P20, P22, P24-P27, P33, P34, $\overline{RESET}$		0		0.2V_{DD}	V
	V_{IL3}	P70-P74	V_{DD} = 4.5 to 6.0 V	0		0.3V_{DD}	V
				0		0.2V_{DD}	V
	V_{IL4}	X1, X2[Note 2]		0		0.4	V
	V_{IL5}	XT1/P04, XT2[Note 2]	V_{DD} = 4.5 to 6.0 V	0		0.4	V
				0		0.3	V
	V_{IL6}	P10-P17, P30-P32, P35-P37		0		0.3V_{DD}	V
	V_{IL7}	P110-P117, P120-P127		V_{DD} − 35		0.3V_{DD}	V
High-level output voltage	V_{OH}	P01-P03, P10-P17, P20-P27, P30-P37, P80, P81, P90-P97, P100-P107, P110-P117, P120-P127	V_{DD} = 4.5 to 6.0 V, I_{OH} = −1 mA	V_{DD} − 1.0			V
			I_{OH} = −100 μA	V_{DD} − 0.5			V
Low-level output voltage	V_{OL1}	P30-P37, P70-P74	V_{DD} = 4.5 to 6.0 V, I_{OL} = 15 mA		0.4	2.0	V
		P01-P03, P10-P17, P20-P27	V_{DD} = 4.5 to 6.0 V, I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	SB0, SB1, $\overline{SCK0}$	V_{DD} = 4.5 to 6.0 V, With open-drain and pull-up (R = 1 kΩ)			0.2V_{DD}	V
	V_{OL3}	P01-P03, P10-P17, P20-P27, P30-P37, P70-P74	I_{OL} = 400 μA			0.5	V

Notes 1. Pins to which pull-up resistors are connected by the mask option become V_{DD}.

2. If the X1 pin is used for high-level voltage input, the X2 pin is used for low-level voltage input, or vice versa. This is also true for the XT1/P04 pin and XT2 pin.

Remark Unless otherwise specified, the characteristics of a shared pin are the same as those of a port pin.

DC CHARACTERISTICS (T_A = −40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-level input leakage current	I_{LIH1}	$V_{IN} = V_{DD}$	P00-P03, P10-P17, P20-P27, P30-P37, $\overline{RESET}$			3	μA
	I_{LIH2}		X1, X2, XT1/P04, XT2			20	μA
	I_{LIH3}	V_{IN} = 15 V	P70-P74			80	μA
	I_{LIH4}	P110-P117, P120-P127, $V_{IN} = V_{DD}$	V_{DD} = 4.5 to 6.0 V			3 Note 1	μA
						3 Note 2	μA
Low-level input leakage current	I_{LIL1}	V_{IN} = 0 V	P00-P03, P10-P17, P20-P27, P30-P37, $\overline{RESET}$			−3	μA
	I_{LIL2}		X1, X2, XT1/P04, XT2			−20	μA
	I_{LIL3}		P70-P74			−3 Note 3	μA
	I_{LIL4}		P110-P117, P120-P127			−10	μA
High-level output leakage current Note 4	I_{LOH1}	$V_{OUT} = V_{DD}$	P01-P03, P10-P17, P20-P27, P30-P37, P80, P81, P90-P97, P100-P107, P110-P117, P120-P127			3	μA
★	I_{LOH2}	V_{OUT} = 15 V	P70-74, N-ch open drain			80	μA
Low-level output leakage current Note 4	I_{LOL1}	V_{OUT} = 0 V	P01-P03, P10-P17, P20-P27, P30-P37, P70-P74			−3	μA
★	I_{LOL2}	$V_{OUT} = V_{LOAD} = V_{DD}$ − 35 V	P80, P81, P90-P97, P100-107, P110-P117, P120-P127			−10	μA
Display output current	I_{OD}	V_{DD} = 4.5 to 6.0 V, $V_{OD} = V_{DD}$ − 2 V		−13	−18		mA
Mask option pull-up resistor	R_1	V_{IN} = 0 V, P70-P74		20	40	90	kΩ
Software pull-up resistor	R_2	V_{IN} = 0 V P01-P03, P10-P17, P20-P27, P30-P37	V_{DD} = 4.5 to 6.0 V	15	40	90	kΩ
				20		500	kΩ
Mask option pull-down resistor	R_3	P80, P81, P90-P97, P100-P107, P110-P117, P120-P127	$V_{OD} - V_{LOAD}$ = 35 V	25	70	135	kΩ
			$V_{OD} - V_{SS}$ = 5 V	20	55	100	kΩ
	R_4	P30-P37, $V_{IN} = V_{DD}$		40	80	150	kΩ

Notes 1. The maximum value is 50 μA for only 1.5 clocks (PCC = 00H) during the read instruction execution of ports 11 and 12 (P11, P12). Otherwise, it is 3 μA.

2. The maximum value is 30 μA for only 1.5 clocks (PCC = 00H) during the read instruction execution of ports 11 and 12 (P11, P12). Otherwise, it is 3 μA.

3. The maximum value is -150 μA for only 1.5 clocks (PCC = 00H) during the read instruction execution of port 7 (P7). Otherwise, it is -3 μA.

4. Current which flows in the built-in pull-up or pull-down resistor is not included.

Remark Unless otherwise specified, the characteristics of a shared pin are the same as those of a port pin.

DC CHARACTERISTICS (T_A = −40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Power supply current[Note 1]	I_{DD1}	5.0 MHz crystal oscillation Operating mode	V_{DD} = 5.0 V ±10%[Note 2]		7.2	21.6	mA
			V_{DD} = 3.0 V ±10%[Note 3]		0.9	2.7	mA
	I_{DD2}	5.0 MHz crystal oscillation HALT mode	V_{DD} = 5.0 V ±10%		1.3	3.9	mA
			V_{DD} = 3.0 V ±10%		550	1650	μA
	I_{DD3}	32.768 kHz crystal oscillation Operating mode[Note 4]	V_{DD} = 5.0 V ±10%		60	120	μA
			V_{DD} = 3.0 V ±10%		35	70	μA
	I_{DD4}	32.768 kHz crystal oscillation HALT mode[Note 4]	V_{DD} = 5.0 V ±10%		25	50	μA
			V_{DD} = 3.0 V ±10%		5	10	μA
	I_{DD5}	XT1 = 0 V STOP mode Feedback resistor connected	V_{DD} = 5.0 V ±10%		1	20	μA
			V_{DD} = 3.0 V ±10%		0.5	10	μA
	I_{DD6}	XT1 = 0 V STOP mode Feedback resistor not connected	V_{DD} = 5.0 V ±10%		0.1	20	μA
			V_{DD} = 3.0 V ±10%		0.05	10	μA

Notes 1. This current excludes the AV_{REF} current, port current, and current which flows in the built-in pull-down resistor (mask option).

2. When operating at high-speed mode (when the processor clock control register is set to 00H)
3. When operating at low-speed mode (when the processor clock control register is set to 04H)
4. When the main system clock is stopped

AC CHARACTERISTICS

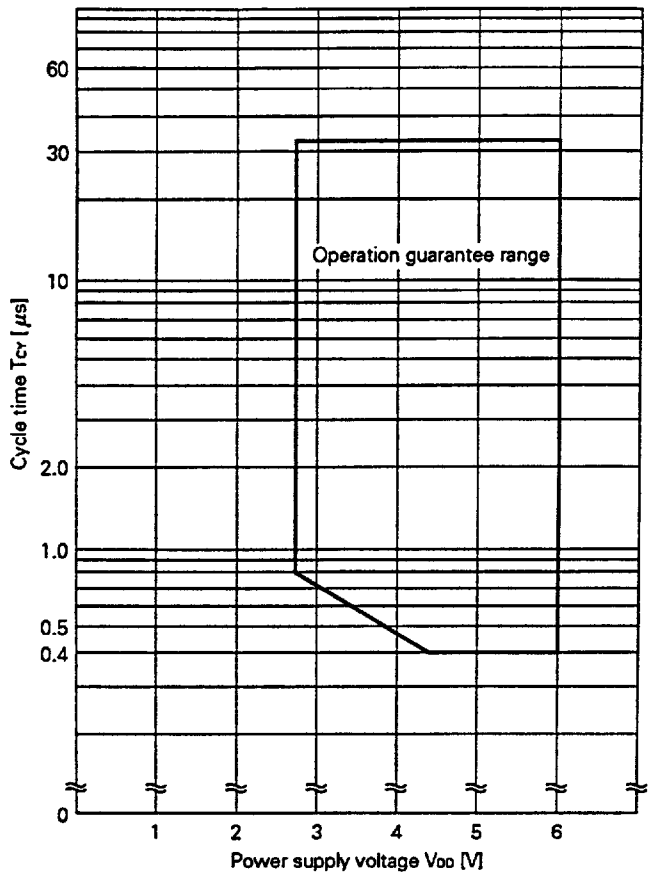
(1) Basic operation (T_A = −40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	Operated with main system clock	V_{DD} = 4.5 to 6.0 V	0.4		32	μs
				0.8		32	μs
		Operated with subsystem clock		80[Note 1]	122	125	μs
TI1, 2 input frequency	f_{TI}	V_{DD} = 4.5 to 6.0 V		0		2	MHz
				0		138	kHz
TI1, 2 input high, low-level width	t_{TIH} t_{TIL}	V_{DD} = 4.5 to 6.0 V		250			ns
				3.6			μs
Interrupt input high, low-level width	t_{INTH} t_{INTL}	INTP0		$8/f_{sam}$[Note 2]			μs
		INTP1-INTP3		10			μs
$\overline{RESET}$ low-level width	t_{RSL}			10			μs

Notes 1. Value when external clock input is used as subsystem clock. When crystal is used, the value becomes 114 μs.

2. Selection of $f_{sam} = fx/2^{N+1}$, fx/64, fx/128 is available (N = 0 to 4) by bits 0 and 1 of sampling clock select register (SCS0, SCS1).

T_{CY} vs V_{DD} (with main system clock operated)



(2) Serial interface (T_A = −40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

(a) Three-wire serial I/O mode ($\overline{SCK}$: Internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY1}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ high, low-level width	t_{KH1}	V_{DD} = 4.5 to 6.0 V		$t_{KCY1}/2$ - 50			ns
	t_{KL1}			$t_{KCY1}/2$ - 150			ns
SI setup time to $\overline{SCK}$↑	t_{SIK1}			100			ns
SI hold time from $\overline{SCK}$↑	t_{KSI1}			400			ns
$\overline{SCK}$↓→ SO output delay time	t_{KSO1}	C = 100 pF[Note]	V_{DD} = 4.5 to 6.0 V			300	ns
						1000	ns

Note C is a load capacitance of the $\overline{SCK}$ or SO output line.

(b) Three-wire serial I/O mode ($\overline{SCK}$: External clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY2}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ high, low-level width	t_{KH2}, t_{KL2}	V_{DD} = 4.5 to 6.0 V		400			ns
				1600			ns
SI setup time to $\overline{SCK}$↑	t_{SIK2}	V_{DD} = 4.5 to 6.0 V		100			ns
SI hold time from $\overline{SCK}$↑	t_{KSI2}			400			ns
$\overline{SCK}$↓→ SO output delay time	t_{KSO2}	C = 100 pF[Note]	V_{DD} = 4.5 to 6.0 V			300	ns
						1000	ns
$\overline{SCK}$ rise time and fall time	t_{R2}, t_{F2}					160	ns ★

Note C is a load capacitance of the SO output line.

(c) SBI mode ($\overline{SCK}$: Internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY3}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ high, low-level width	t_{KH3}, t_{KL3}	V_{DD} = 4.5 to 6.0 V		$t_{KCY3}/2-50$			ns
				$t_{KCY3}/2-150$			ns
SB0, SB1 setup time to $\overline{SCK}$↑	t_{SIK3}	V_{DD} = 4.5 to 6.0 V		100			ns
				300			ns
SB0, SB1 hold time from $\overline{SCK}$↑	t_{KSI3}			$t_{KCY3}/2$			ns
$\overline{SCK}$↓→SB0, SB1 output delay time	t_{KSO3}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 4.5 to 6.0 V	0		250	ns
				0		1000	ns
$\overline{SCK}$↑→SB0, SB1↓	t_{KSB}			t_{KCY3}			ns
SB0, SB1↓ →$\overline{SCK}$↓	t_{SBK}			t_{KCY3}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY3}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY3}			ns

Note R is a load resistance of the $\overline{SCK}$, SB0, or SB1 output line, and C is its load capacitance.

(d) SBI mode ($\overline{SCK}$: External clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY4}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ high, low- level width	t_{KH4}	V_{DD} = 4.5 to 6.0 V		400			ns
	t_{KL4}			1600			ns
SB0, SB1 setup time to $\overline{SCK}$↑	t_{SIK4}	V_{DD} = 4.5 to 6.0 V		100			ns
				300			ns
SB0, SB1 hold time from $\overline{SCK}$↑	t_{KSI4}			$t_{KCY4}/2$			ns
$\overline{SCK}$↓→SB0, SB1 output delay time	t_{KSO4}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		1000	ns
$\overline{SCK}$↑→SB0, SB1↓	t_{KSB}			t_{KCY4}			ns
SB0, SB1↓→$\overline{SCK}$↓	t_{SBK}			t_{KCY4}			ns
SB0, SB1 high- level witdh	t_{SBH}			t_{KCY4}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY4}			ns
★ $\overline{SCK}$ rise time and fall time	t_{R4} t_{F4}					160	ns

Note R is a load resistance of the SB0 or SB1 output line, and C is its load capacitance.

(e) Two-wire serial I/O mode ($\overline{SCK}$: Internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY5}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 4.5 to 6.0 V	1600			ns
				3800			ns
$\overline{SCK}$ high-level width	t_{KH5}			$t_{KCY5}/2-160$			ns
$\overline{SCK}$ low- level width	t_{KL5}			$t_{KCY5}/2 - 50$			ns
SB0, SB1 setup time to $\overline{SCK}$↑	t_{SIK5}			300			ns
SB0, SB1 hold time from $\overline{SCK}$↑	t_{KSI5}			600			ns
$\overline{SCK}$↓→ SB0, SB1 output delay time	t_{KSO5}		V_{DD} = 4.5 to 6.0 V	0		250	ns
				0		1000	ns

Note R is a load resistance of the $\overline{SCK}$, SB0, or SB1 output line, and C is its load capacitance.

(f) Two-wire serial I/O mode ($\overline{SCK}$: External clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY6}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK}$ high-level width	t_{KH6}			650			ns
$\overline{SCK}$ low- level width	t_{KL6}			800			ns
SB0, SB1 setup time to $\overline{SCK}$↑	t_{SIK6}			100			ns
SB0, SB1 hold time from $\overline{SCK}$↑	t_{KSI6}			$t_{KCY6}/2$			ns
$\overline{SCK}$↓→ SB0, SB1 output delay time	t_{KSO6}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		1000	ns
★ $\overline{SCK}$ rise time and fall time	t_{R6} t_{F6}					160	ns

Note R is a load resistance of the SB0 or SB1 output line, and C is its load capacitance.

(g) 3-wire serial I/O mode with automatic transmission/reception function ($\overline{SCK}$: internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY7}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ high, low-level width	t_{KH7}	V_{DD} = 4.5 to 6.0 V		$t_{KCY7}/2-50$			ns
	t_{KL7}			$t_{KCY7}/2-150$			ns
SI setup time to $\overline{SCK}\uparrow$	t_{SIK7}			100			ns
SI hold time from $\overline{SCK}\uparrow$	t_{KSI7}			400			ns
$\overline{SCK}\downarrow\rightarrow$ SO output delay time	t_{KSO7}	C = 100 pF[Note]	V_{DD} = 4.5 to 6.0 V			300	ns
						1000	ns
$\overline{SCK}\uparrow\rightarrow$STB$\uparrow$	t_{SBD}			$t_{KCY7}/2-100$		$t_{KCY7}/2+100$	ns
Strobe signal high level width	t_{SBW}			$t_{KCY7}-30$		$t_{KCY7}+30$	ns
Busy signal setup time (to busy signal detection timing)	t_{BYS}			100			ns
Busy signal hold time (to busy signal detection timing)	t_{BYH}			100			ns
Busy inactive $\rightarrow \overline{SCK}\downarrow$	t_{SPS}					$2t_{KCY7}$	ns

Note C is a load capacitance of the $\overline{SCK}$ or SO output line.

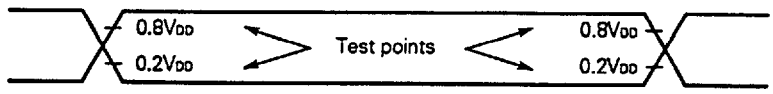
(h) 3-wire serial I/O mode with automatic transmission/reception function ($\overline{SCK}$: external clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY8}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ high, low-level width	t_{KH8}	V_{DD} = 4.5 to 6.0 V		400			ns
	t_{KL8}			1600			ns
SI setup time to $\overline{SCK}\uparrow$	t_{SIK8}			100			ns
SI hold time from $\overline{SCK}\uparrow$	t_{KSI8}			400			ns
$\overline{SCK}\downarrow\rightarrow$ SO output delay time	t_{KSO8}	C = 100 pF[Note]	V_{DD} = 4.5 to 6.0 V			300	ns
						1000	ns
$\overline{SCK}$ rise time and fall time	t_{R8}					160	ns
	t_{F8}						

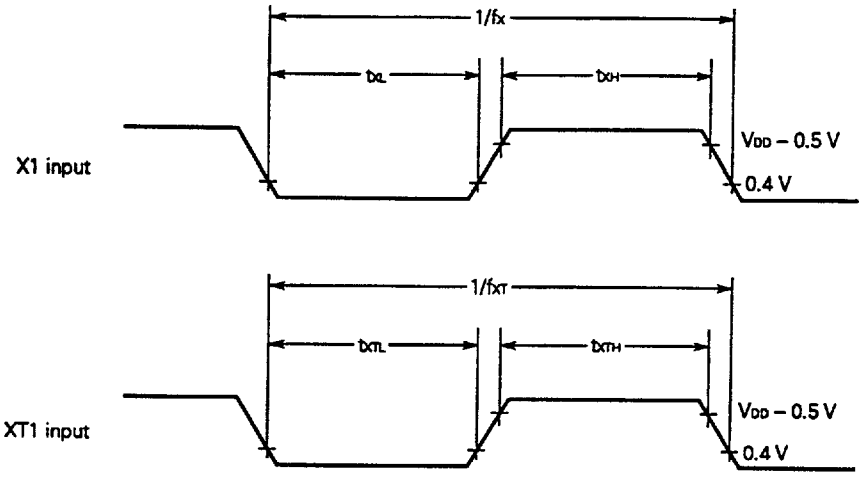
★

Note C is a load capacitance of the SO output line.

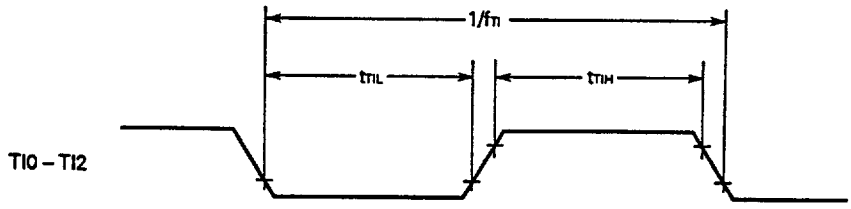
AC timing test points (except X1, XT1 input)



Clock timing

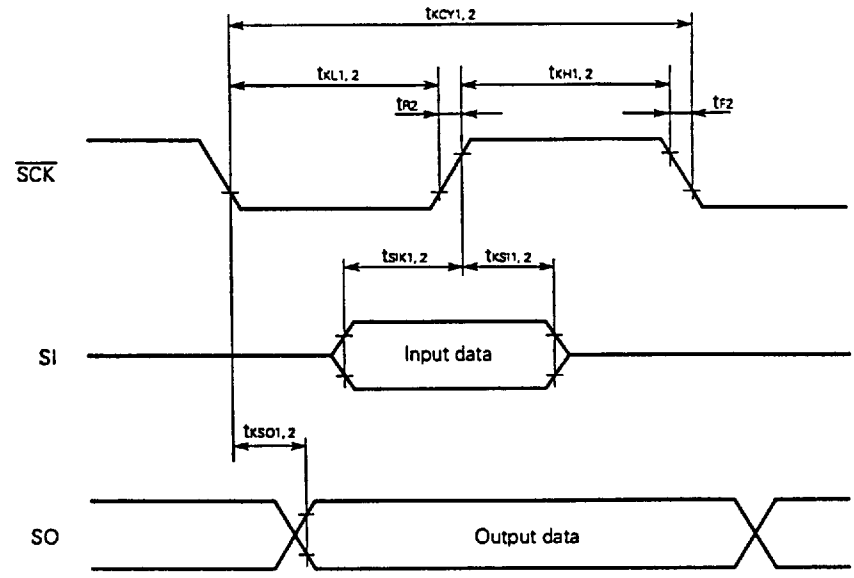


TI timing



Serial transfer timing

3-wire serial I/O mode:



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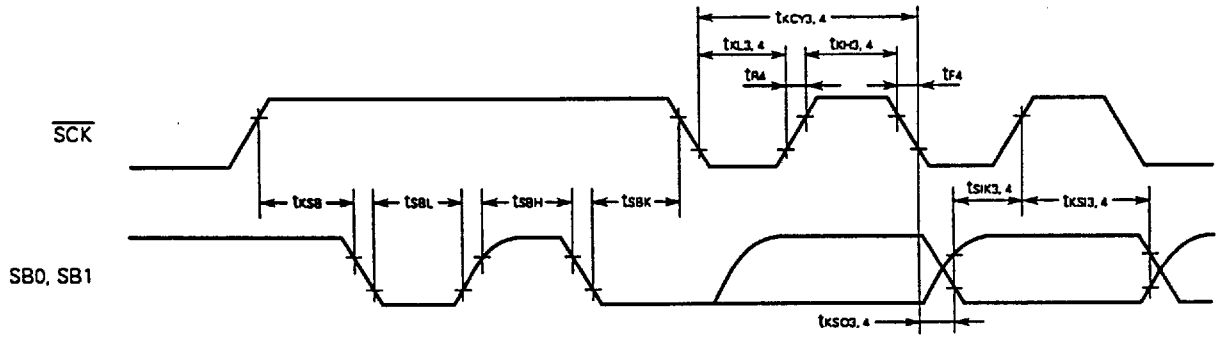
SBI mode (bus release signal transfer):



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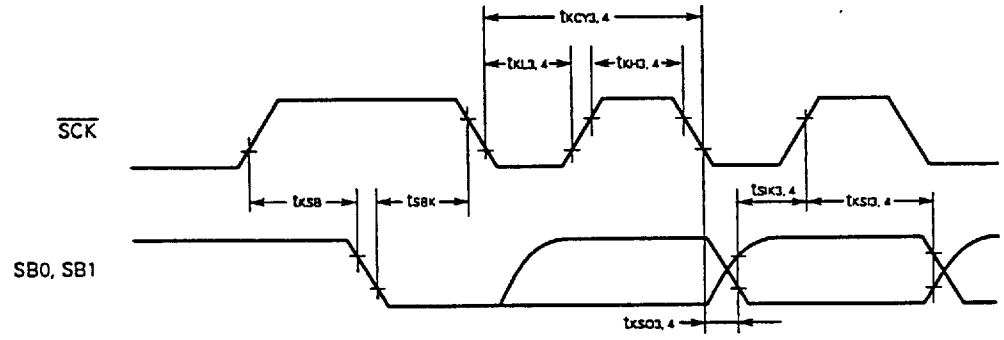
SBI mode (command signal transfer):



2-wire serial I/O mode:

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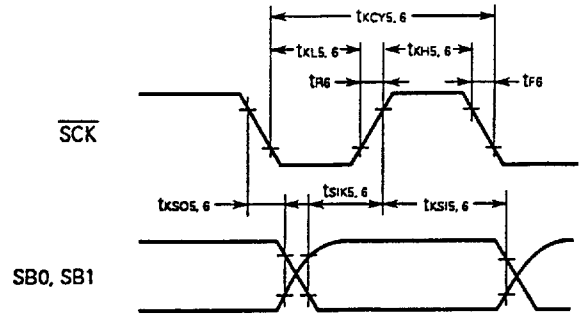

3-wire serial I/O mode with automatic transmission/reception function:

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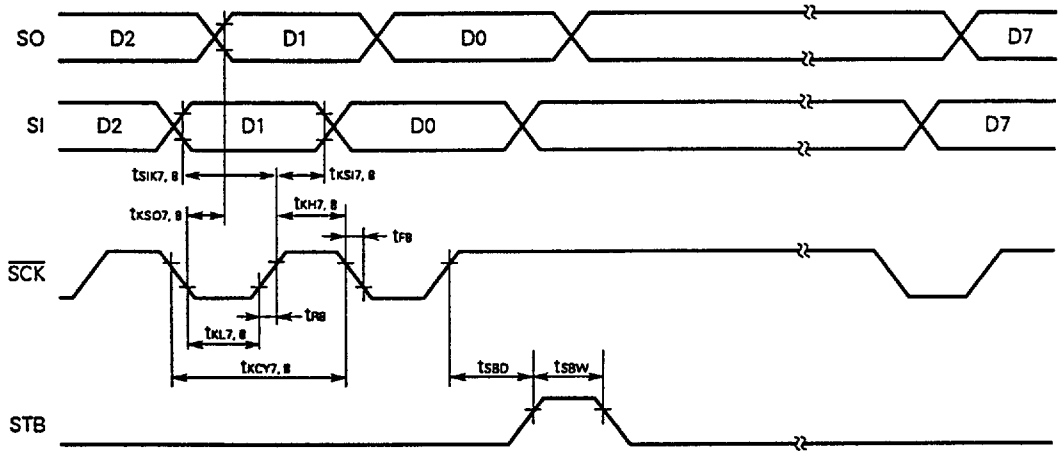
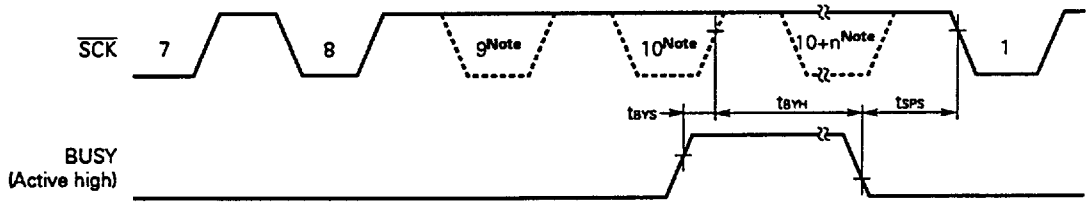


3-wire serial I/O mode with automatic transmission/reception function (busy processing):



Note SCK does not become low actually at this point, but is indicated so to conform to the timing specification.

A/D Converter Characteristics (T_A = −40 to +85 °C, AV_{DD} = V_{DD} = 4.0 to 6.0 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Total error[Note 1]					0.8	%
Conversion time[Note 2]	t_{CONV}	1 MHz ≦ fx ≦ 5.0 MHz	19.1		200	μs
Sampling time[Note 3]	t_{SAMP}		2.86		30	μs
Analog signal input voltage	V_{IAN}		AV_{SS}		AV_{REF}	V
Reference voltage	AV_{REF}		4.0		AV_{DD}	V
AV_{REF} resistor	R_{AVREF}		4	14		kΩ
AV_{DD} current	AI_{DD}			200	400	μA

Notes 1. Quantization error (±1/2LSB) is not included. This parameter is indicated as the ratio to the full-scale value.

2. Set the A/D conversion time to 19.1 μs or more.

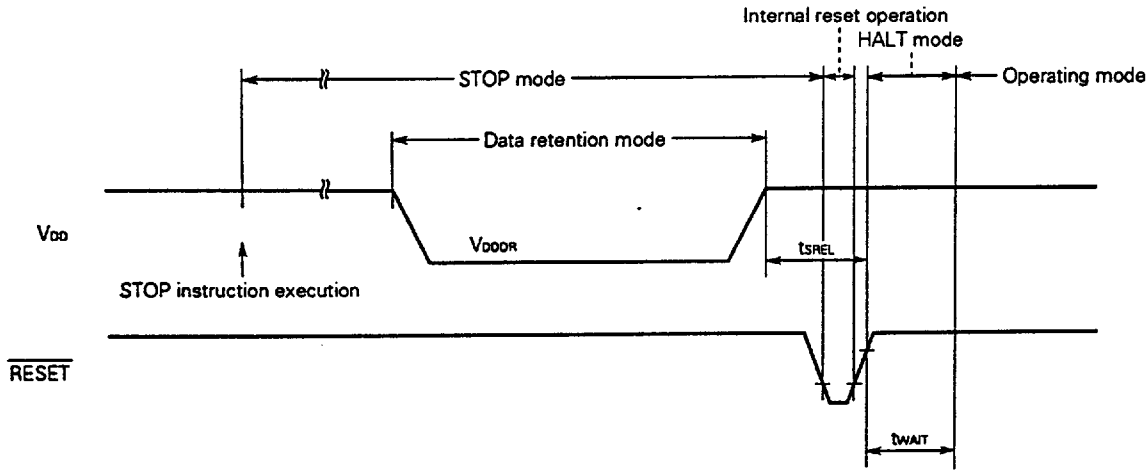
3. Sampling time depends on the conversion time.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = −40 to +85 °C)

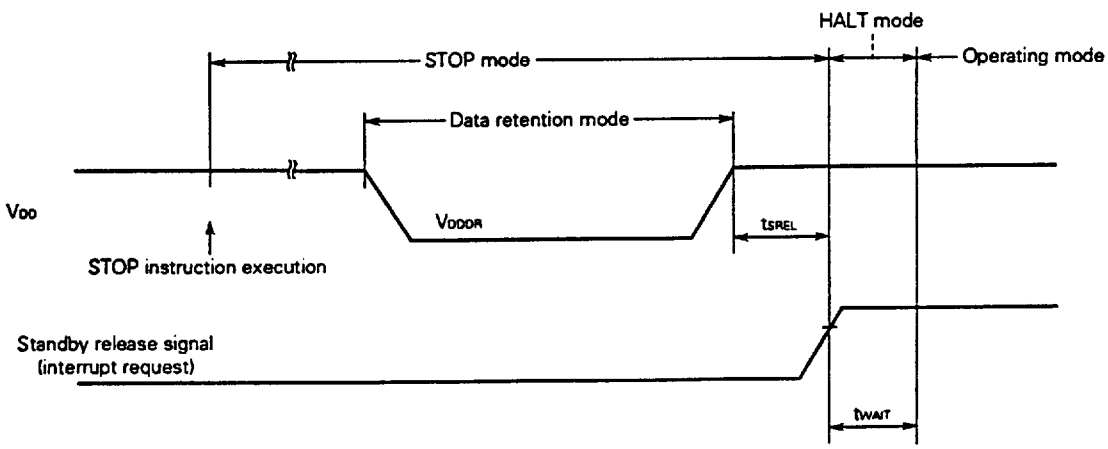
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		2.0		6.0	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 2.0 V Subsystem clock stopped, Feedback resistor not connected		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{RESET}$		$2^{17}/fx$		ms
		Release by interrupt		Note		ms

Note Selection of $2^{12}/fx$, $2^{14}/fx$ to $2^{17}/fx$ is available by bits 0 to 2 of oscillation stabilization time select register (OSTS0 to OSTS2).

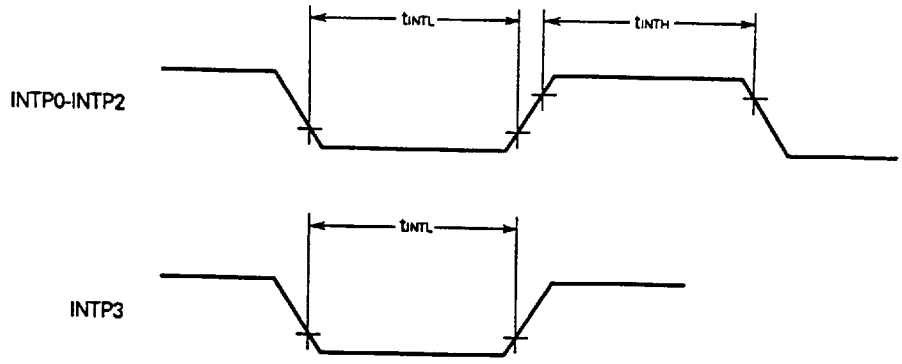
Data retention timing (STOP mode release by $\overline{RESET}$)



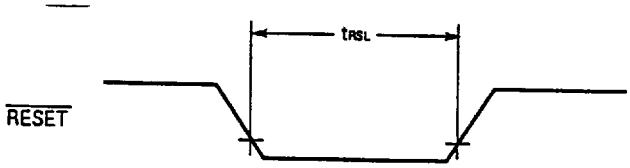
Data retention timing (standby release signal: STOP mode release by interrupt signal)



Interrupt input timing



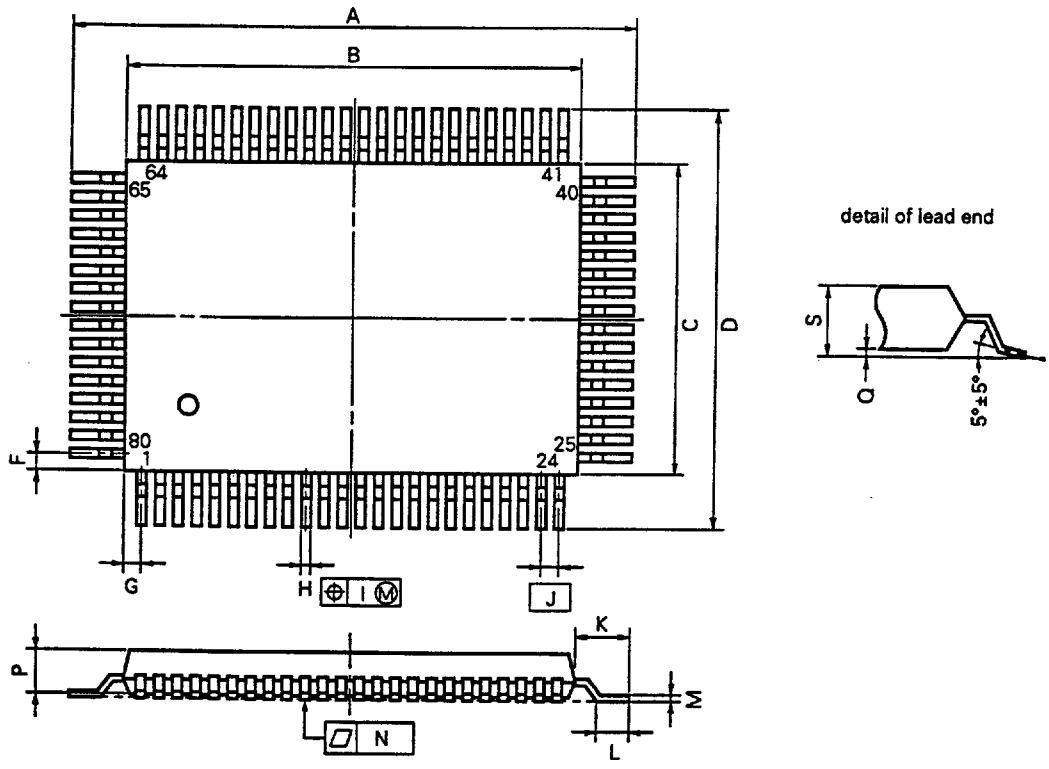
$\overline{\text{RESET}}$ input timing



11. PACKAGE DRAWINGS

PACKAGE DRAWING OF MASS-PRODUCED PRODUCT

80 PIN PLASTIC QFP (14x20)



P80GF-80-3B9-2

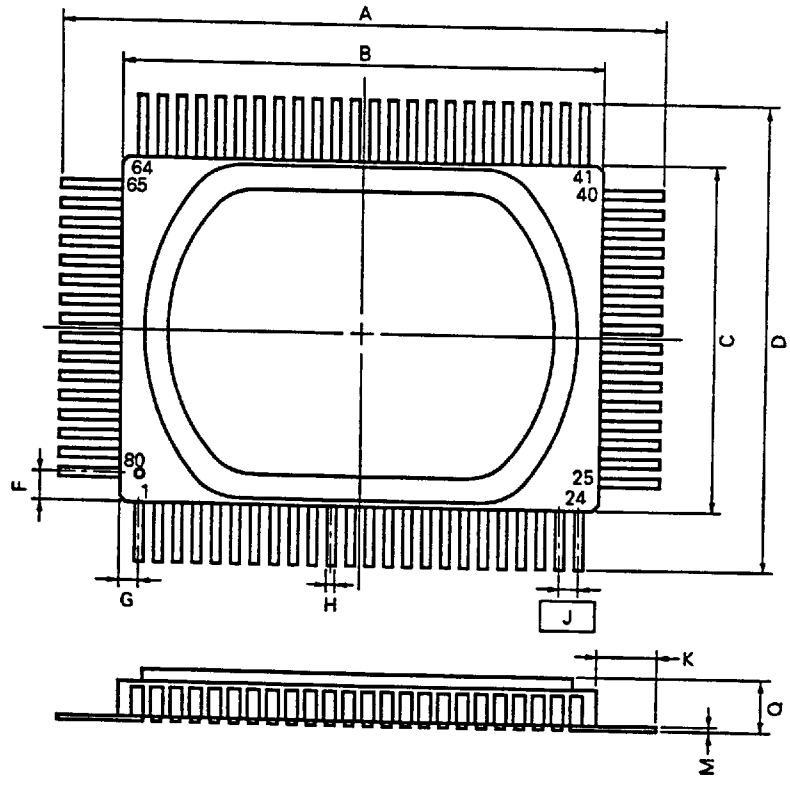
NOTE
Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

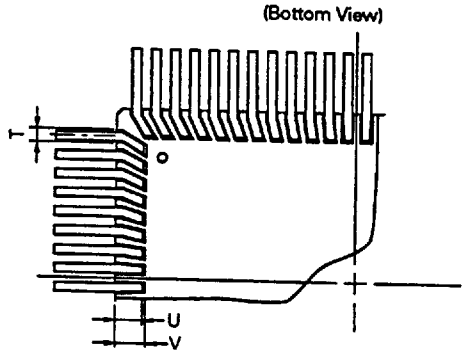
ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	0.8	0.031
H	0.35±0.10	$0.014^{+0.004}_{-0.006}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

Caution The ES product is different from the corresponding mass-produced product in shape and material. See "PACKAGE DRAWING OF ES PRODUCT."

PACKAGE DRAWING OF ES PRODUCT

80 PIN CERAMIC QFP (14 × 20) (FOR ES)





X80B-80A-1

ITEM	MILLIMETERS	INCHES
A	24.7±0.4	$0.972^{+0.017}_{-0.016}$
B	20.0	0.787
C	14.2	0.559
D	18.9±0.4	0.744±0.016
F	1.1	0.043
G	0.8	0.031
H	0.32	0.013
J	0.8 (T.P.)	0.031 (T.P.)
K	2.35±0.15	$0.093^{+0.006}_{-0.007}$
M	0.15	0.006
Q	2.7 MAX.	0.107 MAX.
T	0.55	0.022
U	1.0	0.039
V	1.2	0.047

12. RECOMMENDED SOLDERING CONDITIONS

The conditions listed below shall be met when soldering the μPD78042A, μPD78043A, μPD78044A, μPD78045A.

For details of the recommended soldering conditions, refer to our document *SMD Surface Mount Technology Manual* (IEI-1207).

Please consult with our sales offices in case any other soldering process is used, or in case soldering is done under different conditions.

Table 12-1 Soldering Conditions for Surface-Mount Devices

μPD78042AGF-xxx-3B9: 80-pin plastic QFP (14 × 20 mm)
μPD78043AGF-xxx-3B9: 80-pin plastic QFP (14 × 20 mm)
μPD78044AGF-xxx-3B9: 80-pin plastic QFP (14 × 20 mm)
μPD78045AGF-xxx-3B9: 80-pin plastic QFP (14 × 20 mm)

Soldering process	Soldering conditions	Recommended conditions
Infrared ray reflow	Peak package's surface temperature: 235 °C Reflow time: 30 seconds or less (210 °C or more) Maximum allowable number of reflow processes: 2 <Cautions> (1) Do not start reflow-soldering the device if its temperature is higher than the room temperature because of a previous reflow soldering. (2) Do not use water for flux cleaning before a second reflow soldering.	IR35-00-2
VPS	Peak package's surface temperature: 215 °C Reflow time: 40 seconds or less (200 °C or more) Maximum allowable number of reflow processes: 2 <Cautions> (1) Do not start reflow-soldering the device if its temperature is higher than the room temperature because of a previous reflow soldering. (2) Do not use water for flux cleaning before a second reflow soldering.	VP15-00-2
Wave soldering	Solder temperature: 260 °C or less Flow time: 10 seconds or less Number of flow process: 1 Preheating temperature: 120 °C max. (measured on the package surface)	WS60-00-1
Partial heating method	Terminal temperature: 300 °C or less Heat time: 3 seconds or less (for one side of a device)	–

Caution Do not apply two or more different soldering methods to one chip (except for partial heating method for terminal sections).

APPENDIX A DEVELOPMENT TOOLS

The following tools are available for development of systems using the μPD78042A, μPD78043A, μPD78044A, and μPD78045A:

Software for Language Processing

RA78K/0 Notes 1, 2, 3	Assembler package common to 78K/0 series
CC78K/0 Notes 1, 2, 3	C compiler package common to 78K/0 series
DF78044 Notes 1, 2, 3	Device file common to μPD78044 sub-series ★
CC78K/0-L Notes 1, 2, 3	C compiler library source file common to 78K/0 series

PROM Writing Tools

PG-1500	PROM programmer
PA-78P048GF PA-78P048KL-S	Programmer adapter connected to PG-1500
PG-1500 Controller Notes 1, 2	Control program for PG-1500

Debugging Tools

IE-78000-R	In-circuit emulator common to 78K/0 series
IE-78000-R-BK	Break board common to 78K/0 series
IE-78044-R-EM	Emulation board common to μPD78044 sub-series
EP-78130GF-R	Emulation probe common to μPD78134 sub-series
EV-9200G-80	Socket mounted to user system created for 80-pin plastic QFP
SM78K0 Notes 4, 5	System simulator common to 78K/0 series ★
SD78K/0 Notes 1, 2	Screen debugger for IE-78000-R
DF78044 Notes 1, 2, 4, 5	Device file common to μPD78044 sub-series

Real-Time OS

RX78K/0 Notes 1, 2, 3	Real-time OS for 78K/0 series
MX78K0 Notes 1, 2, 3	OS for 78K/0 series ★

Notes 1. PC-9800 series (MS-DOS™) base
2. IBM PC/AT™ (PC DOS™) base
3. HP9000 series 300™ and HP9000 series 700™ (HP-UX™) base, SPARCstation™ (Sun OS™) base, EWS-4800 series (EWS-UX/V) base ★
4. PC-9800 series (MS-DOS + Windows™) base
5. IBM PC/AT (PC DOS + Windows) base

Fuzzy Inference Development Support Systems

FE9000[Note 1], FE9200[Note 3]	Fuzzy knowledge data creation tool
FT9080[Note 1], FT9085[Note 2]	Translator
FI78K0[Notes 1, 2]	Fuzzy inference module
FD78K0[Notes 1, 2]	Fuzzy inference debugger

Notes 1. PC-9800 series (MS-DOS) base
2. IBM PC/AT (PC DOS) base
3. IBM PC/AT (PC DOS + Windows) base

Remarks 1. Refer to the *78K/0 Series Selection Guide* (IF-1185) for development tools manufactured by third parties.

★ **2.** The RA78K/0, CC78K/0, SM78K0, and SD78K/0 are used with the DF78044.

APPENDIX B RELATED DOCUMENTS ★

Documents Related to Devices

Document name	Document No.	
	Japanese	English
μPD78044A Sub-Series User's Manual	IEU-860	IEU-1394
μPD78042A, 78043A, 78044A, 78045A Data Sheet	This data sheet	IC-3317
μPD78P048A Product Information	IP-8892	IP-3408
μPD78044A Sub-Series Special Function Registers	IEM-5588	—
78K/0 Series User's Manual, Instruction	IEU-849	IEU-1372
78K/0 Series Instruction Summary Sheet	IEM-5522	—
78K/0 Series Instruction Set	IEM-5521	—

Documents Related to Development Tools (User's Manual)

Document name		Document No.	
		Japanese	English
RA78K Series Assembler Package	Operation	EEU-809	EEU-1399
	Language	EEU-815	EEU-1404
RA78K Series Structured Assembler Preprocessor		EEU-817	EEU-1402
CC78K Series C Compiler	Operation	EEU-656	EEU-1280
	Language	EEU-655	EEU-1284
CC78K Series Library Source File		EEU-777	—
PG-1500 PROM Programmer		EEU-651	EEU-1335
PG-1500 Controller	PC-9800 series (MS-DOS) base	EEU-704	To be created
	IBM PC series (PC DOS) base	EEU-5008	EEU-1291
IE-78000-R		EEU-810	EEU-1398
IE-78000-R-BK		EEU-867	EEU-1427
IE-78044-R-EM		EEU-833	EEU-1424
EP-78130GF-R		EEU-943	—
SM78K0 System Simulator	Reference	EEU-5002	To be released soon
SD78K/0 Screen Debugger PC-9800 series (MS-DOS) base	Tutorial	EEU-852	—
	Reference	EEU-816	—
SD78K/0 Screen Debugger IBM PC/AT (PC DOS) base	Tutorial	To be created	EEU-1414
	Reference	EEU-993	EEU-1413

Caution The above documents may be revised without notice. Use the latest versions when you design an application system.

Documents Related to Software to be Incorporated into the Product (User's Manual)

Document name		Document No.	
		Japanese	English
78K/0 Series Real-Time OS	Basic	EEU-912	—
	Installation	EEU-911	—
	Technical	EEU-913	—
OS for 78K/0 Series MX78K0	Basic	EEU-5010	—
Tool for Creating Fuzzy Knowledge Data		EEU-829	EEU-1438
78K/0, 78K/II, and 87AD Series Fuzzy Inference Development Support System, Translator		EEU-829	EEU-1444
78K/0 Series Fuzzy Inference Development Support System, Fuzzy Inference Module		EEU-858	EEU-1441
78K/0 Series Fuzzy Inference Development Support System, Fuzzy Inference Debugger		EEU-921	EEU-1458

Other Documents

Document name	Document No.	
	Japanese	English
Package Manual	IEI-635	IEI-1213
SMD Surface Mount Technology Manual	IEI-616	IEI-1207
Quality Grades on NEC Semiconductor Device	IEI-620	IEI-1209
NEC Semiconductor Device Reliability/Quality Control System	IEM-5068	—
Electrostatic Discharge (ESD) Test	MEM-539	—
Guide to Quality Assurance for Semiconductor Device	MEI-603	MEI-1202
Guide for Products Related to Micro-Computer: Other Companies	MEI-604	—

Caution The above documents may be revised without notice. Use the latest versions when you design an application system.