NEC

MOS FIELD EFFECT TRANSISTOR
2SK3204

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

The 2SK3204 is N-Channel MOS Field Effect Transistor designed for high current switching applications.

★ ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3204	MP-10

★ FEATURES

- Low on-state resistance :
  $R_{DS(on)1}$ = 34 mΩ (MAX.) (V_{GS} = 10 V, I_D = 8 A)
  $R_{DS(on)2}$ = 50 mΩ (MAX.) (V_{GS} = 4 V, I_D = 8 A)
- Low C_{iss} : C_{iss} = 940 pF (TYP.)
- Built-in gate protection diode.

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Drain to Source Voltage	V_{DSS}	60	V
Gate to Source Voltage	$V_{GSS(AC)}$	±20	V
Gate to Source Voltage	$V_{GSS(DC)}$	+20, –10	V
Drain Current (DC)	$I_{D(DC)}$	±15	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	±45	A
Total Power Dissipation (T_A = 25 °C)	P_T	1.8	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C
★ Single Avalanche Current Note2	I_{AS}	15	A
★ Single Avalanche Energy Note2	E_{AS}	22.5	mJ

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1 %

2. Starting T_{ch} = 25 °C, R_G = 25 Ω, V_{GS} = 20 V→0 V

THERMAL RESISTANCE

Channel to Ambient	$R_{th(ch-A)}$	69.4	°C/W

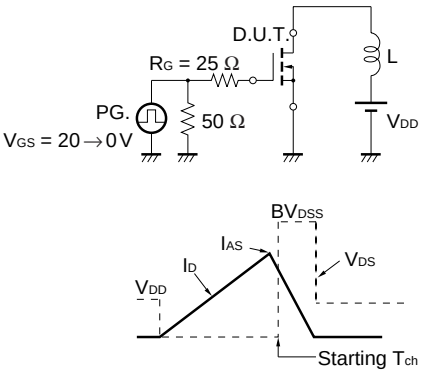
Document No. D13796EJ1V0DS00 (1st edition)
Date Published April 1999 NS CP (K)
Printed in Japan

The mark ★ shows major revised points.

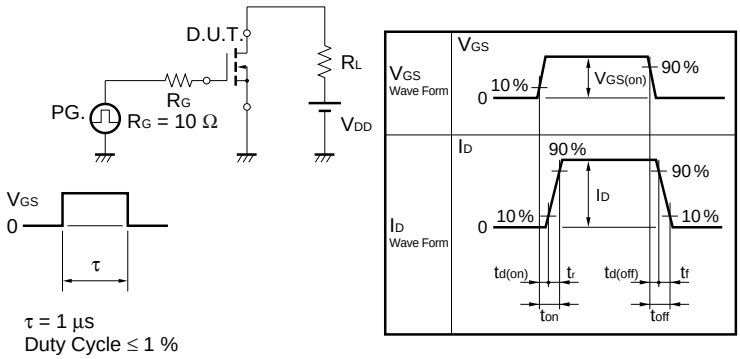
★ ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

PARAMATERS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 8 A		25	34	mΩ
	$R_{DS(on)2}$	V_{GS} = 4 V, I_D = 8 A		35	50	mΩ
Gate to Source Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	1.0	1.5	2.0	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 8 A	8.0	14		S
Drain Leakage Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V			10	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±10	μA
Input Capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz		940		pF
Output Capacitance	C_{oss}			290		pF
Reverse Transfer Capacitance	C_{rss}			120		pF
Turn-on Delay Time	$t_{d(on)}$	I_D = 8 A, $V_{GS(on)}$ = 10 V, V_{DD} = 30 V,		17		ns
Rise Time	t_r	R_G = 10 Ω		150		ns
Turn-off Delay Time	$t_{d(off)}$			58		ns
Fall Time	t_f			52		ns
Total Gate Charge	Q_G	I_D = 15 A, V_{DD} = 48 V, $V_{GS(on)}$ = 10 V		25		nC
Gate to Source Charge	Q_{GS}			2.9		nC
Gate to Drain Charge	Q_{GD}			7.5		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 15 A, V_{GS} = 0 V		0.92		V
Reverse Recovery Time	t_{rr}	I_F = 15 A, V_{GS} = 0 V,		45		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		81		nC

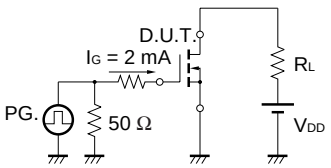
★ TEST CIRCUIT 1 AVALANCHE CAPABILITY



★ TEST CIRCUIT 2 SWITCHING TIME

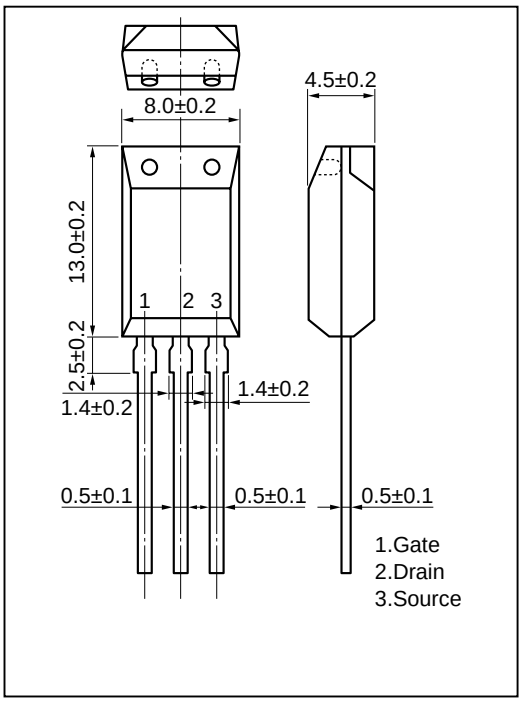


★ TEST CIRCUIT 3 GATE CHARGE

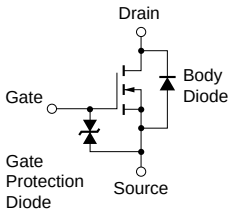


PACKAGE DRAWING (Unit : mm)

MP-10



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD.

When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

- **The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.**
- No part of this document may be copied or reproduced in any form or by any means without the prior written consent of NEC Corporation. NEC Corporation assumes no responsibility for any errors which may appear in this document.
- NEC Corporation does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from use of a device described herein or any other liability arising from use of such device. No license, either express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC Corporation or others.
- Descriptions of circuits, software, and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software, and information in the design of the customer's equipment shall be done under the full responsibility of the customer. NEC Corporation assumes no responsibility for any losses incurred by the customer or third parties arising from the use of these circuits, software, and information.
- While NEC Corporation has been making continuous effort to enhance the reliability of its semiconductor devices, the possibility of defects cannot be eliminated entirely. To minimize risks of damage or injury to persons or property arising from a defect in an NEC semiconductor device, customers must incorporate sufficient safety measures in its design, such as redundancy, fire-containment, and anti-failure features.
- NEC devices are classified into the following three quality grades:
  "Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.
  - Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
  - Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
  - Specific: Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

  The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.

M7 98.8