

## 64K x 16 Static RAM

### Features

- **3.3V operation (3.0V–3.6V)**
- **High speed**  
—  $t_{AA} = 10/12/15$  ns
- **CMOS for optimum speed/power**
- **Low Active Power (L version)**  
— 576 mW (max.)
- **Low CMOS Standby Power (L version)**  
— 1.80 mW (max.)
- **Automatic power-down when deselected**
- **Independent control of upper and lower bits**
- **Available in 44-pin TSOP II and 400-mil SOJ**
- **Available in a 48-Ball Mini BGA package**

### Functional Description

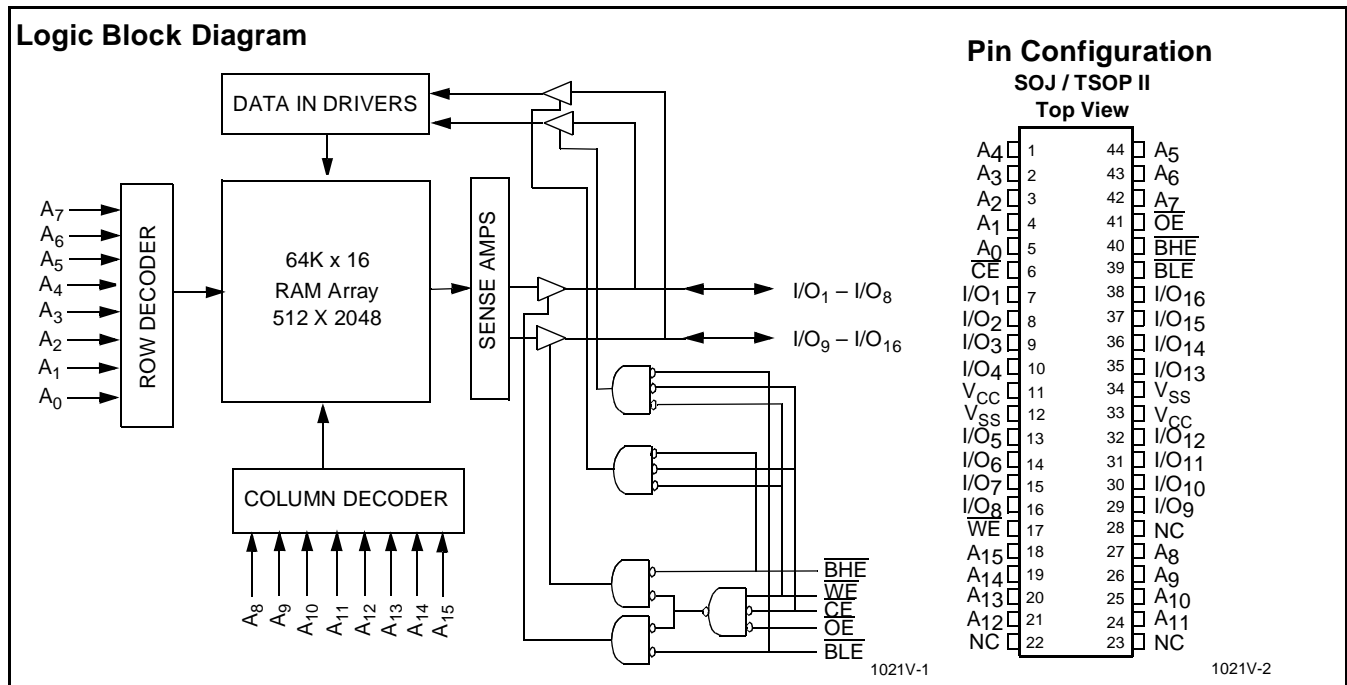
The CY7C1021V is a high-performance CMOS static RAM organized as 65,536 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from I/O pins (I/O<sub>1</sub> through I/O<sub>8</sub>), is written into the location specified on the address pins (A<sub>0</sub> through A<sub>15</sub>). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from I/O pins (I/O<sub>9</sub> through I/O<sub>16</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>15</sub>).

Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins will appear on I/O<sub>1</sub> to I/O<sub>8</sub>. If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory will appear on I/O<sub>9</sub> to I/O<sub>16</sub>. See the truth table at the back of this data sheet for a complete description of read and write modes.

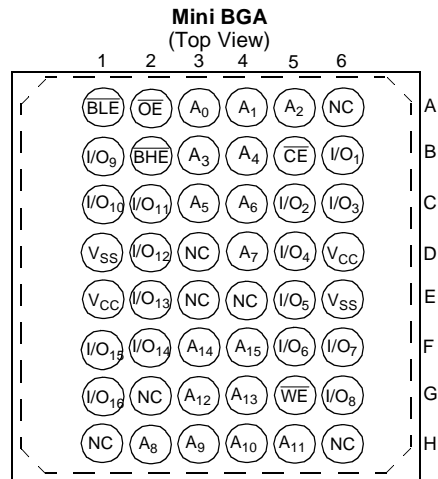
The input/output pins (I/O<sub>1</sub> through I/O<sub>16</sub>) are placed in a high-impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), the  $\overline{BHE}$  and  $\overline{BLE}$  are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH), or during a write operation ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW).

The CY7C1021V is available in 400-mil-wide SOJ, standard 44-pin TSOP Type II, and in 48-ball mini BGA packages.



### Selection Guide

		7C1021V-10	7C1021V-12	7C1021V-15
Maximum Access Time (ns)		10	12	15
Maximum Operating Current (mA)	Commercial	210	200	190
	L	160	150	140
Maximum CMOS Standby Current (mA)	Commercial	5	5	5
	L	0.500	0.500	0.500

**Pin Configurations** (continued)

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with Power Applied ..... -55°C to +125°C

Supply Voltage on V<sub>CC</sub> to Relative GND<sup>[1]</sup> ..... -0.5V to +4.6V

DC Voltage Applied to Outputs in High Z State<sup>[1]</sup> ..... -0.5V to V<sub>CC</sub>+0.5V

DC Input Voltage<sup>[1]</sup> ..... -0.5V to V<sub>CC</sub>+0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V  
(per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

**Operating Range**

Range	Ambient Temperature <sup>[2]</sup>	V <sub>CC</sub>
Commercial	0°C to +70°C	3.3V ± 10%
Industrial	-40°C to +85°C	3.3V ± 10%

**Notes:**

- V<sub>IL</sub> (min.) = -2.0V for pulse durations of less than 20 ns.
- T<sub>A</sub> is the "instant on" case temperature.

**Electrical Characteristics** Over the Operating Range

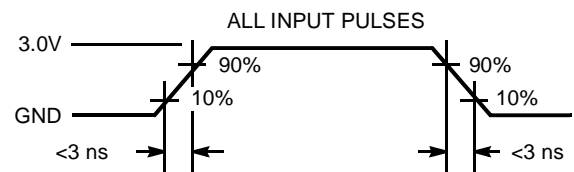
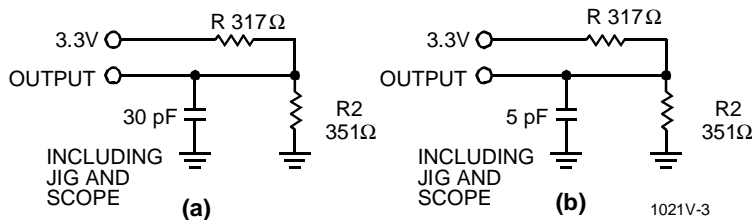
Parameter	Description	Test Conditions	7C1021V-10		7C1021V-12		7C1021V-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.3V	2.2	V <sub>CC</sub> + 0.3V	2.2	V <sub>CC</sub> + 0.3V	V
V <sub>IL</sub>	Input LOW Voltage <sup>[1]</sup>		-0.3	0.8	-0.3	0.8	-0.3	0.8	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1	+1	-1	+1	-1	+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	-1	+1	-1	+1	-1	+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>		210		200		190	mA
			L	160		150		140	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current — TTL Inputs	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>		40		40		40	mA
I <sub>SB2</sub>	Automatic CE Power-Down Current — CMOS Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>CC</sub> - 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V, or V <sub>IN</sub> ≤ 0.3V, f = 0		5		5		5	mA
			L	500		500		500	μA

**Capacitance<sup>[3]</sup>**

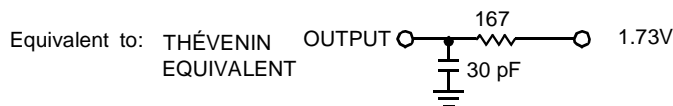
Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz	6	pF
C <sub>OUT</sub>	Output Capacitance		8	pF

**Note:**

3. Tested initially and after any design or process changes that may affect these parameters.

**AC Test Loads and Waveforms**


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**Switching Characteristics<sup>[4]</sup> Over the Operating Range**

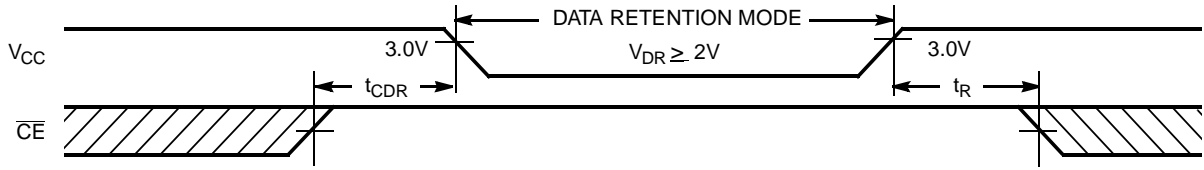
Parameter	Description	7C1021V-10		7C1021V-12		7C1021V-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>								
$t_{RC}$	Read Cycle Time	10		12		15		ns
$t_{AA}$	Address to Data Valid		10		12		15	ns
$t_{OHA}$	Data Hold from Address Change	3		3		3		ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid		10		12		15	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		4		6		7	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z	0		0		0		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[5, 6]</sup>		5		6		7	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low Z <sup>[6]</sup>	3		3		3		ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High Z <sup>[5, 6]</sup>		5		6		7	ns
$t_{PU}$	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
$t_{PD}$	$\overline{CE}$ HIGH to Power-Down		12		12		15	ns
$t_{DBE}$	Byte Enable to Data Valid		5		6		7	ns
$t_{LZBE}$	Byte Enable to Low Z	0		0		0		ns
$t_{HZBE}$	Byte Disable to High Z		5		6		7	ns
<b>WRITE CYCLE<sup>[7]</sup></b>								
$t_{WC}$	Write Cycle Time	10		12		15		ns
$t_{SCE}$	$\overline{CE}$ LOW to Write End	8		9		10		ns
$t_{AW}$	Address Set-Up to Write End	7		8		10		ns
$t_{HA}$	Address Hold from Write End	0		0		0		ns
$t_{SA}$	Address Set-Up to Write Start	0		0		0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	8		8		10		ns
$t_{SD}$	Data Set-Up to Write End	6		6		8		ns
$t_{HD}$	Data Hold from Write End	0		0		0		ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[6]</sup>	3		3		3		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[5, 6]</sup>		5		6		7	ns
$t_{BW}$	Byte Enable to End of Write	8		8		9		ns

**Data Retention Characteristics Over the Operating Range (L version only)**

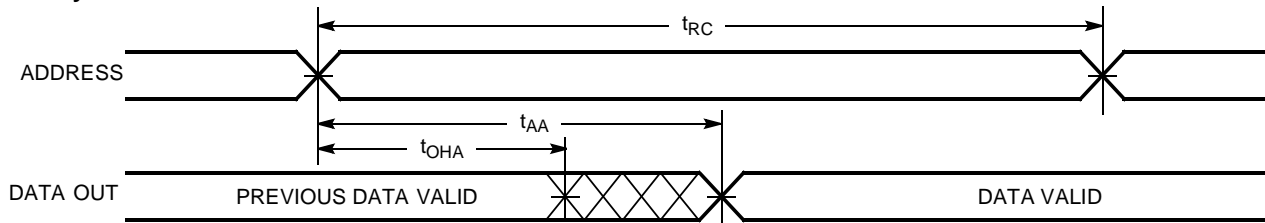
Parameter	Description	Conditions <sup>[10]</sup>	Min.	Max.	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		2.0		V
$I_{CCDR}$	Data Retention Current	Com'l		100	$\mu$ A
$t_{CDR}$ <sup>[8]</sup>	Chip Deselect to Data Retention Time		0		ns
$t_R$ <sup>[9]</sup>	Operation Recovery Time		$t_{RC}$		ns

**Notes:**

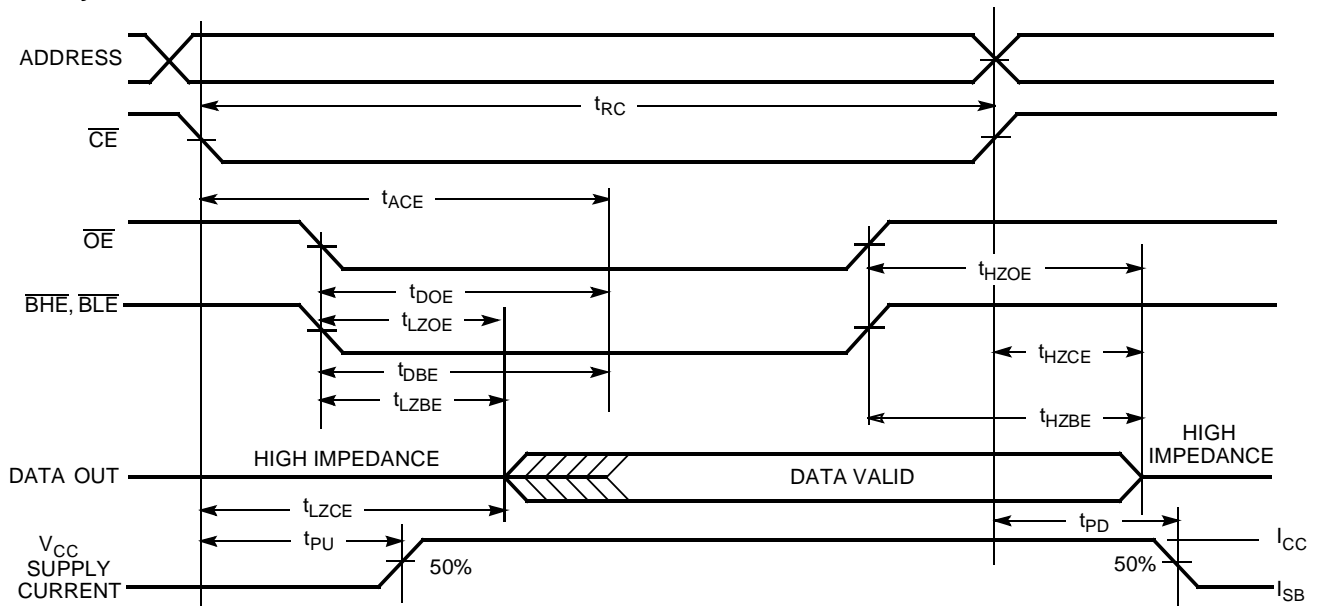
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
- $t_{HZOE}$ ,  $t_{HZBE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW,  $\overline{WE}$  LOW and  $BHE$  /  $BLE$  LOW.  $\overline{CE}$ ,  $\overline{WE}$  and  $BHE$  /  $BLE$  must be LOW to initiate a write, and the transition of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- Tested initially and after any design or process changes that may affect these parameters.
- $t_r \leq 3$  ns for the -12 and -15 speeds.  $t_r \leq 5$  ns for the -20 and slower speeds.
- No input may exceed  $V_{CC} + 0.5V$ .

**Data Retention Waveform**


1021V-5

**Switching Waveforms**
**Read Cycle No. 1** <sup>[11, 12]</sup>


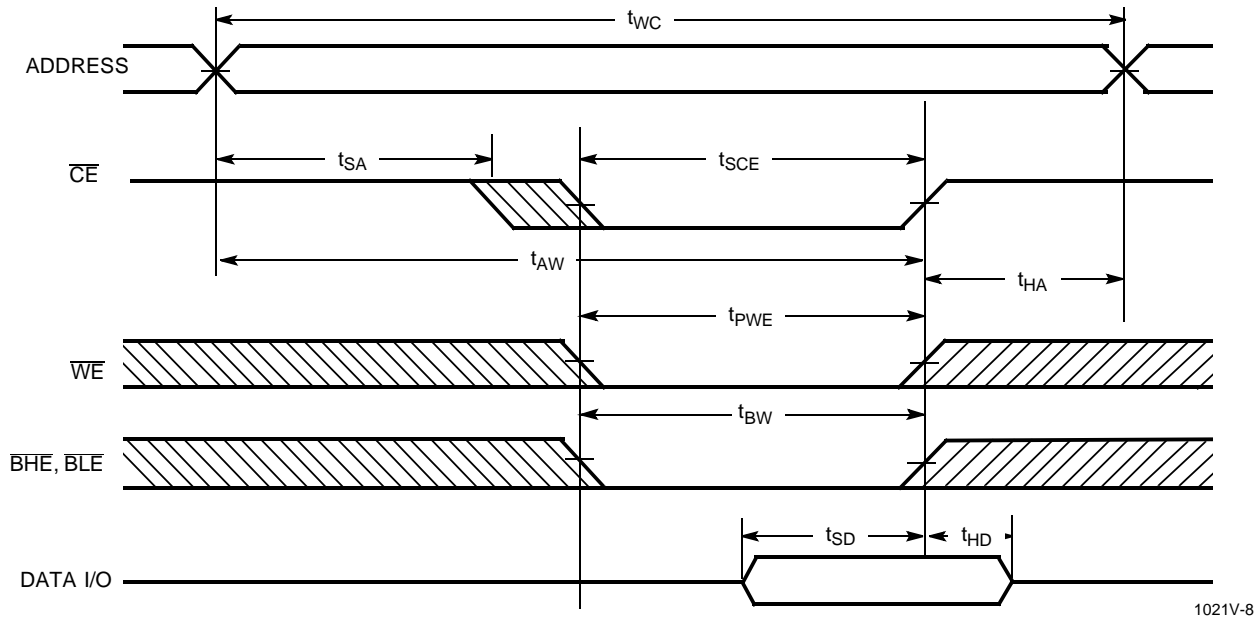
1021V-6

**Read Cycle No. 2 ( $\overline{OE}$  Controlled)** <sup>[12, 13]</sup>


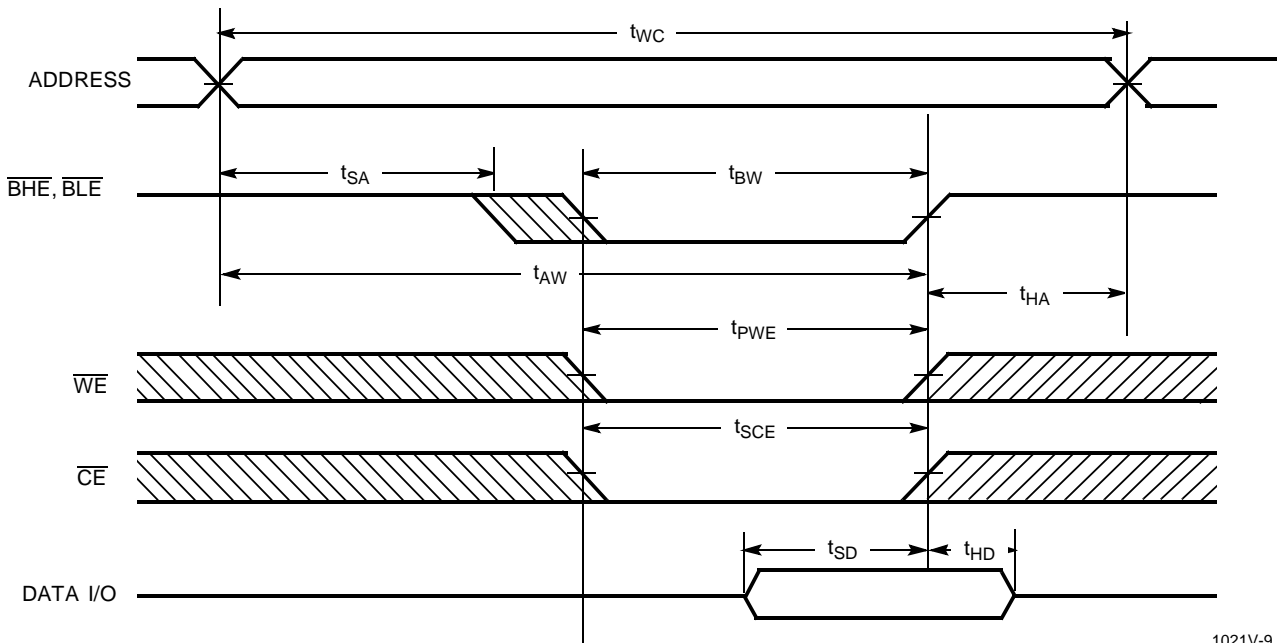
1021V-7

**Notes:**

11. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$ ,  $\overline{BHE}$  and/or  $\overline{BLE}$  =  $V_{IL}$ .
12.  $\overline{WE}$  is HIGH for read cycle.
13. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

**Switching Waveforms (continued)**
**Write Cycle No. 1 ( $\overline{CE}$  Controlled)** <sup>[14, 15]</sup>


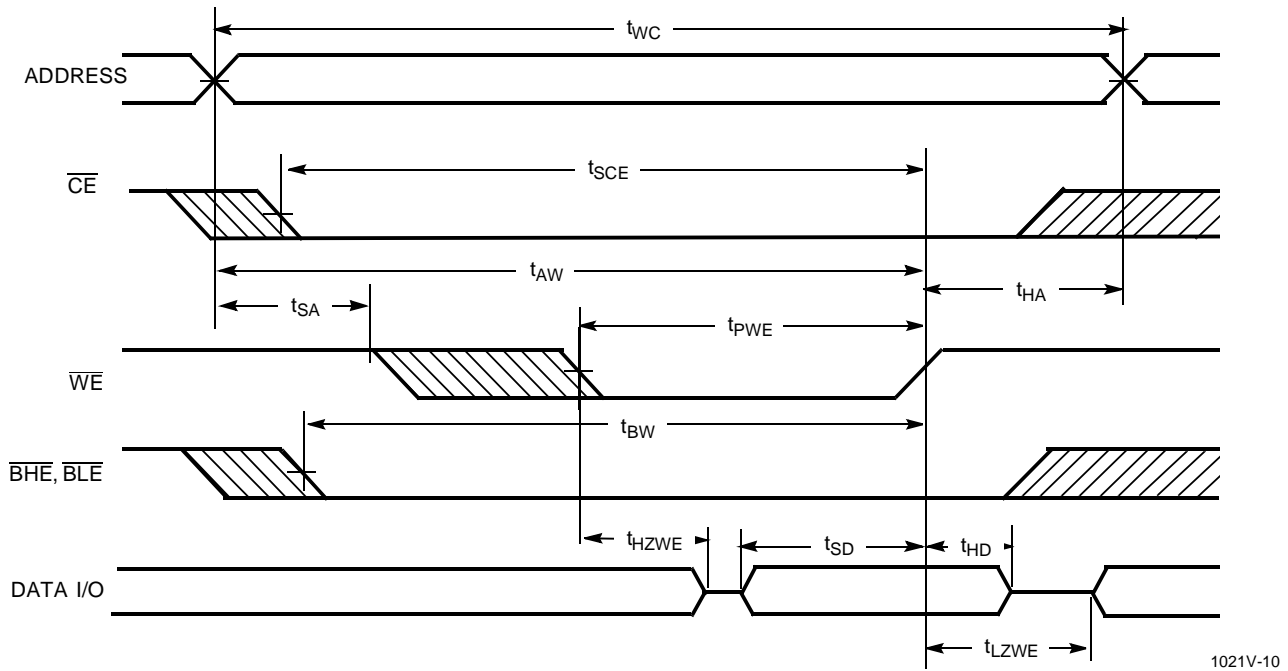
1021V-8

**Write Cycle No. 2 ( $\overline{BLE}$  or  $\overline{BHE}$  Controlled)**


1021V-9

**Notes:**

14. Data I/O is high impedance if  $\overline{OE}$  or  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IH}$ .
15. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.

**Switching Waveforms (continued)**
**Write Cycle No. 3 ( $\overline{WE}$  Controlled, LOW)**


1021V-10

**Truth Table**

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O <sub>1</sub> -I/O <sub>8</sub>	I/O <sub>9</sub> -I/O <sub>16</sub>	Mode	Power
H	X	X	X	X	High Z	High Z	Power-Down	Standby ( $I_{SB}$ )
L	L	H	L	L	Data Out	Data Out	Read - All bits	Active ( $I_{CC}$ )
			L	H	Data Out	High Z	Read - Lower bits only	Active ( $I_{CC}$ )
			H	L	High Z	Data Out	Read - Upper bits only	Active ( $I_{CC}$ )
L	X	L	L	L	Data In	Data In	Write - All bits	Active ( $I_{CC}$ )
			L	H	Data In	High Z	Write - Lower bits only	Active ( $I_{CC}$ )
			H	L	High Z	Data In	Write - Upper bits only	Active ( $I_{CC}$ )
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active ( $I_{CC}$ )
L	X	X	H	H	High Z	High Z	Selected, Outputs Disabled	Active ( $I_{CC}$ )

**Ordering Information**

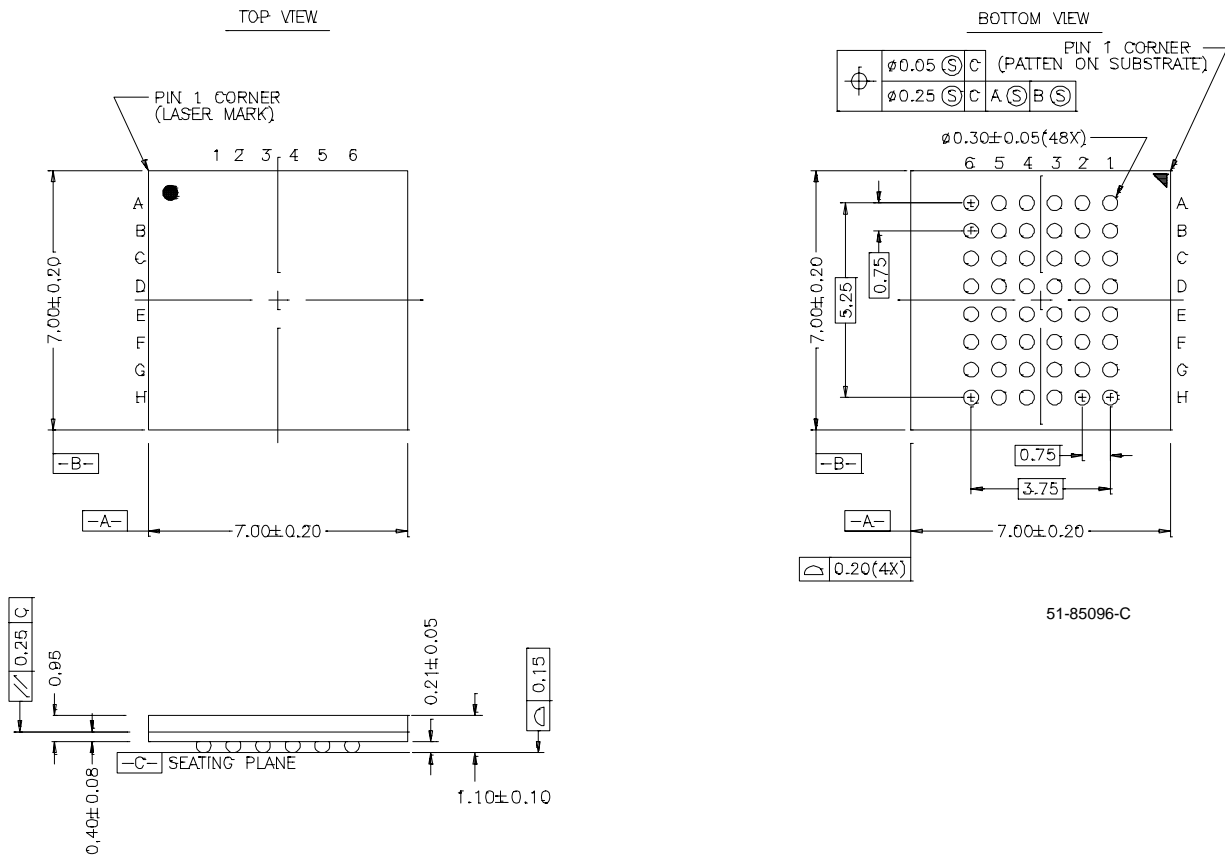
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C1021V33-10BAC	BA48	48-Ball Mini Ball Grid Array (7.00 mm x 7.00 mm)	Commercial
	CY7C1021V33-10VC	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1021V33L-10VC	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1021V33-10ZC	Z44	44-Lead TSOP Type II	
	CY7C1021V33L-10ZC	Z44	44-Lead TSOP Type II	
12	CY7C1021V33-12BAC	BA48	48-Ball Mini Ball Grid Array (7.00 mm x 7.00 mm)	Commercial
	CY7C1021V33-12VC	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1021V33L-12VC	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1021V33-12ZC	Z44	44-Lead TSOP Type II	
	CY7C1021V33L-12ZC	Z44	44-Lead TSOP Type II	
	CY7C1021V33-12BAI	BA48	48-Ball Mini Ball Grid Array (7.00 mm x 7.00 mm)	Industrial
	CY7C1021V33-12VI	V34	44-Lead (400-Mil) Molded SOJ	
15	CY7C1021V33-15BAC	BA48	48-Ball Mini Ball Grid Array (7.00 mm x 7.00 mm)	Commercial
	CY7C1021V33L-15BAC	BA48	48-Ball Mini Ball Grid Array (7.00 mm x 7.00 mm)	
	CY7C1021V33-15VC	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1021V33L-15VC	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1021V33-15ZC	Z44	44-Lead TSOP Type II	
	CY7C1021V33L-15VC	Z44	44-Lead TSOP Type II	
	CY7C1021V33-15BAI	BA48	48-Ball Mini Ball Grid Array (7.00 mm x 7.00 mm)	Industrial
	CY7C1021V33L-15BAI	BA48	48-Ball Mini Ball Grid Array (7.00 mm x 7.00 mm)	
	CY7C1021V33-15VI	V34	44-Lead (400-Mil) Molded SOJ	
	CY7C1021V33L-15ZI	Z44	44-Lead TSOP Type II	

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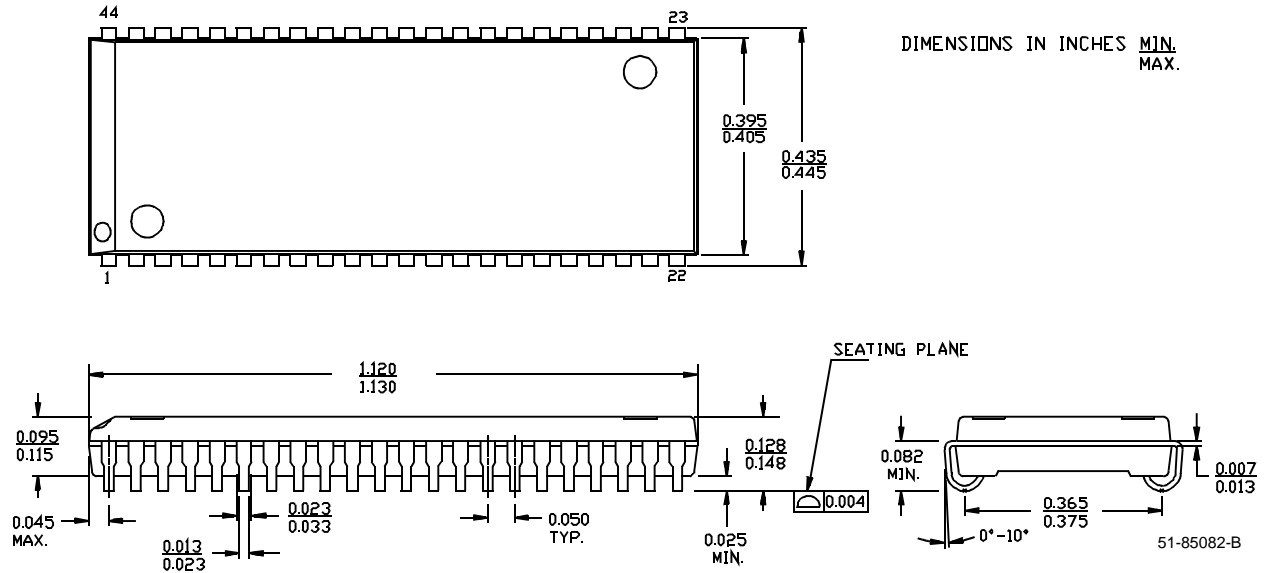


Package Diagrams

48-Ball (7.00 mm x 7.00 mm) FBGA BA48



51-85096-C

**Package Diagrams (continued)**
**44-Lead (400-Mil) Molded SOJ V34**

**44-Pin TSOP II Z44**
