

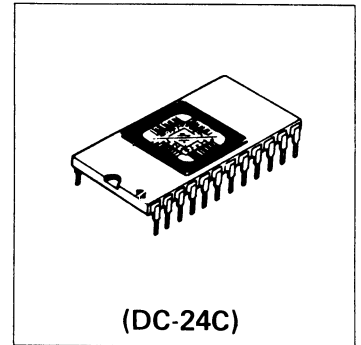
HN462732

4096-word × 8-bit UV Erasable and Programmable Read Only Memory

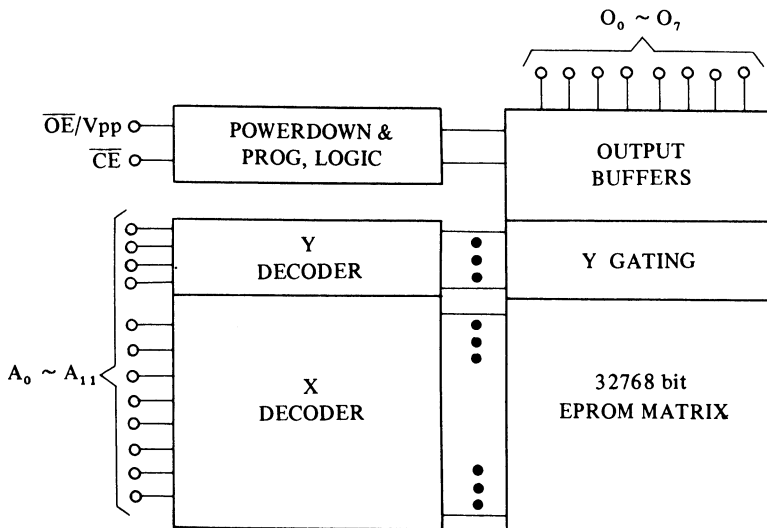
The HN462732 is a 4096 word by 8 bit erasable and electrically programmable ROM. This device is packaged in a 24-pin, dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern, whereby a new pattern can then be written into the device.

■ FEATURES

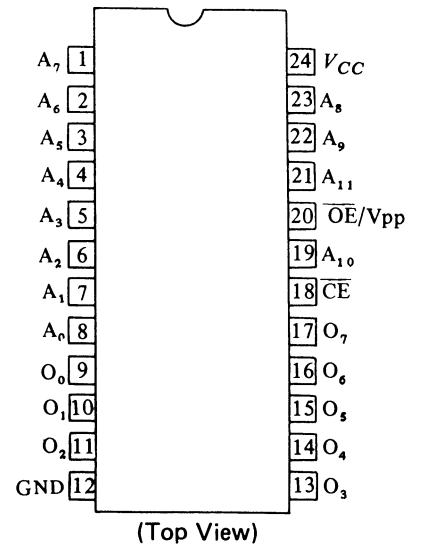
- Single Power Supply +5V ±5%
- Simple Programming Program Voltage: +25V D.C.
Program with One 50ms Pulse
- Static No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Fully Decoded On-Chip Address Decode
- Access Time 450ns Max.
- Low Power Dissipation 150mA Max. Active Current
30mA Max. Standby Current
- Three State Output OR-Tie-Capability
- Compatible with INTEL 2732



■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



■ MODE SELECTION

Mode \ Pins	\overline{CE} (18)	\overline{OE}/V_{PP} (20)	V_{CC} (24)	Outputs (9 ~ 11, 13 ~ 17)
Read	V_{IL}	V_{IL}	+5	Dout
Stand by	V_{IH}	Don't Care	+5	High Z
Program	V_{IL}	V_{PP}	+5	Din
Program Verify	V_{IL}	V_{IL}	+5	Dout
Program Inhibit	V_{IH}	V_{PP}	+5	High Z

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +125	°C
All Input and Output Voltages*	V_{IN}, V_{out}	-0.3 to +7	V
V_{PP} Voltage*	\overline{OE}/V_{PP}	-0.3 to +28	V

*with respect to GND

■ READ OPERATION

● D. C. AND OPERATING CHARACTERISTICS ($T_a=0$ to +70°C, $V_{CC}=5V\pm 5\%$)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current (Except \overline{OE}/V_{PP})	I_{LI1}	$V_{IN} = 5.25$ V	-	-	10	μA
\overline{OE}/V_{PP} Input Leakage Current	I_{LI2}	$V_{IN} = 5.25$ V	-	-	300	μA
Output Leakage Current	I_{LO}	$V_{out} = 5.25$ V	-	-	10	μA
V_{CC} Current (Standby)	I_{CC1}	$\overline{CE} = V_{IH}, \overline{OE} = V_{IL}$	-	-	30	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{OE} = \overline{CE} = V_{IL}$	-	-	150	mA
Input Low Voltage	V_{IL}		-0.1	-	0.8	V
Input High Voltage	V_{IH}		2.0	-	$V_{CC} + 1$	V
Output Low Voltage	V_{OL}	$I_{OL} = 2.1$ mA	-	-	0.45	V
Output High Voltage	V_{OH}	$I_{OH} = -400$ μA	2.4	-	-	V

● A. C. CHARACTERISTICS ($T_a=0$ to +70°C, $V_{CC}=5V\pm 5\%$)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Address to Output Delay	t_{ACC}	$\overline{CE} = \overline{OE} = V_{IL}$	-	-	450	ns
\overline{CE} to Output Delay	t_{CE}	$\overline{OE} = V_{IL}$	-	-	450	ns
Output Enable to Output Delay	t_{OE}	$\overline{CE} = V_{IL}$	-	-	120	ns
Output Enable High to Output Float	t_{DF}	$\overline{CE} = V_{IL}$	0	-	100	ns
Address to Output Hold	t_{OH}	$\overline{CE} = \overline{OE} = V_{IL}$	0	-	-	ns

● SWITCHING CHARACTERISTICS

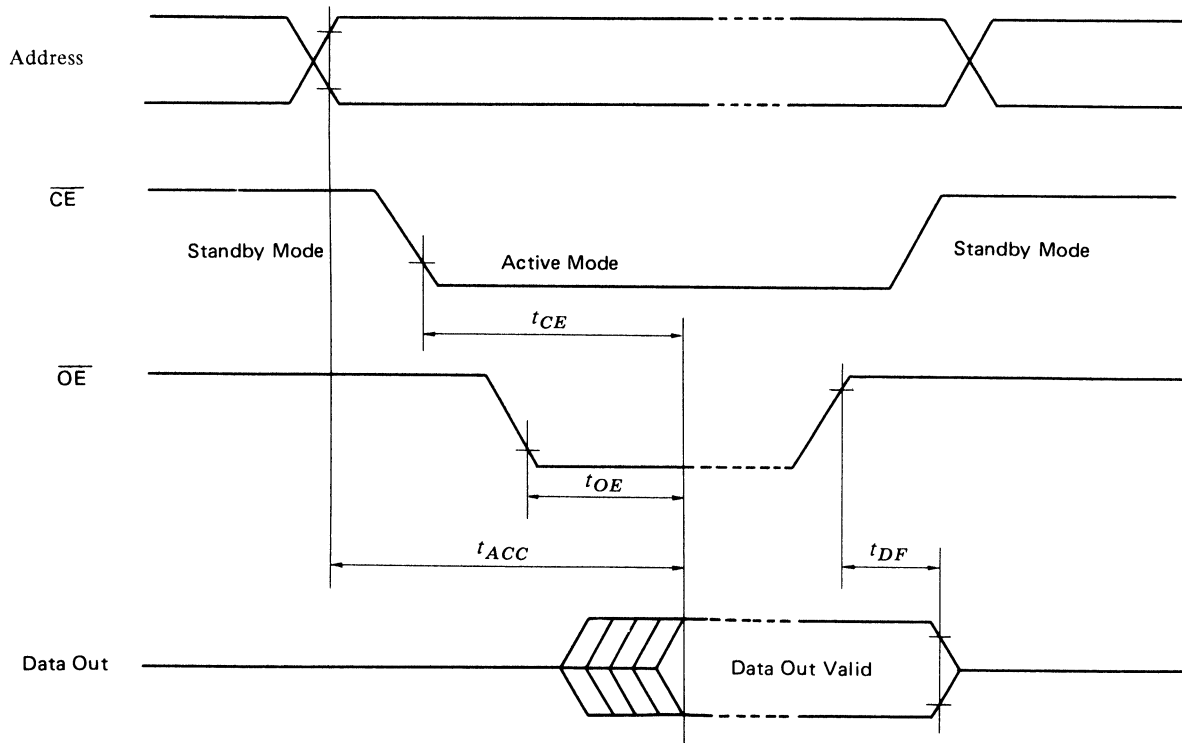
Test Condition

Input Pulse Levels: 0.8V to 2.2V

Input Rise and Fall Times: $\leq 20\text{ns}$

Output Load: 1TTL Gate + 100pF

Reference Level for Measuring Timing: Inputs 1V and 2V
Outputs 0.8V and 2V



● CAPACITANCE ($T_a=25^\circ\text{C}$, $f=1\text{ MHz}$)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Capacitance (Except \overline{OE}/V_{PP})	C_{IN1}	$V_{IN} = 0\text{ V}$	–	–	6	pF
\overline{OE}/V_{PP} Input Capacitance	C_{IN2}	$V_{IN} = 0\text{ V}$	–	–	20	pF
Output Capacitance	C_{out}	$V_{out} = 0\text{ V}$	–	–	12	pF

■ PROGRAMMING OPERATION

- D.C. PROGRAMMING CHARACTERISTICS ($V_{CC}=5V\pm 5\%$, $V_{pp}=25V\pm 1V$, $T_a=25^\circ C\pm 5^\circ C$)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	$V_{IN} = 5.25/0.4 V$	–	–	10	μA
Output Low Voltage During Verify	V_{OL}	$I_{OL} = 2.1 mA$	–	–	0.4	V
Output High Voltage During Verify	V_{OH}	$I_{OH} = -400 \mu A$	2.4	–	–	V
V_{CC} Supply Current	I_{CC}		–	–	150	mA
Input Low Level	V_{IL}		–0.1	–	0.8	V
Input High Level (All Inputs Except \overline{OE}/V_{PP})	V_{IH}		2.0	–	$V_{CC} + 1$	V
V_{PP} Supply Current	I_{PP}	$\overline{CE} = V_{IL}, \overline{OE} = V_{PP}$	–	–	30	mA

- A.C. PROGRAMMING CHARACTERISTICS ($V_{CC}=5V\pm 5\%$, $V_{pp}=25V\pm 1V$, $T_a=25^\circ C\pm 5^\circ C$)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Address Setup Time	t_{AS}		2	–	–	μs
\overline{OE} Setup Time	t_{OES}		2	–	–	μs
Data Setup Time	t_{DS}		2	–	–	μs
Address Hold Time	t_{AH}		0	–	–	μs
\overline{OE} Hold Time	t_{OEH}		2	–	–	μs
Data Hold Time	t_{DH}		2	–	–	μs
Chip Enable to Output Float Delay	t_{DF}		0	–	120	ns
Data Valid from \overline{CE}	t_{DV}	$\overline{CE} = V_{IL}, \overline{OE} = V_{IL}$	–	–	1	μs
\overline{CE} Pulse Width During Programming	t_{PW}		45	50	55	ms
\overline{OE} Pulse Rise Time During Programming	t_{PRT}		50	–	–	ns
V_{PP} Recovery Time	t_{VR}		2	–	–	μs

● SWITCHING CHARACTERISTICS

Test Conditions

Input Pulse Level: 0.8V to 2.2V

Input Rise and Fall Times: $\leq 20ns$

Output Load: 1 TTL Gate + 100pF

Reference Level for Measuring Timing: Inputs; 1V and 2V,
Outputs; 0.8V and 2V