

# SIEMENS

**3.3V 2M x 64/72-Bit 1 BANK SDRAM Module**

**HYS64/72V2200GU-8/-10**

**3.3V 4M x 64/72-Bit 2 BANK SDRAM Module**

**HYS64/72V4220GU-8/-10**

## 168 pin unbuffered DIMM Modules

- 168 Pin PC100 and PC66 compatible unbuffered 8 Byte Dual-In-Line SDRAM Modules for PC main memory applications
- 1 bank 2M x 64, 2M x 72 and 2 bank 4M x 64, 4M x 72 organisation
- Optimized for byte-write non-parity or ECC applications
- JEDEC standard Synchronous DRAMs (SDRAM)
- Fully PC board layout compatible to INTEL's Rev. 1.0 module specification
- SDRAM Performance:

		-8	-8-3	-10	Units
f <sub>CK</sub>	Clock frequency (max.)	100	100	66	MHz
t <sub>AC</sub>	Clock access time	6	6	8	ns

- Programmed Latencies :

Product Speed		CL	tRCD	tRP
-8	PC100	2	2	2
-8-3	PC100	3	2	3
-10	PC66	2	2	2

- Single +3.3V(± 0.3V ) power supply
- Programmable  $\overline{\text{CAS}}$  Latency, Burst Length and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- Decoupling capacitors mounted on substrate
- All inputs, outputs are LVTTTL compatible
- Serial Presence Detect with E<sup>2</sup>PROM
- Utilizes 2M x 8 SDRAMs in TSOPII-44 packages
- 4096 refresh cycles every 64 ms
- 133,35 mm x 31.75 mm x 4,00 mm card size with gold contact pads

The HYS64(72)2200 and HYS64(72)4220 are industry standard 168-pin 8-byte Dual in-line Memory Modules (DIMMs) which are organised as 2M x 64, 2M x 72 in 1 bank and 4M x 64 and 4M x 72 in two banks high speed memory arrays designed with Synchronous DRAMs (SDRAMs) for non-parity and ECC applications. The DIMMs use -8 speed sort 2M x 8 SDRAM devices in TSOP44 packages to meet the PC100 requirement. Modules which use -10 parts are suitable for PC66 applications only. Decoupling capacitors are mounted on the PC board. The PC board design is according to INTEL's PC SDRAM Rev.1.0 module specification.

The DIMMs have a serial presence detect, implemented with a serial E<sup>2</sup>PROM using the two pin I<sup>2</sup>C protocol. The first 128 bytes are utilized by the DIMM manufacturer and the second 128 bytes are available to the end user.

All SIEMENS 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 133,35 mm long footprint, with 1,25" ( 31,75 mm) height

### Ordering Information

Type	Ordering Code	Package	Descriptions	Module Height
HYS 64V2200GU-8	PC100-222-620	L-DIM-168-29	100 Mhz 2M x 64 1 bank SDRAM module	1,25"
HYS 72V2200GU-8	PC100-222-620	L-DIM-168-29	100 MHz 2M x 72 1 bank SDRAM module	1,25"
HYS 64V4220GU-8	PC100-222-620	L-DIM-168-29	100 Mhz 4M x 64 2 bank SDRAM module	1,25"
HYS 72V4220GU-8	PC100-222-620	L-DIM-168-29	100 Mhz 4M x 72 2 bank SDRAM module	1,25"
HYS 64V2200GU-8-3	PC100-323-620	L-DIM-168-29	100 Mhz 2M x 64 1 bank SDRAM module	1,25"
HYS 72V2200GU-8-3	PC100-323-620	L-DIM-168-29	100 MHz 2M x 72 1 bank SDRAM module	1,25"
HYS 64V4220GU-8-3	PC100-323-620	L-DIM-168-29	100 Mhz 4M x 64 2 bank SDRAM module	1,25"
HYS 72V4220GU-8-3	PC100-323-620	L-DIM-168-29	100 Mhz 4M x 72 2 bank SDRAM module	1,25"
HYS 64V2200GU-10	PC66-222-920	L-DIM-168-29	66 Mhz 2M x 64 1 bank SDRAM module	1,25"
HYS 72V2200GU-10	PC66-222-920	L-DIM-168-29	66 MHz 2M x 72 1 bank SDRAM module	1,25"
HYS 64V4220GU-10	PC66-222-920	L-DIM-168-29	66 Mhz 4M x 64 2 bank SDRAM module	1,25"
HYS 72V4220GU-10	PC66-222-920	L-DIM-168-29	66 Mhz 4M x 72 2 bank SDRAM module	1,25"

### Pin Names

A0-A10	Address Inputs	CLK0 - CLK3	Clock Input
BA	Bank Address	DQMB0 - DQMB7	Data Mask
DQ0 - DQ63	Data Input/Output	CS0 - CS3	Chip Select
CB0-CB7	Check Bits (x72 organisation only)	Vcc	Power (+3.3 Volt)
RAS	Row Address Strobe	Vss	Ground
CAS	Column Address Strobe	SCL	Clock for Presence Detect
WE	Read / Write Input	SDA	Serial Data Out for Presence Detect
CKE0, CKE1	Clock Enable	N.C.	No Connection

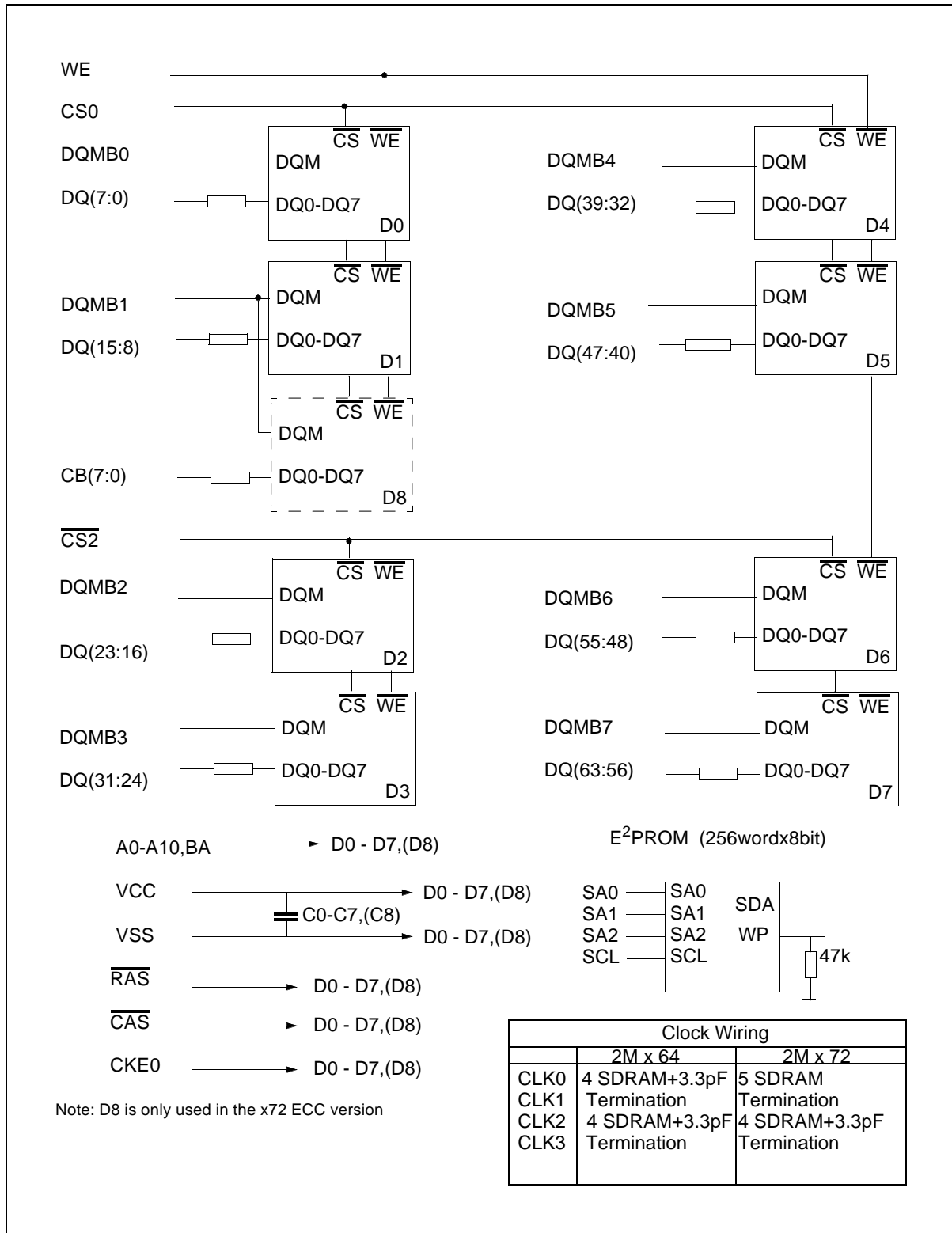
### Address Format:

	Part Number	Rows	Columns	Banks	Refresh	Period	Interval
2M x 64	HYS 64V2200GU	11	9	1	4k	64 ms	15,6 μs
2M x 72	HYS 72V2200GU	11	9	1	4k	64 ms	15,6 μs
4M x 64	HYS 64V4220GU	11	9	1	4k	64 ms	15,6 μs
4M x 72	HYS 72V4220GU	11	9	1	4k	64 ms	15,6 μs

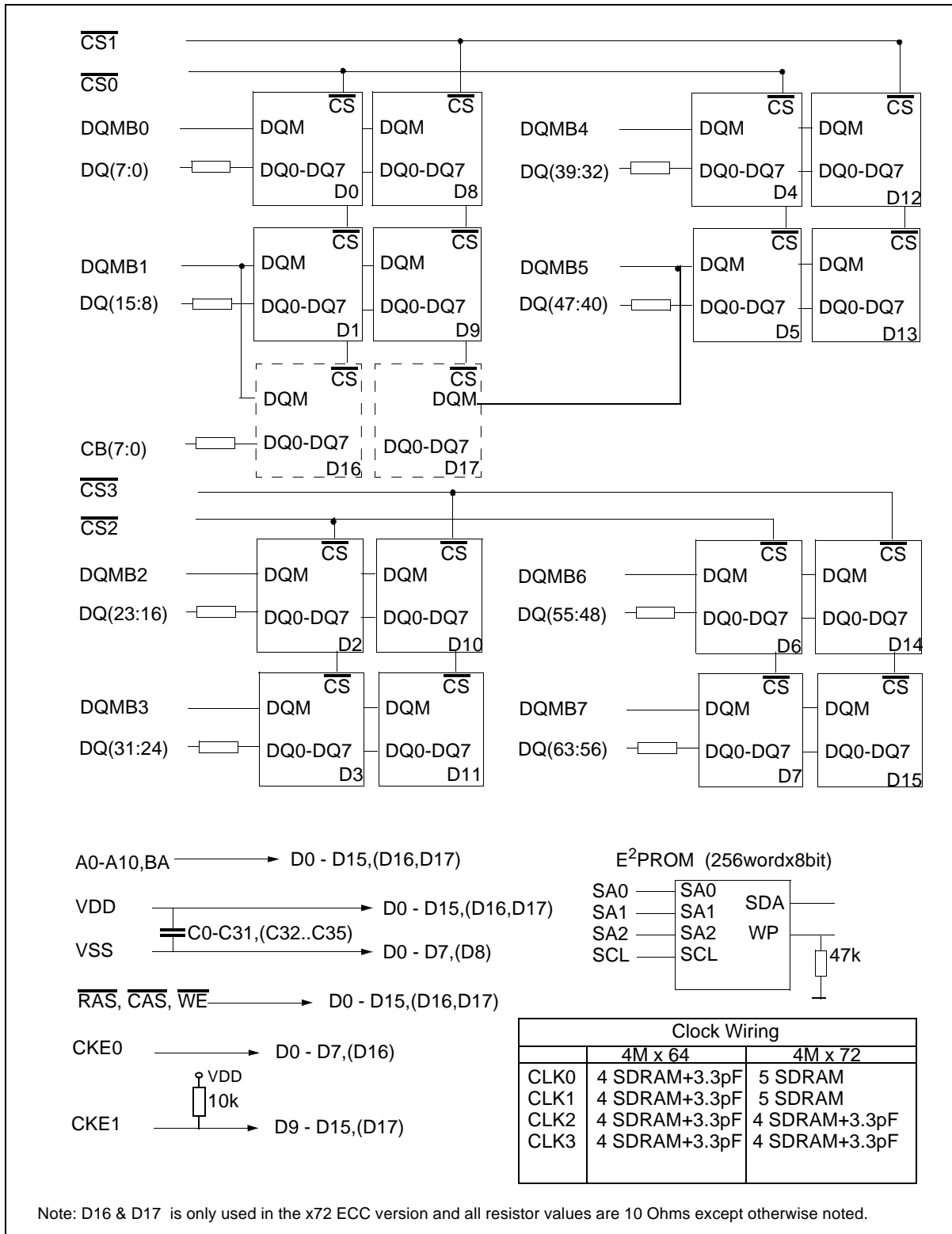
### Pin Configuration

PIN #	Symbol	PIN #	Symbol	PIN #	Symbol	PIN #	Symbol
1	VSS	43	VSS	85	VSS	127	VSS
2	DQ0	44	DU	86	DQ32	128	CKE0
3	DQ1	45	CS2	87	DQ33	129	CS3
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	VCC	48	DU	90	VCC	132	NC
7	DQ4	49	VCC	91	DQ36	133	VCC
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	NC (CB2)	94	DQ39	136	CB6
11	DQ8	53	NC (CB3)	95	DQ40	137	CB7
12	VSS	54	VSS	96	VSS	138	VSS
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	VCC	101	DQ45	143	VCC
18	VCC	60	DQ20	102	VCC	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	DU	104	DQ47	146	DU
21	NC (CB0)	63	CKE1	105	NC (CB4)	147	NC
22	NC (CB1)	64	VSS	106	NC (CB5)	148	VSS
23	VSS	65	DQ21	107	VSS	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	VCC	68	VSS	110	VCC	152	VSS
27	WE	69	DQ24	111	CAS	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	CS0	72	DQ27	114	CS1	156	DQ59
31	DU	73	VCC	115	RAS	157	VCC
32	VSS	74	DQ28	116	VSS	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	VSS	120	A7	162	VSS
37	A8	79	CLK2	121	A9	163	CLK3
38	A10	80	NC	122	BA	164	NC
39	NC	81	WP	123	NC	165	SA0
40	VCC	82	SDA	124	VCC	166	SA1
41	VCC	83	SCL	125	CLK1	167	SA2
42	CLK0	84	VCC	126	NC	168	VCC

Note : Pinnames in brackets are for the x72 ECC versions



Block Diagram for 2M x 64/72 SDRAM DIMM modules (HYS64/72V2200GU)



Block Diagram for 4M x 64/72 SDRAM DIMM modules (HYS64/72V4220GU)

### DC Characteristics

$T_A = 0$  to  $70$  °C;  $V_{SS} = 0$  V;  $V_{DD}, V_{DDQ} = 3.3$  V  $\pm$  0.3 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input high voltage	$V_{IH}$	2.0	$V_{CC}+0.3$	V
Input low voltage	$V_{IL}$	-0.5	0.8	V
Output high voltage ( $I_{OUT} = -2.0$ mA)	$V_{OH}$	2.4	-	V
Output low voltage ( $I_{OUT} = 2.0$ mA)	$V_{OL}$	-	0.4	V
Input leakage current, any input ( $0$ V < $V_{IN} < 3.6$ V, all other inputs = 0 V)	$I_{I(L)}$	-40	40	$\mu$ A
Output leakage current (DQ is disabled, $0$ V < $V_{OUT} < V_{CC}$ )	$I_{O(L)}$	-40	40	$\mu$ A

### Capacitance

$T_A = 0$  to  $70$  °C;  $V_{DD} = 3.3$  V  $\pm$  0.3 V,  $f = 1$  MHz

Parameter	Symbol	Limit Values				Unit
		max. 2Mx64	max. 2Mx72	max. 4Mx64	max. 4Mx72	
Input capacitance (A0 to A10, BA, $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ )	$C_{I1}$	45	55	80	90	pF
Input capacitance (CS0 -CS3)	$C_{I2}$	20	25	30	35	pF
Input capacitance (CLK0 - CLK3)	$C_{ICL}$	22	38	22	38	pF
Input capacitance (CKE0, CKE1)	$C_{I3}$	22	38	50	55	pF
Input capacitance (DQMB0 - DQMB7)	$C_{I4}$	13	13	20	20	pF
Input / Output capacitance (DQ0-DQ63, CB0-CB7)	$C_{IO}$	13	12	20	20	pF
Input Capacitance (SCL, SA0-2)	$C_{SC}$	8	8	8	8	pF
Input/Output Capacitance	$C_{sd}$	10	10	10	10	pF

### Standby and Refresh Currents ( $T_a = 0$ to $70^\circ\text{C}$ , $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$ ) <sup>1)</sup>

Parameter	Symbol	Test Condition	X64	X72		Note
			max.			
Operating Current	Icc1	Burst length = 4, CL=3 trc>=trc(min.), tck>=tck(min.), lo=0 mA 2 bank interleave operation	800	900	mA	1,2
Precharged Standby Current in Power Down Mode	Icc2P	CKE<=VIL(max), tck>=tck(min.)	24	27	mA	
	Icc2PS	CKE<=VIL(max), tck=infinite	16	18	mA	
Precharged Standby Current in Non-power Down Mode	Icc2N	CKE>=VIH(min), tck>=tck (min.), input changed once in 3 cycles	160	180	mA	$\overline{\text{CS}} = \text{High}$
	Icc2NS	CKE>=VIH(min), tck=infinite, no input change	80	90	mA	
Active Standby Current in Power Down Mode	Icc3P	CKE<=VIL(max), tck>=tck(min.)	24	27	mA	
	Icc3PS	CKE<=VIL(max), tck=infinite	16	18	mA	
Active Standby Current in Non-power Down Mode	Icc3N	CKE>=VIH(min), tck>=tck (min.) input changed one time	200	225	mA	$\overline{\text{CS}} = \text{High}$
	Icc3NS	CKE=>VIH(min),tck=infinite, no input change	120	135	mA	
Burst Operating Current	Icc4	Burst length = full page, trc = infinite, CL = 3, tck>=tck (min.), lo = 0 mA 2 banks activated	760	855	mA	1,2
Auto (CBR) Refresh Current	Icc5	trc>=trc(min)	720	810	mA	1,2
Self Refresh Current	Icc6	CKE=<0,2V	16	18	mA	1,2

### AC Characteristics 3)4)

$T_A = 0$  to  $70$  °C;  $V_{SS} = 0$  V;  $V_{CC} = 3.3$  V  $\pm$  0.3 V,  $t_T = 1$  ns

Parameter	Symbol	Limit Values						Unit	Note
		-8 PC100 2-2-2		-8-3 PC100 3-2-3		-10 PC66 2-2-2			
		min.	max.	min.	max.	min.	max.		

### Clock and Clock Enable

Clock Cycle Time $\overline{\text{CAS}}$ Latency = 3 $\overline{\text{CAS}}$ Latency = 2	$t_{CK}$								
		10		10		10		ns	
		10		10		15		ns	
System Frequency $\overline{\text{CAS}}$ Latency = 3 $\overline{\text{CAS}}$ Latency = 2	$f_{CK}$								
		–	100	–	100	–	100	MHz	
		–	100	–	100	–	66	MHz	
Clock Access Time $\overline{\text{CAS}}$ Latency = 3 $\overline{\text{CAS}}$ Latency = 2	$t_{AC}$								
		–	6	–	6	–	8	ns	4,5)
		–	6	–	7	–	9	ns	
Clock High Pulse Width	$t_{CH}$	3	–	3	–	3.5	–	ns	6)
Clock Low Pulse Width	$t_{CL}$	3	–	3	–	3.5	–	ns	6)
Input Setup time	$t_{CS}$	2	–	2	–	3	–	ns	7)
Input Hold Time	$t_{CH}$	1	–	1	–	1	–	ns	7)
CKE Setup Time (Power down mode)	$t_{CKSP}$	2.5	–	2.5	–	3	–	ns	8)
CKE Setup Time (Self Refresh Exit)	$t_{CKSR}$	8	–	8	–	8	–	ns	9)
Transition time (rise and fall)	$t_T$	1	–	1	–	1	–	ns	

### Common Parameters

$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay	$t_{RCD}$	20	–	20	–	30	–	ns	
Cycle Time	$t_{RC}$	70	120k	70	120k	75	120k	ns	
Active Command Period	$t_{RAS}$	45	–	45	–	45	–	ns	
Precharge Time	$t_{RP}$	20	–	30	–	30	–	ns	
Bank to Bank Delay Time	$t_{RRD}$	16	–	20	–	20	–	ns	
$\overline{\text{CAS}}$ to $\overline{\text{CAS}}$ delay time (same bank)	$t_{CCD}$	1	–	1	–	1	–	CLK	



Parameter	Symbol	Limit Values						Unit	Note
		-8 PC100 2-2-2		-8-3 PC100 3-2-3		-10 PC66 2-2-2			
		min.	max.	min.	max.	min.	max.		

### Refresh Cycle

Self Refresh Exit Time	$t_{SREX}$	10	–	10	–	10	–	ns	9)
Refresh Period (4096 cycles)	$t_{REF}$	64	–	64	–	64	–	ms	8)

### Read Cycle

Data Out Hold Time	$t_{OH}$	3	–	3	–	3	–	ns	4)
Data Out to Low Impedance Time	$t_{LZ}$	0	–	0	–	0	–	ns	
Data Out to High Impedance Time	$t_{HZ}$	3	9	3	9	3	9	ns	10)
DQM Data Out Disable Latency	$t_{DQZ}$	2	–	2	–	2	–	CLK	

### Write Cycle

Data input to Precharge (write recovery)	$t_{DPL}$	2	–	2	–	2	–	CLK	
Data In to Active/refresh	$t_{DAL}$	5	–	5	–	5	–	CLK	11)
DQM Write Mask Latency	$t_{DQW}$	0	–	0	–	0	–	CLK	

### Notes:

1. The specified values are valid when addresses are changed no more than once during  $t_{CK}(min.)$  and when No Operation commands are registered on every rising clock edge during  $t_{RC}(min.)$ . Values are shown per module bank.
2. The specified values are valid when data inputs (DQs) are stable during  $t_{RC}(min.)$ .
3. All AC characteristics are shown for device level.  
An initial pause of  $100\mu s$  is required after power-up, then a Precharge All Banks command must be given followed by 8 Auto Refresh (CBR) cycles before the Mode Register Set Operation can begin.
4. AC timing tests have  $V_{il} = 0.4 V$  and  $V_{ih} = 2.4 V$  with the timing referenced to the 1.4 V crossover point. The transition time is measured between  $V_{ih}$  and  $V_{il}$ . All AC measurements assume  $t_T=1ns$  with the AC output load circuit show. Specified  $t_{AC}$  and  $t_{OH}$  parameters are measured with a 50 pF only, without any resistive termination and with a input signal of 1V / ns edge rate between 0.8V and 2.0 V.

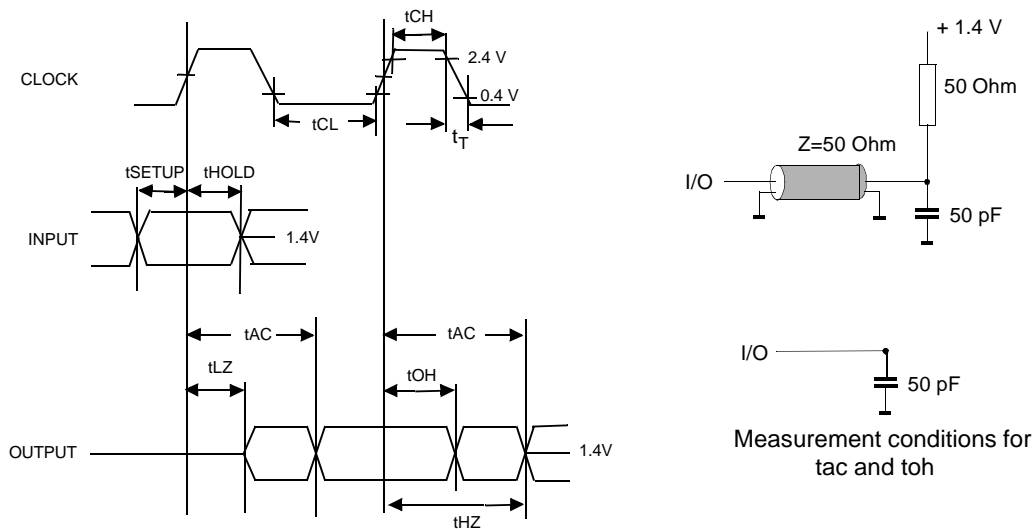


fig.1

5. If clock rising time is longer than 1ns, a time  $(t_T/2 - 0.5)$  ns has to be added to this parameter.
6. Rated at 1.5 V
7. If  $t_T$  is longer than 1 ns, a time  $(t_T - 1)$  ns has to be added to this parameter.
8. Any time that the refresh Period has been exceeded, a minimum of two Auto (CBR) Refresh commands must be given to 'wake-up' the device.
9. Self Refresh Exit is a synchronous operation and begins on the 2nd positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to  $t_{RC}$  is satisfied once the Self Refresh Exit command is registered.
10. Referenced to the time which the output achieves the open circuit condition, not to output voltage levels.
11.  $t_{DAL}$  is equivalent to  $t_{DPL} + t_{RP}$ .

A serial presence detect storage device - E<sup>2</sup>PROM - is assembled onto the module. Information about the module configuration, speed, etc. is written into the E<sup>2</sup>PROM device during module production using a serial presence detect protocol (I<sup>2</sup>C synchronous 2-wire bus)

### SPD-Table:

Byte#	Description	SPD Entry Value	Hex			
			2Mx64 -8	2Mx72 -8	4Mx64 -8	4Mx72 -8
0	Number of SPD bytes	128	80	80	80	80
1	Total bytes in Serial PD	256	08	08	08	08
2	Memory Type	SDRAM	04	04	04	04
3	Number of Row Addresses (without BS bits)	11	0B	0B	0B	0B
4	Number of Column Addresses (for x8 SDRAM)	9	09	09	09	09
5	Number of DIMM Banks	1 / 2	01	01	02	02
6	Module Data Width	64 / 72	40	48	40	48
7	Module Data Width (cont'd)	0	00	00	00	00
8	Module Interface Levels	LVTTTL	01	01	01	01
9	SDRAM Cycle Time at CL=3	10.0 ns	A0	A0	A0	A0
10	SDRAM Access time from Clock at CL=3	6.0 ns	60	60	60	60
11	Dimm Config (Error Det/Corr.)	none / ECC	00	02	00	02
12	Refresh Rate/Type	Self-Refresh, 15.6µs	80	80	80	80
13	SDRAM width, Primary	x8	08	08	08	08
14	Error Checking SDRAM data width	n/a / x8	00	08	00	08
15	Minimum clock delay for back-to-back random column address	t <sub>ccd</sub> = 1 CLK	01	01	01	01
16	Burst Length supported	1, 2, 4, 8 & full page	8F	8F	8F	8F
17	Number of SDRAM banks	2	02	02	02	02
18	Supported CAS Latencies	CAS lat. = 2 & 3	06	06	06	06
19	CS Latencies	CS latency = 0	01	01	01	01
20	WE Latencies	Write latency = 0	01	01	01	01
21	SDRAM DIMM module attributes	non buffered/non reg.	00	00	00	00
22	SDRAM Device Attributes :General	Vcc tol +/- 10%	06	06	06	06
23	Min. Clock Cycle Time at CAS Latency = 2	10.0 ns	A0	A0	A0	A0
24	Max. data access time from Clock for CL=2	6.0 ns	60	60	60	60
25	Minimum Clock Cycle Time at CL = 1	not supported	FF	FF	FF	FF
26	Maximum Data Access Time from Clock at CL=1	not supported	FF	FF	FF	FF
27	Minimum Row Precharge Time	20 ns	14	14	14	14
28	Minimum Row Active to Row Active delay tRRD	16 ns	10	10	10	10

### SPD-Table (cont'd):

Byte#	Description	SPD Entry Value	Hex			
			2Mx64 -8	2Mx72 -8	4Mx64 -8	4Mx72 -8
29	Minimum RAS to CAS delay tRCD	20 ns	14	14	14	14
30	Minimum RAS pulse width tRAS	45 ns	2D	2D	2D	2D
31	Module Bank Density (per bank)	16 MByte	04	04	04	04
32	SDRAM input setup time	2 ns	20	20	20	20
33	SDRAM input hold time	1 ns	10	10	10	10
34	SDRAM data input setup time	2 ns	20	20	20	20
35	SDRAM data input hold time	1 ns	10	10	10	10
36-61	Superset information (may be used in future)		FF	FF	FF	FF
62	SPD Revision	Revision 1.2	12	12	12	12
63	Checksum for bytes 0 - 62		C9	DB	CA	DC
64-125	Manufacturers information (optional) (FFh if not used)		XX	XX	XX	XX
126	Frequency Specification	100 MHz	64	64	64	64
127	Details of 100 MHz Support		AF	AF	FF	FF
128+	Unused storage locations		FF	FF	FF	FF

SPD-Table:

Byte#	Description	SPD Entry Value	Hex			
			2Mx64 -8-3	2Mx72 -8-3	4Mx64 -8-3	4Mx72 -8-3
0	Number of SPD bytes	128	80	80	80	80
1	Total bytes in Serial PD	256	08	08	08	08
2	Memory Type	SDRAM	04	04	04	04
3	Number of Row Addresses (without BS bits)	11	0B	0B	0B	0B
4	Number of Column Addresses (for x8 SDRAM)	9	09	09	09	09
5	Number of DIMM Banks	1 / 2	01	01	02	02
6	Module Data Width	64 / 72	40	48	40	48
7	Module Data Width (cont'd)	0	00	00	00	00
8	Module Interface Levels	LVTTL	01	01	01	01
9	SDRAM Cycle Time at CL=3	10.0 ns	A0	A0	A0	A0
10	SDRAM Access time from Clock at CL=3	6.0 ns	60	60	60	60
11	Dimm Config (Error Det/Corr.)	none / ECC	00	02	00	02
12	Refresh Rate/Type	Self-Refresh, 15.6µs	80	80	80	80
13	SDRAM width, Primary	x8	08	08	08	08
14	Error Checking SDRAM data width	n/a / x8	00	08	00	08
15	Minimum clock delay for back-to-back random column address	t <sub>ccd</sub> = 1 CLK	01	01	01	01
16	Burst Length supported	1, 2, 4, 8 & full page	8F	8F	8F	8F
17	Number of SDRAM banks	2	02	02	02	02
18	Supported CAS Latencies	CAS lat. = 2 & 3	06	06	06	06
19	CS Latencies	CS latency = 0	01	01	01	01
20	WE Latencies	Write latency = 0	01	01	01	01
21	SDRAM DIMM module attributes	non buffered/non reg.	00	00	00	00
22	SDRAM Device Attributes :General	Vcc tol +/- 10%	06	06	06	06
23	Min. Clock Cycle Time at CAS Latency = 2	10.0 ns	A0	A0	A0	A0
24	Max. data access time from Clock for CL=2	7.0 ns	70	70	70	70
25	Minimum Clock Cycle Time at CL = 1	not supported	FF	FF	FF	FF
26	Maximum Data Access Time from Clock at CL=1	not supported	FF	FF	FF	FF
27	Minimum Row Precharge Time	30 ns	1E	1E	1E	1E
28	Minimum Row Active to Row Active delay tRRD	20 ns	14	14	14	14

### SPD-Table (cont'd):

Byte#	Description	SPD Entry Value	Hex			
			2Mx64 -8-3	2Mx72 -8-3	4Mx64 -8-3	4Mx72 -8-3
29	Minimum RAS to CAS delay tRCD	20 ns	14	14	14	14
30	Minimum RAS pulse width tRAS	45 ns	2D	2D	2D	2D
31	Module Bank Density (per bank)	16 MByte	04	04	04	04
32	SDRAM input setup time	2 ns	20	20	20	20
33	SDRAM input hold time	1 ns	10	10	10	10
34	SDRAM data input setup time	2 ns	20	20	20	20
35	SDRAM data input hold time	1 ns	10	10	10	10
36-61	Superset information (may be used in future)		FF	FF	FF	FF
62	SPD Revision	Revision 1.2	12	12	12	12
63	Checksum for bytes 0 - 62		E7	F9	E8	FA
64-125	Manufacturers information (optional) (FFh if not used)		XX	XX	XX	XX
126	Frequency Specification	100 MHz	64	64	64	64
127	Details of 100 MHz Support		AD	AD	FD	FD
128+	Unused storage locations		FF	FF	FF	FF

### SPD-Table:

Byte#	Description	SPD Entry Value	Hex			
			2Mx64 -10	2Mx72 -10	4Mx64 -10	4Mx72 -10
0	Number of SPD bytes	128	80	80	80	80
1	Total bytes in Serial PD	256	08	08	08	08
2	Memory Type	SDRAM	04	04	04	04
3	Number of Row Addresses (without BS bits)	11	0B	0B	0B	0B
4	Number of Column Addresses (for x8 SDRAM)	9	09	09	09	09
5	Number of DIMM Banks	1 / 2	01	01	02	02
6	Module Data Width	64 / 72	40	48	40	48
7	Module Data Width (cont'd)	0	00	00	00	00
8	Module Interface Levels	LVTTL	01	01	01	01
9	SDRAM Cycle Time at CL=3	10.0 ns	A0	A0	A0	A0
10	SDRAM Access time from Clock at CL=3	8.0 ns	80	80	80	80
11	Dimm Config (Error Det/Corr.)	none / ECC	00	02	00	02
12	Refresh Rate/Type	Self-Refresh, 15.6µs	80	80	80	80
13	SDRAM width, Primary	x8	08	08	08	08
14	Error Checking SDRAM data width	n/a / x8	00	08	00	08
15	Minimum clock delay for back-to-back random column address	t <sub>ccd</sub> = 1 CLK	01	01	01	01
16	Burst Length supported	1, 2, 4, 8 & full page	8F	8F	8F	8F
17	Number of SDRAM banks	2	02	02	02	02
18	Supported CAS Latencies	CAS lat. = 2 & 3	06	06	06	06
19	CS Latencies	CS latency = 0	01	01	01	01
20	WE Latencies	Write latency = 0	01	01	01	01
21	SDRAM DIMM module attributes	non buffered/non reg.	00	00	00	00
22	SDRAM Device Attributes :General	Vcc tol +/- 10%	06	06	06	06
23	Min. Clock Cycle Time at CAS Latency = 2	15.0 ns	F0	F0	F0	F0
24	Max. data access time from Clock for CL=2	9.0 ns	90	90	90	90
25	Minimum Clock Cycle Time at CL = 1	not supported	FF	FF	FF	FF
26	Maximum Data Access Time from Clock at CL=1	not supported	FF	FF	FF	FF
27	Minimum Row Precharge Time	30 ns	1E	1E	1E	1E
28	Minimum Row Active to Row Active delay tRRD	20 ns	14	14	14	14

### SPD-Table (cont'd):

Byte#	Description	SPD Entry Value	Hex			
			2Mx64 -10	2Mx72 -10	4Mx64 -10	4Mx72 -10
29	Minimum RAS to CAS delay tRCD	30 ns	1E	1E	1E	1E
30	Minimum RAS pulse width tRAS	45 ns	2D	2D	2D	2D
31	Module Bank Density (per bank)	16 MByte	04	04	04	04
32	SDRAM input setup time	3 ns	30	30	30	30
33	SDRAM input hold time	1 ns	10	10	10	10
34	SDRAM data input setup time	3 ns	30	30	30	30
35	SDRAM data input hold time	1 ns	10	10	10	10
36-61	Superset information (may be used in future)		FF	FF	FF	FF
62	SPD Revision	Revision 1.2	12	12	12	12
63	Checksum for bytes 0 - 62		A1	B3	A2	B4
64-125	Manufacturers information (optional) (FFh if not used)		XX	XX	XX	XX
126	Frequency Specification	66 MHz	66	66	66	66
127	Details		AF	AF	FF	FF
128+	Unused storage locations		FF	FF	FF	FF



