Integrated Circuit Systems, Inc.

ICS9250-33

Advance Information

Frequency Generator for Celeron/PIII™

Recommended Application:

Output Features:

- 4 Differential CPU Clock Pairs @ 3.3V
- 2 - 3V MREF clocks for memory reference seeds, (separate single ended but 180 degrees out of phase)
- 4 - 66MHz reference output
- 10 - 3V 33MHz PCI clocks
- 2 - 48MHz clocks
- 2 - 14.318 reference output

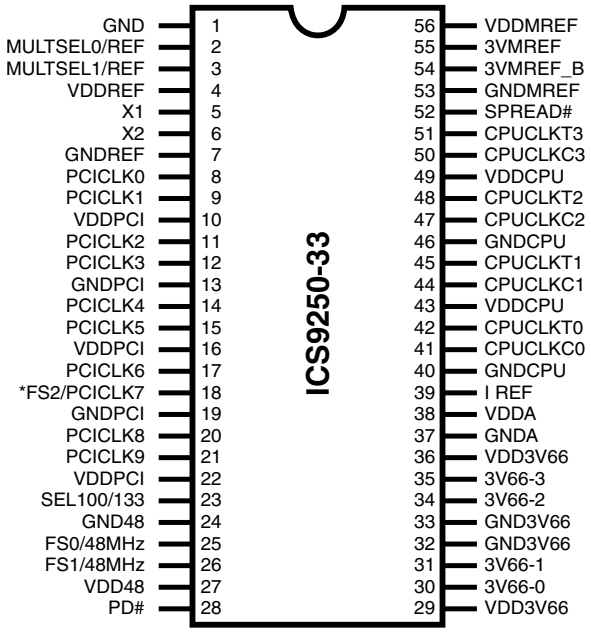
Features:

- Up to 156MHz frequency support
- Support power management: Power Down Mode
- Supports Spread Spectrum modulation: 0 to -0.5% down spread.
- Uses external 14.318MHz crystal
- Select logic for Differential Swing Control, Test mode, Tristate, Power down, Spread Spectrum, limited frequency select, selective clock enable.
- External resistor for current reference
- FS pins for frequency select

Key Specifications:

- 3V66 Output jitter <300ps
- CPU Output Jitter <200ps
- MREF Output jitter <250ps

Pin Configuration



56-Pin 300mil SSOP & TSSOP

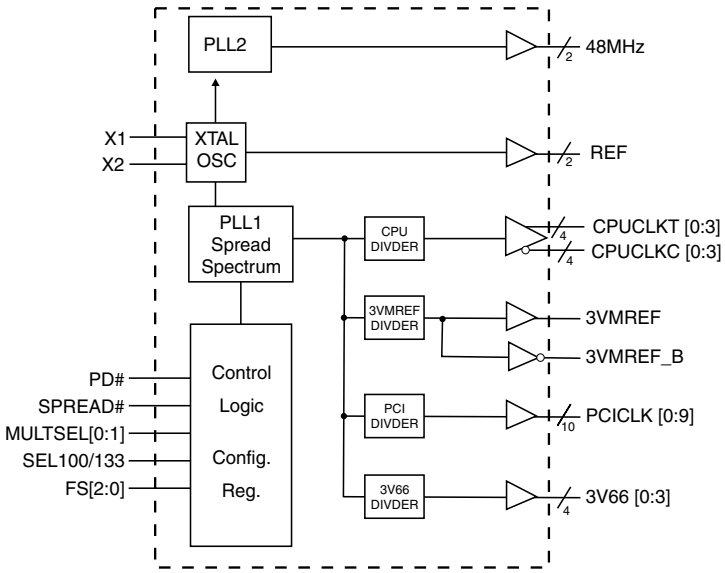
* This input has a 120K internal pull down to GND.

Functionality

SEL133/ 100	FS0	FS1	Function
0	0	0	Active 100MHz
0	0	1	105MHz
0	1	0	200MHz
0	1	1	Tristate all outputs
1	0	0	Active 133MHz
1	0	1	126MHz
1	1	0	200MHz
1	1	1	Test Mode

* FS2 = 1: Margin testing mode

Block Diagram



Power Groups

VDDREF, GNDREF= REF, X1, X2
VDDPCI, GNDPCI = PCICLK
VDD48, GND48 = 48MHz, PLL2
VDD3V66, GND3V66=3V66
VDDCPU, GNDCPU = CPUCLK
VDDMREF, GNDMREF=3VMREF, 3VMREF_B
VDDA=VDD (core supply voltage 3.3V)
GNDA=Ground for core supply

General Description

The **ICS9250-33** is a single chip clock solution, for multi processor server or high-end desktop applications.

Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The ICS9250-33 employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

Pin Configuration

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1, 7, 13, 19, 24, 32, 33, 37, 40, 46, 53	GND	PWR	Ground pins for 3.3V supply
2, 3	REF/MULTSEL [0:1]	IN	MULTSEL0 and MULTSEL1 inputs are sensed on power-up and then internally latched prior to the pin being used for output on 3V 14.318MHz clocks.
4, 10, 16, 22, 27, 29, 36, 38, 43, 49, 56	VDD	PWR	3.3V power supply
5	X1	X2 Crystal Input	14.318MHz Crystal input
6	X2	X1 Crystal Output	14.318MHz Crystal output
8, 9, 11, 12, 14, 15, 17, 20, 21	PCICLK [0:6][8:9]	OUT	PCI clock outputs
18	FS2[1]	IN	Margin testing frequency select pin
	PCICLK7	OUT	PCI clock output
23	SEL100/133	IN	CPU Frequency Select. Low=100MHz, High=133MHz
25, 26	FS [0:1]	IN	Frequency select pins
	48MHz	OUT	48MHz clock output
28	PD#	IN	Invokes power-down mode. Active Low.
30, 31, 34, 35	3V66 [0:3]	OUT	66MHz reference clocks
39	I REF	OUT	This pin establishes the reference current for the CPUCLK pairs. This pin takes a fixed precision resistor tied to ground in order to establish the required current.
42, 45, 48, 51	CPUCLKT [0:3]	OUT	"True" clocks of differential pair CPU outputs. These are current outputs and external resistors are required for voltage bias.
41, 44, 47, 50	CPUCLKC [0:3]	OUT	"Complementory" clocks of differential pair CPU outputs. These are current outputs and external resistors are required for voltage bias.
52	SPREAD#	IN	Invokes Spread Spectrum functionality on the Differential host clocks, MRef/MRef_b clocks, 66MHz clocks, and 33MHz PCI clocks. Active Low
54	3VMREF_B	OUT	3V reference to memory clock driver (out of phase with 3Vmref)
55	3VMREF	OUT	3V reference to memory clock driver

Note1: To ensure proper Intel defined frequency is used, an external 10K ohm pull down resistor is recommended

Truth Table

FS2	SEL 133/100	FS0	FS1	CPU	MRef	3V66	REF	Spread Percentage
0	0	0	0	100MHz	50MHz	66MHz	14.318MHz	0 to -0.5% Down Spread
0	0	0	1	105MHz	52.5MHz	70MHz	14.318MHz	0 to -0.5% Down Spread
0	0	1	0	200MHz	50MHz	66.7MHz	14.318MHz	0 to -0.5% Down Spread
0	0	1	1	Tristate	Tristate	Tristate	Tristate	0 to -0.5% Down Spread
0	1	0	0	133MHz	66MHz	66MHz	14.318MHz	0 to -0.5% Down Spread
0	1	0	1	126.7MHz	63.3MHz	63.3MHz	14.318MHz	0 to -0.5% Down Spread
0	1	1	0	200MHz	66.7MHz	66.7MHz	14.318MHz	0 to -0.5% Down Spread
0	1	1	1	TCLK/2	TCLK/4	TCLK	TCLK	0 to -0.5% Down Spread
1	0	0	0	100.50	50.25	67.00	14.318MHz	± 0.25% Center Spread
1	0	0	1	105.00	52.50	70.00	14.318MHz	± 0.25% Center Spread
1	0	1	0	110.00	55.00	73.34	14.318MHz	± 0.25% Center Spread
1	0	1	1	166.67	83.34	83.34	14.318MHz	± 0.25% Center Spread
1	1	0	0	133.73	66.86	66.86	14.318MHz	± 0.25% Center Spread
1	1	0	1	140.00	70.00	70.00	14.318MHz	± 0.25% Center Spread
1	1	1	0	146.66	73.33	73.33	14.318MHz	± 0.25% Center Spread
1	1	1	1	156.46	78.23	78.23	14.318MHz	± 0.25% Center Spread*

Note: * 48MHz will be at TCLK/2 frequency if entry 1111 is slected.

Group Offset Limits

Group	Offset	Measurement Loads (lumped)	Measure Points
CPU to 3V66	No Requirement		
CPU to PCI			
3V66 to PCI	1.5 - 3.5ns 3V66 leads	30pF	1.5V

CPUCLK Buffer Configuration

	Conditions	Configuration	Load	Min	Max
Iout	Vdd = nominal (3.30V)	All combinations of M0, M1 and Rr shown in table below	Nominal test load for given configuration	-7% I nominal	+7% I nominal
Iout	Vdd = 3.30 ± 5%	All combinations of M0, M1 and Rr shown in table below	Nominal test load for given configuration	-12% I nominal	+12% I nominal

CPUCLK Swing Select Functions

MULTSEL0	MULTSEL1	Board Target Trace/Term Z	Reference R, Iref= Vdd/(3*Rr)	Output Current	Voh @ Z, Iref=2.32mA
0	0	60 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 5*Iref	0.71V @ 60
0	0	50 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 5*Iref	0.59V @ 50
0	1	60 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 6*Iref	0.85V /2 60
0	1	50 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 6*Iref	0.71V @ 50
1	0	60 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 4*Iref	0.56V @ 60
1	0	50 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 4*Iref	0.47V @ 50
1	1	60 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 7*Iref	0.99V @ 60
1	1	50 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 7*Iref	0.82V @ 50
0	0	30 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 5*Iref	0.75V @ 30
0	0	25 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 5*Iref	0.62V @ 20
0	1	30 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 6*Iref	0.90V @ 30
0	1	25 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 6*Iref	0.75V @ 20
1	0	30 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 4*Iref	0.60 @ 20
1	0	25 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 4*Iref	0.5V @ 20
1	1	30 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 7*Iref	1.05V @ 30
1	1	25 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 7*Iref	0.84V @ 20

Absolute Maximum Ratings

Supply Voltage ..... 5.5 V
Logic Inputs ..... GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature ..... 0°C to +70°C
Case Temperature ..... 115°C
Storage Temperature ..... –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V ±5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	$V_{IN} = V_{DD}$	-5		5	µA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			µA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			µA
Operating Supply Current	$I_{DD3.3OP}$	C_L = 0 pF; Select @ 66M			100	mA
Power Down Supply Current	$I_{DD3.3PD}$	C_L = 0 pF; With input address to Vdd or GND			600	µA
Input frequency	F_i	V_{DD} = 3.3 V;				MHz
Pin Inductance	L_{pin}				7	nH
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{out}	Out put pin capacitance			6	pF
	C_{INX}	X1 & X2 pins	27		45	pF
Transition Time[1]	T_{trans}	To 1st crossing of target Freq.			3	mS
Settling Time[1]	T_s	From 1st crossing to 1% target Freq.			3	mS
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			3	mS
Delay	t_{PZH},t_{PZH}	output enable delay (all outputs)	1		10	nS
	t_{PLZ},t_{PZH}	output disable delay (all outputs)	1		10	nS

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - CPU

T_A = 0 - 70C, V_{DDL} = 2.5 V +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP2B}[1]	$V_O = V_{DD}*(0.5)$	13.5		45	Ω
Output Impedance	R_{DSN2B}[1]	$V_O = V_{DD}*(0.5)$	13.5		45	Ω
Output High Voltage	V_{OH2B}	I_{OH} = -1 mA	2			V
Output Low Voltage	V_{OL2B}	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH2B}[2]	$V_{OH@MIN}$ = 1.0V , $V_{OH@MAX}$ = 2.375V	-27		-27	mA
Output Low Current	I_{OL2B}[2]	$V_{OL@MIN}$ = 1.2V , $V_{OL@MAX}$ = 0.3V	27		30	mA
Rise Time	t_{r2B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V	0.4		1.6	ns
Fall Time	t_{f2B}[1]	V_{OH} = 0.4 V, V_{OL} = 2.0 V	0.4		1.6	ns
Duty Cycle	d_{t2B}[1]	V_T = 1.25 V	45		55	%
Skew	t_{sk2B}[1]	V_T = 1.25 V			100	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.25 V			150	ps

[1]Guarenteed by design, not 100% tested in production.

[2] I_{OWT} can be varied and is selectable thru the MULTSEL pin.

Electrical Characteristics - REF

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L =10-20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{OI}					MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	20		60	Ω
Output High Voltage	V_{OH1}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH1}	VOH@ MIN = 1.0 V, VOH@ MAX = 3.135 V	-29		-23	mA
Output Low Current	I_{OL1}	VOL@ MIN = 1.95 V, VOL@ MAX= 0.4	29		27	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1		4	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1		4	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45		55	%
Skew	t_{sk1}[1]	V_T = 1.5 V			N/A	ps
Jitter	$t_{jcyc-cyc}$	V_T = 1.5 V			1000	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - MREF/MREF_B

T_A = 0 - 70C; V_{DD} = 3.3 V ± 5%; C_L =10-20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}					MHz
Output Impedance	R_{DSP1} [1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH1}	VOH@ MIN = 1.0 V, VOH@ MAX = 3.135 V	-33		-33	mA
Output Low Current	I_{OL1}	VOL@ MIN = 1.95 V, VOL@ MAX= 0.4	30		38	mA
Rise Time	t_{r1} [1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns
Fall Time	t_{f1} [1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns
Duty Cycle	d_{t1} [1]	V_T = 1.5 V	45		55	%
Skew	t_{sk1} [1]	V_T = 1.5 V			N/A	ps
Jitter	$t_{jcyc-cyc}$	V_T = 1.5 V			250	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - 3V66

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L =10-30 pF (unless otherwise stated)

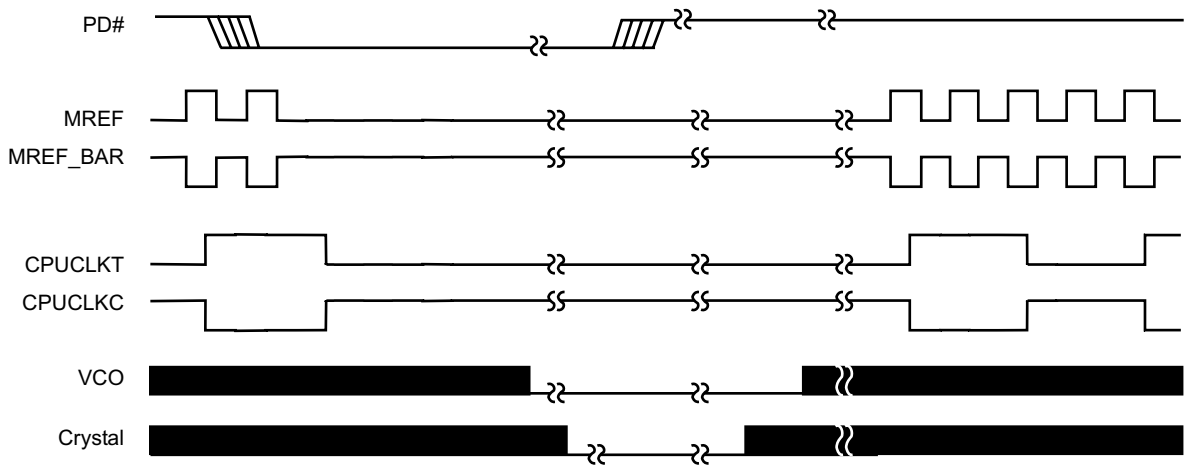
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}					MHz
Output Impedance	R_{DSP1} [1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH1}	VOH@ MIN = 1.0 V, VOH@ MAX = 3.135 V	-33		-33	mA
Output Low Current	I_{OL1}	VOL@ MIN = 1.95 V, VOL@ MAX= 0.4	30		38	mA
Rise Time	t_{r1} [1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns
Fall Time	t_{f1} [1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns
Duty Cycle	d_{t1} [1]	V_T = 1.5 V	45		55	%
Skew	t_{sk1} [1]	V_T = 1.5 V			250	ps
Jitter	$t_{jcyc-cyc}$	V_T = 1.5 V			300	ps

[1]Guarenteed by design, not 100% tested in production.

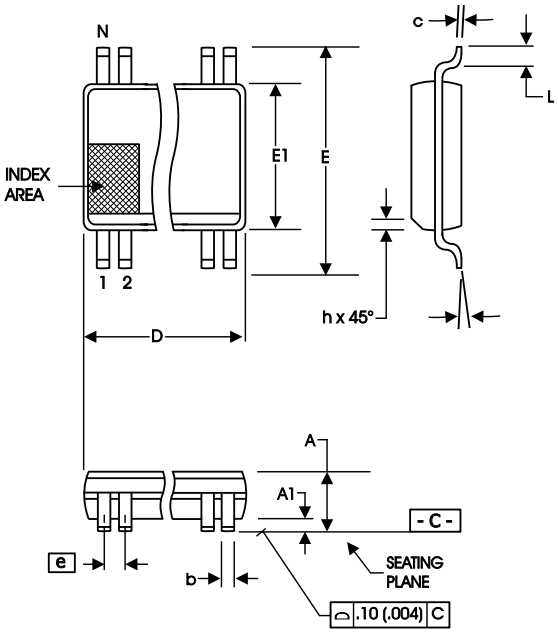
PD# Timing Diagram

The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal needs to be synchronized internal to the device prior to powering down the clock synthesizer.

Internal clocks are not running after the device is put in power down. When PD# is active low all clocks need to be driven to a low value and held prior to turning off the VCOs and crystal. The power up latency needs to be less than 3 mS. The power down latency should be as short as possible but conforming to the sequence requirements shown below.



Notes:
1. As shown, the outputs Stop Low on the next falling edge after PD# goes low.
2. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside this part.
3. The shaded sections on the VCO and the Crystal signals indicate an active clock.



300 mil SSOP Package

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	18.31	18.55	.720	.730

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

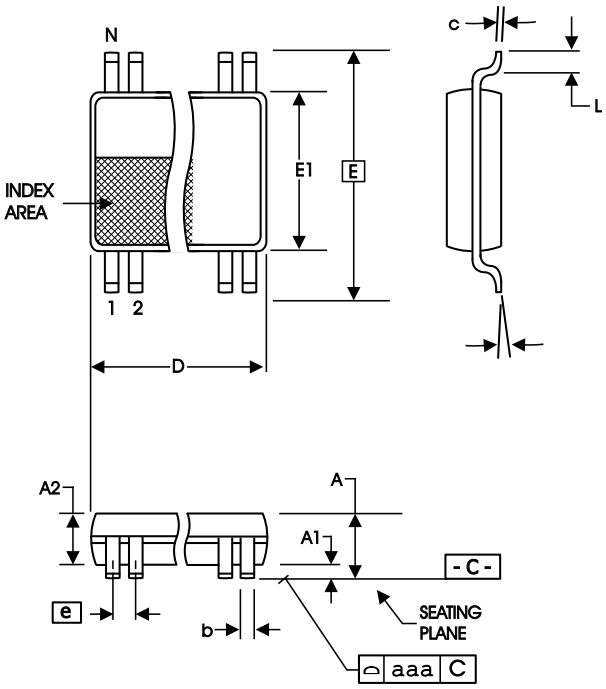
Ordering Information

ICS9250yF-33-T

Example:

ICS XXXX y F - PPP - T

- **Designation for tape and reel packaging**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  F=SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS, AV = Standard Device



6.10 mm. Body, 0.50 mm. pitch TSSOP
(240 mil) (0.020 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	13.90	14.10	.547	.555

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

Ordering Information

ICS9250yG-33-T

Example:

ICS XXXX y G - PPP - T

- **Designation for tape and reel packaging**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  G=TSSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS, AV = Standard Device