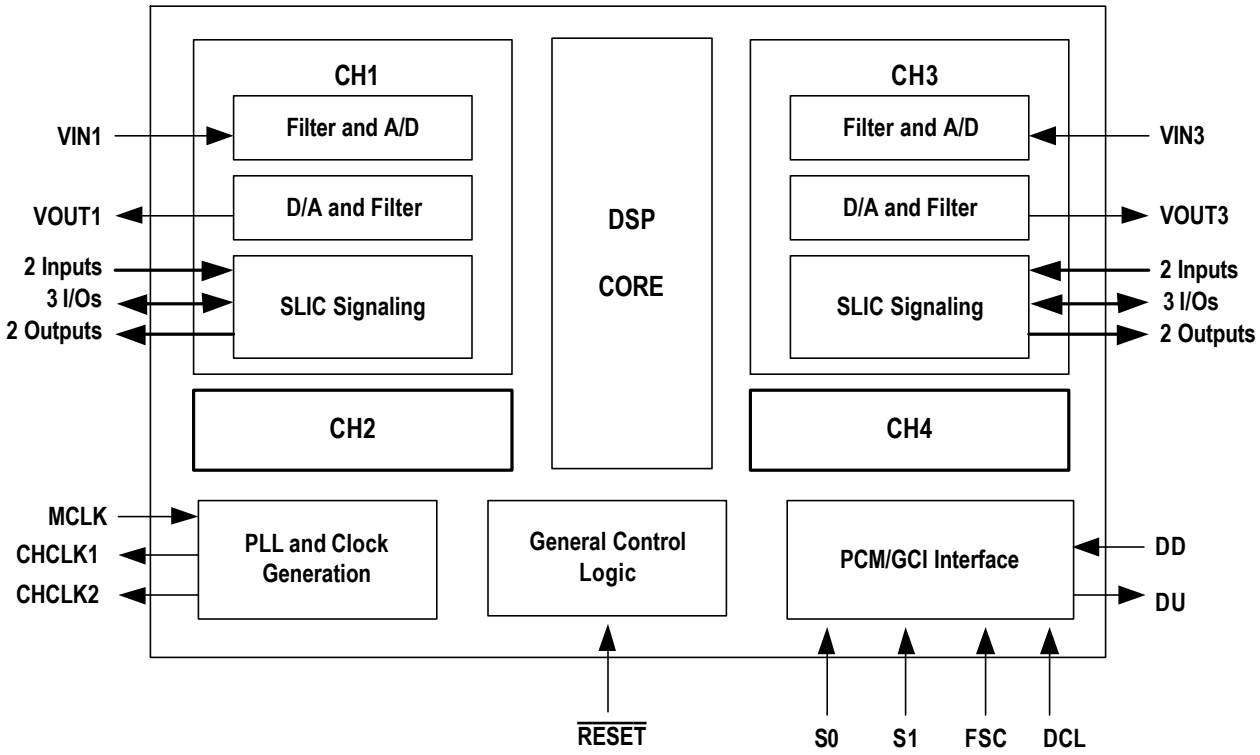
QUAD PROGRAMMABLE PCM CODEC WITH GCI INTERFACE

IDT821064

FEATURES

- 4 channel CODEC with on-chip digital filters
- Software selectable compressed (A/μ-law) or linear code conversion
- Meets ITU-T G.711 - G.714 requirements
- Programmable digital filter adapting to system demands:
  - *AC impedance matching*
  - *Transhybrid balance*
  - *Frequency response correction*
  - *Gain setting*
- GCI (IOM-2) control interface
- Broadcast mode for coefficient setting
- 7 SLIC signaling pins (including 2 debounced pins) per channel
- Fast hardware ring trip mechanism
- Two programmable tone generators per channel for testing, ringing and DTMF generation
- FSK generator
- Two programmable chopper clocks
- Master clock frequency selectable: 2.048 MHz or 4.096 MHz
- Advanced test capabilities
  - *3 analog loop back tests*
  - *5 digital loop back tests*
  - *Level metering function*
- High analog driving capability (300Ω AC)
- TTL and CMOS compatible digital I/O
- CODEC identification
- +5 V single power supply
- Low power consumption
- Operating temperature range: -40 °C to +85 °C
- Package available: 64 pin PQFP

FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION

The IDT821064 is a feature rich, single-chip, programmable 4 channel PCM CODEC with on-chip filters. Besides the μ-Law/A-Law companding and linear coding/decoding (14 effective bits + 2 extra sign bits), IDT821064 also provides 1 FSK generator (can be used for sending Caller-ID messages), 2 programmable Tone generators per channel (which can also generate ring signals) together with 2 programmable chopper clocks for SLIC.

The digital filters in IDT821064 provide the necessary transmit and receive filtering for voice telephone circuit to interface with time-division multiplexed systems. An integrated programmable DSP realizes AC Impedance Matching, Transhybrid Balance, Frequency Response Correction and Gain Setting functions. The device also provides 7 signaling pins to SLIC on per channel basis.

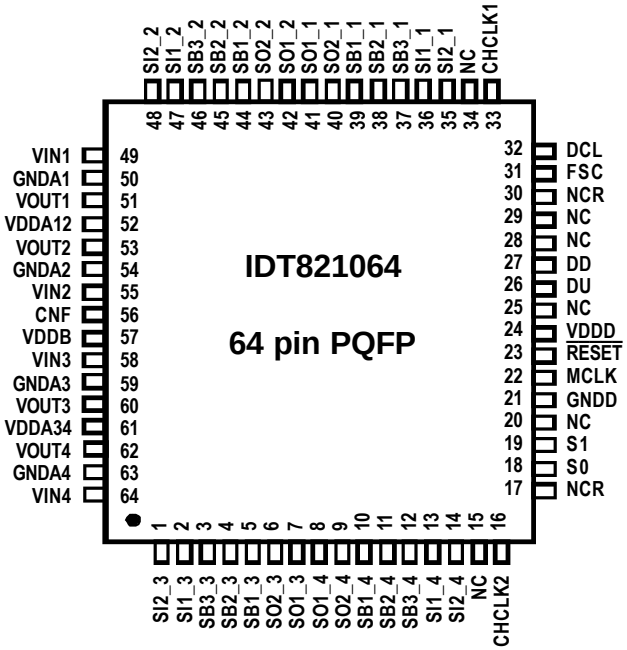
The IDT821064 has a General Control Interface (GCI), which is also known as ISDN Oriented Module (IOM®-2). The IDT821064 supports both compressed and linear data format. This function provides convenience for the VoXXX applications.

The device also offers strong test capability with several analog/digital loopbacks and level metering function. It brings convenience to system maintenance and diagnosis.

A unique feature of 'Hardware Ring Trip' is implemented in IDT821064. When off-hook signal is detected, IDT821064 can reverse an output pin to stop ringing immediately.

The IDT821064 can be used in Integrated Access Devices (IADs), i.e. VoIP and VoDSL.

PIN CONFIGURATIONS



IOM®-2 is a registered trademark of Siemens AG.

PIN DESCRIPTION

Name	Type	Pin Number	Description
GNDA1 GNDA2 GNDA3 GNDA4	P	50 54 59 63	**Analog Ground.** All ground pins should be connected together.
GNDD	P	21	**Digital Ground.** All digital signals are referred to this pin.
VDDA12 VDDA34	P	52 61	**+5V Analog Power Supply.** These pins should be connected to ground via a 0.1μF capacitor. All power supply pins should be connected together.
VDDD	P	24	**+5V Digital Power Supply.**
VDDB	P	57	**+5V Analog Power Supply.** This pin should be connected to ground via a 0.1μF capacitor. All power supply pins should be connected together.
CNF	-	56	**Capacitor Noise Filter** This pin should be connected to ground via a 0.22μF capacitor.
VIN1-4	I	49, 55, 58, 64	**Analog Voice Inputs.** These pins should be connected to the SLIC via a capacitor (0.22 μF).
VOUT1-4	O	51, 53, 60, 62	**Voice Frequency Receiver Outputs.** These pins can drive 300 Ω AC load. They can drive transformers directly.
SI1_(1-4) SI2_(1-4)	I	36, 47, 2, 13 35, 48, 1, 14	**SLIC signalling Inputs with debounced function for Channel 1-4.**
SB1_(1-4) SB2_(1-4) SB3_(1-4)	I/O	39, 44, 5, 10 38, 45, 4, 11 37, 46, 3, 12	**Bi-directional SLIC Signalling I/Os for Channel 1-4, can be programmed as Input or Output.**
SO1_(1-4) SO2_(1-4)	O	41, 42, 7, 8 40, 43, 6, 9	**SLIC Signalling Outputs for Channel 1-4.**
DU	O	26	**GCI Data Upstream** GCI data is serially transmitted to this pin for all 4 channels of IDT821064.
DD	I	27	**GCI Data Downstream** GCI data is received serially from this pin for all 4 channels of IDT821064.
FSC	I	31	**Frame Sync.** FSC is an 8 kHz signal that identifies the beginning of Timeslot 0 in the GCI frame.
DCL	I	32	**Data Clock.** The data clock is either 2.048 MHz or 4.096 MHz, which is determined automatically by IDT821064.
S0 S1	I	18 19	**Time Slot Select** These pins are used to select one of the four time slot positions for Voice channels, Monitor and C/I channels.
MCLK	I	22	**Master Clock Input.** Master clock provides the clock for DSP. It can be 2.048 MHz or 4.096 MHz, which is determined automatically by IDT821064. It is recommended to connect MCLK pin and DCL pin together.
$\overline{\text{RESET}}$	I	23	**Reset Input.** Forces the device to default state. Active low.
CHCLK1	O	33	**Chopper Clock Output.** Provides a programmable (2 -28 ms) output signal synchronous to MCLK.
CHCLK2	O	16	**Chopper Clock Output.** Provides a programmable 256 kHz, or 512 kHz or 16.384 MHz output signal synchronous to MCLK
NCR		17,30	Recommend to be connected to GNDD.
NC		15,20,25 28,29,34	No connection

FUNCTIONAL DESCRIPTION

The IDT821064 is a four-channel PCM CODEC with on-chip digital filters. It provides the four-wire solution for the subscriber line circuitry in digital switches. The IDT821064 converts analog voice signals to digital PCM samples and digital PCM samples back to analog voice signals. Digital filters are used to bandlimit the voice signals during conversion. High performance oversampling Analog-to-Digital Converters (ADC) and Digital-to-Analog Converters (DAC) in the IDT821064 provide the required conversion accuracy. The associated decimation and interpolation filters are realized with both dedicated hardware and Digital Signal Processor (DSP). The DSP also handles all other necessary functions such as PCM bandpass filtering, sample rate conversion and PCM companding. See the Functional Block Diagram.

In the transmit path, the analog voice signal input from VIN pin is converted to PCM code by ADC, DSP and PCM companding circuits. Band-limiting functions as specified in ITU-T are implemented by digital filters. At last the fully processed signal is transferred to the GCI interface, in a compressed or linear signal presentation.

In the receive path, the digital signal is received via the GCI interface. Then it is expanded and sent to the DSP for interpolation and receive channel filtering function. The filtered signal is then sent to an oversampling DAC. The DAC output is post-filtered and then delivered at VOUT pin by a power amplifier. The amplifier can drive resistive load higher than 300 Ω AC.

GCI INTERFACE

The General Control Interface (GCI) provides communication of both control and voice data between the GCI highway and SLIC over a pair of pins on the IDT821064. The IDT821064 sends Data Upstream out of the DU pin and receives Data Downstream on the DD pin. DCL and FS are two input clock signals providing Data Clock (DCL) and Frame Synchronization (FS) information for the device. A complete GCI frame is sent upstream on DU pin and received downstream on DD pin every 125 μs.

The Frame Sync (FSC) pulse identifies the beginning of the Transmit and Receive frames and all GCI time slots are referenced to it. The Data Clock (DCL) is either 2.048 MHz or 4.096MHz, the internal circuit of IDT821064 monitors this input to determine which frequency is being used. The internal timing will be adjusted according to the DCL frequency so that DU and DD operate at 2M rate.

IDT821064 allows both compressed and linear data format coding/ decoding. VDS bit in Global Regiser 5 makes the selection of voice data format.

COMPRESSED GCI MODE

In GCI compressed mode, one GCI frame consists of 8 GCI time slots, the Data Upstream Interface transmits four 8-bit bytes per GCI time slot. They are:

- Two voice data bytes from the A-law or μ-law compressor for two different channel, for easy description, we name the two channels as channel A and channel B. The compressed voice data bytes for channel A and B are 8-bit wide;
- One Monitor channel byte, which is used for reading control data from the device for Channel A and B;
- One C/I channel byte, which contains a 6 bit width C/I channel sub-byte together with an MX bit and an MR bit. All real time signaling information is carried on the C/I channel sub-byte. The MX (Monitor Transmit) bit and MR (Monitor Receive) bit are used for handshaking functions for Channel A and B. Both MX and MR are active low.

Transmit logic controls the transmission of data onto the GCI bus.

The data structure of the Data Downstream is as same as that of Upstream. The Data Downstream Interface logic controls the reception of data bytes from the GCI bus. The two compressed voice channel data bytes of the GCI time slot are transferred to the A-law or μ-law expansion logic circuit. The expanded data is passed to the receive path of the signal processor. The Monitor Channel and C/I Channel bytes are transferred to the GCI control logic for processing.

Figure 1 shows the overall compressed GCI frame structure.

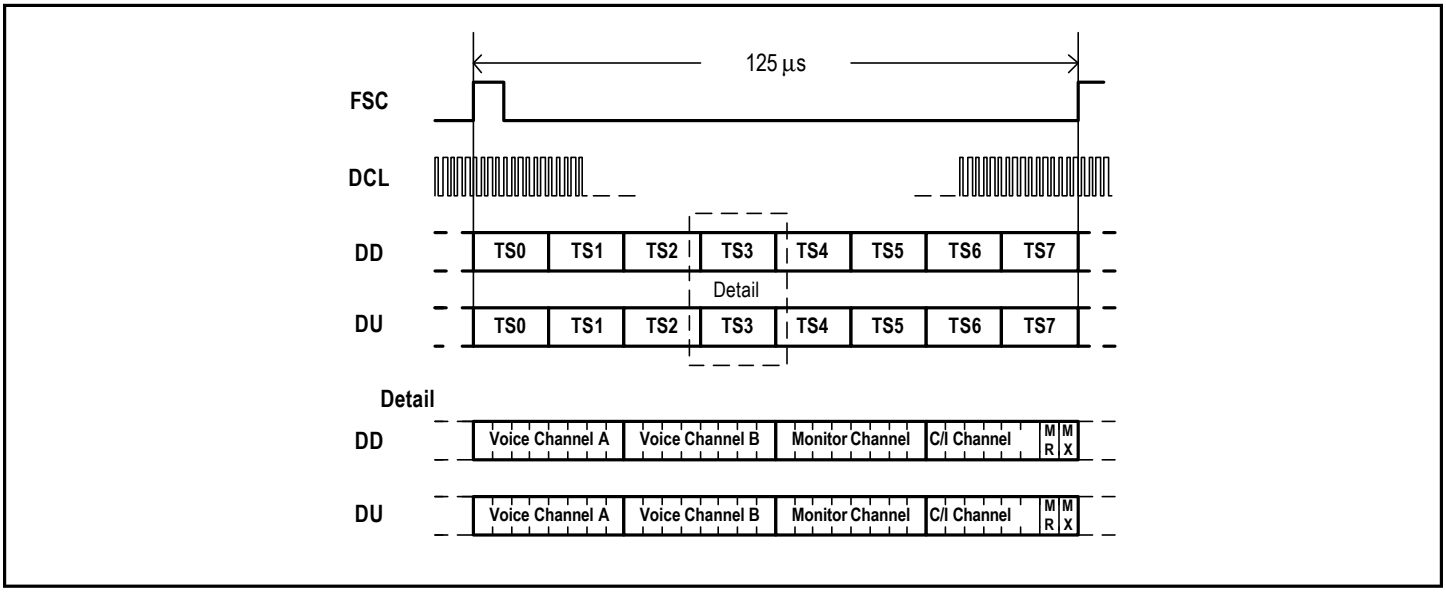


Figure 1. Compressed GCI Frame Structure

Table 1 - Time Slot Selection for Compressed GCI

IDT821064 Channels	S1=0,S0=0		S1=0,S0=1		S1=1,S0=0		S1=1,S0=1	
	Time Slot	Voice Channel	Time Slot	Voice Channel	Time Slot	Voice Channel	Time Slot	Voice Channel
1	Time slot 0	A	Time slot 2	A	Time slot 4	A	Time slot 6	A
2	Time slot 0	B	Time slot 2	B	Time slot 4	B	Time slot 6	B
3	Time slot 1	A	Time slot 3	A	Time slot 5	A	Time slot 7	A
4	Time slot 1	B	Time slot 3	B	Time slot 5	B	Time slot 7	B

In compressed operation, two GCI time slots are required to access the four channels of IDT821064. The GCI time slot assignment is determined by S1 and S0 as shown in Table 1.

LINEAR GCI MODE

In GCI linear mode, one GCI frame consists of 8 GCI time slots, each GCI time slot consists of four 8-bits bytes. Four of the 8 GCI time slots are used as Monitor Channel and C/I octet, they have a common data structure:

- Two don't_care bytes.
- One Monitor Channel byte, which is used for reading/writing control data/coefficients from/to the device for Channel A and B.
- One C/I byte, which contains a 6 bit width C/I channel sub-byte together with an MX bit and an MR bit. All real time signaling information is carried on the C/I channel sub-byte. The MX (Monitor Transmit) bit and MR (Monitor Receive) bit are used for handshaking functions for Channel A and B. Both MX and MR bits are active low .

Other four GCI time slots are used for linear voice data (a 16-bit 2's complement number, b15 and b14 are the same as b13, which is the sign bit, b13 to b0 are effective bits). Each GCI time slot consists of two 16-bit linear voice data bytes: one byte contains the linear voice data for Channel A, the other byte contains the linear voice data for Channel B.

The GCI time slot assignment is determined by S1 and S0 pin. When S0 and S1 are both low, the linear GCI Frame Structure is shown in Figure 2.

In linear operation, because one chip of the four-channel IDT821064 occupies four GCI time slots (two for voice data and two for C/I and monitor), the rest four GCI time slots can be used by other device. There are four locations in the 8-time-slots GCI bus for one IDT821064 to select, see Table 2.

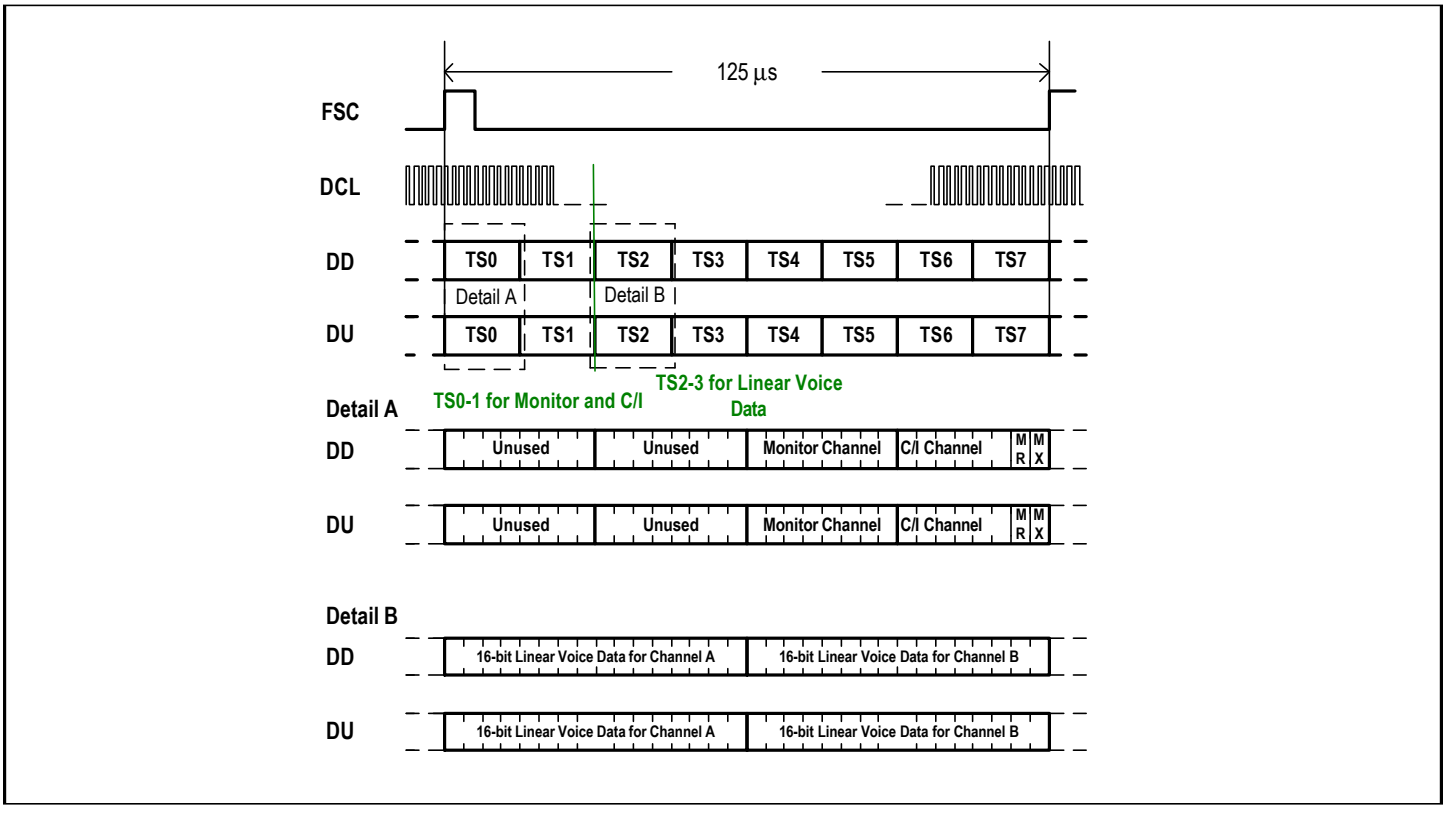


Figure 2. Linear GCI Frame Structure

Table 2 - Time Slot Selection for Linear GCI

IDT821064 Channels	S1 = 0, S0= 0				S1 = 0, S0= 1			
	Time Slot	Monitor and C/I	Time Slot	Voice Channel	Time Slot	Monitor and C/I	Time Slot	Voice Channel
1	Time slot 0	A	Time slot 2	A	Time slot 2	A	Timeslot4	A
2	Time slot 0	B	Time slot 2	B	Time slot 2	B	Timeslot4	B
3	Time slot 1	A	Time slot 3	A	Time slot 3	A	Timeslot5	A
4	Time slot 1	B	Time slot 3	B	Time slot 3	B	Timeslot5	B
	S1 = 1, S0= 0				S1 = 1, S0= 1			
	Time Slot	Monitor and C/I	Time Slot	Voice Channel	Time Slot	Monitor and C/I	Time Slot	Voice Channel
1	Time slot 4	A	Time slot 6	A	Time slot 6	A	Time slot 0	A
2	Time slot 4	B	Time slot 6	B	Time slot 6	B	Time slot 0	B
3	Time slot 5	A	Time slot 7	A	Time slot 7	A	Time slot 1	A
4	Time slot 5	B	Time slot 7	B	Time slot 7	B	Time slot 1	B

C/I CHANNEL

In both compressed GCI and linear GCI mode, the upstream and downstream C/I channel bytes are continuously carrying I/O information every frame to and from the IDT821064. In this way, the upstream processor can have an immediate access to SLIC output data present on IDT821064's programmable I/O port through downstream C/I channel, as well as to SLIC input data through upstream C/I channel. The IDT821064 transmits or receives the C/I channel data with the Most Significant Bit first.

The MR and MX bits are used for handshaking during data exchanges on the monitor channel.

Upstream C/I Channel

The C/I Channel which includes six C/I channel bits, is transmitted upstream by the IDT821064 every frame. The bit definitions for the upstream C/I channel are shown below.

Upstream C/I Octet

MSB LSB

b7	b6	b5	b4	b3	b2	b1	b0
SI1(A)	SI2(A)	SB1(A)	SI1(B)	SI2(B)	SB1(B)	MR	MX

The logic state of input ports SI1 and SI2 for channel A and channel B, as well as the bidirectional port SB1 for channel A and B if SB1 is programmed as an input, are read and transmitted in the upstream C/I channel. When SB2 and SB3 are programmed as inputs, their data are not available in upstream C/I channel and can be read by Global Command 9 and 10 only.

Downstream C/I Channel

The downstream C/I octet is defined as:

Downstream C/I Octet

MSB LSB

b7	b6	b5	b4	b3	b2	b1	b0
$\overline{A}$/B	SO2	SO1	SB3	SB2	SB1	MR	MX

where, $\overline{A}$/B selects channel A or Channel B:

$\overline{A}$/B = 0: Channel A is selected; $\overline{A}$/B = 1: Channel B is selected.

The downstream C/I channel carries the SLIC output data bits of SO1 and SO2 for channel A or B, as well as SB1, SB2 and SB3 output bits if SB1, SB2 and SB3 are programmed as outputs.

MONITOR CHANNEL

The monitor channel is used to read and write the internal global/local registers and coefficient/FSK RAM of the IDT821064, or to provide SLIC signaling. Using two monitor control bits (MR and MX) per direction, data is transferred between the upstream and downstream devices in a complete handshake procedure. The MR and MX bits are contained in the C/I channel byte of the GCI frame. See Figure 3.

The monitor channel transmission operates on a pseudo-asynchronous basis:

- Data transfer (bits) on the bus is synchronized to FSC;

- Data flow (bytes) are asynchronously controlled by the handshake procedure.

For example: Data is placed onto the DD Monitor Channel by the Monitor Transmitter of the master device (DD MX bit is activated and set to '0'). This data transfer will be repeated within each frame (125 µs rate) until it is acknowledged by the IDT821064 Monitor Receiver by setting the DU MR bit to '0', which is checked by the Master Transmitter of the master device. Thus, the data rate is not 8-kbytes/sec.

Monitor Handshake

The monitor channel works in 3 states:

I. Idle state: A pair of inactive (high) MR and MX bits during two or more consecutive frames shows an idle state on the monitor channel and the End of Message (EOM);

II. Sending state: MX bit is activated (low) by the Monitor Transmitter, together with data-bytes (can be changed) on the monitor channel;

III. Acknowledging: MR bit is set to active (low) by the Monitor Receiver, together with a data byte remaining in the monitor channel.

A start of transmission is initiated by a monitor transmitter by sending out an active MX bit together with the first byte of data to be transmitted in the monitor channel. This state remains until the addressed monitor receiver acknowledges the receipt of data by sending out an active low MR bit. The data transmission is repeated each 125 µs frame (minimum is one repetition). During this time the Monitor Transmitter keeps evaluating the MR bit.

Flow control, means in the form of transmission delay, can only take place when the transmitters MX and the receivers MR bit are in active state.

Since the receiver is able to receive the monitor data at least twice (in

two consecutive frames), it is able to check for data errors. If two different bytes are received the receiver will wait for the receipt of two identical successive bytes (last look function).

A collision resolution mechanism (check if another device is trying to send data during the same time) is implemented in the transmitter. This is done by looking for the inactive ('1') phase of the MX bit and making a per bit collision check on the transmitted monitor data (check if transmitted '1's are on DU/DD line; DU/DD line are open drain lines).

Any abort leads to a reset of the IDT821064 command stack, the device is ready to receive new commands.

To obtain a maximum speed data transfer, the transmitter anticipates the falling edge of the receivers acknowledgment.

Due to the inherent programming structure, duplex operation is not possible. It is not allowed to send any data to the IDT821064, while transmission is active.

Refer to Figure 4 and 5 for more information about monitor handshake procedure.

The IDT821064 can be controlled very flexibly by commands operating on registers or RAM via the GCI monitor channel, refer to "Programming Description" for further details.

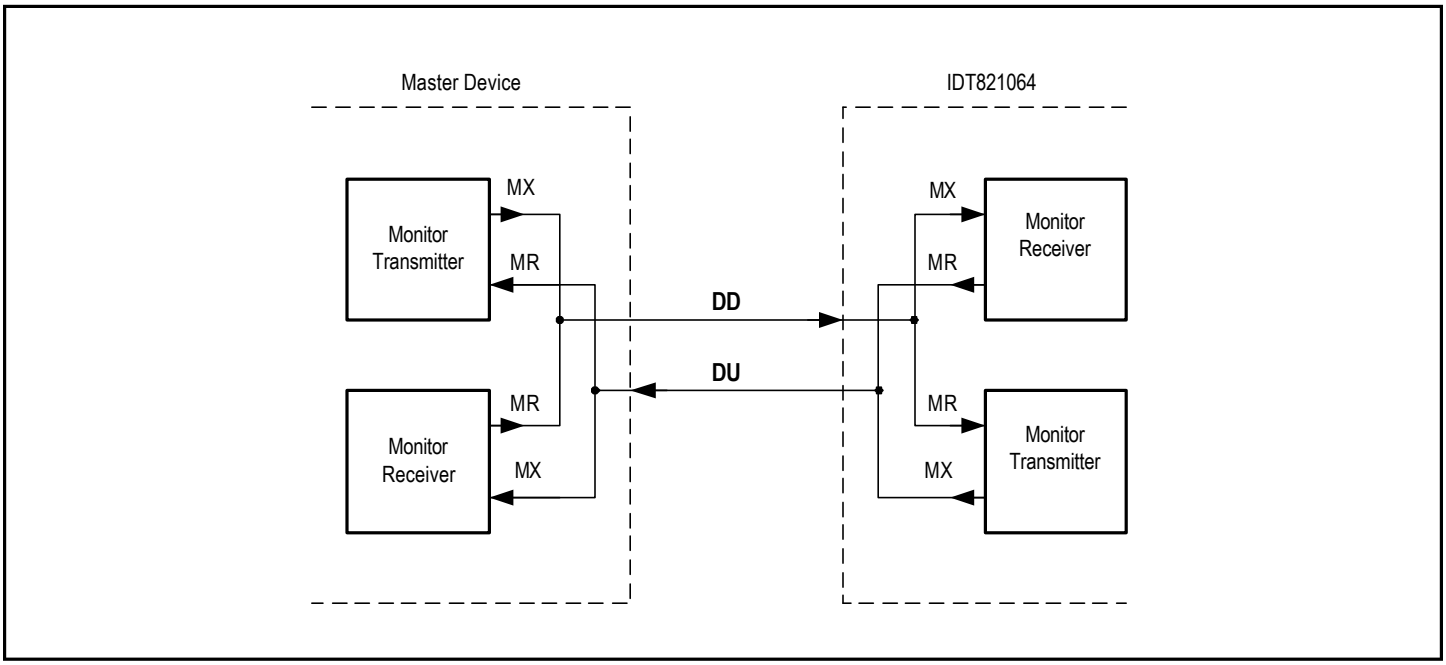


Figure 3. Monitor Channel Operation

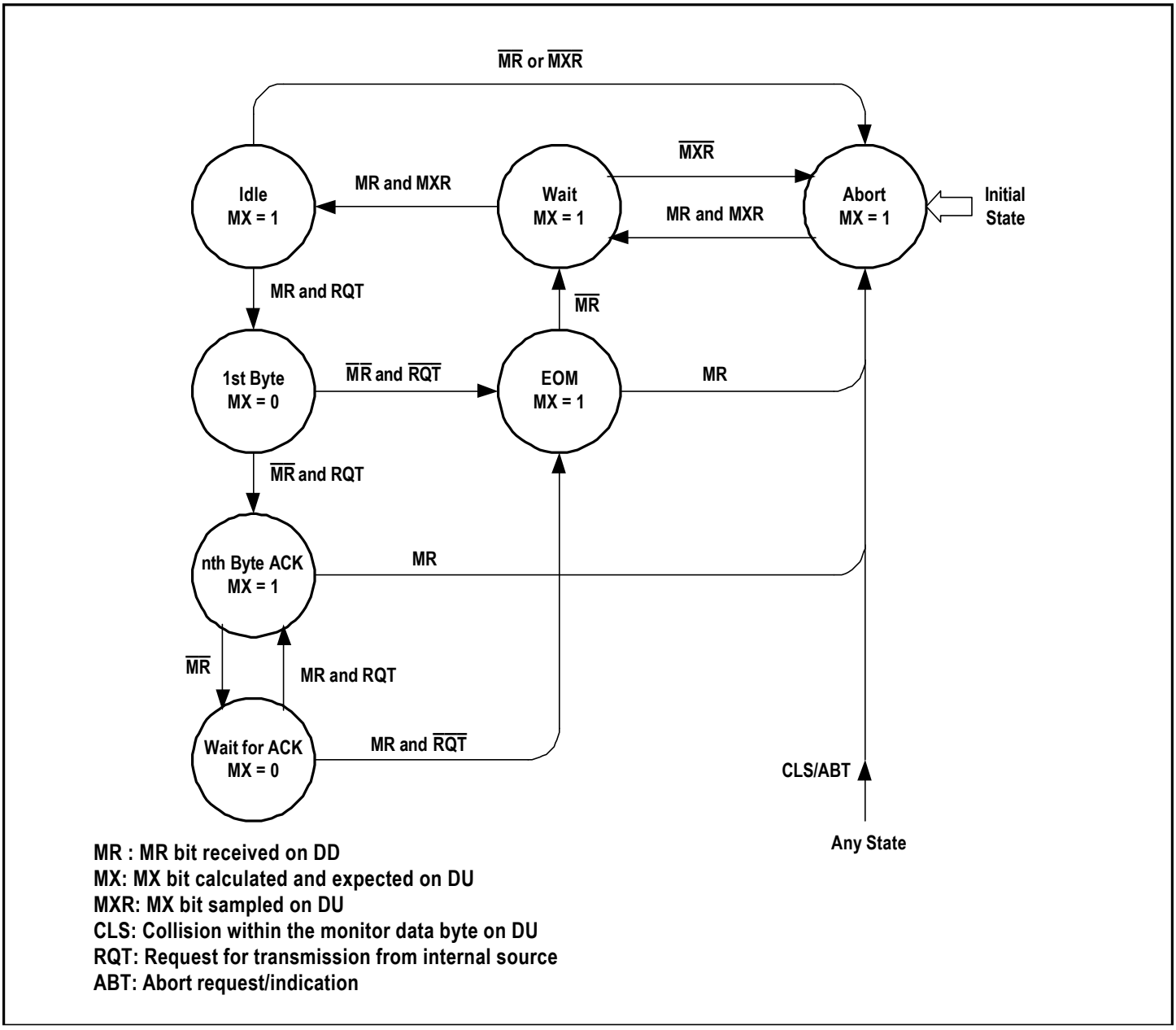
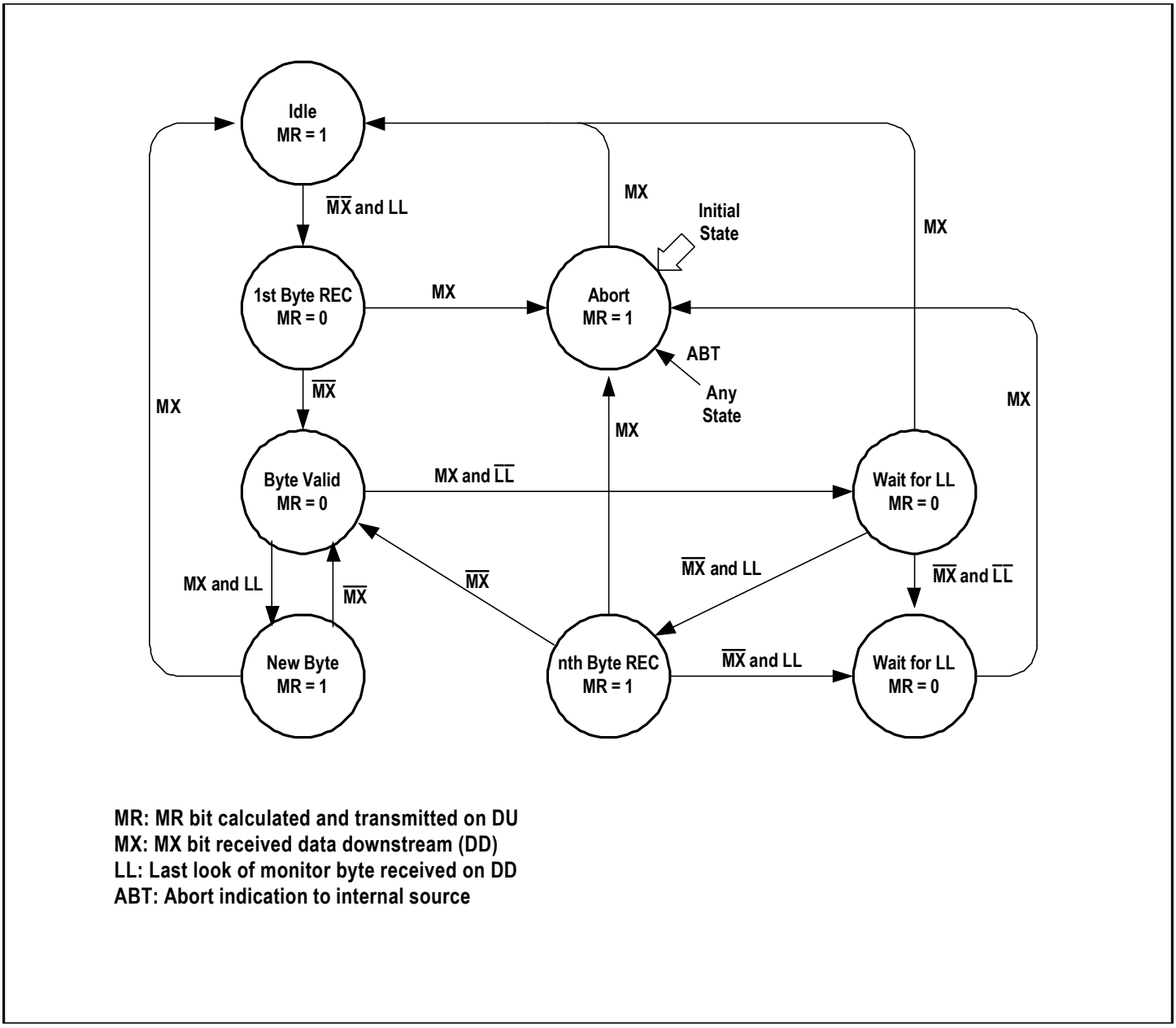


Figure 4. State Diagram of Monitor Transmitter



MR: MR bit calculated and transmitted on DU
MX: MX bit received data downstream (DD)
LL: Last look of monitor byte received on DD
ABT: Abort indication to internal source

Figure 5. State Diagram of Monitor Receiver

DSP PROGRAMMING

SIGNAL PROCESSING

Several blocks are programmable for signal processing. This allows users to optimize the performance of the IDT821064 for the system. Figure 6 shows the Signal Flow for each channel and indicate the programmable blocks.

The programmable digital filters are used to adjust gain and impedance, balance transhybrid and correct frequency response. All the coefficients of the digital filters can be calculated automatically by a software provided by IDT. Users should provide accurate SLIC model, impedance and gain requirements, then the software will calculate all the coefficients automatically. When these coefficients are written to the coefficient RAM of the IDT82V1064, the final AC characteristics of the line card (consists of SLIC and CODEC) will meet the ITU-T specifications.

GAIN ADJUSTMENT

The analog gain and digital gain of each channel can be adjusted separately in IDT821064.

For each individual channel, in transmit path, analog A/D gain can be selected as 0 dB or 6 dB. The selection is done by A/D Gain (GAD) bit in Local Command 4. The default analog gain for transmit path is 0 dB.

For each individual channel, in receive path, analog D/A gain can be selected as 0 dB or -6 dB. The selection is done by D/A Gain (GDA) bit in Local Command 4. The default analog gain for receive path is 0 dB.

Digital gain of transmit path (GTX) can be programmed from -3 dB to +12 dB with minimum 0.1 dB step. If CS[5] bit is '0' in Local Command 1, the digital gain in transmit path is set to be the default value. If CS[5] bit is '1' in Local Command 1, the digital gain in transmit path will be decided by the coefficient in GTX RAM.

Digital gain of receive path (GRX) can be programmed from -12 dB to +3 dB with minimum 0.1 dB step. If CS[7] bit is '0' in Local Command 1, the digital gain in receive path is set to be the default value. If CS[7] bit is '1' in Local Command 1, the digital gain in receive path will be decided by the coefficient in GRX RAM.

IMPEDANCE MATCHING

There is a programmable feedback path on each channel from VIN to VOUT in the IDT821064. It synthesizes the two-wire impedance of the SLIC. The Impedance Matching Filter (IMF) and the Gain of Impedance Scaling (GIS) are adjustable, they work together to realize impedance matching. If the CS[0] bit in Local Command 1 is '0', the IMF coefficient is set to be default value; if CS[0] is '0', the IMF coefficient is set by the IMF RAM. The CS[2] bit in Local Command 1 decides if the GIS coefficient is programmable: if it's '0' ,the GIS coefficient is set to be default value; if it's '0', the GIS coefficient is set by the GIS RAM.

TRANSHYBRID BALANCE

Transhybrid balancing filter is used to adjust transhybrid balance to ensure the echo cancellation meets the ITU-T specifications. The coefficient for Echo Cancellation (ECF) can be programmed. If the CS[1] bit in Local Command 1 is '0', the coefficient of ECF is set to be default value; if CS[1] is '1', the coefficient of ECF is decided by the ECF RAM.

FREQUENCY RESPONSE CORRECTION

The IDT821064 provides two filters that can be programmed to correct any frequency distortion caused by the impedance matching filter, they are: Frequency Response Correction for Transmit path (FRX) filter and Frequency Response Correction for Receive path (FRR) filter. The coefficients of FRX filter and FRR filter can be programmed. If the CS[4] bit in Local Command 1 is '0', the FRX coefficient is set to be default value, while if CS[4] is '1', the FRX coefficient is decided by the FRX RAM. If the CS[6] bit in Local Command 1 is '0', the FRR coefficient is set to be default value, while if CS[6] is '1', the FRR coefficient is decided by the FRR RAM.

The address of the Coe-RAM including GTX, GRX, FRX, FRR, GIS, ECF and IMF RAM are listed in APPENDIX.

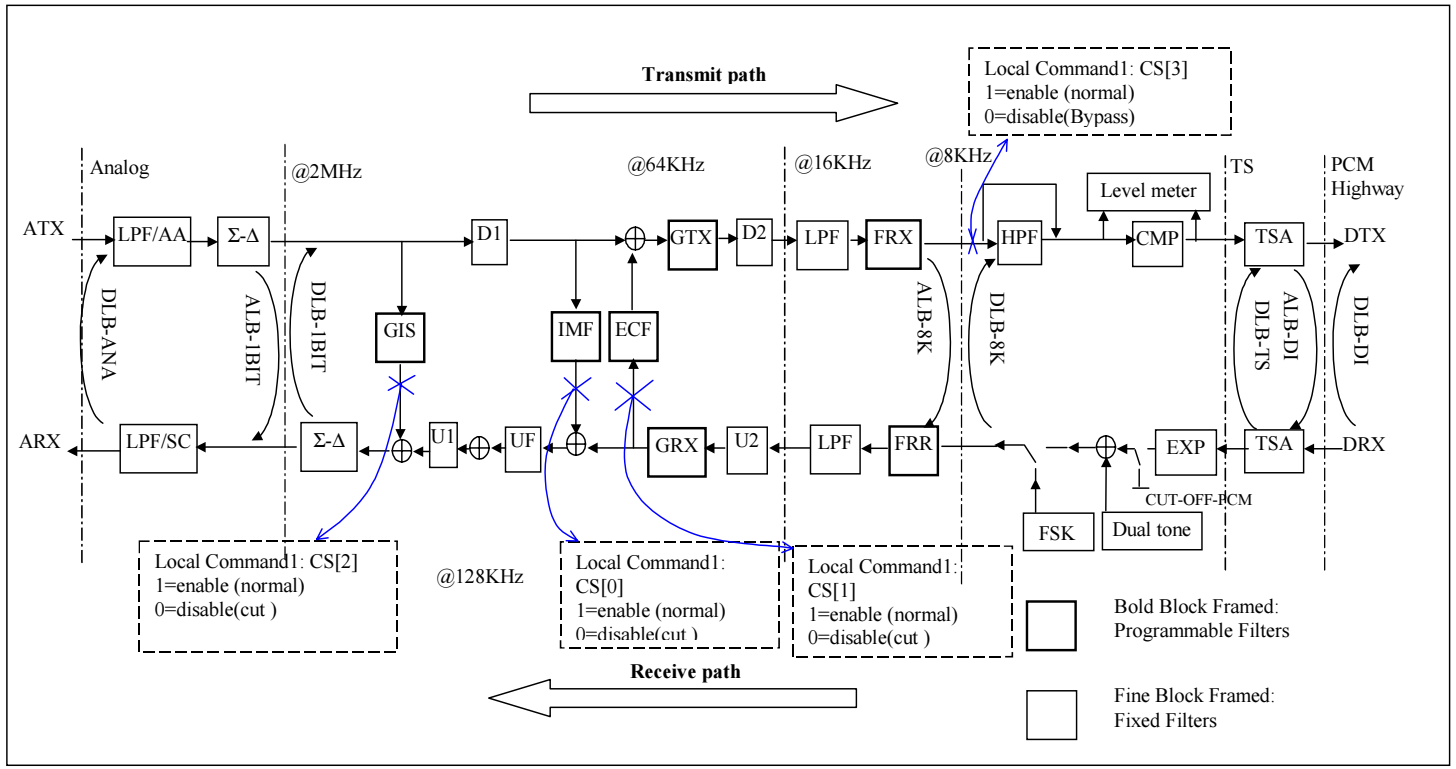


Figure 6. Signal Flow for Each Channel

Abbreviation List

LPF/AA: Anti-Alias Low-pass Filter
LPF/SC: Smoothing Low-pass Filter
LPF: Low-pass Filter
HPF: High-pass Filter
GIS: Gain for Impedance Scaling
D1: 1st Down Sample Stage
D2: 2nd Down Sample Stage
U1: 1st Up Sample Stage
U2: 2nd Up Sample Stage
UF: Up Sampling Filter (64k-128k)

IMF: Impedance Matching Filter
ECF: Echo Cancellation Filter
GTX: Gain for Transmit Path
GRX: Gain for Receive Path
FRX: Frequency Response Correction for Transmit
FRR: Frequency Response Correction for Receive
CMP: Compression
EXP: Expansion

SLIC CONTROL

The SLIC interface of IDT821064 for each channel consists of 7 pins: 2 inputs SI1 and SI2, 3 I/O pins SB1, SB2 and SB3, together with 2 outputs SO1 and SO2.

SI1 AND SI2

SLIC inputs SI1 and SI2 can be read in 2 ways - via Global Command 7 or via the field of upstream C/I octet.

SI1 and SI2 data of all 4 channels can be read by executing a read operation of Global Command 7. The SIA[3:0] bits of Global Command 7 represent the debounced SI1 signal of channel 4 to channel 1. The SIB[3:0] bits of Global Command 7 represent the debounced SI2 signal of channel 4 to channel 1.

Both SI1 and SI2 can be assigned to off-hook, ring trip, ground key signals or other signals. The Global Command 7 provides for users a more efficient way to obtain time-critical data such as on/off-hook and ring trip information from the SLIC inputs SI1 and SI2.

SI1 and SI2 data for each channel can also be obtained in the upstream C/I channel. See page 6 for details.

SB1, SB2 AND SB3

SLIC I/O pin SB1 for each channel can be configured as input or output separately, by Global Command 8. The SB1C[3:0] bits of this command correspond to the SB1 directions of channel 4 to channel 1: '0' means input and '1' means output. Similarly, the SB2C[3:0] bits of Global Command 9 determine the I/O direction of the SB2 pins for each channel, and the SB3C[3:0] bits of Global Command 10 determine the I/O direction of the SB3 pins for each channel.

When the SB1, SB2 or SB3 pin is selected as input, its information can be read by Global Command. By executing a read operation of Global Command 8, 9 or 10, users can obtain information of SB1, SB2 or SB3 respectively. The SB1[3:0] bits in Global Command 8, the SB2[3:0] bits in Global Command 9 and the SB3[3:0] bits of Global Command 10 provide the SB1, SB2 and SB3 information respectively for all four channels. For SB1, the information of it can also be read through upstream C/I channel. But for SB2 and SB3, the information of them only can be read by Global Command.

When SB1, SB2 and SB3 are configured as outputs, they can only be written through the downstream C/I channel. Refer description of C/I channel in page 6 for details.

SO1 AND SO2

SO1 and SO2 are two SLIC signaling outputs, data can only be written to them through downstream C/I channel.

HARDWARE RING TRIP

In order to prevent the damage caused by high voltage ring signal, the IDT821064 offers a hardware ring trip function to respond to the off-hook signal as fast as possible. This function can be enabled by setting RTE bit in Global Command 6.

The off-hook signal can be input via either SI1 or SI2, while the ring control signal can be output via any pin of SO1, SO2, SB1, SB2 and SB3 (when SB1-SB3 configured as output). In Global Command 6, IS bit determines which input is used and OS[2:0] bits determine which output is used.

When a valid off-hook signal arrives on SI1 or SI2, the IDT821064 will turn off the ring signal by inverting the selected output, regardless of the value in corresponding SLIC output control register (the content in the corresponding SLIC control register should be changed later). This function provides a much faster response to off-hook signal than the software ring trip which turns off the ring signal by changing the value of selected output in the corresponding register.

The IPI bit in Global Command 6 is used to indicate the valid polarity of input. If the off-hook signal is active low, the IPI should be set to '0'; if the off-hook signal is active high, the IPI should be set to '1'.

The OPI bit in Global Command 6 is used to indicate the valid polarity of output. If the ring control signal is required to be low in normal status and be high to activate a ring, the OPI should be set to '1'; if it is required to be high in normal status and be low to activate a ring, the OPI should be set to '0'.

For example, in a system where the off-hook signal is active low and ring control signal is active high, the IPI in Global Command 6 should be set to '0' and the OPI bit should be set to '1'. In normal status, the selected input (off-hook signal) is high and the selected output (ring control signal) is low. When the ring is activated by setting the output (ring control signal) high, a low pulse appearing on the input (off-hook signal) will inform the device to invert the output to low and cut off the ring signal.

CHOPPER CLOCK

IDT821064 offers two programmable chopper clock outputs: CHCLK1 and CHCLK2. Both CHCLK1 and CHCLK2 are synchronous to MCLK. CHCLK1 outputs signal with programmable 2-28 ms clock cycle, while the frequency of CHCLK2 can be any of 256 kHz, 512 kHz and 16.384 MHz. The frequency selection of chopper clocks can be implemented by Global Command 4. The chopper clocks can be used to drive the power supply switching regulators on SLICs.

DEBOUNCE FILTERS

For each channel, IDT821064 provides two debounce filter circuits: Debounced Switch Hook (DSH) Filter for SI1 and Ground Key (GK) Filter for SI2 as shown in Figure 7. They are used to buffer the input signals on SI1 and SI2 pins before changing the state of the SLIC Debounced Input SI1/SI2 Register (Global Command 7). Frame Sync (FS) is necessary for both DSH filter and GK filter.

DSH Debounce bits in Local Command 3 can program the debounce time of SI1 input from SLIC on individual channel. The DSH filter is initially clocked at half of the frame sync rate (250 μs), and any data changing at this sample rate resets a programmable counter. The counter clocks at the rate of 2 ms, and the value of the counter can be varied from 0 to 30 which is determined by Local Command 3. The corresponding SIA bit in the SLIC Debounced Input SI1 Register (accessed by Global Command 7) would not be updated until the value of the counter is reached. SI1 bit usually contains SLIC switch hook status.

GK Debounce bits in Local Command 3 can program the debounce interval of SI2 input from SLIC on corresponding channel. The debounced signal will be output to SIB of SLIC Debounced Input SI2 Register (accessed by Global Command 7). The GK debounce filter consists of an up/down counter that ranges between 0 and 6. This six-state counter is clocked by the GK timer at the sampling period of 0-30 ms, as programmed by Local Command 3. When the sampled value is low, the counter is decremented by each clock pulse. When the sampled value is high, the counter is incremented by each clock pulse. When the counter increments to 6, it sets a latch whose output is routed to the corresponding SIB bit. If the counter decrements to 0, this latch is cleared

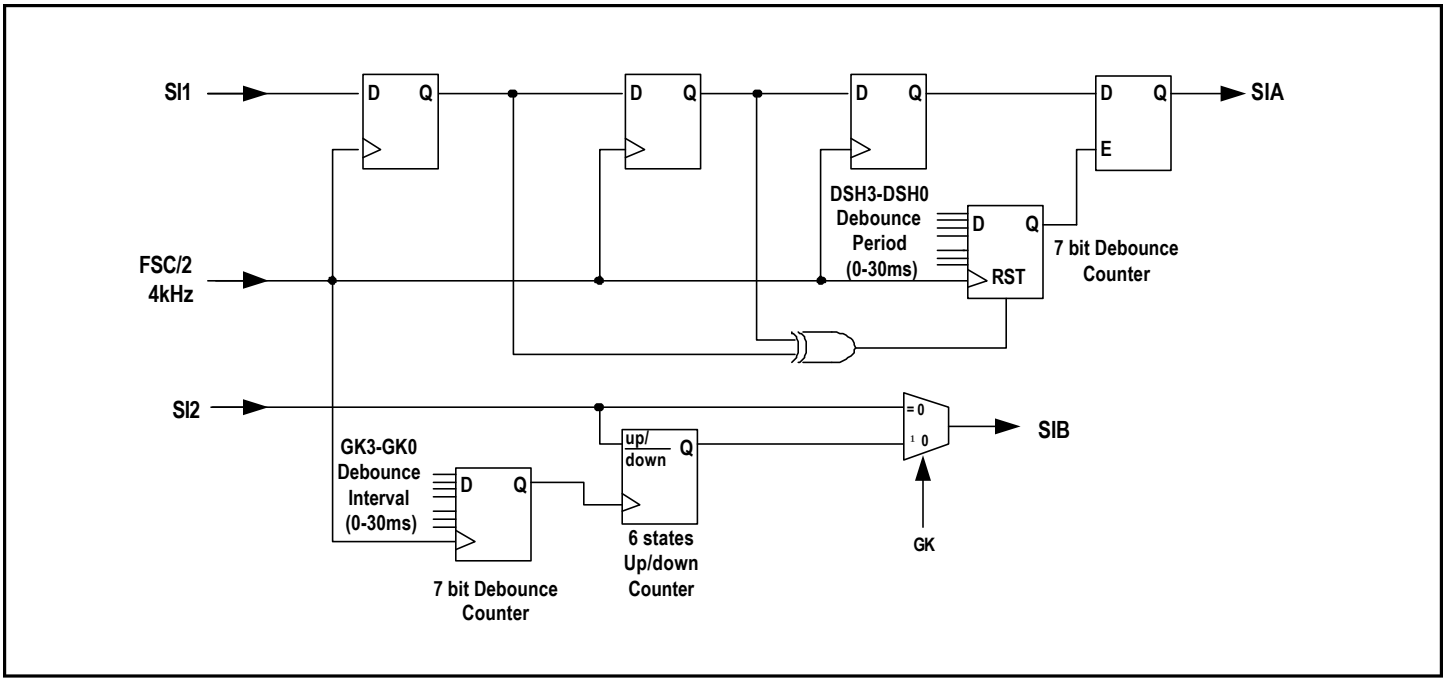


Figure 7. Debounce Filters

and the output bit is set to 0. In other cases, the latch, the SIB status remains in their previous state without being changed. In this way, at least six consecutive GK clocks with the debounce input remaining at the same state to effect an output change.

DUAL TONE AND RING GENERATION

Each channel of IDT821064 has two tone generators, Tone 0 generator and Tone 1 generator, which can produce a gain-adjustable dual tone signal and output it to VOUT pin. The tone generators can be used to generate signals such as test tone, DTMF, dial tone, busy tone, congestion tone and Caller-ID Alerting Tone etc.

The Tone 0 generator and Tone 1 generator of each channel can be enabled or disabled independently by setting the TEN0 and TEN1 bits in Local Command 5.

The tone generator is user-programmable, the frequency and amplitude of the tone can be programmed by writing coefficient into the Coe-RAM. The frequency coefficient and amplitude coefficient can be calculated by the following formulas:

Frequency Coefficient = $32767 * \cos(f/8000 * 2*\pi)$

Amplitude Coefficient = $A * 32767 * \sin(f/8000 * 2 *\pi)$

Herein, 'f ' is the desired frequency of the tone; 'A' is scaling parameter for the amplitude of the tone. The range of 'A' is from 0 to 1:

A = 1, corresponding to the maximum amplitude, 1.57 V ;

A = 0, corresponding to minimum amplitude, 0 V.

It is a linear relationship between 'A' and amplitude, which means if 'A'=β ($0< \beta< 1$), then the amplitude will be $1.57*\beta$ (V).

The Frequency range is from 25 Hz to 3400 Hz. The frequency tolerances are as the following:

25 Hz < f < 40 Hz, tolerance< $\pm$12%

40 Hz < f < 60 Hz, tolerance< $\pm$5%

60 Hz < f < 100 Hz, tolerance< $\pm$2.5%

100Hz < f < 3400 Hz, tolerance< $\pm$1%

The Frequency Coefficient and Amplitude Coefficient should be converted to corresponding hexadecimal value before being written into the Coe-RAM. Refer to Appendix for address of Tone-RAM.

Ring signal is a special signal generated by the dual tone generators. When only one tone generator is enabled or both tone generators produce the same tone, and frequency of the tone is set as ring signal required (10 Hz to 100 Hz), the VOUT pin will output the Ring signal.

FSK SIGNAL GENERATION

The IDT821064 provides a FSK signal generator to send Caller-ID messages. Generally, the procedure of sending Caller-ID messages by FSK codes is as the following:

Step 1: Start, Send Seizure Signal;

Step 2: Send Mark Signal;

Step 3: Send one byte Caller-ID message, then send Flag Signal;

Step 4: If the messages to be sent are finished, stop;
otherwise, return to step 3.

Herein, the Seizure Signal is a string of '01' pairs to inform telephone set that Caller-ID message will come; the Mark Signal is a string of '1', which follows the Seizure Signal to inform telephone set that Caller-ID message is coming; while the Flag Signal is a string of '1' sending between two bytes of Caller-ID message, with this the telephone set can have enough time to process the received byte.

According to the generic procedure of FSK signal sending, a recommended programming flow chart for IDT821064 FSK generator is shown in Figure 8.

To make it easy for users to understand the flow chart, several notes is given below:

1. The FSK function block will be enabled when FSK On/Off bit (FO) in Global Command 15 is set to '1'. After finishing sending the FSK signal, the FO bit should be set to '0' to disable the generation function.

2. The FSK Start bit (FS) in Global Command 15 is used to indicate the start of the FSK signal generation, when FS is '0' which means the function block is idle, users can go on with the operation; when FS is '1' which means FSK generator is busy, users should wait until it turns to '0'

(after the message data in the FSK-RAM having been sent, the FS bit will be cleared to '0' automatically).

3. The length of the Seizure Signal, Mark Signal and Flag Signal are different in different system, for IDT821064, they can be programmed by Global Command 13,14 and 11 respectively. It should be noted that, the Seizure Length is two times of the value that set in Global Command 13, for example, if the SL[7:0] bits of Global Command 13 is 1(d), it means that the Seizure Length is 2(d).

4. As is described in "Addressing of FSK-RAM", the FSK-RAM consists of 32 words, and each word consists of 16 bits (2 bytes), so it can contain up to 64 bytes of message at one time. If the message data is longer than 64 bytes, users should write them into the FSK-RAM two or more times according to the length of the message.

5. The "Data length" is the number of bytes that written in the FSK-RAM and need to be sent out. During the transmission of FSK signal, an internal counter will count the number of data bytes that transmitted, once it reaches the Data length, the FSK transmission is completed and the FS bit is set to '0'.

6. Because there is only one FSK-RAM shared by four channels of IDT821064, the FSK signal can only generate on one channel at one time, the channel selection is done by the FCS[2:0] bits of Global Command 15.

7. The FSK signal generated by the IDT821064 follows the BELL 202 and CCITT V.23 specifications. Users can select BT or Bellcore standard by setting the BT/Bellcore Select bit (BS) in Global Command 15. The difference between BT and Bellcore is shown in Table 3.

8. The "Mark After Send" bit (MAS) is useful if the total message data is longer than 64 bytes. If the MAS is set to '1', then after sending one frame of FSK-RAM message(=< 64 bytes), IDT821064 will keep sending a series of '1' to hold the communication channel for sending next frame of FSK message, and at the same time, users can update the FSK-RAM with new data. This series of '1' will stop by set the MAS bit to '0' or set the FO bit to '0'.

9. It should be noted that, when writing/reading message data to/from the FSK-RAM via GCI interface, the sequence of read/write is MSB first; but the FSK generator will send these signal (message data) out through channel port with LSB first.

Refer to the IDT821064 Application Note for more information.

Table 3 - BT/Bellcore Standard of FSK Signal

Item	BT	Bellcore
Mark(1) frequency	1300 Hz ± 1.5%	1200Hz ± 1.1%
Space (0) frequency	2100 Hz ± 1.1%	2200 Hz ± 1.1%
Transmission rate	1200 baud ± 1%	1200 baud ± 1 %
Word format	1 start bit which is '0', 8 word bits (with least significant bit LSB first), 1 stop bit which is '1'	1 start bit which is '0' 8 word bits (with least significant bit LSB first) 1 stop bit which is '1'

LEVEL METERING

The IDT821064 has a level meter which can be shared by all 4 signal channels. The level meter is designed to emulate the off-chip PCM test equipment so as to facilitate the line-card, subscriber line and user telephone set monitoring. The level meter tests the returned signal and reports the measurement result via MPI interface. When combined with Tone Generation and Loopback modes, this allows the microprocessor to test channel integrity. CS[1:0] bits in Global Command 19 select the channel, signal on which will be metered.

Level Metering function is enabled by setting LMO bit to '1' in Global Command 19. There is a Level Meter Counter register for this function. It can be accessed by Global Command 18. This register is used to configure the number of time cycles for sampling PCM data (8 kHz sampling rate). The output of Level Metering will be sent to Level Meter Result Low and Level Meter Result High registers (Global Command 16 and 17). The LVLL register contains the lower 7 bits of the output and a data-ready bit (LVLL[0]), while the LVLH register contains the higher 8 bits of the output. An internal accumulator sums the rectified samples until the number configured by Level Meter Counter register is reached. By then, the LVLL[0] bit is set to '1' and accumulation result is latched into the LVLL and LVLH registers simultaneously.

Once the LVLH register is read, the LVLL[0] bit will be reset. The LVLL[0] bit will be set high again by a new data available. The contents in LVLL and LVLH will be overwritten by later metering result if they are not read out yet. In Level Metering result read operation, it is highly recommended to read LVLL first.

L/C bit in Global Command 19 determines the mode of Level Meter operation. When L/C bit is '1', the Level Meter will measure the linear PCM data, and if LVLL[0] bit is '1' , the measure result will be output to LVLH and LVLL. When L/C bit is '0', compressed PCM will be output transparently to LVLH.

The calculation and method of level metering will be described in the Application Note.

CHANNEL POWER DOWN/STANDBY MODE

Each individual channel of IDT821064 can be powered down independently by Local Command 9. When the channel is powered down (enters into standby mode), The transmission and reception of PCM data, D/A and A/D converters are disabled. In this way, power consumption of the device can be reduced. When IDT821064 is powered up or reset, all four channels will be powered down. All circuits that contain programmed information retain their data when powered down. MPI (Microprocessor Interface) is always active so that new command could be received and executed.

POWER DOWN PLL/SUSPEND MODE

A suspend mode is offered to the whole chip to save power. In this mode, the PLL block is turned off and DSP operation is disabled. This mode saves much more power consumption than standby mode. In this mode, only Global Command and Local Command can be executed. RAM operation is disabled as internal clock has been turned off. The PLL blocks can be powered down by Global Command 20. Suspend mode can be entered by powering down PLL and all channels.

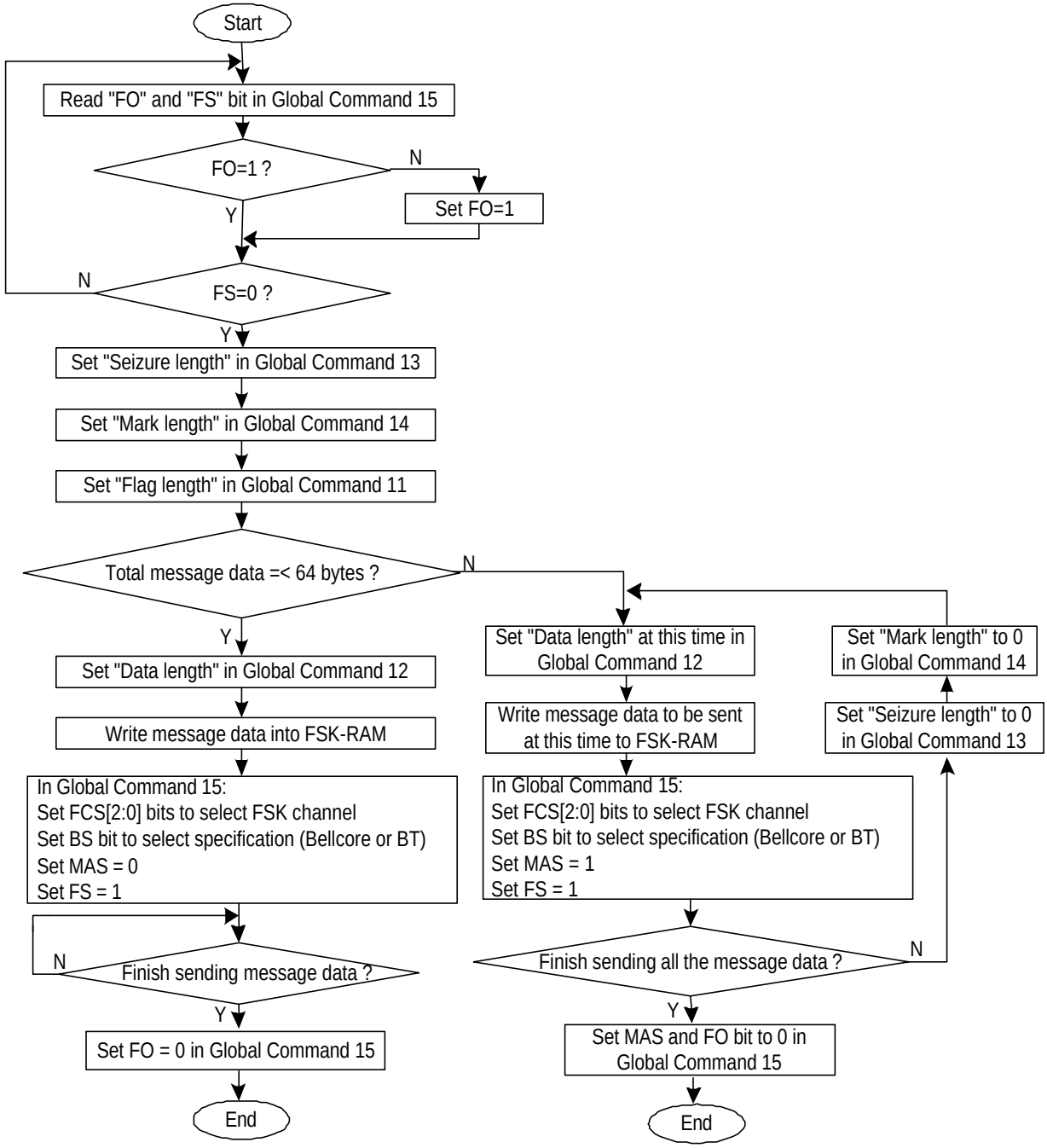


Figure 8. A Recommended Programming Flow Chart for FSK Generator

OPERATING THE IDT821064

PROGRAMMING DESCRIPTION

PROGRAM START BYTE

The IDT821064 uses the monitor channel for the exchange of status or mode information with high level processors. The messages transmitted in the monitor channel have different data structures. For a complete command operation, the first byte of monitor channel data indicates the address of the device either sending or receiving the data. All monitor channel messages to/from IDT821064 begin with the following Program Start (PS) byte:

b7	b6	b5	b4	b3	b2	b1	b0
1	0	0	$\overline{A}$/B	0	0	0	1

Because one monitor channel is shared by two voice data channels to transmit maintenance information, so an $\overline{A}$/B bit is used in the PS byte to identify the two channels. For easy description, we name them as Channel A and Channel B. Herein,

$\overline{A}$/B = 0: means that Channel A is the source (upstream) or destination (downstream) - 81H;

$\overline{A}$/B = 1: means that Channel B is the source (upstream) or destination (downstream) - 91H.

The Program Start byte is followed by a command (global/local register command or RAM command) byte. For Global Command, the $\overline{A}$/B bit in the PS byte can be ignored. If the command byte specifies a write, then from 1 to 16 additional data bytes may follow (1-4 for registers, 1-16 for RAM). If the command byte specifies a read, additional data bytes may follow. IDT821064 responds to the read command by sending up to 16 data bytes upstream containing the information requested by the upstream controller. Each byte on monitor channel must be transferred at least twice and in two consecutive frames.

IDENTIFICATION COMMAND

In order to distinguish different devices unambiguously by software, a two byte identification command is defined for analog lines GCI devices (8000H):

1	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0

Each device will then respond with its specific identification code. For IDT821064, this two byte identification code is (8082H):

1	0	0	0	0	0	0	0
1	0	0	0	0	0	1	0

REGISTER COMMAND AND RAM COMMAND

There are three types of commands used in monitor channel to accessing registers and RAM, they are:

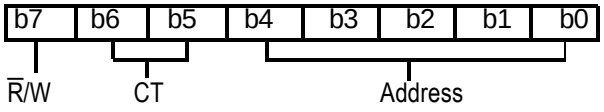
Local Command (LC), which is used to configure each channel by reading/writing the Local Registers, there are 5 Local Registers per channel available;

Global Command (GC), which is used to configure all 4 channels by reading/writing the Global Registers, there are totally 21 Global Registers shared by the 4 channels;

RAM Command (RC), which is used to read/write Coe-RAM and FSK-RAM, there are 40 words (divided into 5 blocks) with 14 bits per word Coe-RAM for each channel, and 32 words (divided into 4 blocks) with 16 bits per word FSK-RAM shared by four channels. When a RC is executed, 8 words of RAM (14 or 16 bits/word) will be accessed.

Register/RAM Command Format

The format of register command and RAM command is as the following:



$\overline{R}$/W: Read/Write Command bit.

b7 = 0: Read Command

b7 = 1: Write Command

CT: Command Type

b6 b5 = 00: LC - Local Command

b6 b5 = 01: GC - Global Command

b6 b5 = 10: Not Allowed

b6 b5 = 11: RC - RAM Command

Address: Specify which register or which block of RAM will be read or written.

For both Local Command and Global Command, b[4:0] are used to address the Local Registers or Global Registers.

For RAM Command, b4 is used to distinguish the Coe-RAM and the FSK RAM:

b4 = 0: The RAM Command is for Coe-RAM

b4 = 1: The RAM Command is for FSK-RAM

When the RAM Command is for Coe-RAM, b[3:0] are used to address the blocks of the Coe-RAM. When the RAM Command is for FSK-RAM, b3 is always '0' and b[2:0] are used to address the blocks of the FSK-RAM.

Addressing Local Register

When addressing Local Registers, both the location of time slot (determined by S1 and S0 pin) and the b4 bit in Program Start Byte would indicate which channel to be addressed.

IDT821064 provides a Consecutive Adjacent Addressing for Read/Write Local Registers. If the address for Local Register is specified in a Local Command, then, according to the value of 'b1b0' of the address, there will be 1 to 4 adjacent local registers will be read/write automatically with the highest order first. For example, if the address of the register specified by the Local Command is end with '11' (b1b0='11'), 4 adjacent registers will be Read/Write by this Command. If b1b0 ='10' , then 3 adjacent registers will be Read/Write. If b1b0 = '01', then only 2 adjacent registers will be Read/Write. If b1b0 = '00', then only this specified register will be Read/Write. The details of the Consecutive Adjacent Addressing is shown in Table 4.

The Consecutive Adjacent Addressing can not be stopped once a command is initiated. For write command, the number of bytes following the command must be the same as the number of registers being written.

The transmission sequence of Local Command is shown in Table 5.

Addressing Global Register

The address of the 21 Global Registers is : 00000 - 10101 and 10111. For the consecutive address, IDT821064 also provides a Consecutive Adjacent Addressing for Read/Write, which is exactly the same as the

Local Registers. The procedure of Consecutive Adjacent Addressing also can not be stopped once a Global Command is initiated. The transmission sequence of Global Command is shown in Table 5.

Table 4 - Consecutive Adjacent Addressing

Address Specified by Local Command	In/Out Data	Registers being $\overline{R}$/W
b4 b3 b2 b1 b0		
X X X 1 1	Byte 1	X X X 11
(b1b0 = 11, 4 bytes DATA)	Byte 2	X X X 10
	Byte 3	X X X 01
	Byte 4	X X X 00
X X X 1 0	Byte 1	X X X 10
(b1b0 = 10, 3 bytes DATA)	Byte 2	X X X 01
	Byte 3	X X X 00
X X X 0 1	Byte 1	X X X 01
(b1b0 = 01, 2 bytes DATA)	Byte 2	X X X 00
X X X 0 0	Byte 1	X X X 00
(b1b0 = 00, 1 byte DATA)		

Table 5 - Local/Global Command Transmission Sequence

GCI Monitor Channel	
Downstream	Upstream
Program Start byte (81H/91H) Local/Global Command byte, write Data byte 1 . . . Data byte m* Program Start byte (81H/91H) Local/Global Command byte, read	 Program Start byte (81H/91H) Data byte 1 . . . Data byte m*

Addressing Coe-RAM

The Coe-RAM (Coefficient RAM) is consisted of 5 blocks for per channel and totally 40 words. Each block contains 8 words. The 5 blocks are:

- IMF RAM (Word 0 - Word 7), for Impedance Matching Filter coefficient;
- ECF RAM (Word 8 - Word 15), for Echo Cancellation Filter coefficient;
- GIS RAM (Word 16 - Word 19) and Tone Generator RAM (Word 20 - Word 23), for Gain of Impedance Scaling and amplitude or frequency for Tone Generator ;
- FRX RAM (Word 24 - Word 30) and GTX RAM (Word 31), for Frequency Response Correction in Transmit Path coefficient and Gain in Transmit Path;
- FRR RAM (Word 32 - Word 38) and GRX RAM (Word 39), for Frequency Response Correction in Receive Path coefficient and Gain in Receive Path.

Refer to APPENDIX (Coe-RAM Mapping) for further details.

Each word in Coe-RAM is 14-bit wide. To write a Coe-RAM word, 16 bits (or, two 8-bit bytes) are needed to fulfill one word with MSB first, but the last two bits (LSB) will be neglected. When read, each Coe-RAM word will output 16 bits with MSB first, but the last two bits are meaningless.

When addressing Coe-RAM, both the location of time slot (determined by S1 and S0 pin) and the b4 bit in Program Start Byte would indicate which channel to be addressed.

When the address of a Coe-RAM block is specified in a RAM Command, all 8 words of this block will be Read/Write automatically, with the highest order word first.

Only b[3:0] of a Coe-RAM Command can be used to address the 5 blocks in Coe-RAM, as b4 is used to distinguish the Coe-RAM and FSK-RAM.

The transmission sequence of the Coe-RAM command is shown in Table 6.

Table 6 - Coe-RAM/FSK-RAM Command Transmission Sequence

GCI Monitor Channel	
Downstream	Upstream
Program Start byte (81H/91H) RAM Command byte, write Data byte 1(Data_H of Word1) Data byte 2(Data_L** of Word1) Data byte 3(Data_H of Word2) Data byte 4(Data_L of Word2) . . . Data byte 15(Data_H of Word8) Data byte 16(Data_L of Word8) Program Start byte (81H/91H) RAM Command byte, read	 Program Start byte (81H/91H) Data byte 1(Data_H of Word1) Data byte 2(Data_L** of Word1) Data byte 3(Data_H of Word2) Data byte 4(Data_L of Word2) . . . Data byte 15(Data_H of Word8) Data byte 16(Data_L of Word8)

Addressing FSK-RAM

The FSK-RAM is used to store the message data that need to be sent by the FSK generator (Refer to FSK Signal Generation). The FSK-RAM is consisted of 4 blocks, each block has eight 16-bit words.

To write a FSK-RAM word, 16 bits (or, two 8-bit bytes) are needed to fulfill one word with MSB first. When being read, each FSK-RAM word in FSK-RAM will output 16 bits with MSB first.

Only b[2:0] of a FSK-RAM Command are needed to address the 4 blocks in FSK-RAM, b3 should be always '0', and b4 is always '1' to indicate the address is for FSK-RAM.

When the address of a FSK-RAM block is specified in a RAM Command, all 8 words of this block will be Read/Write automatically, with the highest order word first.

The transmission sequence of the FSK-RAM command is shown in Table 6.

Notes:

* The number of the data bytes can be 1 to 4 depending on the two bits 'b1b0' of the Local/Global Command.

** When addressing the Coe-RAM, the data word is 14-bit wide, the lowest two bits in Data_L of each word are ignored; When addressing the FSK-RAM, the data word is 16-bit wide.

POWER ON SEQUENCE

To power on IDT821064, users should follow this sequence:

1. Apply ground first;
2. Apply VCC, finish signal connections and set $\overline{\text{RESET}}$ low, thus the device goes into default state;
3. Set $\overline{\text{RESET}}$ high;
4. Select master clock frequency;
5. Write two initialization commands to the IDT821064: Command A5H followed by a data byte of F2H, then Command 84H followed by a data byte of 40H;
6. Program filter coefficients and other parameters as required.

Note that every time after the IDT821064 is powered on, or reset either by the $\overline{\text{RESET}}$ pin or by the Hardware/Software Reset Command, users must write these two initialization commands to the device before executing any other commands.

DEFAULT STATE AFTER RESET

When the IDT821064 is powered on, or reset either by $\overline{\text{RESET}}$ pin or by GCI command, the device defaults to the following state:

1. All four channels are powered down and in standby mode;
2. All loopbacks and cutoff are disabled;
3. The master clock frequency is 2.048 MHz;
4. Time slots for transmitting and receiving are determined by S1 and S0 pin. DD, DU clocks data on rising edges of DCL;
5. A-Law is selected;
6. Coefficients of FRX, FRR, GTX, GTR, IMF, GIS and ECF are set to be default values. The analog gains are set to be 0 dB. The High-Pass Filters (HPF) are enabled;
7. SB1, SB2 and SB3 are configured as inputs;
8. SI1 and SI2 are configured as no debounce.
9. All feature function blocks including FSK, Dual Tone, Ring Trip and Level Metering are turned off.
10. CHCLK1 and CHCLK2 are set to be high.

The data stored in RAM will not be changed or lost by any kind of resets. In this way, the RAM data will not lost unless the device is powered down physically.

COMMANDS LIST

Notes: 1. $\overline{R}$/W = 0: Read ; $\overline{R}$/W = 1: Write

2. *'R'* means Reserved for future use. This bit will always be filled in ' 0 ' in Write-Command, and be ignored in Read-command.

GLOBAL COMMANDS:

1. Version Number (20H)/No Operation (A0H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	0	0	0	0	0
I/O Data	0	0	0	0	0	0	0	1

By executing this read-command (20H), users can read out the version number of the IDT821064. The default value is 01H.

When executing the no operation command (A0H), a data byte (FFH) must follow to ensure proper operation.

2. Software Reset (A2H), Write Only

	b7	b6	b5	b4	b3	b2	b1	b0
Command	1	0	1	0	0	0	1	0

This command resets all Local Registers, but does not reset Global Registers and RAM. When executing this command, a data byte (FFH) must follow to ensure proper operation.

3. Hardware Reset (A3H), Write Only

	b7	b6	b5	b4	b3	b2	b1	b0
Command	1	0	1	0	0	0	1	1

The action of this command is equivalent to pulling the $\overline{RESET}$ pin to low (Refer to page 18 for information about $\overline{RESET}$ operation). When executing this command, a data byte (FFH) must follow to ensure proper operation.

4. Chopper Clock Select (24H/A4H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	0	0	1	0	0
I/O data	*R*	*R*	CHclk2 [1]	CHclk2 [0]	CHclk1 [3]	CHclk1 [2]	CHclk1 [1]	CHclk1 [0]

This command is used to determine the CHclk2 and CHclk1 output signals, the frequency is shown below:

CHclk2[1:0]=00: chclk2 outputs 1 permanently (default);
CHclk2[1:0]=01: chclk2 outputs digital signal at the frequency of 512 kHz;
CHclk2[1:0]=10: chclk2 outputs digital signal at the frequency of 256 kHz;
CHclk2[1:0]=11: chclk2 outputs digital signal at the frequency of 16384 kHz;
CHclk1[3:0]=0000: chclk1 outputs 1 permanently (default);
CHclk1[3:0]=0001: chclk1 outputs digital signal at the frequency of 1000/2 Hz;
CHclk1[3:0]=0010: chclk1 outputs digital signal at the frequency of 1000/4 Hz;
CHclk1[3:0]=0011: at the frequency of 1000/6 Hz;
CHclk1[3:0]=0100: at the frequency of 1000/8 Hz;
CHclk1[3:0]=0101: at the frequency of 1000/10 Hz;
CHclk1[3:0]=0110: at the frequency of 1000/12 Hz;
CHclk1[3:0]=0111: at the frequency of 1000/14 Hz;
CHclk1[3:0]=1000: at the frequency of 1000/16 Hz;
CHclk1[3:0]=1001: at the frequency of 1000/18 Hz;
CHclk1[3:0]=1010: at the frequency of 1000/20 Hz;
CHclk1[3:0]=1011: at the frequency of 1000/22 Hz;
CHclk1[3:0]=1100: at the frequency of 1000/24 Hz;
CHclk1[3:0]=1101: at the frequency of 1000/26 Hz;
CHclk1[3:0]=1110: at the frequency of 1000/28 Hz;
CHclk1[3:0]=1111: chclk1 outputs 0 permanently.

5. A/μ-law, Linear/Compressed Code Selection (26H/A6), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	0	0	1	1	0
I/O data	A-μ	VDS	*R*	*R*	*R*	*R*	*R*	*R*

A/μ-law select bit (A-μ) selects the companding law:

A-μ = 0: A-law is selected (default)

A-μ = 1: μ-law is selected.

Voice Data select bit (VDS) defines the format of the voice data:

VDS = 0: Compressed code (default)

VDS = 1: Linear code

6. SLIC Ring Trip Setting and Control (27H/A7H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	1	0	0	1	1	1
I/O data	OPI	*R*	IPI	IS	RTE	OS[2]	OS[1]	OS[0]

Output Polarity Indicator bit (OPI) indicates the valid polarity of output:

OPI = 0: the selected output pin changes from low to high to activate the ring (default);

OPI = 1: the selected output pin changes from high to low to activate the ring.

Input Polarity Indicator bit (IPI) indicates the valid polarity of input:

IPI = 0: active low (default); IPI = 1: active high.

Input Selection bit (IS) determines which input will be selected as the off-hook indication signal source.

IS = 0: SI1 is selected (default); IS = 1: SI2 is selected.

Ring Trip Enable bit (RTE) enables or disables the ring trip function block:

RTE = 0: the ring trip function block is disabled (default);

RTE = 1: the ring trip function block is enabled.

Output Selection bits (OS[2:0]) determine which output will be selected as the ring control signal source.

OS[2:0] = 000 - 010: not defined;

OS[2:0] = 011: SB1 is selected (when it is configured as an output);

OS[2:0] = 100: SB2 is selected (when it is configured as an output);

OS[2:0] = 101: SB3 is selected (when it is configured as an output);

OS[2:0] = 110: SO1 is selected;

OS[2:0] = 111: SO2 is selected.

7. Read SI Data (28H), Read Only

	b7	b6	b5	b4	b3	b2	b1	b0
Command	0	0	1	0	1	0	0	0
I/O data	SIB[3]	SIB[2]	SIB[1]	SIB[0]	SIA[3]	SIA[2]	SIA[1]	SIA[0]

SIA bits contain SLIC status which SLIC Interface Pin SI1 receives. The value of SIA [0], SIA[1], SIA[2] and SIA[3] represent the debounced data on channel 1, channel 2, channel 3 and channel 4 respectively. SIB bits contain SLIC ground key status which SLIC Interface Pin SI2 receives. The value of SIB [0], SIB[1], SIB[2] and SIB[3] represent the debounced data on channel 1, channel 2, channel 3 and channel 4 respectively.

8. SB1 Direction Control, SB1 Data (29H/A9H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	1	0	1	0	0	1
I/O data	SB1C[3]	SB1C[2]	SB1C[1]	SB1C[0]	SB1[3]	SB1[2]	SB1[1]	SB1[0]

SLIC SB1 direction control bits (SB1C[3:0]) configure the direction of SLIC bidirectional interface pin SB1.

SB1C[0]=0: SB1 pin of channel 1 is configured as input (default);

SB1C[0]=1: SB1 pin of channel 1 is configured as output;

SB1C[1]=0: SB1 pin of channel 2 is configured as input (default);

SB1C[1]=1: SB1 pin of channel 2 is configured as output;

SB1C[2]=0: SB1 pin of channel 3 is configured as input (default);

SB1C[2]=1: SB1 pin of channel 3 is configured as output;

SB1C[3]=0: SB1 pin of channel 4 is configured as input (default);

SB1C[3]=1: SB1 pin of channel 4 is configured as output.

When SB1 pin of one channel is configured as input, the corresponding SB1 bit of this command contains the SB1 information of this channel;

When SB1 pin of one channel is configured as output, the corresponding SB1 bit of this command is reserved, data can only be written to the SB1 pin of the corresponding channel via GCI C/I octet.

9. SB2 Direction Control, SB1 Data (2AH/AAH), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	1	0	1	0	1	0
I/O data	SB2C[3]	SB2C[2]	SB2C[1]	SB2C[0]	SB2[3]	SB2[2]	SB2[1]	SB2[0]

SLIC SB2 direction control bits (SB2C[3:0]) configure the direction of SLIC bidirectional interface pin SB2.

SB2C[0]=0: SB2 pin of channel 1 is configured as input (default);
SB2C[0]=1: SB2 pin of channel 1 is configured as output;
SB2C[1]=0: SB2 pin of channel 2 is configured as input (default);
SB2C[1]=1: SB2 pin of channel 2 is configured as output;
SB2C[2]=0: SB2 pin of channel 3 is configured as input (default);
SB2C[2]=1: SB2 pin of channel 3 is configured as output;
SB2C[3]=0: SB2 pin of channel 4 is configured as input (default);
SB2C[3]=1: SB2 pin of channel 4 is configured as output.

When SB2 pin of one channel is configured as input, the corresponding SB2 bit of this command contains the SB2 information of this channel;

When SB2 pin of one channel is configured as output, the corresponding SB2 bit of this command is reserved, data can only be written to the SB2 pin of the corresponding channel via GCI C/I octet.

10. SB3 Direction Control, SB1 Data (2BH/ABH), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	1	0	1	0	1	1
I/O data	SB3C[3]	SB3C[2]	SB3C[1]	SB3C[0]	SB3[3]	SB3[2]	SB3[1]	SB3[0]

SLIC SB3 direction control bits (SB3C[3:0]) configure the direction of SLIC bidirectional interface pin SB3.

SB3C[0]=0: SB3 pin of channel 1 is configured as input (default);
SB3C[0]=1: SB3 pin of channel 1 is configured as output;
SB3C[1]=0: SB3 pin of channel 2 is configured as input (default);
SB3C[1]=1: SB3 pin of channel 2 is configured as output;
SB3C[2]=0: SB3 pin of channel 3 is configured as input (default);
SB3C[2]=1: SB3 pin of channel 3 is configured as output;
SB3C[3]=0: SB3 pin of channel 4 is configured as input (default);
SB3C[3]=1: SB3 pin of channel 4 is configured as output.

When SB3 pin of one channel is configured as input, the corresponding SB3 bit of this command contains the SB3 information of this channel;

When SB3 pin of one channel is configured as output, the corresponding SB3 bit of this command is reserved, data can only be written to the SB3 pin of the corresponding channel via GCI C/I octet.

11. FSK Flag Length (2CH/ACH), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	1	0	1	1	0	0
I/O data	FL[7]	FL[6]	FL[5]	FL[4]	FL[3]	FL[2]	FL[1]	FL[0]

Flag Length bits (FL[7:0]) determine the number of flag bits '1' which will be transmitted between the transmission of message bytes. The value is valid from 0 to 255(d). The default value is 0(d). If 0(d) is selected, no flag signal will be sent.

12. FSK Data Length (2DH/ADH), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	1	0	1	1	0	1
I/O data	WL[7]	WL[6]	WL[5]	WL[4]	WL[3]	WL[2]	WL[1]	WL[0]

Data Length bits (WL[7:0]) determine the number of all the data bytes which will be transmitted except flag. The value is valid from 0 to 64(d). Any value larger than 64(d) will be taken as 64(d) by the CPU.

The default value of this register is 0(d). When 0(d) is selected, none of the word data will be sent out. When Mark After Send (MAS bit in Global Command 15) is set to '1', the mark signal will be sent; while Mark After Send is set to '0', the transmission of mark signal will be terminated.

13. FSK Seizure Length (2EH/AEH), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	1	0	1	1	1	0
I/O data	SL[7]	SL[6]	SL[5]	SL[4]	SL[3]	SL[2]	SL[1]	SL[0]

Seizure Length bits (SL[7:0]) determine the number of '01' pairs which represent seizure phase(Seizure Length is two times of the value in SL[7:0], which is valid from 0 to 255(d), corresponding to Seizure Length 0 to 510). The default value is 0(d). When 0(d) is selected, no seizure signal will be sent.

14. FSK Mark Length (2FH/AFH), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	1	0	1	1	1	1
I/O data	ML[7]	ML[6]	ML[5]	ML[4]	ML[3]	ML[2]	ML[1]	ML[0]

Mark Length bits (ML[7:0]) determine the number of mark bits '1' which will be transmitted in initial flag phase. The value is valid from 0 to 255(d). The default value is 0(d). When 0(d) is selected, no mark signal will be sent.

15. FSK Start, Mark After Send, BT/Bellcore Select, FSK Channel Select and FSK On/Off (30H/B0H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	1	1	0	0	0	0
I/O data	*R*	*R*	FCS[1]	FCS[0]	FO	BS	MAS	FS

FSK Channel Select bits (FCS[1:0]) selects the channel on which FSK operation will be implemented.

FCS[1:0] = 00: Channel 1 is selected (default);
FCS[1:0] = 01: Channel 2 is selected;
FCS[1:0] = 10: Channel 3 is selected;
FCS[1:0] = 11: Channel 4 is selected;

FSK On/Off (FO) enables or disables the whole FSK function block.

FO = 0: FSK is disabled (default);
FO = 1: FSK is enabled.

BT/Bellcore Select bit (BS) determines which specification the IDT821064 follows:

BS = 0: Bellcore specification is selected (default);
BS = 1: BT specification is selected.

Mark After Send bit (MAS) determines the FSK block operation after the word data has been sent.

MAS = 0: The output will be muted after sending out word data (default);
MAS = 1: After sending one frame of message data (=< 64 bytes), IDT821064 keeps sending a series of '1' until the MAS bit is set to '0' and the FS bit is set to '1'.

FSK Start bit (FS) should be set to '1' when users are going to send out FSK data. It will be cleared to the default value '0' at the end of word data. When Seizure Length, Mark Length together with Data Length bits are all set to 0, the Transmit Start bit will be reset to '0' immediately after it is set to '1'.

FS = 0: disable (default); FS = 1: transmit start.

16. Level Meter Result Low Register (31H), Read Only

	b7	b6	b5	b4	b3	b2	b1	b0
Command	0	0	1	1	0	0	0	1
I/O data	LVLL[7]	LVLL[6]	LVLL[5]	LVLL[4]	LVLL[3]	LVLL[2]	LVLL[1]	LVLL[0]

This register contains the lower 8 bits of Level Meter output with the default value of '0000-0000', LVLL[0] is the high active data_ready bit. To read the level meter result, users should read the low register which contains LVLL[7:0] data first, then read the high register which contains LVLH[7:0] data. Once the high register is read, the LVLL[0] bit is cleared immediately.

17. Level Meter Result High Register (32H), Read Only

	b7	b6	b5	b4	b3	b2	b1	b0
Command	0	0	1	1	0	0	1	0
I/O data	LVLH[7]	LVLH[6]	LVLH[5]	LVLH[4]	LVLH[3]	LVLH[2]	LVLH[1]	LVLH[0]

This register contains the higher 8 bits of Level Metering output with the default value of 0(d).

18. Level Meter Count Number (33H/B3H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	1	1	0	0	1	1
I/O data	CN[7]	CN[6]	CN[5]	CN[4]	CN[3]	CN[2]	CN[1]	CN[0]

Level Meter Count Number register is used to configure the number of time cycles for sampling PCM data.

CN[7:0] = 0000-0000: the linear or compressed PCM data is output to LVLH and LVLL directly (default);
CN[7:0] = N: PCM data is sampled for N * 125 μs (N from 1 to 255).

19. Level Meter Channel Select, Linear/Compressed, Level Meter On/off (34H/B4H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	1	1	0	1	0	0
I/O data	*R*	*R*	*R*	*R*	LMO	L/C	CS[1]	CS[0]

Level Meter On/off bit (LMO) enables/disable the level meter.

LMO = 0: Level meter is disabled (default);

LMO = 1: Level meter is enabled.

Linear/Compressed bit (L/C) determines the mode of level meter operation.

L/C = 0: Message mode is selected, compressed PCM will be output to LVLH transparently (default).

L/C = 1: Metering mode is selected, linear PCM data will be metered and output to LVLH and LVLL, when data_ready bit in LVLL register is '1'.

Level Meter Channel Select bits (CS[1:0]) select the channel, data on which will be level metered.

CS[1:0] = 00: Channel 1 is selected (default);

CS[1:0] = 01: Channel 2 is selected;

CS[1:0] = 10: Channel 3 is selected;

CS[1:0] = 11: Channel 4 is selected;

20. Loop Control and PLL Power Down (35H/B5H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	1	1	0	1	0	1
I/O data	*R*	*R*	PPD	DLB_ANA	ALB_8k	DLB_8k	DLB_DI	ALB_DI

PLL Power Down bit (PPD) controls the operation of Phase Lock Loop.

PPD = 0: PLL disable, the device is in normal operation (default);

PPD = 1: PLL is powered down. The device works in Power-Saving mode. All clocks stop running.

Loop Control bits determine the loopback status. Refer to Figure 6 for details.

DLB_ANA = 0: Digital Loopback via Analog Interface is disabled (default);

DLB_ANA = 1: Digital Loopback via Analog Interface is enabled;

ALB_8k = 0: Analog Loopback via 8 kHz Interface is disabled (default);

ALB_8k = 1: Analog Loopback via 8 kHz Interface is enabled;

DLB_8k = 0: Digital Loopback via 8 kHz Interface is disabled (default);

DLB_8k = 1: Digital Loopback via 8 kHz Interface is enabled;

DLB_DI = 0: Digital Loopback from DR to DX is disabled (default);

DLB_DI = 1: Digital Loopback from DR to DX is enabled;

ALB_DI = 0: Analog Loopback from DX to DR is disabled (default);

ALB_DI = 1: Analog Loopback from DX to DR is enabled.

21. Over-sampling Timing Tuning (37H/B7H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	1	1	0	1	1	1

To improve the performance of total distortion, it is recommended to write a data byte of 40H to this Global Register. The default value is 00H.

LOCAL COMMANDS:

1. Coefficient Select (00H/80H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	0	0	0	0	0	0
I/O data	CS[7]	CS[6]	CS[5]	CS[4]	CS[3]	CS[2]	CS[1]	CS[0]

Coefficient Select bits (CS[7:0]) are used to control digital filters and function blocks on corresponding channel such as Impedance Matching Filter, Echo Cancellation Filter, High-Pass Filter, Gain for Impedance Scaling, Gain in Transmit/Receive Path and Frequency Response Correction in Transmit/Receive Path. See Figure 6 for details. It should be noted that Impedance Matching Filter and Gain for Impedance Scaling are working together to adjust impedance. That is to say, CS [0] and CS[2] should be set to the same value to ensure the correct operation.

CS [7] = 0: Gain in Receive Path coefficient is set to default value (default);
CS [7] = 1: Gain in Receive Path coefficient is set by GRX RAM.
CS [6] = 0: Frequency Response Correction in Receive Path coefficient is set to default value (default);
CS [6] = 1: Frequency Response Correction in Receive Path coefficient is set by FRR RAM;
CS [5] = 0: Gain in Transmit Path coefficient is set to default value (default);
CS [5] = 1: Gain in Transmit Path coefficient is set by GTX RAM;
CS [4] = 0: Frequency Response Correction in Transmit Path coefficient is set to default value (default);
CS [4] = 1: Frequency Response Correction in Transmit Path coefficient is set by FRX RAM;
CS [3] = 0: High-Pass Filter is bypassed/disabled;
CS [3] = 1: High-Pass Filter is enabled (default);
CS [2] = 0: Gain for Impedance Scaling coefficient is set to default value (default);
CS [2] = 1: Gain for Impedance Scaling coefficient is set by GIS RAM;
CS [1] = 0: Echo Cancellation Filter coefficient is set to default value (default);
CS [1] = 1: Echo Cancellation Filter coefficient is set by ECF RAM;
CS [0] = 0: Impedance Matching Filter coefficient is set to default value (default);
CS [0] = 1: Impedance Matching Filter coefficient is set by IMF RAM;

2. Loop Status Control (01H/81H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	0	0	0	0	0	1
I/O data	*R*	*R*	*R*	*R*	*R*	LPC[2]	LPC[1]	LPC[0]

Loop Status Control Bits (LPC[2:0]) determine the loopback status on corresponding channel. Refer to Figure 6 for detailed information.

LPC[2] = 0: Digital Loopback via Time slots is disabled on the corresponding channel (default);
LPC[2] = 1: Digital Loopback via Time slots is enabled on the corresponding channel.
LPC[1] = 0: Analog Loopback via Onebit is disabled on the corresponding channel (default);
LPC[1] = 1: Analog Loopback via Onebit is enabled on the corresponding channel;
LPC[0] = 0: Digital Loopback via Onebit is disabled on the corresponding channel (default);
LPC[0] = 1: Digital loopback via Onebit is enabled on the corresponding channel;

3. DSH Debounce and GK Debounce (02H/82H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	0	0	0	0	1	0
I/O data	GK[3]	GK[2]	GK[1]	GK[0]	DSH[3]	DSH[2]	DSH[1]	DSH[0]

DSH Debounce bits DSH[3:0] set the debounce time of SI1 input from SLIC for corresponding channel.

DSH[3:0] = 0000: 0 ms (default);
DSH[3:0] = 0001: 2 ms;
DSH[3:0] = 0010: 4 ms;
DSH[3:0] = 0011: 6 ms;
DSH[3:0] = 0100: 8 ms;
DSH[3:0] = 0101: 10 ms;
DSH[3:0] = 0110: 12 ms;
DSH[3:0] = 0111: 14 ms;
DSH[3:0] = 1000: 16 ms;
DSH[3:0] = 1001: 18 ms;
DSH[3:0] = 1010: 20 ms;

DSH[3:0] = 1011: 22 ms;
DSH[3:0] = 1100: 24 ms;
DSH[3:0] = 1101: 26 ms;
DSH[3:0] = 1110: 28 ms;
DSH[3:0] = 1111: 30 ms.

GK Debounce bits GK[3:0] set the debounce time of SI2 input from SLIC for corresponding channel.

GK[3:0] = 0000: 0 ms (default);
GK[3:0] = 0001: 2 ms;
GK[3:0] = 0010: 4 ms;
GK[3:0] = 0011: 6 ms;
GK[3:0] = 0100: 8 ms;
GK[3:0] = 0101: 10 ms;
GK[3:0] = 0110: 12 ms;
GK[3:0] = 0111: 14 ms;
GK[3:0] = 1000: 16 ms;
GK[3:0] = 1001: 18 ms;
GK[3:0] = 1010: 20 ms;
GK[3:0] = 1011: 22 ms;
GK[3:0] = 1100: 24 ms;
GK[3:0] = 1101: 26 ms;
GK[3:0] = 1110: 28 ms;
GK[3:0] = 1111: 30 ms;

4. A/D Gain, D/A Gain, Power Down and PCM Receive Path Cutoff (08H/88H),Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	0	0	1	0	0	0
I/O data	PD	PCMCT	GAD	GDA	0	0	0	0

Channel Power Down bit (PD) selects the operation mode on corresponding channel:

PD = 0: the corresponding channel is in normal operation;
PD = 1: the corresponding channel is powered down (default).

PCMCT bit determines the operation of PCM Receive Path on corresponding channel:

PCMCT = 0: PCM Receive Path is in normal operation (default);
PCMCT = 1: PCM Receive Path is cut off.

A/D Gain bit (GAD) sets the gain of analog A/D for corresponding channel:

GAD = 0: 0 dB (default);
GAD = 1: +6 dB.

D/A Gain bit (GDA) sets the gain of analog D/A for corresponding channel:

GDA = 0: 0 dB (default);
GDA = 1: -6 dB.

Attention: The lower 4 bits of the I/O data byte that follows this write-command (88H) must be '0000' to ensure proper operation.

5. Tone Generator Enable (09H/89H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}/W$	0	0	0	1	0	0	1
I/O data	*R*	*R*	*R*	*R*	1	1	TEN1	TEN0

TEN1 = 0: Tone1 generator is disabled (default);
TEN1 = 1: Tone1 generator is enabled.
TEN0 = 0: Tone0 generator is disabled (default);
TEN0 = 1: Tone0 generator is enabled.

Attention: The b2 and b3 of the I/O data byte that follows this write-command (89H) must be '11' to ensure proper operation.

ABSOLUTE MAXIMUM RATINGS

Rating	Com'l & Ind'l	Unit
Power Supply Voltage	≤ 6.5	V
Voltage on Any Pin with Respect to Ground	-0.5 to 5.5	V
Package Power Dissipation	≤1.5	W
Storage Temperature	-65 to +150	°C

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature	-40		+85	°C
Power Supply Voltage	4.75		5.25	V

NOTES:

1 .MCLK: 2.048 MHz or 4.096 MHz with tolerance of ± 50 ppm

ELECTRICAL CHARACTERISTICS

Digital Interface

Parameter	Description	Min	Typ	Max	Units	Test Conditions
V_{IL}	Input Low Voltage			0.8	V	All digital inputs
V_{IH}	Input High Voltage	2.0			V	All digital inputs
V_{OL}	Output Low Voltage			0.8	V	DX, I_L = 8 mA All other digital outputs, I_L = 4 mA.
V_{OH}	Output High Voltage	VDD - 0.6			V	DX, I_L = -8 mA All other digital outputs, I_L = -4 mA.
I_I	Input Current	-10		10	µA	All digital inputs, GND<VIN<VDD
I_{OZ}	Output Current in High-impedance State	-10		10	µA	DX
C_I	Input Capacitance			5	pF	

Power Dissipation

Parameter	Description	Min	Typ	Max	Units	Test Conditions
I_{DD1}	Operating Current		50		mA	All channels are active.
I_{DD0}	Standby Current			6	mA	All channels are powered down, with MCLK present.

Note: Power measurements are made at MCLK = 2.048MHz, outputs unloaded

Analog Interface

Parameter	Description	Min	Typ	Max	Units	Test Conditions
V_{OUT1}	Output Voltage, VOUT	2.25	2.4	2.6	V	Alternating ±zero µ-law PCM code applied to DR
V_{OUT2}	Output Voltage Swing, VOUT	3.25			Vp-p	RL = 300 Ω
R_I	Input Resistance, VIN	30	40	60	kΩ	0.25 V < VIN < 4.75 V
R_O	Output Resistance VOUT			20	Ω	0 dBm0, 1020 Hz PCM code applied to DR.
R_L	Load Resistance, VOUT	300			Ω	External loading
C_L	Load Capacitance, VOUT			100	pF	External loading

TRANSMISSION CHARACTERISTICS

0 dBm0 is defined as 0.775 Vrms for A-law and 0.769 Vrms for μ-law, both for 600 Ω load. Unless otherwise noted, the analog input is a 0 dBm0, 1020 Hz sine wave; the input amplifier is set for unity gain. The digital input is a PCM bit stream equivalent to that obtained by passing a 0 dBm0, 1020 Hz sine wave through an ideal encoder. The output level is sin(x)/x-corrected. Typical values are for V_{DD} = 5V and T_A=25°C.

Absolute Gain

Parameter	Description	Min	Typ	Max	Units	Test Conditions
G_{XA}	Transmit Gain, Absolute	-0.25		0.25	dB	Signal input of 0 dBm0, μ-law or A-law
G_{RA}	Receive Gain, Absolute	-0.25		0.25	dB	Measured relative to 0 dBm0, μ-law or A-law, PCM input of 0 dBm0 1020 Hz , R_L = 10 kΩ

Gain Tracking

Parameter	Description	Min	Typ	Max	Units	Test Conditions
GT_X	Transmit Gain Tracking					Tested by Sinusoidal Method, μ-law/A-law
	+3 dBm0 to –37 dBm0 (exclude –37 dBm0)	-0.25		0.25	dB	
	-37 dBm0 to -50 dBm0 (exclude –50 dBm0)	-0.5		0.50	dB	
	-50 dBm0 to -55 dBm0	-1.4		1.4	dB	
GT_R	Receive Gain Tracking					Tested by Sinusoidal Method, μ-law/A-law
	+3 dBm0 to - 40 dBm0 (exclude –40 dBm0)	-0.10		0.10	dB	
	-40 dBm0 to -50 dBm0 (exclude –50 dBm0)	-0.25		0.50	dB	
	-50 dBm0 to -55 dBm0	-0.50		0.50	dB	

Frequency Response

Parameter	Description	Min	Typ	Max	Units	Test Conditions
G_{XR}	Transmit Gain, relative to G_{XA}					
	f = 50 Hz			-30	dB	
	f = 60 Hz			-30	dB	
	f = 300 Hz	-0.10		0.20	dB	The High-pass filter is enabled.
	f = 300 Hz to 3000 Hz (exclude 3000 Hz)	-0.15		0.15	dB	
	f = 3000 Hz to 3400 Hz	-0.60		0.15	dB	
	f = 3600 Hz			-0.10	dB	
	f ≥ 4600 Hz			-35	dB	
G_{RR}	Receive Gain, relative to G_{RA}					
	f < 300 Hz			0	dB	
	f = 300 Hz to 3000 Hz (exclude 3000 Hz)	-0.15		0.15	dB	
	f = 3000 Hz to 3400 Hz	-0.60		0.15	dB	
	f = 3600 Hz			-0.20	dB	
	f ≥ 4600 Hz			-35	dB	

Group Delay

Parameter	Description	Min	Typ	Max	Units	Test Conditions
D_{XR}	Transmit Delay, Relative to 1800 Hz					
	f = 500 Hz – 600 Hz			280	μs	
	f = 600 Hz –1000 Hz			150	μs	
	f = 1000 Hz – 2600 Hz			80	μs	
	f = 2600 Hz – 2800 Hz			280	μs	
D_{RR}	Receive Delay, Relative to 1800 Hz					
	f = 500 Hz – 600 Hz			50	μs	
	f = 600 Hz –1000 Hz			80	μs	
	f = 1000 Hz – 2600 Hz			120	μs	
	f = 2600 Hz – 2800 Hz			150	μs	

Distortion

Parameter	Description	Min	Typ	Max	Units	Test Conditions
STDX	Transmit Signal to Total Distortion Ratio					ITU-T O.132
	A-law :					Sine Wave Method,Psophometric Weighted for A-law, C Message Weighted for μ-law.
	Input level = 0 dBm0	36			dB	
	Input level = -30 dBm0	36			dB	
	Input level = -40 dBm0	30			dB	
	Input level = -45 dBm0	24			dB	
	μ-law :					
	Input level = 0 dBm0	36			dB	
	Input level = -30 dBm0	36			dB	
	Input level = -40 dBm0	31			dB	
	Input level = -45 dBm0	27			dB	
STDR	Receive Signal to Total Distortion Ratio					ITU-T O.132
	A-law :					
	Input level = 0 dBm0	36			dB	Sine Wave Method,Psophometric Weighted for A-law;Sine Wave Method,C Message Weighted for μ-law;
	Input level = -30 dBm0	36			dB	
	Input level = -40 dBm0	30			dB	
	Input level = -45 dBm0	24			dB	
	μ-law :					
	Input level = 0 dBm0	36			dB	
	Input level = -30 dBm0	36			dB	
	Input level = -40 dBm0	31			dB	
	Input level = -45 dBm0	27			dB	
SFDX	Single Frequency Distortion, Transmit			-42	dBm0	200 Hz - 3400 Hz, 0 dBm0 input, output any other single frequency ≤ 3400 Hz
SFDR	Single Frequency Distortion, Receive			-42	dBm0	200 Hz - 3400 Hz, 0 dBm0 input, output any other single frequency ≤ 3400 Hz
IMD	Intermodulation Distortion			-42	dBm0	Transmit or receive,two frequencies in the range (300 Hz– 3400 Hz) at –6 dBm0

Noise

Parameter	Description	Min	Typ	Max	Units	Test Conditions
NXC	Transmit Noise, C Message Weighted for μ-law			15	dBrnC0	
NXP	Transmit Noise, Psophometric Weighted for A-law			-70	dBm0p	
NRC	Receive Noise, C Message Weighted for μ-law			10	dBrnC0	
NRP	Receive Noise, Psophometric Weighted for A-law			-80	dBm0p	
NRS	Noise, Single Frequency			-53	dBm0	VIN = 0 Vrms, tested at VOUT
	f = 0 kHz – 100 kHz					
PSRX	Power Supply Rejection Transmit					VDD = 5.0 VDC + 100 mVrms
	f = 300 Hz – 3.4 kHz	40			dB	
	f = 3.4 kHz – 20 kHz	25			dB	
PSRR	Power Supply Rejection Receive					PCM code is positive one LSB, VDD = 5.0 VDC + 100 mVrms
	f = 300 Hz – 3.4 kHz	40			dB	
	f = 3.4 kHz – 20 kHz	25			dB	
SOS	Spurious Out-of-Band Signals at VOUT Relative to Input PCM code applied:					0 dBm0, 300 Hz – 3400 Hz input
	4600 Hz – 20 kHz			-40	dB	
	20 kHz – 50 kHz			-30	dB	

Interchannel Crosstalk

Parameter	Description	Min	Typ	Max	Units	Test Conditions
XT_{X-R}	Transmit to Receive Crosstalk		-85	-78	dB	300 Hz – 3400 Hz, 0 dBm0 signal into VIN of interfering channel. Idle PCM code into channel under test.
XT_{R-X}	Receive to Transmit Crosstalk		-85	-80	dB	300 Hz – 3400 Hz, 0 dBm0 PCM code into interfering channel. VIN = 0 Vrms for channel under test.
XT_{X-X}	Transmit to Transmit Crosstalk		-85	-78	dB	300 Hz – 3400 Hz, 0 dBm0 signal into VIN of interfering channel. VIN = 0 Vrms for channel under test.
XT_{R-R}	Receive to Receive Crosstalk		-85	-80	dB	300 Hz – 3400 Hz, 0 dBm0 PCM code into interfering channel. Idle PCM code into channel under test.

Note: Crosstalk into the transmit channels (VIN) can be significantly affected by parasitic capacitive coupling from VOUT outputs. PCB layouts should be arranged to minimize these parasitics.

Intrachannel Crosstalk

Parameter	Description	Min	Typ	Max	Units	Test Conditions
XT_{X-R}	Transmit to Receive Crosstalk		-80	-70	dB	300 Hz – 3400 Hz, 0 dBm0 signal into VIN. Idle PCM code into DR.
XT_{R-X}	Receive to Transmit Crosstalk		-80	-70	dB	300 Hz – 3400 Hz, 0 dBm0 PCM code into DR. VIN = 0 Vrms.

Note: Crosstalk into the transmit channels (VIN) can be significantly affected by parasitic capacitive coupling VOUT outputs. PCB layouts should be arranged to minimize these parasitics.

TIMING CHARACTERISTICS

Reset and Clock

Parameter	Description	Min	Typ	Max	Units	Test Conditions
t0	Reset pulse width	50			µs	
t1	MCLK pulse width	48			ns	
t2	MCLK Rise and Fall time			15	ns	
t3	DCL period F = 2.048 kHz F = 4.096 kHz		488 244		ns	
t4	DCL Rise and Fall Time			60	ns	
t5	DCL pulse width	90			ns	

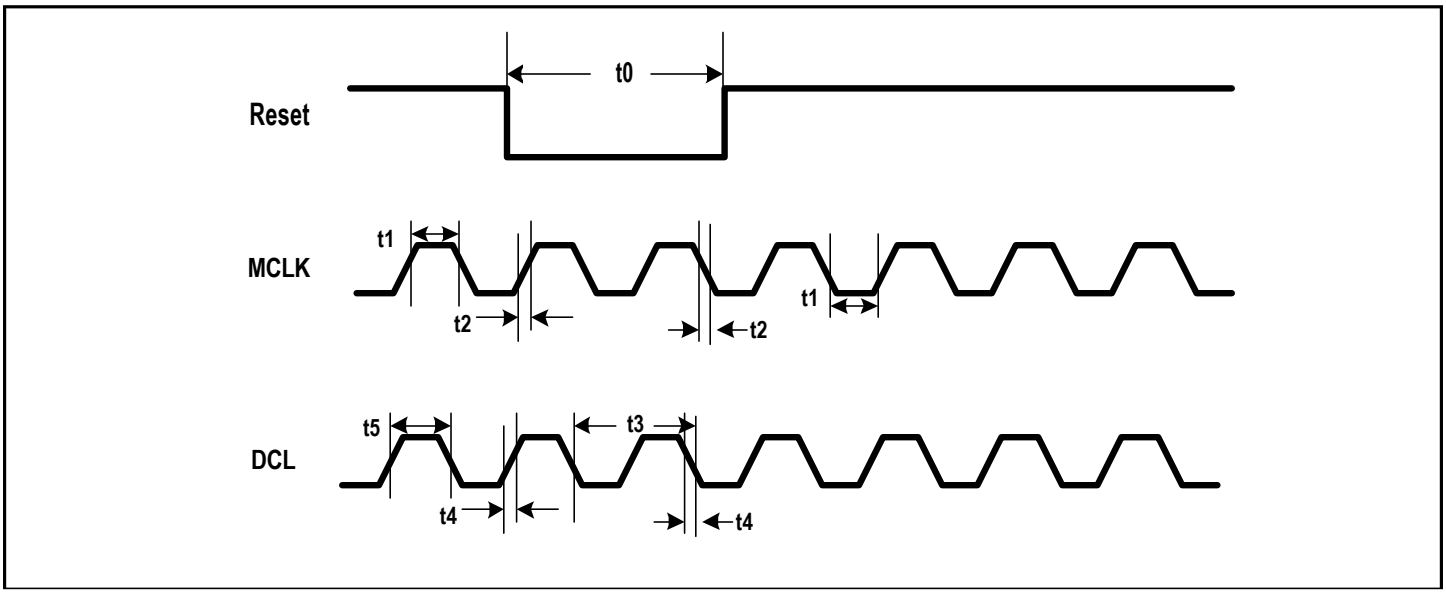


Figure 9. Reset and Clock Timing

GCI Interface

Parameter	Description	Min	Typ	Max	Units	Test Conditions
t71	FSC rise and fall time			60	ns	
t72	FSC setup time	70		t3 - 50	ns	
t73	FSC hold time	50			ns	
t74	FSC high pulse width	130			ns	
t75	DU data delay time			100	ns	
t77	DD data setup time	110			ns	
t78	DD data hold time	50			ns	

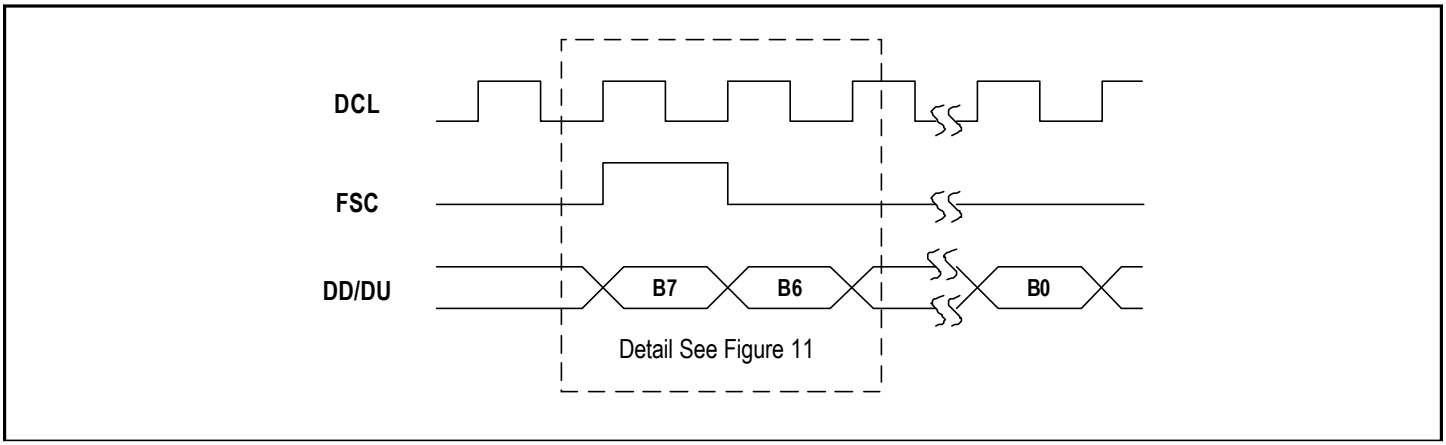
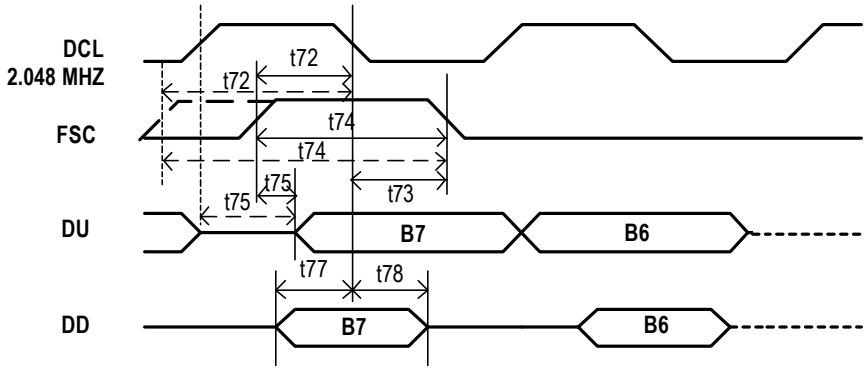
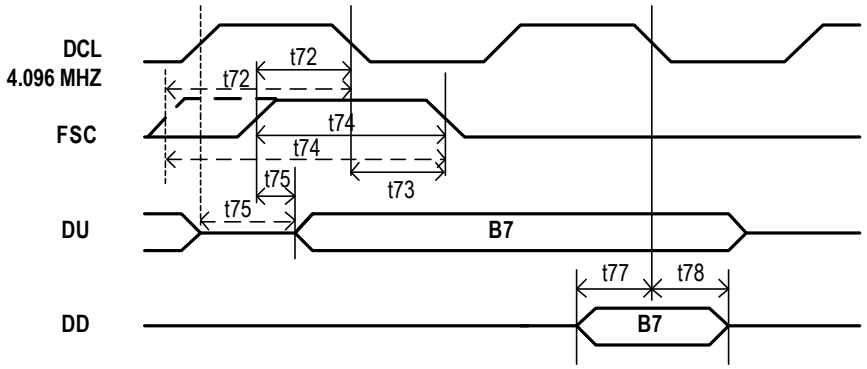


Figure 10. GCI Interface Timing



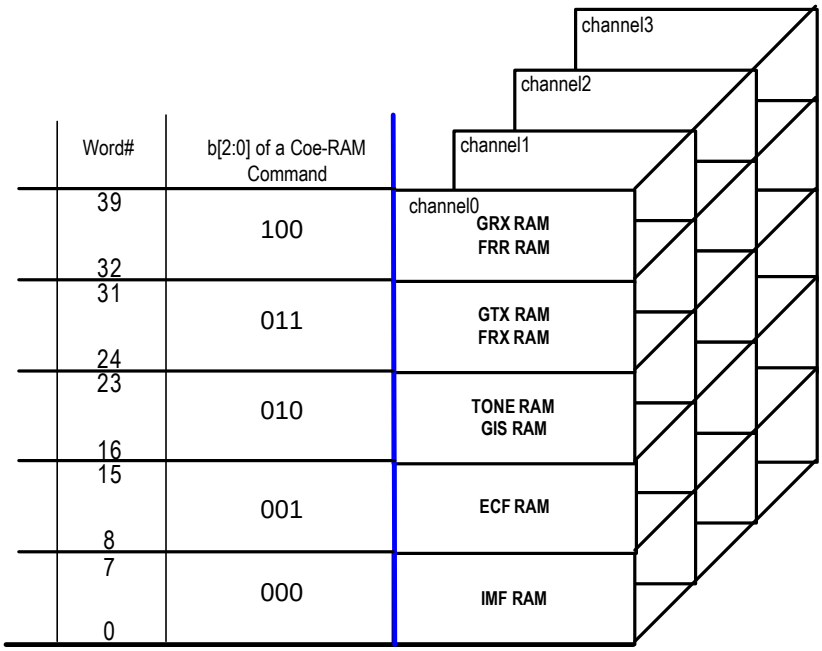
DCL Operation at 2.048 MHz



DCL Operation at 4.096 MHz

Figure 11. Transmit and Receive Timing for GCI Interface (Detailed Timing for Figure 10)

APPENDIX: IDT821064 Coe-RAM Address Mapping



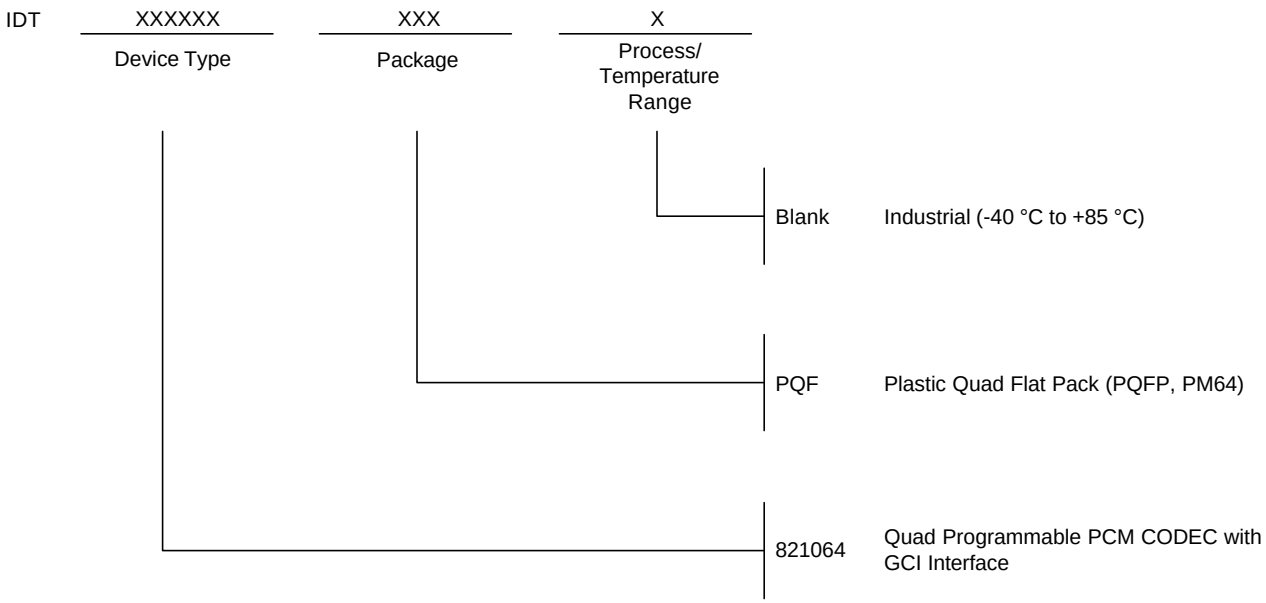
Generally, 6 bits of address are needed to locate each word of the 40 Coe-RAM words. The 40 words of Coe-RAM are divided into 5 blocks with 8 words per block in IDT821064, so only 3 bits of address are needed to locate each of the block. When the address of a Coe-RAM block (b[2:0]) is specified in a Coe-RAM Command, all 8 words of this block will be addressed automatically, with the highest order word first (IDT821064 will count down from '111' to '000' so that it accesses the 8 words successively). Refer to page 16 and 17 for more information.

The address assignment for the 40 words Coe-RAM is shown in the following table. The number in the "Address" column is the actual hexadecimal address of the Coe-RAM word, as the IDT821064 handles the lower 3 bits automatically, only the higher 3 bits (in bold style) are needed for a Coe-RAM Command. It should be noted that, when addressing the GRX RAM, the FRR RAM will be addressed at the same time.

Table 7 - Coe-RAM Address Allocation

Word #	Address	Function	Word #	Address	Function
39	**100**,111	GRX RAM	19	**010**,011	GIS RAM
38	**100**,110	FRR RAM	18	**010**,010	
37	**100**,101		17	**010**,001	
36	**100**,100		16	**010**,000	
35	**100**,011		15	**001**,111	ECF RAM
34	**100**,010		14	**001**,110	
33	**100**,001		13	**001**,101	
32	**100**,000		12	**001**,100	
31	**011**,111	GTX RAM	11	**001**,011	
30	**011**,110	FRX RAM	10	**001**,010	
29	**011**,101		9	**001**,001	
28	**011**,100		8	**001**,000	
27	**011**,011		7	**000**,111	IMF RAM
26	**011**,010		6	**000**,110	
25	**011**,001		5	**000**,101	
24	**011**,000		4	**000**,100	
23	**010**,111	Amplitude Coefficient of Tone Generator 1	3	**000**,011	
22	**010**,110	Frequency Coefficient of Tone Generator 1	2	**000**,010	
21	**010**,101	Amplitude Coefficient of Tone Generator 0	1	**000**,001	
20	**010**,100	Frequency Coefficient of Tone Generator 0	0	**000**,000	

ORDERING INFORMATION



Data Sheet Document History

12/21/2001	pgs. 11, 23, 26, 27
01/23/2002	pgs. 1, 2, 4, 10, 13, 14, 17
02/19/2002	pg. 27
10/30/2002	pgs. 16, 23, 25, 27
01/09/2003	pgs. 1, 14, 18, 24, 33
02/20/2003	pg. 27
03/14/2003	pgs. 13, 18

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