



# LC651204N/F/L, LC651202N/F/L

## 4-Bit Single-Chip Microcontroller for Small-Scale Control Applications

### Preliminary

#### Overview

The LC651204N/F/L and LC651202N/F/L are small-scale application microcontroller products in Sanyo's LC6500 series of 4-bit single-chip CMOS microcontrollers, and as such they fully support the basic architecture and instruction set of that series. These microcontrollers are provided in a 30-pin package and include 2 kilobytes (KB) and 4 KB of on-chip ROM. These products are appropriate for use in a wide range of applications, from applications that use a small number of controls and circuits that were previously implemented in standard logic to larger scale applications including audio equipment such as decks and players, office equipment, communications equipment, automotive equipment, and home appliances. Except for the lack of an A/D converter, these microcontrollers provide the same functionality as the LC651104:02N/F/L.

#### Features

- (1) Fabricated in a CMOS process for low power (An instruction-controlled standby function is provided.)
- (2) ROM/RAM
  - LC651204N/F/L - ROM: 4K × 8 bits, RAM: 256 × 4 bits
  - LC651202N/F/L - ROM: 2K × 8 bits, RAM: 256 × 4 bits
- (3) Instruction set: The 80-instruction set provided by all members of the LC6500 series.
- (4) Wide operating power-supply voltage range of 2.5 to 5.5 volts (L version).
- (5) Instruction cycle time: 0.92μs (F version)
- (6) On-chip serial I/O circuit
- (7) Highly flexible I/O ports
  - Number of ports: 6 ports with a total of 22 pins
  - All ports: Can be used for both input and output
    - I/O voltage: 15V maximum (Only for C, D, E, and F ports with open-drain output specifications)
    - Output current: 20mA maximum sink current (Capable of directly driving LEDs.)
  - Options that allow specifications to be customized to match those of the application system.
    - Specification of open-drain output or built-in pull-up resistor: Can be specified for all ports in bit units.
    - Specification of the output level at reset: Can be specified to be high or low for ports C and D in port units.
- (8) Interrupt functions
  - Timer overflow vector interrupt (The interrupt state can be tested by the CPU.)
  - Vector interrupts initiated by the INT pin or full/empty states of the serial I/O circuit. (The interrupt state can be tested by the CPU.)
- (9) Stack levels: 8 levels (shared with interrupts)
- (10) Timers: 4-bit prescaler plus 8-bit programmable timers
- (11) Clock oscillator options to match application system specifications.
  - Oscillator circuit options: 2-pin ceramic oscillator (N, F and L versions)
  - Divider circuit option: No divider, built-in divide-by-three circuit, built-in divide-by-four circuit (N and L versions)
- (12) Supports continuous output of a square wave signal (with a period 64 times the cycle time)
- (13) Watchdog timer
  - RC time constant scheme
  - A watchdog timer function can be allocated to one of the external pins as an option.
- (14) EP version: LC65E1104; OTP version: LC65P1104

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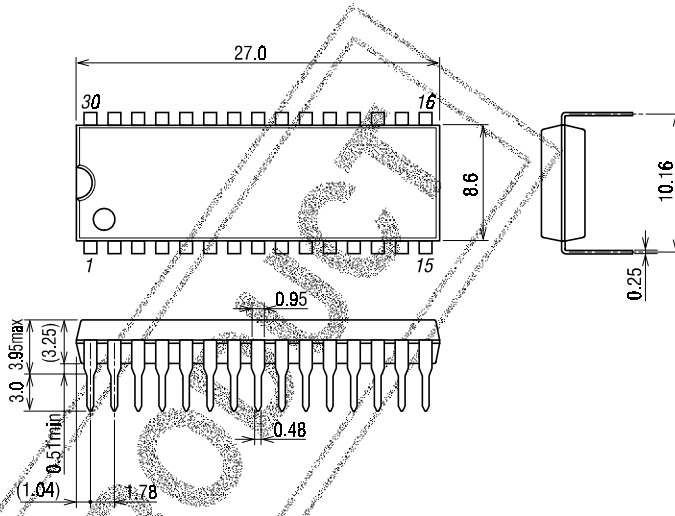
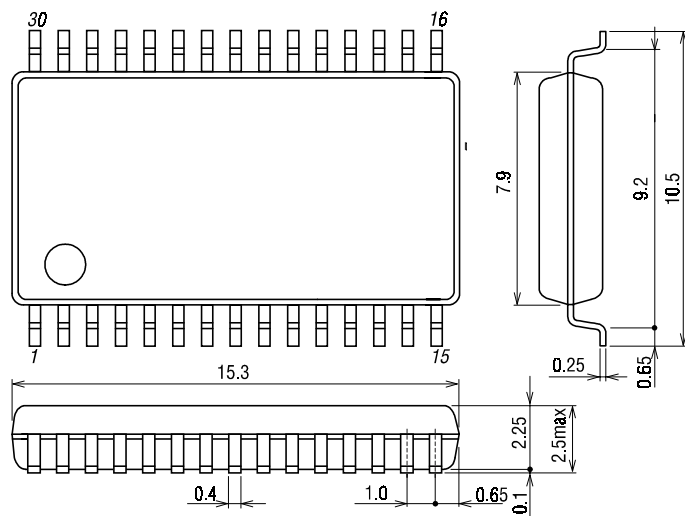
**Package Dimensions**

(unit : mm)  
3073A

(unit : mm)  
3196A

[LC651204N/F/L, 651202N/F/L]

[LC651204N/F/L, 651202N/F/L]



SANYO : MFP-30S

SANYO : DIP-30SD

[Notes]

The package drawings shown above are provided without error tolerances and are for reference purposes only. Contact Sanyo for official package drawings.

**Function Overview**

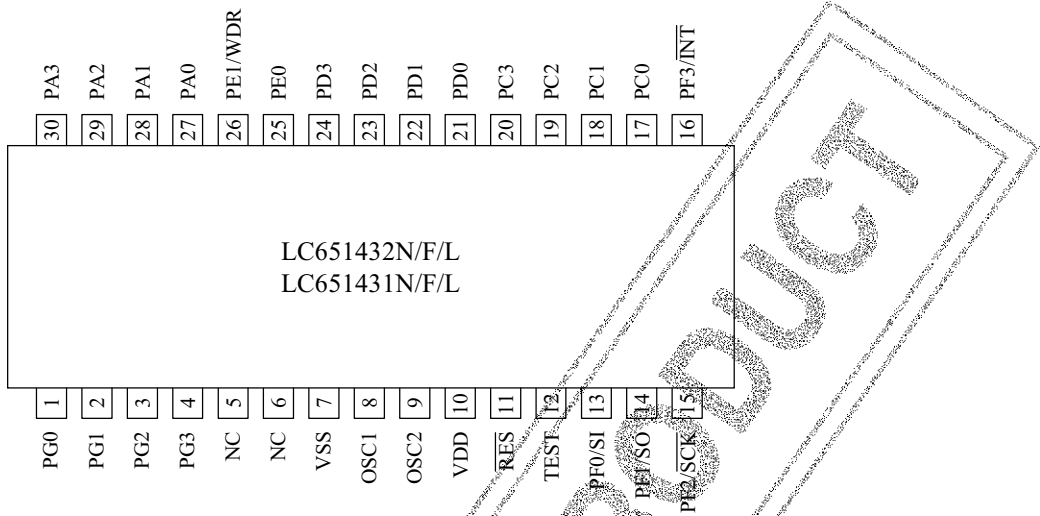
Item		LC651204N/1202N	LC651204F/1202F	LC651204L/1202L
Memory	ROM	4096×8 bits(1204N) 2048×8bits(1202N)	4096×8 bits(1204F) 2048×8 bits(1202F)	4096×8 bits(1204L) 2048×8 bits(1202L)
	RAM	256×4 bits(1204/1202N)	256×4 bits(1204/1202F)	256×4 bits(1204/1202L)
Instruction	Instruction set	80	80	80
	Table reference	Supported	Supported	Supported
Built-in functions	Interrupts	1 external, 1 internal	1 external, 1 internal	1 external, 1 internal
	Timers	4-bit prescaler+8-bit timer	4-bit prescaler+8-bit timer	4-bit prescaler+8-bit timer
	Stack levels	8	8	8
	Standby function	Supports standby mode entered by the HALT instruction	Supports standby mode entered by the HALT instruction	Supports standby mode entered by the HALT instruction
I/O ports	Number of ports	22 I/O pins	22 I/O pins	22 I/O pins
	Serial ports	4-bit or 8-bit I/O	4-bit or 8-bit I/O	4-bit or 8-bit I/O
	I/O voltage	15V max.	15V max.	15V max.
	Output current	10mA typ. 20mA max.	10mA typ. 20mA max.	10mA typ. 20mA max.
	I/O circuit types	Open drain (n-channel) or built-in pull-up resistor output selectable on a per-bit basis.		
	Output levels at reset	High or low can be selected in port units. (ports C and D only)		
	Square wave output	Supported	Supported	Supported
Characteristics	Minimum cycle time	2.77μs (VDD≥3V)	0.92μs (VDD≥3V)	3.84μs (VDD≥2.5V)
	Power-supply voltage	3 to 5.5V	3 to 5.5V	2.5 to 5.5V
	Power-supply current	1.5mA typ.	2mA typ.	1.5mA typ.
Oscillator	Oscillator	Ceramic (800K, 1MHz, 4MHz)	Ceramic (4MHz)	Ceramic (800K, 1MHz, 4MHz)
	Divider circuit option	1/1, 1/3, 1/4	1/1	1/1, 1/3, 1/4
Other functions	Package	DIP30S-D MFP30S	DIP30S-D MFP30S	DIP30S-D MFP30S

[Notes]

Sanyo will announce details on oscillator elements and oscillator circuit constants as recommended application circuits are developed. Customers should check with Sanyo for the latest information as the development process progresses.

## Pin Assignment

Common assignments for the DIP and MFP packages



[Notes]

NC pins must be connected to VSS.

Top view

## Pin Functions

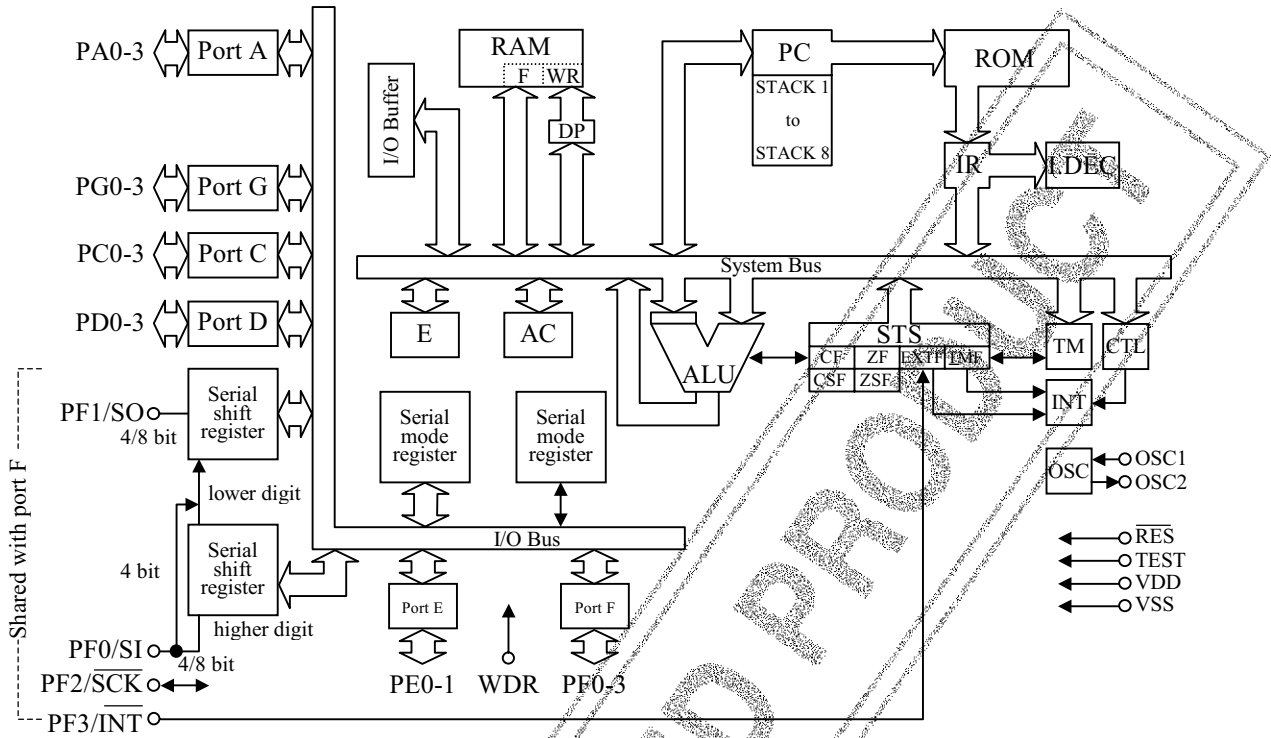
Pin	Function
OSC1, OSC2	Connections for a ceramic oscillator element
$\overline{\text{RES}}$	Reset
PA0 to 3	I/O dual-function port A0 to A3
PC0 to 3	I/O dual-function port C0 to C3
PD0 to 3	I/O dual-function port D0 to D3
PE0 to 1	I/O dual-function port E0 to E1
PF0 to 3	I/O dual-function port F0 to F3
PG0 to 3	I/O dual-function port G0 to G3
TEST	Test
$\overline{\text{INT}}$	Interrupt request
SI	Serial input
SO	Serial output
$\overline{\text{SCK}}$	Serial clock input and output
NC	No connection
WDR	Watchdog reset

[Notes]

The SI, SO,  $\overline{\text{SCK}}$  and  $\overline{\text{INT}}$  pins are shared function pins that are also used as PF0 to PF3.

System Block Diagram

LC651204N/F/L, LC651202N/F/L



- RAM : Data memory
- F : Flag
- WR : Working register
- AC : Accumulator
- ALU : Arithmetic and logic unit
- DP : Data pointer
- E : E register
- CTL : Control register
- OSC : Oscillator circuit
- TM : Timer
- STS : Status register
- ROM : Program memory
- PC : Program counter
- INT : Interrupt control
- IR : Instruction register
- I-DEC : Instruction decoder
- CF, CSF : Carry flag, carry save flag
- ZF, ZSF : Zero flag, zero save flag
- EXTF : External interrupt request flag
- TMF : Internal interrupt request flag

## Development Support

Sanyo provides the following items to support application development using the LC651204 and LC651202.

### 1. User's manual

The "LC651104/1102 User's Manual" is used with these microcontrollers.

### 2. Development tool manual

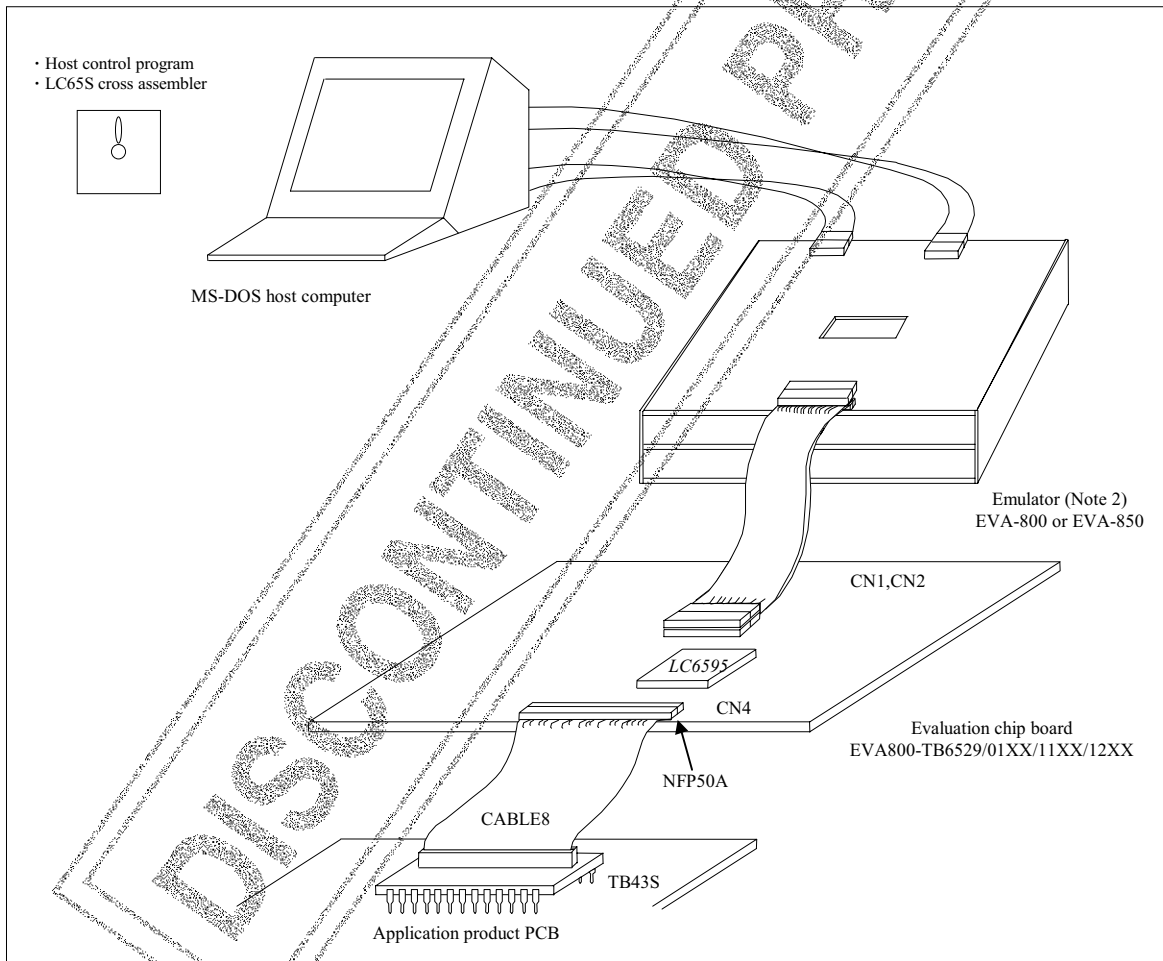
See the "EVA800-LC651104/1102 Development Tool Manual" for details on use of the EVA-800 system.

### 3. Development tool

- Program development (using the EVA-800 system)
  - MS-DOS host computer system \*1
  - Cross assembler ... MS-DOS-based cross assembler: LC65S.EXE
  - Evaluation chip: LC6595
  - Emulator: The EVA-800 main unit plus the evaluation chip
- Program development (using the EVA-800 system): Use the EVA86K-ECB651100.
- Program evaluation
  - The <LC65E1104> on-chip EPROM microcontroller

## Development Support System

### EVA-800 System



### [Notes]

1. MS-DOS is a registered trademark of Microsoft Corporation
2. Here, "EVA-800" is a generic term for several emulators. Suffixes (A, B, etc.) will be attached to the name as new versions are developed. Note that the EVA-800 emulator (i.e., the model with no suffix) is an old version and cannot be used.

Pin Functions

Pin	Pin no.	I/O	Function	Option	State at reset	Handling when unused
VDD	1	-	Power supply	-	-	-
VSS	1	-				
OSC1	1	Input	• System clock oscillator	(1) External clock	-	-
OSC2	1	Output	Connect an external ceramic oscillator element to these pins • Leave OSC2 open if an external clock is supplied.	(2) Two-pin ceramic oscillator (3) Divider circuit option 1. No divider circuit 2. Divide-by-three circuit 3. Divide-by-four circuit		
PA0 to PA3	4	I/O	• I/O port A0 to A3 Input in 4-bit units using the IP instruction Output in 4-bit units using the OP instruction Port bits can be tested in bit units using the BP and BNP instructions. Port bits can be set or cleared in bit units using the SPB and RPB instructions. • PA3 is used for standby control. • Applications must be designed so that no chattering (e.g. switch bounce) occurs on the PA3 pin during a HALT instruction execution cycle.	(1) Output open drain (2) Built-in pull-up resistor • Options (1) and (2) can be specified in bit units.	High-level output (i.e. the output n-channel transistor will be off)	Open drain output select the options, connect to VSS
PC0 to PC3	4	I/O	• I/O port C0 to C3 The PC0 to PC3 pin functions are identical to those of the PA0 to PA3 pins. • High or low can be specified as the output at reset as an option. Note: These pins do not have a standby control function.	(1) Output open drain (2) Built-in pull-up resistor (3) High-Level output at reset (4) Low-Level output at reset • Options (1) and (2) can be specified in bit units • Options (3) and (4) are specified in 4-bit units	• High-level output • Low-level output (Depending on the option specified.)	The same as PA0 to PA3.
PD0 to PD3	4	I/O	• I/O port D0 to D3 The PD0 to PD3 pin functions and options are identical to those of the PC0 to PC3 pins.	The same as PC0 to PC3.	The same as PC0 to PC3.	The same as PA0 to PA3.

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### Oscillator Circuit Options

Option	Circuit	Conditions and notes
External clock		The OSC2 pin must be left open.
Ceramic oscillator		

### Divider Options

Option	Circuit	Conditions and notes
No divider (1/1)		<ul style="list-style-type: none"> <li>• Supports both oscillator options.</li> <li>• The oscillator frequency or the external clock frequency must not exceed 1444 kHz (LC651204N and LC651202N)</li> <li>• The oscillator frequency or the external clock frequency must not exceed 4330 kHz (LC651204F and LC651202F)</li> <li>• The oscillator frequency or the external clock frequency must not exceed 1040 kHz (LC651204L and LC651202L)</li> </ul>
Built-in divide-by-three circuit		<ul style="list-style-type: none"> <li>• Supports both oscillator options.</li> <li>• The oscillator frequency or the external clock frequency must not exceed 4330 kHz</li> </ul>
Built-in divide-by-four circuit		<ul style="list-style-type: none"> <li>• Supports both oscillator options.</li> <li>• The oscillator frequency or the external clock frequency must not exceed 4330 kHz</li> </ul>

[Caution]

The oscillator and divider options are summarized in the following tables. The information presented in those tables is crucial when using these products.



**LC651204N/F/L, LC651202N/F/L**

Divider Options for the LC651204N/1202N, LC651204F/1202F and LC651204L/1202L

**LC651204N/1202N**

Circuit type	Frequency	Divider option (cycle time)	VDD range	Notes
Ceramic oscillator	800kHz	1/1 (5μs)	3 to 5.5V	
	1MHz	1/1 (4μs)	3 to 5.5V	
	4MHz	1/3 (3μs) 1/4 (4μs)	3 to 5.5V 3 to 5.5V	This frequency cannot be used with the 1/1 divider (i.e., no divider circuit) option.
External clock generated by a two-terminal RC oscillator circuit	670k to 1444kHz	1/1 (6 to 2.77μs)	3 to 5.5V	
	2000k to 4330kHz	1/3 (6 to 2.77μs)	3 to 5.5V	
	2600k to 4330kHz	1/4 (6 to 3.70μs)	3 to 5.5V	
Use of external clock with the ceramic oscillator option selected	Driving the circuit with an external clock is not possible. To use external clock drive, specify the two-terminal RC oscillator option.			

**LC651204F/1202F**

Circuit type	Frequency	Divider option (cycle time)	VDD range	Notes
Ceramic oscillator	4MHz	1/1 (1μs)	3 to 5.5V	
External clock generated by a two-terminal RC oscillator circuit	670k to 4330kHz	1/1 (6 to 0.92μs)	3 to 5.5V	
Use of external clock with the ceramic oscillator option selected	Driving the circuit with an external clock is not possible. To use external clock drive, specify the two-terminal RC oscillator option.			

**LC651204L/1202L**

Circuit type	Frequency	Divider option (cycle time)	VDD range	Notes
Ceramic oscillator	800kHz	1/1 (5μs)	2.5 to 5.5V	
	1MHz	1/1 (4μs)	2.5 to 5.5V	
	4MHz	1/4 (4μs)	2.5 to 5.5V	This frequency cannot be used with the 1/1, 1/3 divider (i.e., no divider circuit) option.
External clock generated by a two-terminal RC oscillator circuit	670k to 1040kHz	1/1 (6 to 3.84μs)	2.5 to 5.5V	
	2000k to 3120kHz	1/3 (6 to 3.84μs)	2.5 to 5.5V	
	2600k to 4160kHz	1/4 (6 to 3.84μs)	2.5 to 5.5V	
Use of external clock with the ceramic oscillator option selected	Driving the circuit with an external clock is not possible. To use external clock drive, specify the two-terminal RC oscillator option.			

### Port C and D Output State at Reset Options

The output levels at reset of the I/O ports C and D can be selected form the following two options, which are specified in 4-bit units.

Option	Conditions and notes
High-level output at reset	Ports C and D in 4-bit units
Low-level output at reset	Ports C and D in 4-bit units

### Port Output Circuit Type Option

The output circuit types of the I/O ports can be selected form the following two options in bit units.

Option	Circuit	Conditions and notes
Open drain output		Ports A, C, D, E, F and G
Pull-up resistor output		

### Watchdog Timer Reset Option

Whether the PE1/WDR pin functions as the normal port PE1 or as the WDR watchdog timer reset pin can be selected as an option.

LC651204N, LC651202N

Absolute Maximum Ratings at VSS=0V and Ta=25°C

Parameter	Symbol	Applicable pins/notes	Conditions	Ratings	unit
Maximum supply voltage	VDD max		VDD	-30 to +7.0	V
Output voltage	VO		OSC2	Voltages up to any generated voltage are allowed.	
Input voltage	VI (1)		OSC1 *1	-0.3 to VDD +0.3	mA
	VI (2)		TEST, RES	-0.3 to VDD +0.3	
I/O voltage	VIO (1)	PC0 to 3, PD0 to 3, PE0, 1, PF0 to 3	OD specification ports	-0.3 to +15	
	VIO (2)	PC0 to 3, PD0 to 3, PE0, 1, PF0 to 3	PU specification ports	-0.3 to VDD +0.3	
	VIO (3)	PA0 to 3, PG0 to 3		-0.3 to VDD +0.3	
Peak output current	IOP		I/O ports	-2 to +20	mA
Average output current	IOA	Average value per pin over a 100-ms period	I/O ports	-2 to +20	
	ΣIOA (1)	Total current for pins PC0 to 3, PD0 to 3, and PE0 to 1*2	PC0 to PC3 PD0 to PD3 PE0 to PE1	-15 to +100	
	ΣIOA (2)	Total current for pins PF0 to 3, PG0 to 3, and PA0 to 3*2	PF0 to PF3 PG0 to PG3 PA0 to PA3	-15 to +100	
Allowable power dissipation	Pd max(1)	Ta = -40 to +85°C (DIP package)		250	mW
	Pd max(2)	Ta = -40 to +85°C (MFP package)		150	
Operation temperature	Topr			-40 to +85	°C
Storage temperature	Tstg			-55 to +125	

Allowable Operating Range at Ta=-40°C to +85°C, VSS=0V, VDD=3.5 to 5.5V

(unless otherwise specified)

Parameter	Symbol	Conditions	Applicable pins/notes	Ratings			unit	
				min.	typ.	max.		
Operating power-Supply voltage	VDD		VDD	3.0		5.5	V	
Standby power-Supply voltage	VST	RAM and register values retained *3	VDD	1.8		5.5		
Input high-level voltage	VIH(1)	Output n-channel transistors off	OD specification ports C, D, E, and F	0.7VDD		13.5		
	VIH(2)	Output n-channel transistors off	PU specification ports C, D, E, and F	0.7VDD		VDD		
	VIH(3)	Output n-channel transistors off	Port A, G	0.7VDD		VDD		
	VIH(4)	Output n-channel transistors off	The INT, SCK, and SI pins with OD specifications	0.8VDD		13.5		
	VIH(5)	Output n-channel transistors off	The INT, SCK, and SI pins with PU specifications	0.8VDD		VDD		
	VIH(6)	VDD = 3.8 to 5.5V		RES	0.8VDD		VDD	
	VIH(7)	External clock specifications		OSC1	0.8VDD		VDD	

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Parameter	Symbol	Conditions	Applicable pins/notes	Ratings			unit	
				min.	typ.	max.		
Input low-level voltage	VIL(1)	Output n-channel transistors off	VDD = 4 to 5.5V	Port	VSS		0.2VDD	V
	VIL(2)	Output n-channel transistors off	VDD = 3 to 5.5V	Port	VSS		0.2VDD	
	VIL(3)	Output n-channel transistors off	VDD = 4 to 5.5V	$\overline{\text{INT}}$ , $\overline{\text{SCK}}$ , $\overline{\text{SI}}$	VSS		0.2VDD	
	VIL(4)	Output n-channel transistors off	VDD = 3 to 5.5V	$\overline{\text{INT}}$ , $\overline{\text{SCK}}$ , $\overline{\text{SI}}$	VSS		0.2VDD	
	VIL(5)	External clock specifications	VDD = 4 to 5.5V	OSC1	VSS		0.2VDD	
	VIL(6)	External clock specifications	VDD = 3 to 5.5V	OSC1	VSS		0.2VDD	
	VIL(7)		VDD = 4 to 5.5V	TEST	VSS		0.2VDD	
	VIL(8)		VDD = 3 to 5.5V	TEST	VSS		0.2VDD	
	VIL(9)		VDD = 4 to 5.5V	$\overline{\text{RES}}$	VSS		0.2VDD	
	VIL(10)		VDD = 3 to 5.5V	$\overline{\text{RES}}$	VSS		0.2VDD	
Operating frequency (cycle time)	fop (Tcyc)	Frequencies up to 4.33MHz are supported if the divide-by-three or divide-by-four divider circuit option is used.	VDD = 3 to 5.5V		670 (6)		1444 (2.77)	kHz (μs)
External clock conditions Frequency Pulse width Rise and fall times	text	Figure 1. The divide-by-three or divide-by-four divider circuit option must be used if the clock frequency exceeds 1.444MHz.	VDD = 3 to 5.5V	OSC1	670		4330	kHz
	textH, textL		VDD = 3 to 5.5V	OSC1	69			ns
	textR, textF		VDD = 3 to 5.5V	OSC1				50
Guaranteed oscillator constants Ceramic oscillator		Figure 2				See Table 1.		

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Electrical Characteristics at Ta=-40°C to +85°C, VSS=0V, VDD=3.0 to 5.5V

(unless otherwise specified)

Parameter	Symbol	Conditions	Applicable pins/notes	Ratings			unit
				min.	typ.	max.	
Input high-level current	IIH(1)	Output n-channel transistors off (Includes the n-channel transistors off leakage current.) VIN= 13.5V	Ports C, D, E, and F with open-drain specifications			5.0	μA
	IIH(2)	Output n-channel transistors off (Includes the n-channel transistors off leakage current.) VIN= VDD	Ports A and G with open-drain specifications			1.0	
	IIH(3)	External clock mode, VIN= VDD	OSC1			1.0	
Input low-level current	III(1)	Output n-channel transistors off VIN= VSS	Ports with open-drain specifications	-1.0			
	III(2)	Output n-channel transistors off VIN= VSS	Ports with pull-up resistor specifications	-1.3	-0.35		mA
	III(3)	VIN= VSS	RES	-45	10		μA
	III(4)	External clock mode, VIN= VSS	OSC1	-1.0			
Output high-level voltage	VOH(1)	IOH= -50μA VDD= 4.0 to 5.5V	Ports with pull-up resistor specifications	VDD-1.2			V
	VOH(2)	IOH= -10μA VDD= 3.0 to 5.5V	Ports with pull-up resistor specifications	VDD-0.5			
Output low-level voltage	VOL(1)	IOL= 10mA VDD= 4.0 to 5.5V	Port			1.5	
	VOL(2)	IOL= 1 mA, with the IOL for all ports no more than 1 mA. VDD= 3.0 to 5.5V	Port			0.5	
Schmitt characteristics	Hysteresis voltage	VHIS			0.1VDD		
	High-level threshold voltage	VtH	RES, INT, SCK and SI OSC1 with Schmitt specifications *4	0.4VDD		0.8VDD	
	Low-level threshold voltage	VtL		0.2VDD		0.6VDD	
Current drain	IDDOP(1)	Operating, output n-channel transistors off. Ports = VDD Figure 2, 4 MHz, divide-by-three circuit	VDD		1.5	5	mA
Ceramic oscillator	IDDOP(2)	Figure 2, 4 MHz, divide-by-four circuit	VDD		1.5	4	
	IDDOP(3)	Figure 2, 800 kHz	VDD		1.5	4	
External clock Standby mode	IDDOP(4)	670 to 1444 kHz, no divider circuit 2000 to 4330 kHz, divide-by-three circuit 2600 to 4330 kHz, divide-by-four circuit	VDD		1.5	5	
	IDDst	Output n-channel transistors off. VDD = 5.5V Ports = VDD, VDD= 3V	VDD VDD		0.05 0.025	10 5	μA

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Parameter	Symbol	Conditions	Applicable pins/notes	Ratings			unit	
				min.	typ.	max.		
Oscillator characteristics Ceramic oscillator Oscillator frequency Oscillator stabilization time	fCFOSC *5	Figure 2, fo = 800 kHz	OSC1, OSC2	768	800	832	kHz	
		Figure 2, fo = 1 MHz	OSC1, OSC2	960	1000	1040		
		Figure 2, fo = 4 MHz, divide-by-three or divide-by-four circuit	OSC1, OSC2	3840	4000	1460		
	tCFS	Figure 3, fo = 800 kHz, 1 MHz, 4 MHz Divide-by-three or divide-by-four circuit				5	ms	
Pull-up resistors I/O ports	Rpp	Output n-channel transistors off VIN = VSS, VDD = 5V	Ports with pull-up resistor specifications	8	14	30	kΩ	
	RES	VIN = VSS, VDD = 5V	RES	100	250	400		
External reset characteristics Reset time	tRST				See Figure 4.			
Pin capacitance	Cp	f = 1MHz With all pins other than the pin being measured at VIN = VSS			10		pF	
Serial clock Input clock cycle time Output clock cycle time Input clock low-level pulse width Output clock low-level pulse width Input clock high-level pulse width Output clock high-level pulse width	tCKCY (1)	Figure 5	SCK	3.0			μs	
	tCKCY (2)	Figure 5	SCK		64×Tcyc *6			
	tCKL (1)	Figure 5	SCK	1.0				
	tCKL (2)	Figure 5	SCK		32×Tcyc			
	tCKH (1)	Figure 5	SCK	1.0				
	tCKH (2)	Figure 5	SCK		32×Tcyc			

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DISCONTINUED PRODUCT

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Parameter	Symbol	Conditions	VDD[V]	Applicable pins/notes	Ratings			unit	
					min.	typ.	max.		
Serial input Data setup time Data hold time	t <sub>ICK</sub> t <sub>CKI</sub>	Stipulated with respect to the rising edge of $\overline{SCK}$ . Figure 5		SI	0.4			μs	
				SI	0.4				
Serial output Output delay time	t <sub>CKO</sub>	Stipulated with respect to the falling edge of $\overline{SCK}$ . For n-channel open-drain outputs only: External resistance: 1 kΩ, external capacitance: 50 pF Figure 5		SO			0.6		
Pulse output Period High-level pulse width Low-level pulse width	t <sub>PCY</sub> t <sub>PH</sub> t <sub>PL</sub>	Figure 6 T <sub>CYC</sub> = 4 × the system clock period For n-channel open-drain outputs only: External resistance: 1 kΩ, external capacitance: 50 pF		PE0 PE0 PE0		64×T <sub>CYC</sub> 32×T <sub>CYC</sub> ± 10% 32×T <sub>CYC</sub> ± 10%			
Watchdog timer	Guaranteed constants *7	CW	When PE1 has open-drain output specifications	3 to 5.5	WDR		0.1±5%		μF
		RW	When PE1 has open-drain output specifications		WDR		680±1%		kΩ
		RI	When PE1 has open-drain output specifications		WDR		100±1%		Ω
	Clear time (discharge)	t <sub>WCT</sub>	See Figure 7.		WDR	100			μs
	Clear period (charge)	t <sub>WCCY</sub>	See Figure 7.		WDR	29			ms
	Guaranteed constants *7	CW	When PE1 has open-drain output specifications	4 to 5.5	WDR		0.047±5%		μF
		RW	When PE1 has open-drain output specifications		WDR		680±1%		kΩ
		RI	When PE1 has open-drain output specifications		WDR		100±1%		Ω
	Clear time (discharge)	t <sub>WCT</sub>	See Figure 7.		WDR	40			μs
	Clear period (charge)	t <sub>WCCY</sub>	See Figure 7.		WDR	15			ms

[Notes]

- When driven internally using the oscillator circuit shown in Figure 3 with guaranteed constants, values up to the amplitude of the generated oscillation are allowed.
- The average over a 100-ms period
- The operating power-supply voltage VDD must be maintained from the point where a HALT instruction is executed until the point where the device has fully entered the standby state. Also, applications must be designed so that no chattering (e.g. switch bounce) occurs on the PA3 pin during a HALT instruction execution cycle.
- When external clock is selected as the oscillator option, the OSC1 pin has Schmitt characteristics.
- The values shown for f<sub>CFOSC</sub> are the frequencies for which oscillation is possible. The center frequency when a ceramic oscillator is used may differ by about 1% from the nominal value listed by the manufacturer of the ceramic oscillator element. See the specifications of the ceramic oscillator element for details.
- T<sub>CYC</sub> = 4 × the system clock period
- If this device is used in an environment subject to condensation, extra care is required concerning leakage between PE1 and adjacent pins and leakage associated with external capacitors.

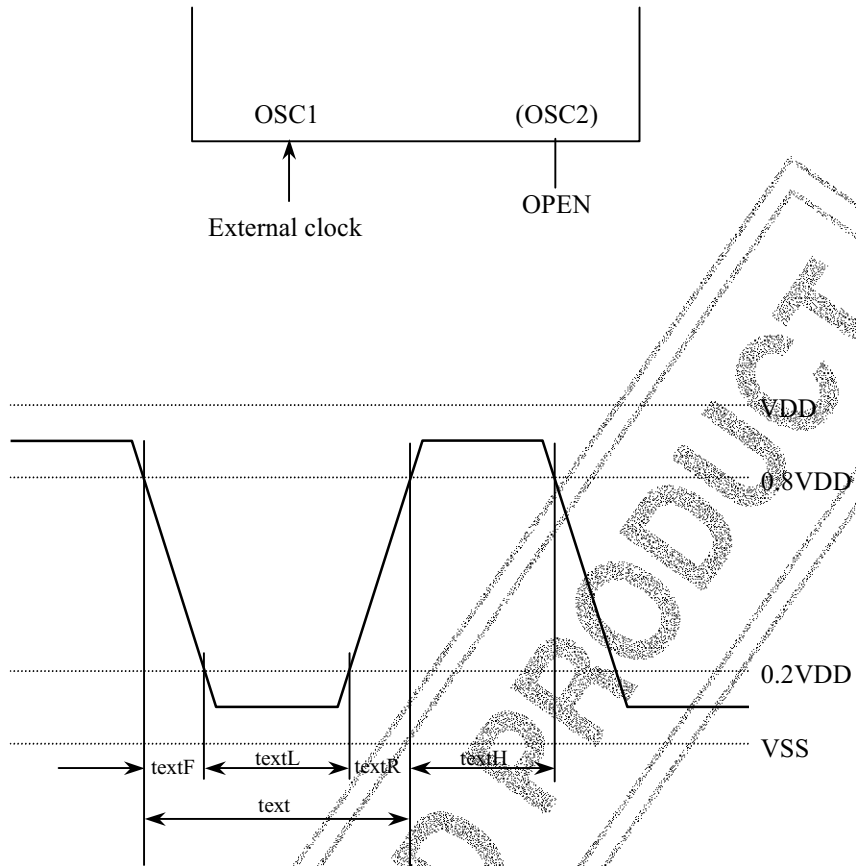


Figure 1 External Clock Input Waveform

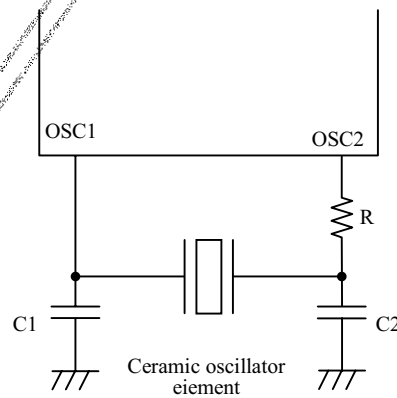


Figure 2 Ceramic Oscillator Circuit



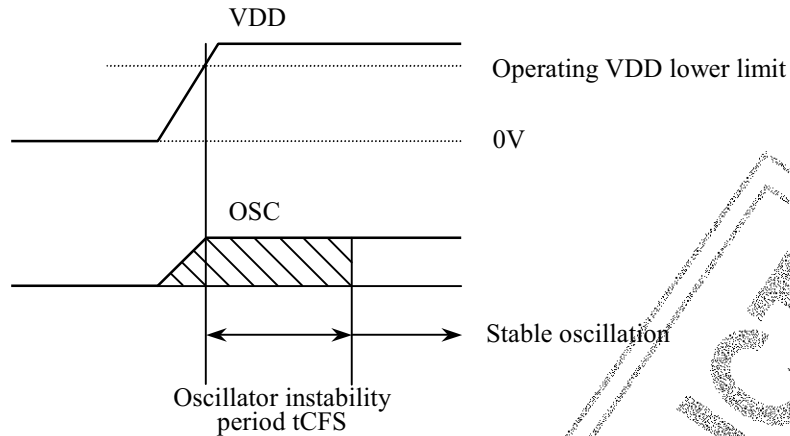


Figure 3 Oscillator Stabilization Period

Table 1 : Guaranteed Ceramic Oscillator Constants

4MHz (Murata Mfg. Co., Ltd.) CSA4.00MG CST4.00MGW (built-in capacitor version)	C1	33 pF±10 %
	C2	33 pF±10 %
	R	0Ω
4MHz (Kyocera Corporation) KBR4.0MSA KBR4.0MKS (built-in capacitor version)	C1	33 pF±10 %
	C2	33 pF±10 %
	R	0Ω
1MHz (Murata Mfg. Co., Ltd.) CSB1000J	C1	100 pF±10 %
	C2	100 pF±10 %
	R	2.2 kΩ
1MHz (Kyocera Corporation) KBR1000F	C1	100 pF±10 %
	C2	100 pF±10 %
	R	0Ω
800kHz (Murata Mfg. Co., Ltd.) CSB800J	C1	100 pF±10 %
	C2	100 pF±10 %
	R	2.2 kΩ
800kHz (Kyocera Corporation) KBR800F	C1	220 pF±10 %
	C2	220 pF±10 %
	R	0Ω

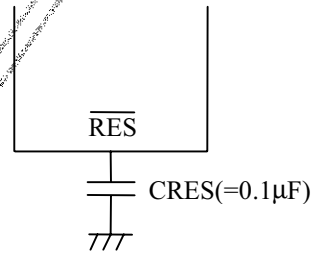


Figure 4 Reset Circuit

Note: When the power supply rise time is zero, the reset time with CRES = 0.1 μF will be between 5 and 50 ms.  
If the power supply rise time is comparatively long, increase the value of CRES so that the reset time is over 5 ms.

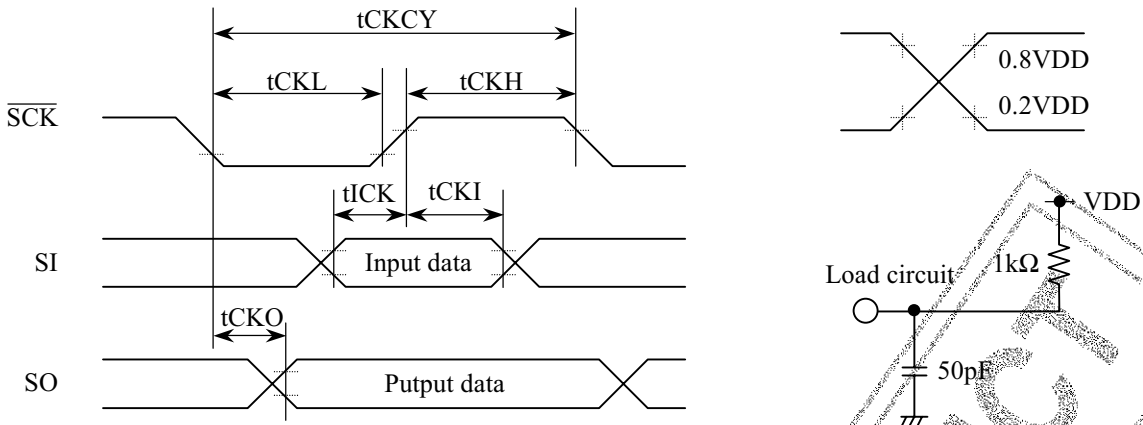


Figure 5 Serial I/O Timing

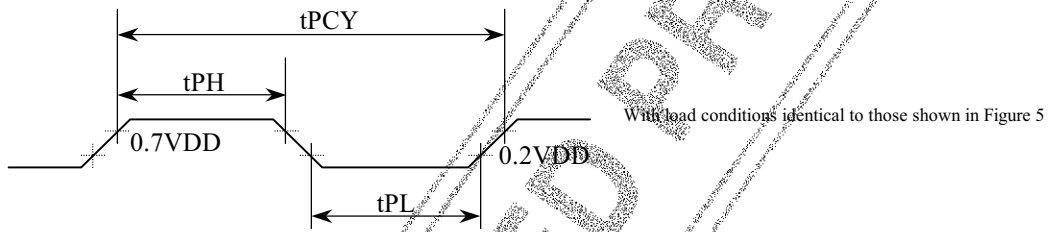


Figure 6 Port PE0 Pulse Output Timing

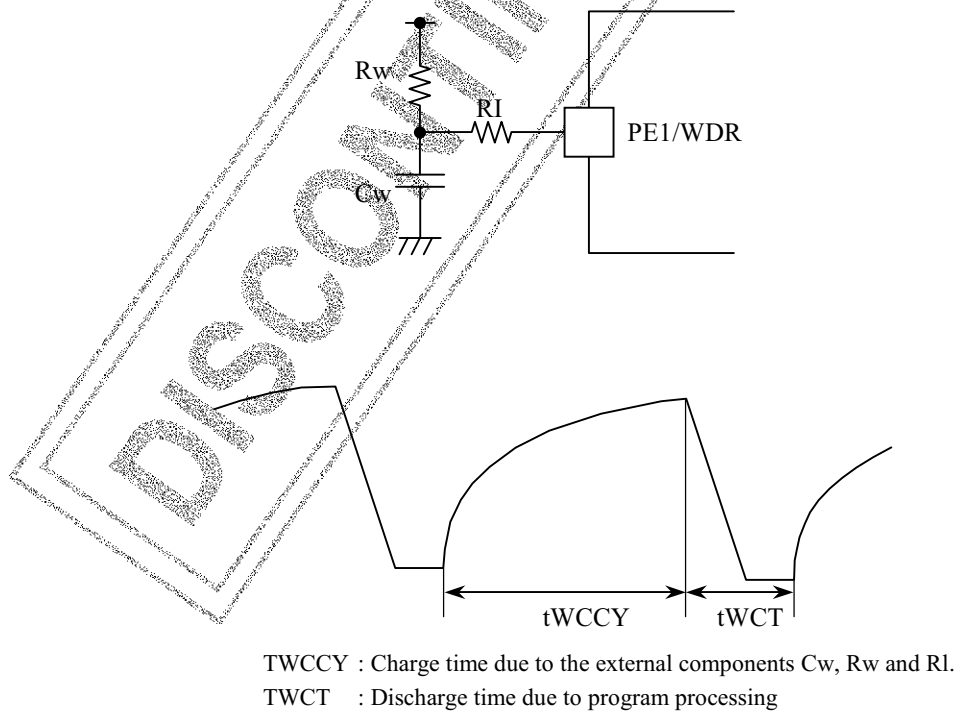


Figure 7 Watchdog Timer Waveform

LC651204F, LC651202F

Absolute Maximum Ratings at VSS=0V and Ta=25°C

Parameter	Symbol	Applicable pins/notes	Conditions	Ratings	unit
Maximum supply voltage	VDD max		VDD	-30 to +7.0	V
Output voltage	VO		OSC2	Voltages up to any generated voltage are allowed.	
Input voltage	VI (1)		OSC1 *1	-0.3 to VDD +0.3	
	VI (2)		TEST, RES	-0.3 to VDD +0.3	
I/O voltage	VIO (1)	PC0 to 3, PD0 to 3, PE0, 1, PF0 to 3	OD specification ports	-0.3 to +15	
	VIO (2)	PC0 to 3, PD0 to 3, PE0, 1, PF0 to 3	PU specification ports	-0.3 to VDD +0.3	
	VIO (3)	PA0 to 3, PG0 to 3		-0.3 to VDD +0.3	
Peak output current	IOP		I/O ports	-2 to +20	mA
Average output current	IOA	Average value per pin over a 100-ms period	I/O ports	-2 to +20	
	Σ IOA (1)	Total current for pins PC0 to 3, PD0 to 3, and PE0 to 1*2	PC0 to 3 PD0 to 3 PE0 to 1	-15 to +100	
	Σ IOA (2)	Total current for pins PF0 to 3, PG0 to 3, and PA0 to 3*2	PF0 to 3 PG0 to 3 PA0 to 3	-15 to +100	
Allowable power dissipation	Pd max(1)	Ta = -40 to +85°C (DIP package)		250	mW
	Pd max(2)	Ta = -40 to +85°C (MFP package)		150	
Operation temperature	Topr			-40 to +85	°C
Storage temperature	Tstg			-55 to +125	

Allowable Operating Range at Ta=-40°C to +85°C, VSS=0V, VDD=3.0 to 5.5V

(unless otherwise specified)

Parameter	Symbol	Conditions	Applicable pins/notes	Ratings			unit	
				min.	typ.	max.		
Operating power-Supply voltage	VDD		VDD	3.0		5.5	V	
Standby power-Supply voltage	VST	RAM and register values retained *3	VDD	1.8		5.5		
Input high-level voltage	VIH(1)	Output n-channel transistors off	OD specification ports C, D, E and F	0.7VDD		13.5		
	VIH(2)	Output n-channel transistors off	PU specification ports C, D, E and F	0.7VDD		VDD		
	VIH(3)	Output n-channel transistors off	Port A, G	0.7VDD		VDD		
	VIH(4)	Output n-channel transistors off	The INT, SCK and SI pins with OD specifications	0.8VDD		13.5		
	VIH(5)	Output n-channel transistors off	The INT, SCK and SI pins with PU specifications	0.8VDD		VDD		
	VIH(6)	VDD = 1.8 to 5.5V		RES	0.8VDD			VDD
	VIH(7)	External clock specifications		OSC1	0.8VDD			VDD
Input low-level voltage	VIL(1)	Output n-channel transistors off	Port	VSS		0.2VDD		
	VIL(2)	Output n-channel transistors off	INT, SCK, SI	VSS		0.2VDD		
	VIL(3)	External clock specifications	OSC1	VSS		0.2VDD		
	VIL(4)		TEST	VSS		0.2VDD		
	VIL(5)		RES	VSS		0.2VDD		

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Parameter	Symbol	Conditions	Applicable pins/notes	Ratings			unit
				min.	typ.	max.	
Operating frequency (cycle time)	fop (T <sub>cyc</sub> )			670 (6)		4330 (0.97)	kHz (μs)
External clock conditions Frequency Pulse width Rise and fall times	text	Figure 1	OSC1	670		4330	kHz
	textH, textL		OSC1	69			ns
	textR, textF		OSC1			50	
Guaranteed oscillator constants Ceramic oscillator		Figure 2		See Table 1.			

Electrical Characteristics at Ta=-40°C to +85°C, VSS=0V, VDD=3.0 to 5.5V

(unless otherwise specified)

Parameter	Symbol	Conditions	Applicable pins/notes	Ratings			unit
				min.	typ.	max.	
Input high-level current	I <sub>IH</sub> (1)	Output n-channel transistors off (Includes the n-channel transistors off leakage current.) VIN= 13.5V	Ports C, D, E, and F with open-drain specifications			5.0	μA
	I <sub>IH</sub> (2)	Output n-channel transistors off (Includes the n-channel transistors off leakage current.) VIN= VDD	Ports A and G with open-drain specifications			1.0	
	I <sub>IH</sub> (3)	External clock mode, VIN= VDD	OSC1			1.0	
Input low-level current	I <sub>IL</sub> (1)	Output n-channel transistors off VIN= VSS	Ports with open-drain specifications	-1.0			
	I <sub>IL</sub> (2)	Output n-channel transistors off VIN= VSS	Ports with pull-up resistor specifications	-1.3	-0.35		mA
	I <sub>IL</sub> (3)	VIN= VSS	RES	-45	-10		μA
	I <sub>IL</sub> (4)	External clock mode, VIN= VSS	OSC1	-1.0			
Output high-level voltage	VOH(1)	I <sub>OH</sub> = -50μA	Ports with pull-up resistor specifications	VDD-1.2			V
	VOH(2)	I <sub>OH</sub> = -10μA	Ports with pull-up resistor specifications	VDD-0.5			
Output low-level voltage	VOL(1)	I <sub>OL</sub> = 10mA	Port			1.5	
	VOL(2)	I <sub>OL</sub> = 1mA, with the I <sub>OL</sub> for all ports no more than 1mA.	Port			0.5	

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Parameter	Symbol	Conditions	Applicable pins/notes	Ratings			unit
				min.	typ.	max.	
Schmitt characteristics	Hysteresis voltage	VHIS	RES, INT, SCK and SI OSC1 with Schmitt specifications *4		0.1VDD		V
	High-level threshold voltage	VtH		0.4VDD		0.8VDD	
	Low-level threshold voltage	VtL		0.25VDD		0.6VDD	
Current drain Ceramic oscillator External clock	IDDOP(1)	Figure 2, 4 MHz 670 to 1444 kHz	VDD		2	6	mA
	IDDOP(2)	*1 Operating, output n-channel transistors off, Ports = VDD	VDD		2	6	
Standby mode	IDDst	Output n-channel transistors off, Ports = VDD	VDD = 5.5V	VDD	0.05	10	μA
			VDD = 3V	VDD	0.025	5	
Oscillator characteristics Ceramic oscillator Oscillator frequency	fCFOSC	Figure 2, fo = 4 MHz *5	OSC1, OSC2	3840	4000	1460	kHz
Oscillator stabilization time	tCFS	Figure 3, fo = 4 MHz				5	ms
Pull-up resistors I/O ports RES	Rpp	Output n-channel transistors off VIN = VSS, VDD = 5V	Ports with pull-up resistor specifications	8	14	30	kΩ
	Ru	VIN = VSS, VDD = 5V	RES	100	250	400	
External reset characteristics Reset time	tRST				See Figure 4.		
Pin capacitance	Cp	f = 1MHz With all pins other than the pin being measured at VIN = VSS			10		pF
Serial clock Input clock cycle time Output clock cycle time Input clock low-level pulse width Output clock low-level pulse width Input clock high-level pulse width Output clock high-level pulse width	tCKCY (1)	Figure 5	SCK	2.0			μs
	tCKCY (2)	Figure 5	SCK		64×Tcyc *6		
	tCKL(1)	Figure 5	SCK	0.6			
	tCKL(2)	Figure 5	SCK		32×Tcyc		
	tCKH(1)	Figure 5	SCK	0.6			
	tCKH(2)	Figure 5	SCK		32×Tcyc		

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Parameter	Symbol	Conditions	VDD[V]	Applicable pins/notes	Ratings			unit
					min.	typ.	max.	
Serial input Data setup time Data hold time	t <sub>ICK</sub> t <sub>CKI</sub>	Stipulated with respect to the rising edge of $\overline{\text{SCK}}$ . Figure 5		SI	0.2			$\mu\text{s}$
				SI	0.2			
Serial output Output delay time	t <sub>CKO</sub>	Stipulated with respect to the rising edge of $\overline{\text{SCK}}$ . For n-channel open-drain outputs only. External resistance: 1 k $\Omega$ , external capacitance: 50 pF Figure 5		SO			0.4	
Pulse output Period High-level pulse width Low-level pulse width	t <sub>PCY</sub> t <sub>PH</sub> t <sub>PL</sub>	Figure 6 T <sub>CYC</sub> = 4 × the system clock period For n-channel open-drain outputs only. External resistance: 1 k $\Omega$ , external capacitance: 50 pF		PE0 PE0 PE0		64×T <sub>CYC</sub> 32×T <sub>CYC</sub> ± 10% 32×T <sub>CYC</sub> ± 10%		
Watchdog timer	Guaranteed constants *7	CW	When PE1 has open-drain output specifications	3 to 5.5	WDR		0.01±5%	$\mu\text{F}$
		RW	When PE1 has open-drain output specifications		WDR		680±1%	k $\Omega$
		RI	When PE1 has open-drain output specifications		WDR		100±1%	$\Omega$
	Clear time (discharge)	t <sub>WCT</sub>	See Figure 7.		WDR	10		$\mu\text{s}$
	Clear period (charge)	t <sub>WCCY</sub>	See Figure 7.		WDR	3.0		ms
	Guaranteed constants *7	CW	When PE1 has open-drain output specifications	4.5 to 5.5	WDR		0.01±5%	$\mu\text{F}$
		RW	When PE1 has open-drain output specifications		WDR		680±1%	k $\Omega$
		RI	When PE1 has open-drain output specifications		WDR		100±1%	$\Omega$
	Clear time (discharge)	t <sub>WCT</sub>	See Figure 7.		WDR	10		$\mu\text{s}$
	Clear period (charge)	t <sub>WCCY</sub>	See Figure 7.		WDR	3.3		ms

[Notes]

1. When driven internally using the oscillator circuit shown in Figure 2 with guaranteed constants, values up to the amplitude of the generated oscillation are allowed.
2. The average over a 100-ms period
3. The operating power-supply voltage VDD must be maintained from the point where a HALT instruction is executed until the point where the device has fully entered the standby state. Also, applications must be designed so that no chattering (e.g. switch bounce) occurs on the PA3 pin during a HALT instruction execution cycle.
4. When external clock is selected as the oscillator option, the OSC1 pin has Schmitt characteristics.
5. The values shown for f<sub>CFOSC</sub> are the frequencies for which oscillation is possible.
6. T<sub>CYC</sub> = 4 × the system clock period
7. If this device is used in an environment subject to condensation, extra care is required concerning leakage between PE1 and adjacent pins and leakage associated with external capacitors.

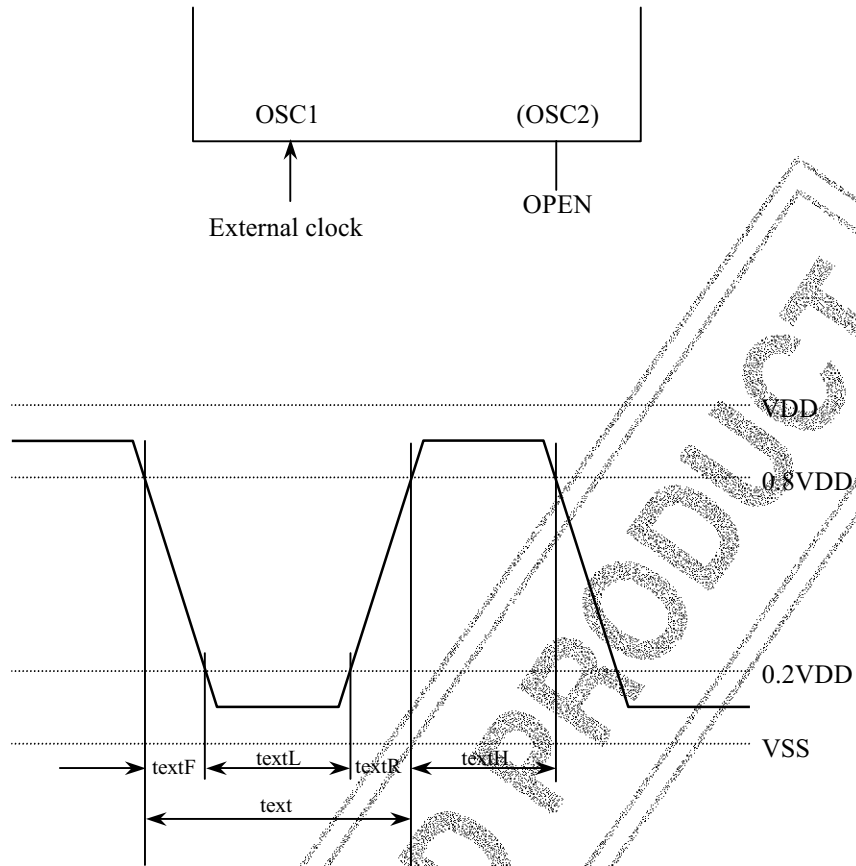


Figure 1 External Clock Input Waveform

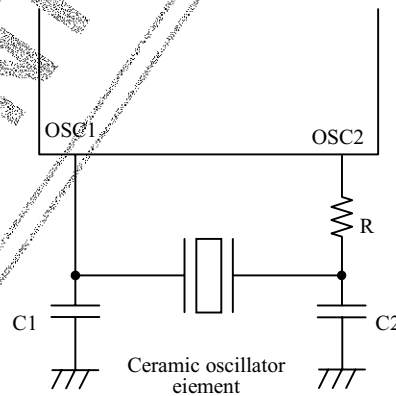


Figure 2 Ceramic Oscillator Circuit

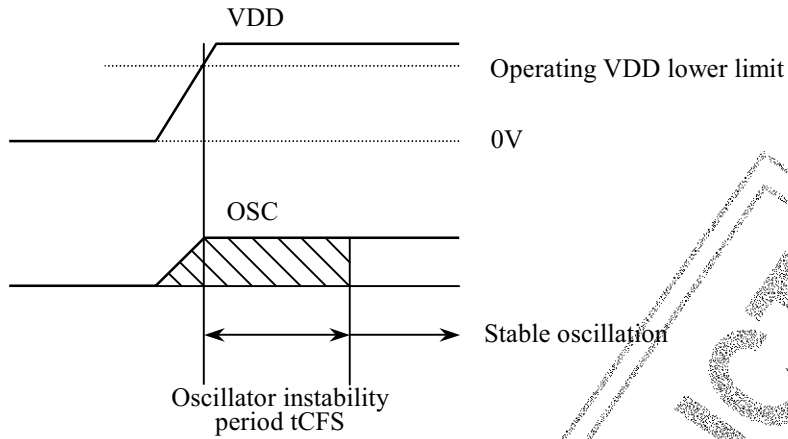


Figure 3 Oscillator Stabilization Period

Table 1 : Guaranteed Ceramic Oscillator Constants

4MHz (Murata Mfg. Co., Ltd.)	C1	33 pF±10 %
CSA4.00MG	C2	33 pF±10 %
CST4.00MGW (built-in capacitor version)	R	0Ω
4MHZ (Kyocera Corporation)	C1	33p.F±10 %
KBR4.0MSA	C2	33p.F±10 %
KBR4.0MKS (built-in capacitor version)	R	0Ω

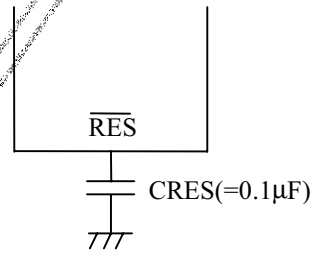


Figure 4 Reset Circuit

Note: When the power supply rise time is zero, the reset time with CRES = 0.1µF will be between 5 and 50 ms.  
If the power supply rise time is comparatively long, increase the value of CRES so that the reset time is over 5 ms.

DISCONTINUED PRODUCT



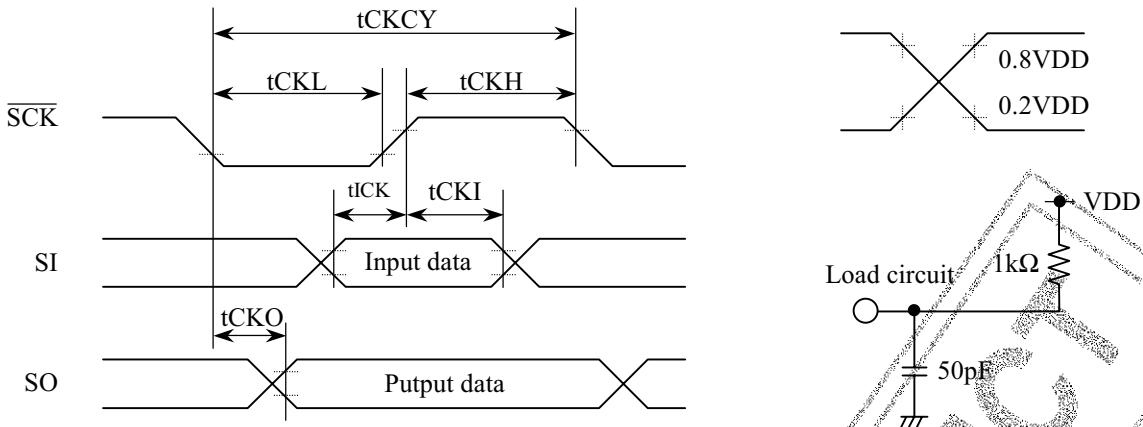


Figure 5 Serial I/O Timing

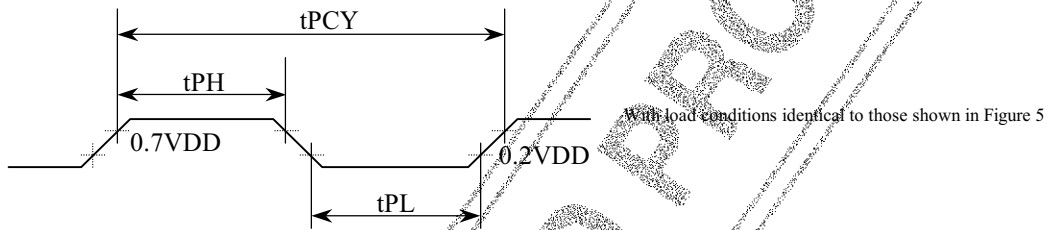


Figure 6 Port PE0 Pulse Output Timing

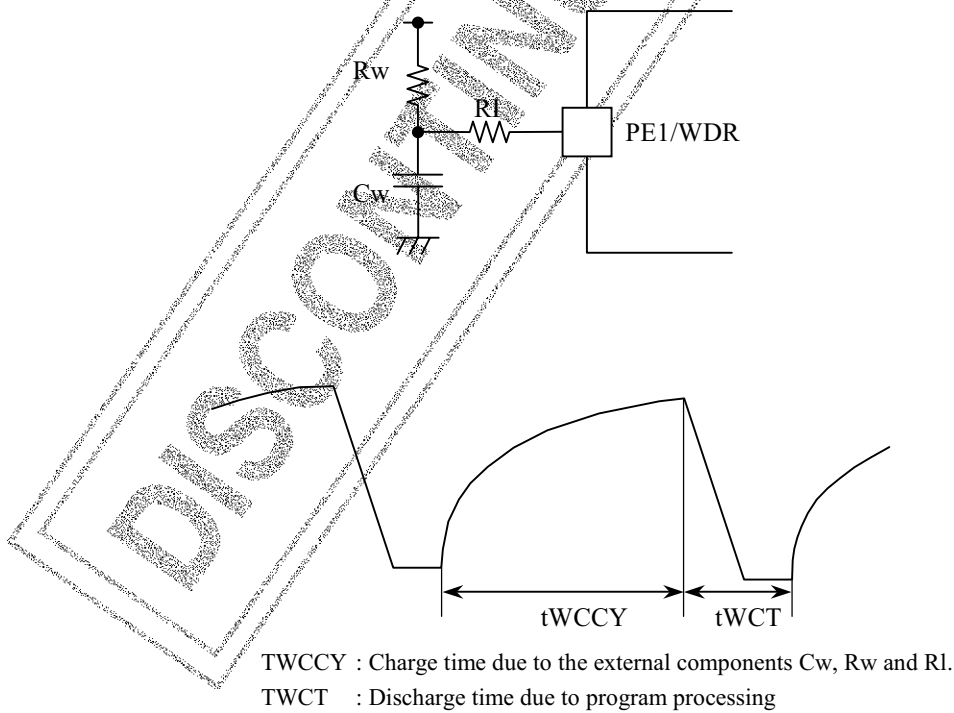


Figure 7 Watchdog Timer Waveform

LC651204L, LC651202L

Absolute Maximum Ratings at VSS=0V and Ta=25°C

Parameter	Symbol	Applicable pins/notes	Conditions	Ratings	unit
Maximum supply voltage	VDD max		VDD	-30 to +7.0	V
Output voltage	VO		OSC2	Voltages up to any generated voltage are allowed.	
Input voltage	VI (1)		OSC1 *1	-0.3 to VDD +0.3	
	VI (2)		TEST, RES	-0.3 to VDD +0.3	
I/O voltage	VIO (1)	PC0 to 3, PD0 to 3, PE0, 1, PF0 to 3	OD specification ports	-0.3 to +15	
	VIO (2)	PC0 to 3, PD0 to 3, PE0, 1, PF0 to 3	PU specification ports	-0.3 to VDD +0.3	
	VIO (3)	PA0 to 3, PG0 to 3		-0.3 to VDD +0.3	
Peak output current	IOP		I/O ports	-2 to +20	mA
Average output current	IOA	Average value per pin over a 100-ms period	I/O ports	-2 to +20	
	Σ IOA (1)	Total current for pins PC0 to 3, PD0 to 3, and PE0 to 1*2	PC0 to 3 PD0 to 3 PE0 to 1	-15 to +100	
	Σ IOA (2)	Total current for pins PF0 to 3, PG0 to 3, and PA0 to 3*2	PF0 to 3 PG0 to 3 PA0 to 3	-15 to +100	
Allowable power dissipation	Pd max(1)	Ta = -40 to +85°C (DIP package)		250	mW
	Pd max(2)	Ta = -40 to +85°C (MFP package)		150	
Operation temperature	Topr			-40 to +85	°C
Storage temperature	Tstg			-55 to +125	

Allowable Operating Range at Ta=-40°C to +85°C, VSS=0V, VDD=2.5 to 5.5V

(unless otherwise specified)

Parameter	Symbol	Conditions	Applicable pins/notes	Ratings			unit	
				min.	typ.	max.		
Operating power-Supply voltage	VDD		VDD	2.5		5.5	V	
Standby power-Supply voltage	VST	RAM and register values retained *3	VDD	1.8		5.5		
Input high-level voltage	VIH(1)	Output n-channel transistors off	OD specification ports C, D, E and F	0.7VDD		13.5		
	VIH(2)	Output n-channel transistors off	PU specification ports C, D, E and F	0.7VDD		VDD		
	VIH(3)	Output n-channel transistors off	Port A, G	0.7VDD		VDD		
	VIH(4)	Output n-channel transistors off	The INT, SCK and SI pins with OD specifications	0.8VDD		13.5		
	VIH(5)	Output n-channel transistors off	The INT, SCK and SI pins with PU specifications	0.8VDD		VDD		
	VIH(6)	VDD = 1.8 to 5.5V		RES	0.8VDD			VDD
	VIH(7)	External clock specifications		OSC1	0.8VDD			VDD
Input low-level voltage	VIL(1)	Output n-channel transistors off	Port	VSS		0.2VDD		
	VIL(2)	Output n-channel transistors off	INT, SCK, SI	VSS		0.15VDD		
	VIL(3)	External clock specifications	OSC1	VSS		0.15VDD		
	VIL(4)		TEST	VSS		0.2VDD		
	VIL(5)		RES	VSS		0.15VDD		

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Parameter	Symbol	Conditions	Applicable pins/notes	Ratings			unit
				min.	typ.	max.	
Operating frequency (cycle time)	fop (Tcyc)	Frequencies up to 4.16MHz are supported if the divide-by-four divider circuit option is used.		670 (6)		1040 (3.84)	kHz (μs)
External clock conditions Frequency Pulse width Rise and fall times	text	Figure 1. The divide-by-three or divide-by-four divider circuit option must be used if the clock frequency exceeds 1.040MHz.	OSC1	670		4160	kHz
	textH, textL		OSC1	150			ns
	textR, textF		OSC1			100	
Guaranteed oscillator constants Ceramic oscillator		Figure 2		See Table 1.			

Electrical Characteristics at Ta=-40°C to +85°C, VSS=0V, VDD=2.5 to 5.5V

(unless otherwise specified)

Parameter	Symbol	Conditions	Applicable pins/notes	Ratings			unit
				min.	typ.	max.	
Input high-level current	IIH(1)	Output n-channel transistors off (Includes the n-channel transistors off leakage current.) VIN= 13.5V	Ports C, D, E and F with open-drain specifications			5.0	μA
	IIH(2)	Output n-channel transistors off (Includes the n-channel transistors off leakage current.) VIN= VDD	Ports A and G with open-drain specifications			1.0	
	IIH(3)	External clock mode, VIN= VDD	OSC1			1.0	
Input low-level current	IIl(1)	Output n-channel transistors off VIN= VSS	Ports with open-drain specifications	-1.0			
	IIl(2)	Output n-channel transistors off VIN= VSS	Ports with pull-up resistor specifications	-1.3	-0.35		mA
	IIl(3)	VIN= VSS	RES	-45	-10		μA
	IIl(4)	External clock mode, VIN= VSS	OSC1	-1.0			
Output high-level voltage	VOH(1)	IOH= -10μA	Ports with pull-up resistor specifications	VDD-0.5			V
Output low-level voltage	VOL(1)	IOL= 3mA	Port			1.5	
	VOL(2)	IOL= 1 mA, with the IOL for all ports no more than 1 mA.	Port			0.4	

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Parameter	Symbol	Conditions	Applicable pins/notes	Ratings			unit
				min.	typ.	max.	
Schmitt characteristics	Hysteresis voltage	VHIS	$\overline{\text{RES}}$ , $\overline{\text{INT}}$ , $\overline{\text{SCK}}$ and SI OSC1 with schmitt specifications *4		0.1VDD		V
	High-level threshold voltage	VtH		0.4VDD		0.8VDD	
	Low-level threshold voltage	VtL		0.2VDD		0.6VDD	
Current drain Ceramic oscillator	IDDOP(1)	Operating, output n-channel transistors off, Ports = VDD Figure 2, 4 MHz, divide-by-three circuit	VDD		1.5	4	mA
	IDDOP(2)	Figure 2, 4 MHz, divide-by-three circuit VDD = 2.5V	VDD		0.5	1	
External clock	IDDOP(3)	Figure 2, 800 kHz	VDD		1.5	4.0	mA
	IDDOP(4)	670 to 1024 kHz, no divider circuit 2000 to 3120 kHz, divide-by-three circuit 2600 to 4160 kHz, divide-by-four circuit	VDD		1.5	4	
Standby mode	IDDst	Output n-channel transistors off, Ports = VDD	VDD = 5.5V	VDD	0.05	10	μA
			VDD = 2.5V	VDD	0.020	4	
Oscillator characteristics Ceramic oscillator Oscillator frequency Oscillator stabilization time	fCFOSC *5	Figure 2, fo = 800 kHz Figure 2, fo = 1 MHz Figure 2, fo = 4 MHz, divide-by-four circuit	OSC1, OSC2	768	800	832	kHz
			OSC1, OSC2	960	1000	1040	
			OSC1, OSC2	3840	4000	4160	
	tCFS	Figure 3, fo = 800 kHz, 1 MHz, 4 MHz, divide-by-four circuit				5	ms
Pull-up resistors I/O ports	Rpp	Output n-channel transistors off VIN = VSS, VDD = 5V	Ports with pull-up resistor specifications	8	14	30	kΩ
	RES	VIN = VSS, VDD = 5V	RES	100	250	400	
External reset characteristics Reset time	tRST			See Figure 4.			
Pin capacitance	Cp	f = 1MHz With all pins other than the pin being measured at VIN = VSS			10		pF
Serial clock Input clock cycle time Output clock cycle time Input clock low-level pulse width Output clock low-level pulse width Input clock high-level pulse width Output clock high-level pulse width	tCKCY (1)	Figure 5	$\overline{\text{SCK}}$	6.0			μs
	tCKCY (2)	Figure 5	$\overline{\text{SCK}}$		64×Tcyc *6		
	tCKL (1)	Figure 5	$\overline{\text{SCK}}$	2.0			
	tCKL (2)	Figure 5	$\overline{\text{SCK}}$			32×Tcyc	
	tCKH (1)	Figure 5	$\overline{\text{SCK}}$	2.0			
	tCKH (2)	Figure 5	$\overline{\text{SCK}}$			32×Tcyc	

Continued on next page.

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Parameter	Symbol	Conditions	VDD[V]	Applicable pins/notes	Ratings			unit	
					min.	typ.	max.		
Serial input Data setup time Data hold time	tICK	Stipulated with respect to the rising edge of SCK .		SI	0.5			μs	
	tCKI	Figure 5		SI	0.5				
Serial output Output delay time	tCKO	Stipulated with respect to the rising edge of SCK . For n-channel open-drain outputs only: External resistance: 1 kΩ, external capacitance: 50 pF Figure 5		SO			1.0		
	tPCY	Figure 6 Tcyc = 4 × the system clock period		PE0		64×Tcyc			
High-level pulse width	tPH	For n-channel open-drain outputs only: External resistance: 1 kΩ, external capacitance: 50 pF		PE0		32×Tcyc ± 10%			
Low-level pulse width	tPL			PE0		32×Tcyc ± 10%			
Watchdog timer	Guaranteed constants *7	CW	When PE1 has open-drain output specifications	2.5 to 5.5	WDR		0.1±5%		μF
		RW	When PE1 has open-drain output specifications		WDR		680±1%		kΩ
		RI	When PE1 has open-drain output specifications		WDR		100±1%		Ω
	Clear time (discharge)	tWCT	See Figure 7.		WDR	100			μs
	Clear period (charge)	tWCCY	See Figure 7.		WDR	26			ms
	Guaranteed constants *7	CW	When PE1 has open-drain output specifications	2.5 to 5.5	WDR		0.047±5%		μF
		RW	When PE1 has open-drain output specifications		WDR		680±1%		kΩ
		RI	When PE1 has open-drain output specifications		WDR		100±1%		Ω
	Clear time (discharge)	tWCT	See Figure 7.		WDR	40			μs
	Clear period (charge)	tWCCY	See Figure 7.		WDR	12			ms

[Notes]

1. When driven internally using the oscillator circuit shown in Figure 2 with guaranteed constants, values up to the amplitude of the generated oscillation are allowed.
2. The average over a 100-ms period.
3. The operating power-supply voltage VDD must be maintained from the point where a HALT instruction is executed until the point where the device has fully entered the standby state. Also, applications must be designed so that no chattering (e.g. switch bounce) occurs on the PA3 pin during a HALT instruction execution cycle.
4. When external clock is selected as the oscillator option, the OSC1 pin has Schmitt characteristics.
5. The values shown for fCFOSC are the frequencies for which oscillation is possible.
6. Tcyc = 4 × the system clock period
7. If this device is used in an environment subject to condensation, extra care is required concerning leakage between PE1 and adjacent pins and leakage associated with external capacitors.

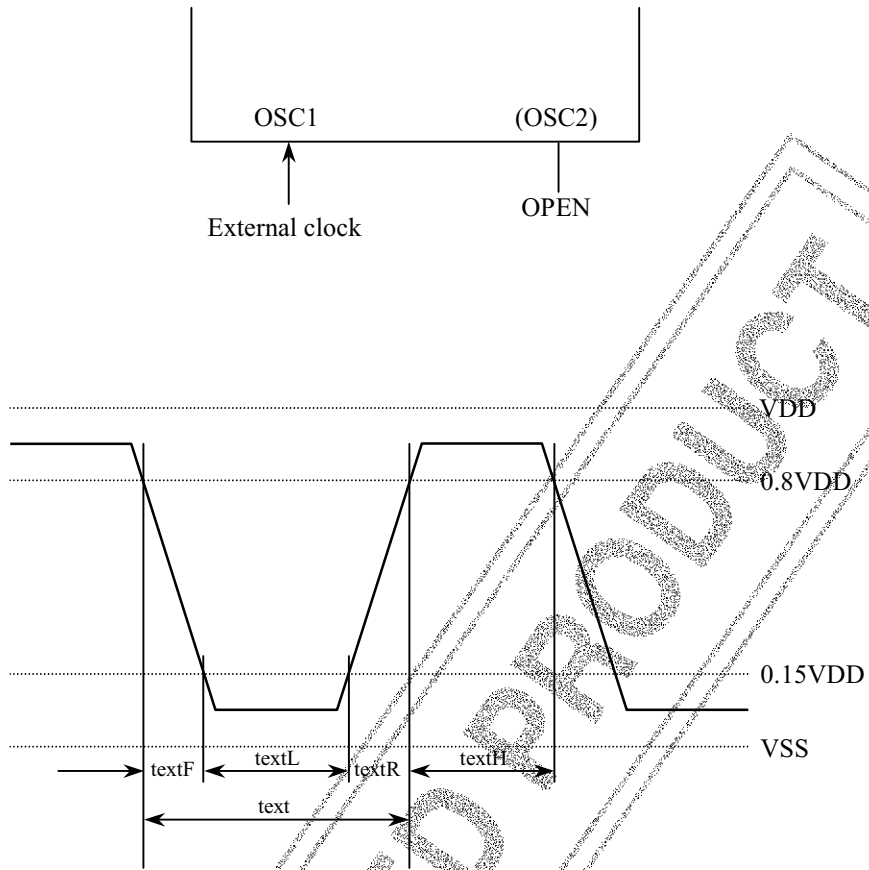


Figure 1 External Clock Input Waveform

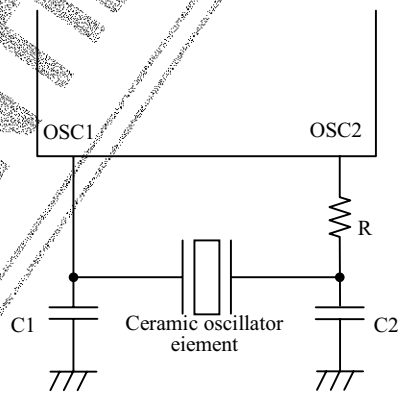


Figure 2 Ceramic Oscillator Circuit

DISCONTINUED PRODUCT

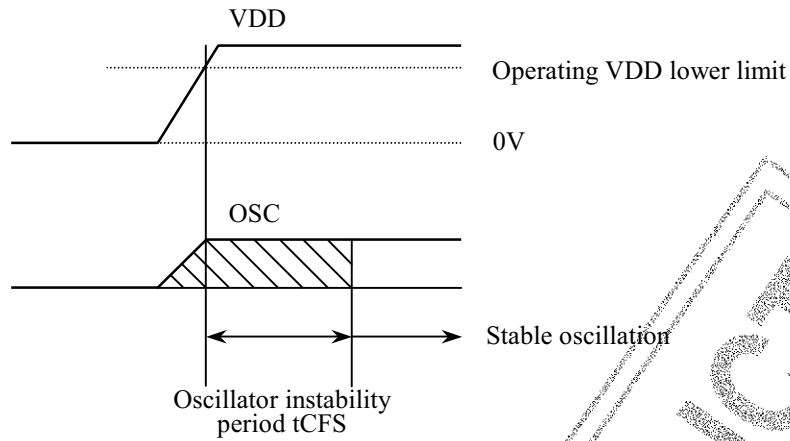


Figure 3 Oscillator Stabilization Period

Table 1 : Guaranteed Ceramic Oscillator Constants

4MHz (Murata Mfg. Co., Ltd.) CSA4.00MGU CST4.00MGWU (built-in capacitor version)	C1	33 pF±10 %
	C2	33 pF±10 %
	R	0Ω
1MHz (Murata Mfg. Co., Ltd.) CSB1000J	C1	100 pF±10 %
	C2	100 pF±10 %
	R	2.2 kΩ
1MHz (Kyocera Corporation) KBR1000F	C1	100 pF±10 %
	C2	100 pF±10 %
	R	0Ω
800kHz (Murata Mfg. Co., Ltd.) CSB800J	C1	100 pF±10 %
	C2	100 pF±10 %
	R	2.2kΩ
800kHz (Kyocera Corporation) KBR800F	C1	220 pF±10 %
	C2	220 pF±10 %
	R	0Ω

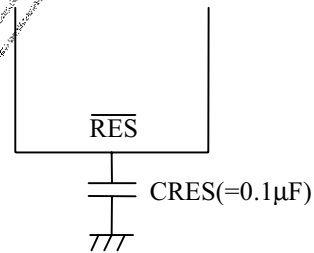


Figure 4 Reset Circuit

Note: When the power supply rise time is zero, the reset time with CRES = 0.1μF will be between 5 and 50 ms.  
If the power supply rise time is comparatively long, increase the value of CRES so that the reset time is over 5 ms.

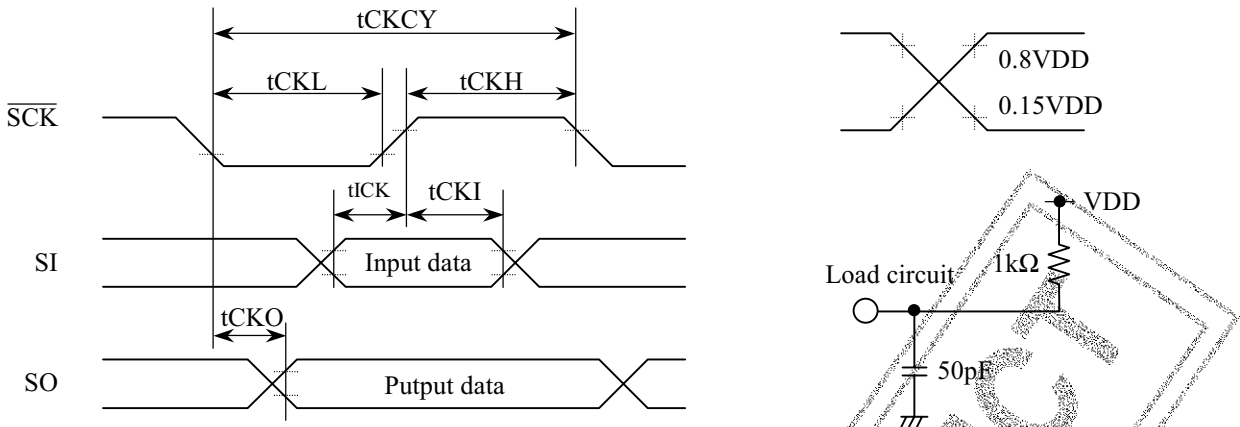


Figure 5 Serial I/O Timing

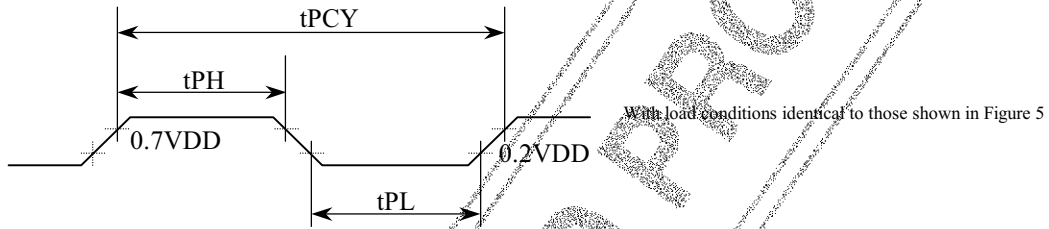
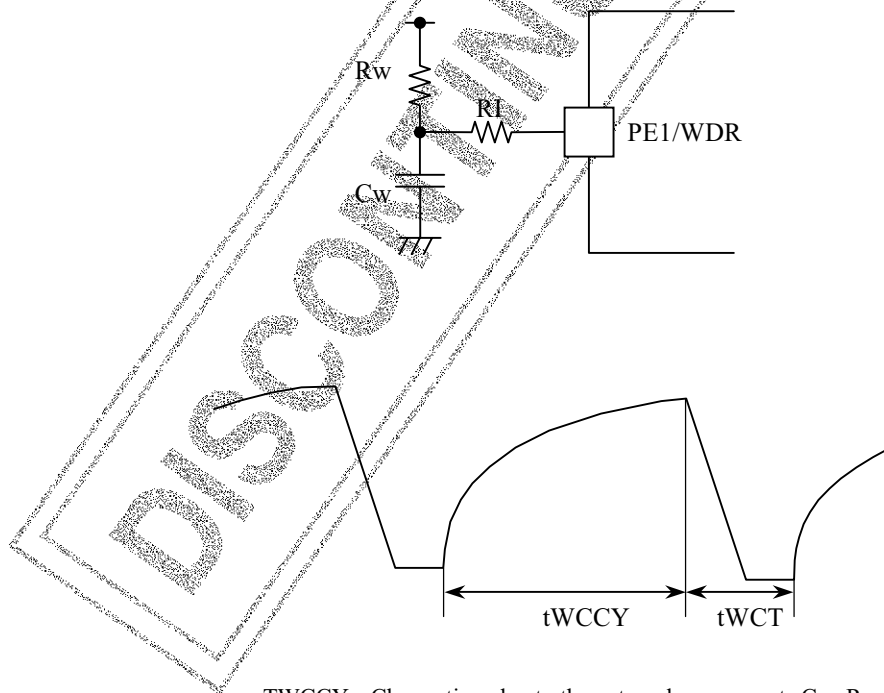


Figure 6 Port PE0 Pulse Output Timing



$t_{WCCY}$  : Charge time due to the external components  $C_w$ ,  $R_w$  and  $R_l$ .

$t_{WCT}$  : Discharge time due to program processing

Figure 7 Watchdog Timer Waveform



**LC651204/1202 Instruction Set (by function)**  
**Abbreviations**

- AC : Accumulator
- ACt : Accumulator bit t
- CF : Carry flag
- CTL : Control register
- DP : Data pointer
- E : E register
- EXTF : External interrupt request flag
- F<sub>n</sub> : Flag bit n
- M : Memory
- M(DP) : Memory addressed by DP
- P(DPL) : I/O port specified by DPL
- PC : Program counter
- STACK : Stack pointer
- TM : Timer
- TMF : Timer (internal) interrupt request flag
- At, Ha, La : Working registers
- ZF : Zero flag
- ( ) [ ] : Indicates the contents of the item enclosed
- ← : Transfer and direction
- + : Addition
- : Subtraction
- ∧ : Logical AND
- ∨ : Logical OR
- ∇ : Logical exclusive OR

Instruction group	Mnemonic		Instruction code		Number of bytes	Number of bytes	Operation	Description	Modified status flags	Notes
			D7 D6 D5 D4	D3 D2 D1 D0						
Accumulator manipulation instructions	CLA	Clear AC	1 1 0 0	0 0 0 0	1	1	AC ← 0	Clears AC.	ZF	*1
	CIC	Clear CF	1 1 1 0	0 0 0 1	1	1	CF ← 0	Clears CF.	CF	
	STC	Set CF	1 1 1 1	0 0 0 1	1	1	CF ← 1	Sets CF.	CF	
	CMA	Complement AC	1 1 1 0	1 0 0 1	1	1	AC ← (AC)	Sets AC to the one's	ZF	
	INC	Increment AC	0 0 0 0	1 1 1 0	1	1	AC ← (AC) + 1	Increments AC.	ZF CF	
	DEC	Decrement AC	0 0 0 0	1 1 1 1	1	1	AC ← (AC) - 1	Decrements AC.	ZF CF	
	RAL	Rotate AC left through CF	0 0 0 0	0 0 0 1	1	1	AC ← (CF), CA <sub>7</sub> ← (AC) <sub>7</sub> , CF ← (AC) <sub>7</sub>	Shifts AC together with CF left.	ZF CF	
	TAE	Transfer AC to E	0 0 0 0	0 0 1 1	1	1	E ← (AC)	Moves the contents of AC to E.		
	XAE	Exchange AC with E	0 0 0 0	1 1 0 1	1	1	(AC) ↔ (E)	Exchanges the contents of AC and E.		
Memory manipulation instructions	INM	Increment M	0 0 1 0	1 1 1 0	1	1	M(DP) ← [M(DP)] + 1	Increments M(DP).	ZF CF	
	DEm	Decrement M	0 0 1 0	0 1 1 1	1	1	M(DP) ← [M(DP)] - 1	Decrements M(DP).	ZF CF	
	SmB bit	Set M data bit	0 0 0 0	1 0 B <sub>1</sub> B <sub>0</sub>	1	1	M(DP, B <sub>1</sub> B <sub>0</sub> ) ← 1	Sets the bit in M(DP) specified by B <sub>1</sub> B <sub>0</sub> to 1.		
	RMB bit	Reset M data bit	0 0 1 0	1 0 B <sub>1</sub> B <sub>0</sub>	1	1	M(DP, B <sub>1</sub> B <sub>0</sub> ) ← 0	Clears the bit in M(DP) specified by B <sub>1</sub> B <sub>0</sub> to 0.		
Arithmetic and comparison instructions	AD	Add M to AC	0 0 1 0	0 0 0 0	1	1	AC ← (AC) + [M(DP)]	Adds the contents of AC and M(DP) as two's complement quantities and stores the result in AC.	ZF CF	
	ADC	Add M to AC with CF	0 0 0 0	0 0 0 0	1	1	AC ← (AC) + [M(DP)] + (CF)	Adds the contents of AC, CF and M(DP) as two's complement quantities and stores the result in AC.	ZF CF	
	DAA	Decimal adjust AC in addition	1 1 1 0	0 1 1 0	1	1	AC ← (AC) + 3	Adds 6 to AC.	ZF	
	DAS	Decimal adjust AC in subtraction	1 1 1 0	1 0 0 0	1	1	AC ← (AC) + 10	Adds 10 to AC.	ZF	
	EXL	Exclusive or M to AC	1 1 1 1	0 1 0 1	1	1	AC ← (AC) ∇ [M(DP)]	Takes the logical exclusive OR of AC and M(DP) and stores the result in AC.	ZF	
	AND	And M to AC	1 1 1 0	0 1 1 1	1	1	AC ← (AC) ∧ [M(DP)]	Takes the logical AND of AC and M(DP) and stores the result in AC.	ZF	
	OR	Or M to AC	1 1 1 0	0 1 0 1	1	1	AC ← (AC) ∨ [M(DP)]	Takes the logical OR of AC and M(DP) and stores the result in AC.	ZF	
	CM	Compare AC with M	1 1 1 1	1 0 0 1	1	1	[M(DP)] + (AC) + 1	Compares the contents of AC and M(DP) and sets or clears CF and ZF accordingly.	ZF CF	

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Instruction group	Mnemonic		Instruction code		Number of bytes	Number of bytes	Operation	Description	Modified status flags	Notes												
			D7 D6 D5 D4	D3 D2 D1 D0																		
Arithmetic and comparison instructions	CI data	Compare AC with immediate data	0 0 1 0 0 1 0 0	1 1 0 0 1 1 1 0	2	2	$I_3 I_2 I_1 I_0 + (AC) + 1$	Compares the contents of AC and the immediate data $I_3 I_2 I_1 I_0$ and sets or clears CF and ZF accordingly. <table border="1"> <tr> <td>Immediate relationship</td> <td>CF</td> <td>ZF</td> </tr> <tr> <td><math>I_3 I_2 I_1 I_0 = (AC)</math></td> <td>0</td> <td>1</td> </tr> <tr> <td><math>I_3 I_2 I_1 I_0 &lt; (AC)</math></td> <td>1</td> <td>0</td> </tr> <tr> <td><math>I_3 I_2 I_1 I_0 &gt; (AC)</math></td> <td>1</td> <td>1</td> </tr> </table>	Immediate relationship	CF	ZF	$I_3 I_2 I_1 I_0 = (AC)$	0	1	$I_3 I_2 I_1 I_0 < (AC)$	1	0	$I_3 I_2 I_1 I_0 > (AC)$	1	1	ZF CF	
	Immediate relationship	CF	ZF																			
$I_3 I_2 I_1 I_0 = (AC)$	0	1																				
$I_3 I_2 I_1 I_0 < (AC)$	1	0																				
$I_3 I_2 I_1 I_0 > (AC)$	1	1																				
	CLI data	Compare DP <sub>L</sub> with immediate data	0 0 1 0 0 1 0 1	1 1 0 0 1 1 1 0	2	2	$(DP_L) \vee I_3 I_2 I_1 I_0$	Compares the contents of DP <sub>L</sub> and the immediate data.	ZF													
Load and store instructions	LI data	Load AC with immediate data	1 1 0 0	1 1 1 0	1	1	$AC \leftarrow I_3 I_2 I_1 I_0$	Loads AC with the immediate data $I_3 I_2 I_1 I_0$ .	ZF	*1												
	S	Store AC to M	0 0 0 0	0 0 1 0	1	1	$M(DP) \leftarrow (AC)$	Stores the contents of AC at M(DP).														
	L	Load AC from M	0 0 1 0	0 0 0 1	1	1	$AC \leftarrow [M(DP)]$	Loads the contents of M(DP) into AC.	ZF													
	XM data	Exchange AC with M then modify DP <sub>H</sub> with immediate data	1 0 1 0	0 M <sub>2</sub> M <sub>1</sub> M <sub>0</sub>	1	2	$(AC) \leftrightarrow [M(DP)]$ $DP_H \leftarrow (DP_H) \vee 0 M_2 M_1 M_0$ $M_2 M_1 M_0$	Exchanges the contents of AC and M(DP). Then, replaces the contents of DP <sub>H</sub> with $(DP_H) \vee 0 M_2 M_1 M_0$ .	ZF	ZF is set to indicate the result of the $(DP_H) \vee 0 M_2 M_1 M_0$ operation.												
	X	Exchange AC with M	1 0 1 0	0 0 0 0	1	2	$(AC) \leftrightarrow [M(DP)]$	Exchanges the contents of AC and M(DP).	ZF	ZF is set according to the contents of DP <sub>H</sub> at the point the instruction was executed.												
	XI	Exchange AC with M then increment DP <sub>L</sub>	1 1 1 1	1 1 1 0	1	2	$(AC) \leftrightarrow [M(DP)]$ $DP_L \leftarrow (DP_L) + 1$	Exchanges the contents of AC and M(DP). Then, increments the contents of DP <sub>L</sub> .	ZF	ZF is set to indicate the result of the DP <sub>L</sub> + 1 operation.												
	XD	Exchange AC with M then increment DP <sub>L</sub>	1 1 1 1	1 1 1 1	1	2	$(AC) \leftrightarrow [M(DP)]$ $DP_L \leftarrow (DP_L) - 1$	Exchanges the contents of AC and M(DP). Then, decrements the contents of DP <sub>L</sub> .	ZF	ZF is set to indicate the result of the DP <sub>L</sub> + 1 operation.												
	RTBI	Read table data from program ROM	0 1 1 0	0 0 1 1	1	2	$AC, E \leftarrow ROM(PCh, E, AC)$	Loads into AC and E the ROM data stored at the location given by the lower 8 bits of the PC, E and AC.														
Data pointer manipulation instructions	LDZ data	Load DP <sub>H</sub> with Zero and DP <sub>L</sub> with immediate data respectively	1 0 0 0	1 1 1 0	1	1	$DP_H \leftarrow 0$ $DP_L \leftarrow I_3 I_2 I_1 I_0$	Loads 0 into DP <sub>H</sub> and the immediate data $I_3 I_2 I_1 I_0$ into DP <sub>L</sub> .														
	LHI data	Load DP <sub>H</sub> with immediate data	0 1 0 0	1 1 1 0	1	1	$DP_H \leftarrow I_3 I_2 I_1 I_0$	Loads the immediate data $I_3 I_2 I_1 I_0$ into DP <sub>H</sub> .														
	IND	Increment DP <sub>L</sub>	1 1 1 0	1 1 1 0	1	1	$DP_L \leftarrow (DP_L) + 1$	Increments the contents of DP <sub>L</sub> .	ZF													
	DED	Decrement DP <sub>L</sub>	1 1 1 0	1 1 1 1	1	1	$DP_L \leftarrow (DP_L) - 1$	Decrements the contents of DP <sub>L</sub> .	ZF													
	TAL	Transfer AC to DP <sub>L</sub>	1 1 1 1	0 1 1 1	1	1	$DP_L \leftarrow (AC)$	Moves the contents of AC to DP <sub>L</sub> .														
	TLA	Transfer DP <sub>L</sub> to AC	1 1 1 0	1 0 0 1	1	1	$AC \leftarrow (DP_L)$	Moves the contents of DP <sub>L</sub> to AC.	ZF													
	XAH	Exchange AC with DP <sub>H</sub>	0 0 1 0	0 0 1 1	1	1	$(AC) \leftrightarrow (DP_H)$	Exchanges the contents of AC and DP <sub>H</sub> .														

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Instruction group	Mnemonic		Instruction code		Number of bytes	Number of bytes	Operation	Description	Modified status flags	Notes
			D7 D6 D5 D4	D3 D2 D1 D0						
Working register manipulation instructions	XAt	Exchange AC with working register At	1 1 1 0	t <sub>1</sub> to	1	1	(AC) ↔ (A <sub>0</sub> )	Exchanges the contents of AC and the working register A <sub>0</sub> , A <sub>1</sub> , A <sub>2</sub> or A <sub>3</sub> specified by t <sub>1</sub> to.		
	XA0		1 1 1 0	0 1 0 0	1	1	(AC) ↔ (A <sub>1</sub> )			
	XA1		1 1 1 0	0 1 0 0	1	1	(AC) ↔ (A <sub>2</sub> )			
	XA2		1 1 1 0	0 1 0 0	1	1	(AC) ↔ (A <sub>3</sub> )			
	XHa	Exchange DP <sub>H</sub> with working register Ha	1 1 1 1	a	1	1	(DP <sub>H</sub> ) ↔ (H <sub>0</sub> )	Exchanges the contents of DP <sub>H</sub> and the working register H <sub>0</sub> or H <sub>1</sub> specified by a.		
	XH0		1 1 1 1	1 0 0 0	1	1	(DP <sub>H</sub> ) ↔ (H <sub>1</sub> )			
XLa	Exchange DP <sub>H</sub> with working register Ha	1 1 1 1	a	1	1	(DP <sub>H</sub> ) ↔ (L <sub>0</sub> )	Exchanges the contents of DP <sub>H</sub> and the working register L <sub>0</sub> or L <sub>1</sub> specified by a.			
		XL0	1 1 1 1	1 0 0 0	1	1		(DP <sub>H</sub> ) ↔ (L <sub>1</sub> )		
Memory manipulation instructions	SFB flag	Set flag bit	0 1 0 1	B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub>	1	1	F <sub>n</sub> ← 1	Sets the flag specified by B <sub>3</sub> , B <sub>2</sub> , B <sub>1</sub> , B <sub>0</sub> to 1.		
	RFB flag	Reset flag bit	0 0 0 1	B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub>	1	1	F <sub>n</sub> ← 0	Clears the flag specified by B <sub>3</sub> , B <sub>2</sub> , B <sub>1</sub> , B <sub>0</sub> to 0.	ZF	The flags are divided into four groups, F <sub>0</sub> to F <sub>3</sub> , F <sub>4</sub> to F <sub>7</sub> , F <sub>8</sub> to F <sub>12</sub> to F <sub>15</sub> . ZF is set or cleared according to the 4 bits included in the specified flags.
Jump and subroutine instructions	JMP addr	Jumping in the current bank	0 1 1 0 P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub>	1 P <sub>10</sub> P <sub>9</sub> P <sub>8</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	PC ← P <sub>10</sub> P <sub>9</sub> P <sub>8</sub> P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	Jumps to the location specified by the immediate data P <sub>10</sub> P <sub>9</sub> P <sub>8</sub> P <sub>7</sub> P <sub>6</sub> P <sub>5</sub> P <sub>4</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub> .		
	JPEA	Jumping current page modified by E and AC	1 1 1 1	1 0 1 0	1	1	PC <sub>0</sub> to <sub>7</sub> ← (E, AC)	Jumps to the location given by replacing the lower 8 bits of the PC with E and AC.		
	CZP addr	Call subroutine in the zero page	1 0 1 1	P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	1	1	STACK ← (PC) + 1 PC <sub>10</sub> to <sub>8</sub> ← PC <sub>1</sub> to <sub>0</sub> ← 0 PC <sub>5</sub> to <sub>3</sub> ← P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	Calls a subroutine on page 0.		
	CAL addr	Call subroutine	1 0 1 0	1 P <sub>10</sub> P <sub>9</sub> P <sub>8</sub> P <sub>3</sub> P <sub>2</sub> P <sub>1</sub> P <sub>0</sub>	2	2	STACK ← (PC) + 2	Calls a subroutine.		
	RT	Return from subroutine	0 1 1 0	0 0 0 0	1	1	PC ← (STACK)	Returns from a subroutine.		
	RTI	Return from interrupt routine	0 0 1 0	0 0 1 0	1	1	PC ← (STACK) CF, ZF ← CSF, ZSF	Returns from an interrupt handling routine.	ZF CF	
	BANK	Change bank	1 1 1 1	1 1 0 1	1	1		Specifies a pseudo I/O port and changes the bank.		Only valid for the immediately following JMP, I/O, or branch instruction.

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Instruction group	Mnemonic		Instruction code		Number of bytes	Number of bytes	Operation	Description	Modified status flags	Notes
			D7 D6 D5 D4	D3 D2 D1 D0						
Branch instructions	BAt addr	Change bank	0 1 1 1 P7 P6 P5 P4	0 0 t1 to P3 P2 P1 P0	2	2	PC7 to 0 ← P7 P6 P5 P4 P3 P2 P1 P0 if ACt = 1	Branches to the location on the same page specified by P7 to P0 if the bit in AC specified by the immediate data t1 to t0 is 1.		The mnemonics are BA0 to BA3, reflecting the value of t.
	BNAt addr	Branch on no AC bit	0 0 1 1 P7 P6 P5 P4	0 0 t1 to P3 P2 P1 P0	2	2	PC7 to 0 ← P7 P6 P5 P4 P3 P2 P1 P0 if ACt = 0	Branches to the location on the same page specified by P7 to P0 if the bit in AC specified by the immediate data t1 to t0 is 0.		The mnemonics are BNA0 to BNA3, reflecting the value of t.
	BMt addr	Branch on M bit	0 1 1 1 P7 P6 P5 P4	0 1 t1 to P3 P2 P1 P0	2	2	PC7 to 0 ← P7 P6 P5 P4 P3 P2 P1 P0 if [M(DP, t1 to t0)] = 1	Branches to the location on the same page specified by P7 to P0 if the bit in M(DP) specified by the immediate data t1 to t0 is 1.		The mnemonics are BM0 to BM3, reflecting the value of t.
	BNMt addr	Branch on no M bit	0 0 1 1 P7 P6 P5 P4	0 1 t1 to P3 P2 P1 P0	2	2	PC7 to 0 ← P7 P6 P5 P4 P3 P2 P1 P0 if [M(DP, t1 to t0)] = 0	Branches to the location on the same page specified by P7 to P0 if the bit in M(DP) specified by the immediate data t1 to t0 is 0.		The mnemonics are BNM0 to BNM3, reflecting the value of t.
	BPt addr	Branch on Port bit	0 1 1 1 P7 P6 P5 P4	1 0 t1 to P3 P2 P1 P0	2	2	PC7 to 0 ← P7 P6 P5 P4 P3 P2 P1 P0 if [P(DP <sub>t1</sub> , t1 to t0)] = 1	Branches to the location on the same page specified by P7 to P0 if the bit in P(DP <sub>t1</sub> ) specified by the immediate data t1 to t0 is 1.		The mnemonics are BP0 to BP3, reflecting the value of t.
	BNPt addr	Branch on no Port bit	0 0 1 1 P7 P6 P5 P4	1 0 t1 to P3 P2 P1 P0	2	2	PC7 to 0 ← P7 P6 P5 P4 P3 P2 P1 P0 if [P(DP <sub>t1</sub> , t1 to t0)] = 0	Branches to the location on the same page specified by P7 to P0 if the bit in P(DP <sub>t1</sub> ) specified by the immediate data t1 to t0 is 0.		The mnemonics are BNP0 to BNP3, reflecting the value of t.
	BTM addr	Branch on timer	0 1 1 1 P7 P6 P5 P4	1 0 0 0 P3 P2 P1 P0	2	2	PC7 to 0 ← P7 P6 P5 P4 P3 P2 P1 P0 if TMF = 0 then TMF ← 0	Branches to the location on the same page specified by P7 to P0 if TMF is 1. Also clears TMF.	TMF	
	BNTM addr	Branch on no timer	0 0 1 1 P7 P6 P5 P4	1 0 0 0 P3 P2 P1 P0	2	2	PC7 to 0 ← P7 P6 P5 P4 P3 P2 P1 P0 if TMF = 0 then TMF ← 0	Branches to the location on the same page specified by P7 to P0 if TMF is 0. Also clears TMF.	TMF	
	BI addr	Branch on interrupt	0 1 1 1 P7 P6 P5 P4	1 1 0 1 P3 P2 P1 P0	2	2	PC7 to 0 ← P7 P6 P5 P4 P3 P2 P1 P0 if EXTF = 1 then EXTF ← 0	Branches to the location on the same page specified by P7 to P0 if EXTF is 1. Also clears EXTF.	EXTF	
	BNI addr	Branch on no interrupt	0 0 1 1 P7 P6 P5 P4	1 1 0 1 P3 P2 P1 P0	2	2	PC7 to 0 ← P7 P6 P5 P4 P3 P2 P1 P0 if EXTF = 0 then EXTF ← 0	Branches to the location on the same page specified by P7 to P0 if EXTF is 0. Also clears EXTF.	EXTF	

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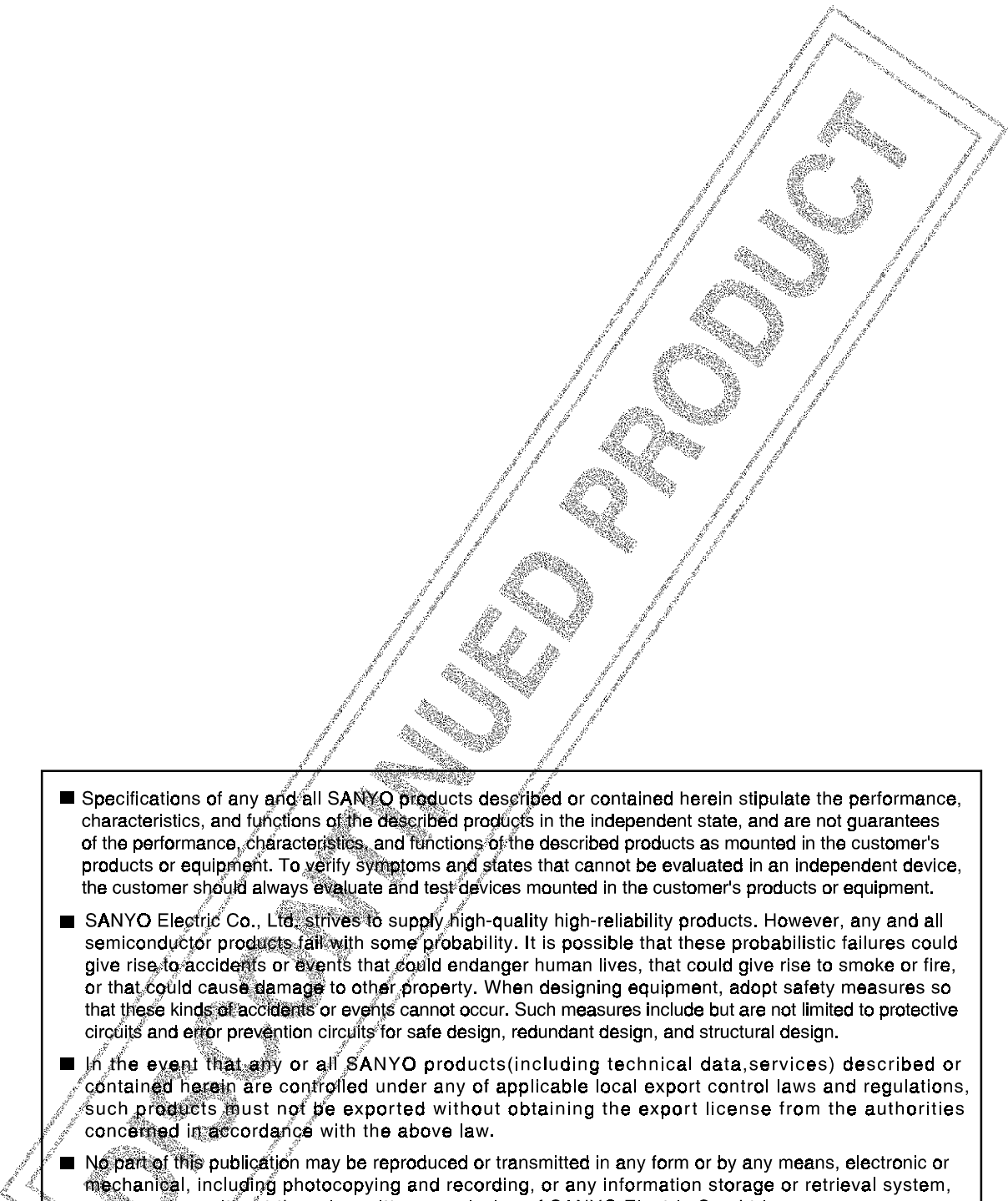
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Instruction group	Mnemonic		Instruction code		Number of bytes	Number of bytes	Operation	Description	Modified status flags	Notes
			D7 D6 D5 D4	D3 D2 D1 D0						
Branch instructions	BC addr	Branch on CF	0 1 1 1 P7 P6 P5 P4	1 1 1 1 P3 P2 P1 P0	2	2	$PC7 \text{ to } 0 \leftarrow P7 P6 P5 P4$ if EXTF = 0	Branches to the location on the same page specified by P7 to P0 if CF is 1.		
	BNC addr	Branch on no CF	0 0 1 1 P7 P6 P5 P4	1 1 1 1 P3 P2 P1 P0	2	2	$PC7 \text{ to } 0 \leftarrow P7 P6 P5 P4$ if CF = 0	Branches to the location on the same page specified by P7 to P0 if CF is 0.		
	BZ addr	Branch on ZF	0 1 1 1 P7 P6 P5 P4	1 1 1 0 P3 P2 P1 P0	2	2	$PC7 \text{ to } 0 \leftarrow P7 P6 P5 P4$ if ZF = 1	Branches to the location on the same page specified by P7 to P0 if ZF is 1.		
	BNZ addr	Branch on no ZF	0 0 1 1 P7 P6 P5 P4	1 1 1 0 P3 P2 P1 P0	2	2	$PC7 \text{ to } 0 \leftarrow P7 P6 P5 P4$ if ZF = 0	Branches to the location on the same page specified by P7 to P0 if ZF is 0.		
	BFn addr	Branch on flag bit	1 1 0 1 P7 P6 P5 P4	n3 n2 n1 n0 P3 P2 P1 P0	2	2	$PC7 \text{ to } 0 \leftarrow P7 P6 P5 P4$ if Fn = 1	Branches to the location on the same page specified by P7 to P0 if the bit in the 16 flags specified by n3 n2 n1 n0 is 1.		The mnemonics are BF0 to BF15, reflecting the value of n.
	BNFn addr	Branch on no flag bit	1 0 0 1 P7 P6 P5 P4	n3 n2 n1 n0 P3 P2 P1 P0	2	2	$PC7 \text{ to } 0 \leftarrow P7 P6 P5 P4$ if Fn = 0	Branches to the location on the same page specified by P7 to P0 if the bit in the 16 flags specified by n3 n2 n1 n0 is 0.		The mnemonics are BF0 to BF15, reflecting the value of n.
I/O instructions	IP	Input port to AC	0 0 0 0	1 1 0 0	1	1	$AC \leftarrow [P(DP_L)]$	Inputs the contents of port P(DP <sub>L</sub> ) to AC.	ZF	
	OP	Output port to AC	0 1 1 0	0 0 0 1	1	1	$P(DP_L B_i B_o) \leftarrow (AC)$	Outputs the contents of AC to port P(DP <sub>L</sub> ).		
	SPB bit	Set port bit	0 0 0 0	0 1 B <sub>i</sub> B <sub>o</sub>	1	2	$P(DP_L B_i B_o) \leftarrow 1$	Sets to 1 the bit in port P(DP <sub>L</sub> ) specified by the immediate data B <sub>i</sub> B <sub>o</sub> .		Executing this instruction destroys the contents of the E register.
	RPB bit	Reset port bit	0 0 1 0	0 1 B <sub>i</sub> B <sub>o</sub>	1	2	$P(DP_L B_i B_o) \leftarrow 0$	Clears to 0 the bit in port P(DP <sub>L</sub> ) specified by the immediate data B <sub>i</sub> B <sub>o</sub> .	ZF	Executing this instruction destroys the contents of the E register.
Other instructions	SCTL bit	Set control register bit (S)	0 0 1 0	1 0 0 0	2	2	$CTL \leftarrow (CTL) \vee B_3 B_2 B_1 B_0$	Sets the bit (or bits) in the control register specified by B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub> .		
	RCTL bit	Reset control register bit (S)	0 0 1 0 1 0 0 1	1 1 0 0 B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub>	2	2	$CTL \leftarrow (CTL) \vee B_3 B_2 B_1 B_0$	Clears the bit (or bits) in the control register specified by B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub> .	ZF	
	WTTM	Write timer	1 1 1 1	1 0 0 1	1	1	$TM \leftarrow (E), (AC)$ TMF ← 0	Loads the contents of E and AC into the timer. Also clears TMF.	TMF	
	HALT	Halt	1 1 1 1	0 1 1 0	1	1	Halt	Stops all operations.		This instruction is disabled only when all bits in port PA are 0.
	NOP	No operation	0 0 0 0	0 0 0 0	1	1	No operation	Consumes one machine cycle while performing no operation.		

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