OKI semiconductor

MSM5219B

48-DOT STATIC LCD DRIVER

GENERAL DESCRIPTION

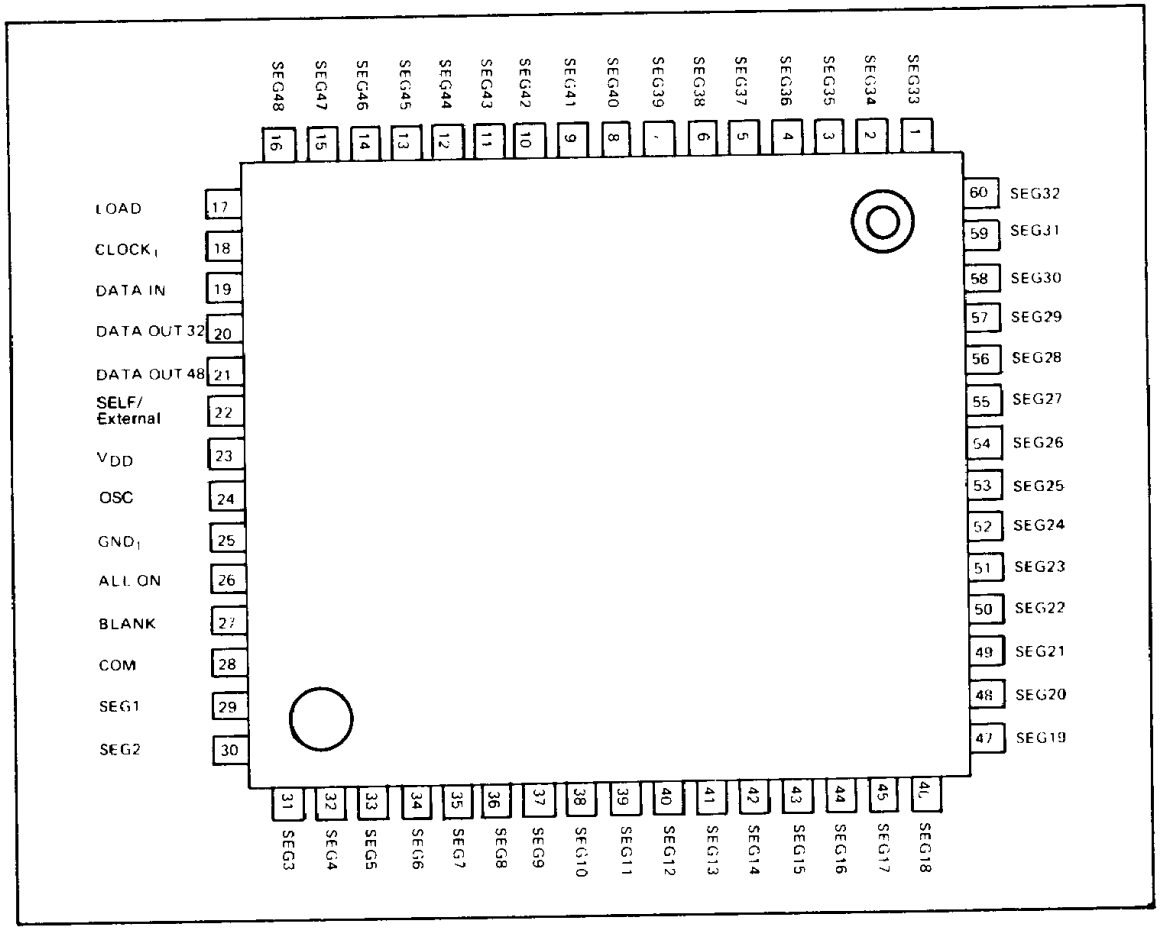
The OKI MSM5219BGS is a 48 dot static LCD driver which is fabricated by low power CMOS metal gate technology. This LSI consists of 48-bit shift register, 48-bit latch and 48-bit LCD driver. The display data, which was input to the 48-bit shift register, is shifted to the 48-bit latch by the LOAD signal. Then the data is output to the LCD panel through the 48-bit LCD driver.

FEATURES

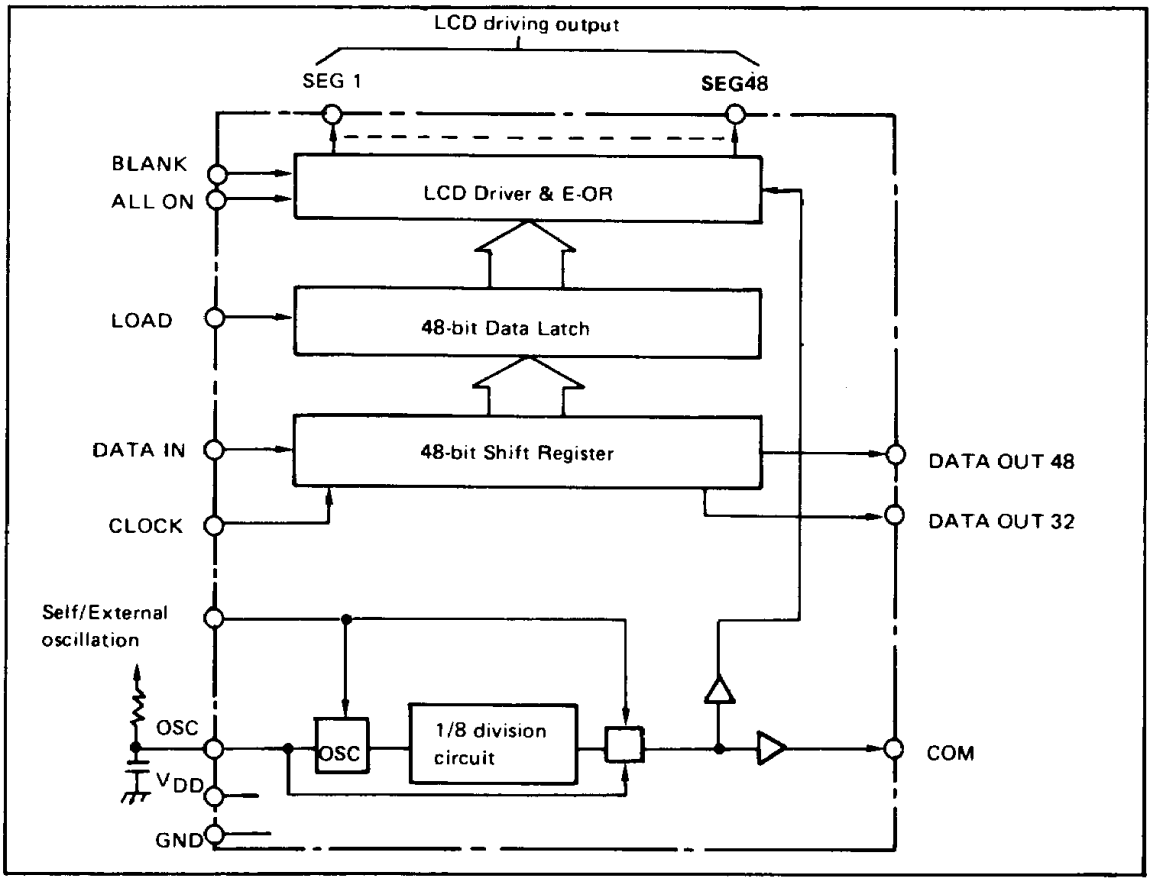
- 48 dots static LCD driving capability
- Simple interface with microcomputer chip (controlled by three input signals)
- Bit-to-bit correspondence between the input and the output
- Cascade connection capability
- LCD driving AC frequency is directly input externally
- Applicable as an output expander
- Supply voltage: 3 ~ 7V
- 60 pin plastic QFP (QFP60-P-1519-K)
- 60 pin -V plastic QFP (QFP60-P-1519-VK)

PIN CONFIGURATION

(Top view) 60 pin plastic QFP



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Limits	Unit
Supply voltage	$V_{DD} - V_{SS}$	T_a = 25°C	−0.3 ~ +7	V
Input voltage	V_I	T_a = 25°C	V_{SS} − 0.3 ~ V_{DD} + 0.3	V
Storage temperature	T_{stg}	—	−55 ~ +150	°C

OPERATING RANGE

Parameter	Symbol	Condition	Limits	Unit
Supply voltage	$V_{DD} - V_{SS}$	Self-Oscillation circuit	4 ~ 7	V
		External oscillation	3 ~ 7	V
Operating temperature	Top	—	−40 ~ +85	°C

DC CHARACTERISTICS

($V_{DD} - V_{SS}$ = 5V, T_a = −40 ~ +85°C)

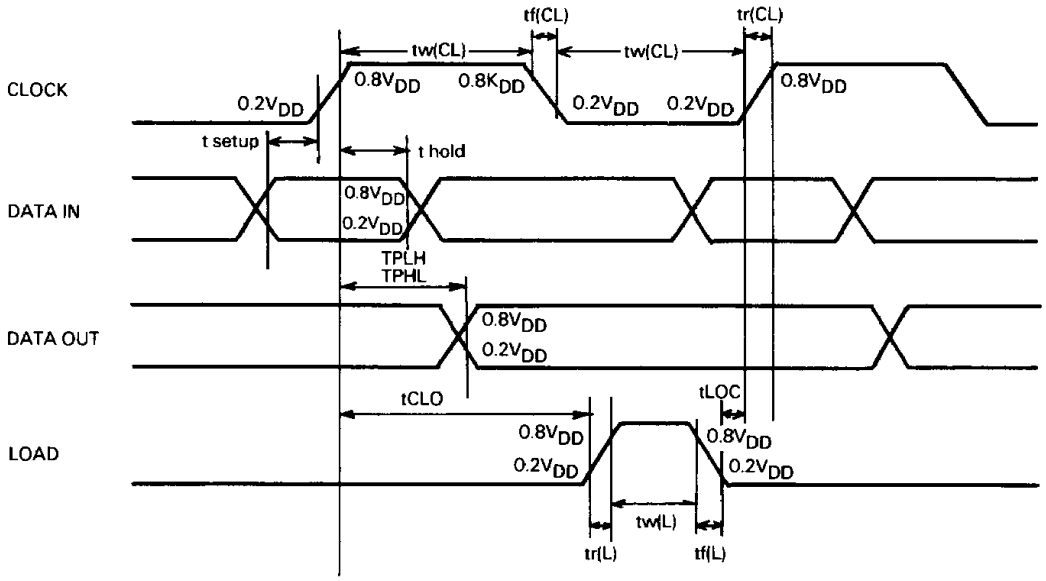
Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
"H" Input voltage*1	V_{IH}	—	3.6	–	–	V
"L" Input voltage*1	V_{IL}	—	–	–	1.0	V
Input leakage current*1	I_{IH}/I_{IL}	V_I = 5V/V_I = 0V	–	–	1/−1	μA
SEG "H" Output voltage	V_{OHS}	I_O = −30μA	4.8	–	–	V
SEG "L" Output voltage	V_{OLS}	I_O = 30μA	–	–	0.2	V
COM "H" Output voltage	V_{OHC}	I_O = −150μA	4.8	–	–	V
COM "L" Output voltage	V_{OLC}	I_O = 150μA	–	–	0.2	V
SEG Output current 1	I_{OHS1}/I_{OLS1}	V_{OH} = 4.5V/V_{OL} = 0.5V	−100/ 100	–	–	μA
SEG Output current 2	I_{OHS2}/I_{OLS2}	V_{OH} = 1V/V_{OL} = 4V	−400/ 400	–	–	μA
COM Output current 1	I_{OHC1}/I_{OLC1}	V_{OH} = 4.5V/V_{OL} = 0.5V	−500/ 500	–	–	μA
COM Output current 2	I_{OHC2}/I_{OLC2}	V_{OH} = 1V/V_{OL} = 4V	−2/2	–	–	mA
"H" Output voltage*2	V_{OH}	I_O = −40μA	4.2	–	–	V
"L" Output voltage*2	V_{OL}	I_O = 1.6mA	–	–	0.4	V
Output current*2	I_{OH}/I_{OL}	V_O = 2.5V/V_O = 0.4V	−0.2/ 1.6	–	–	V
Clock pulse width	$t_{W\phi}$	*3	5	–	–	μS
		*4	0.5	–	–	
Max. clock pulse frequency	$f_{\phi MAX}$	*3	0.1	–	–	MHz
		*4	1	–	–	
Input signal rising/falling time	$t_{r\phi}$, $t_{f\phi}$	*5	–	–	5	μS
Static current consumption	I_{DD1}	—	–	–	100	μA
Active current consumption	I_{DD2}	No load when R_{OSC} = 150 kΩ, C_{OSC} = 0.015 μF	–	–	2	mA
COM Frequency (Self oscillation)	f_{COM}	No load when V_{DD} = 5V	25	–	300	Hz

*1: Applicable to all terminals except OSC. This condition is applied to OSC in the external oscillation mode.
*2: Applicable to DATA OUT 32, DATA OUT 48.
*3: Applicable to OSC.
*4: Applicable to CLOCK.
*5: Applicable to all terminals except OSC terminal.

Switching Characteristisc

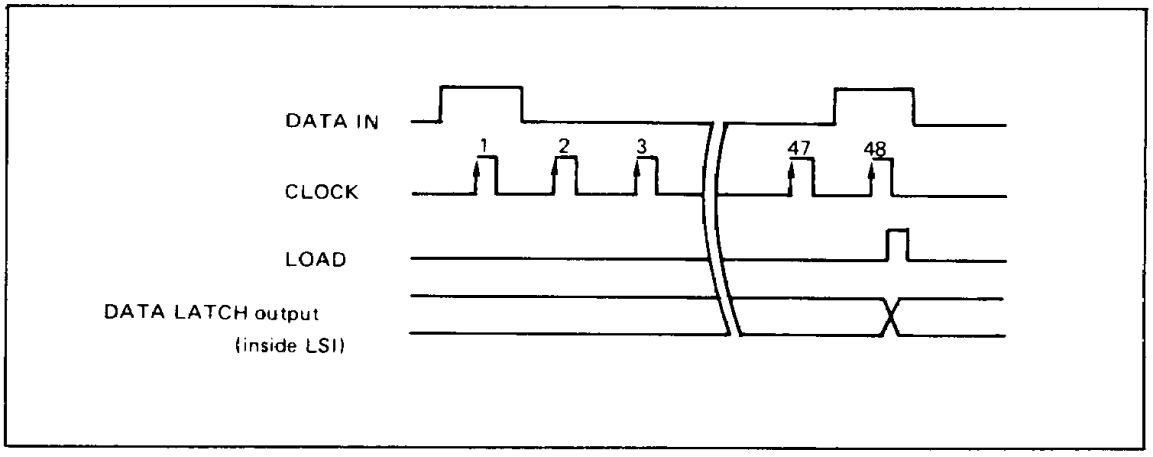
(V_{DD} = 5V ± 10% Ta = 25°C)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Propagation delay time	tP HL	—	—	—	600	ns
Data out delay time	tP LH	—	—	—	600	ns
Maximum clock frequency	fCL	DUTY = 50%	1	—	—	MHz
Clock width	tw (CL)	—	400	—	—	ns
Load width	tw (L)	—	400	—	—	ns
Data setup time	t setup	—	300	—	—	ns
Data hold time	t hold	—	300	—	—	ns
Clock-to-load time	t CLO	—	500	—	—	ns
Load-to-clock time	t LOC	—	0	—	—	ns
Clock rise/fall time	tr (CL), td (CL)	—	50	—	—	ns
Load rise/fall time	tr (L), tf (L)	—	1	—	—	ns



FUNCTIONAL DESCRIPTION

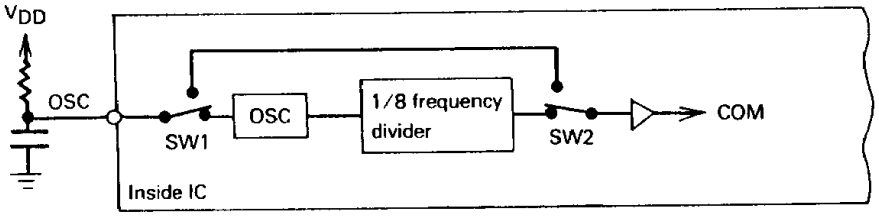
- **Operational Description**
  The display data is input to the shift register by the DATA IN signal and CLOCK signal. It is transferred to the 48-bit latch by the LOAD signal and it is output to the LCD panel through 48-bit LCD driver.



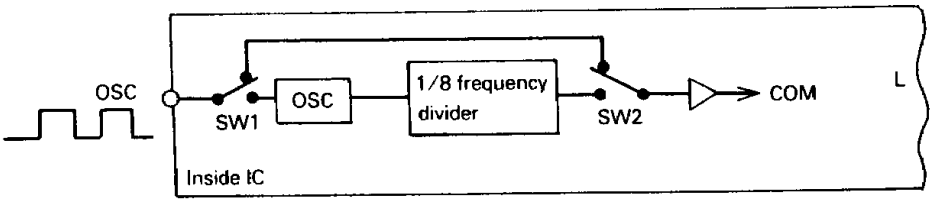
- **OSC**
  The clock, which is used to generate the COM signal and the LCD driving signal, is input to this pin.

- **OSC Terminal**
  This terminal is used to generate COM signal.
  When the self-excited/separately-excited terminal is set to "H" level, the oscillation circuit is formed by connecting the resistor and capacitor to this terminal, and the 1/8 divided frequency of the oscillation frequency is output as COM signal. When the self-excited/separately-excited terminal is set to "L" level, the logical level of the OSC terminal is used as COM signal without change. This is used for cascaded connection in the IC.

In case that the self-excited/separately-excited terminal is at "H" level.



In case that the self-excited/separately-excited terminal is at "L" level.



- **DATA IN CLOCK$_1$**
  DATA IN is a data input pin which enables the LCD to display when DATA IN pin is at high level. The 48-bit shift register is shifted at the rising edge of the CLOCK signal. Initially, the first bit of the shift register contains the current logic level of the DATA IN pin, and the bit N (N = 2 ~ 48) contains the data which was in bit N − 1 (N = 2 ~ 48) before the start of the operation. The data which was in bit 48 before the operation start is considered invalid.

- **LOAD**
  The data in the 48-bit shift register is shifted to the 48-bit latch when the LOAD pin set at high level, while the last data which was transferred to the latch when the LOAD pin was set at high level is constantly output when the LOAD pin is set at low level.

- **ALL SEG ON**
  When this pin is set at high level, all segments display turn on. This pin has the priority to the BLANK pin described as below.

- **BLANK**
  When this pin is set at high level, all segments display turn off. The ALL SEG ON pin has the priority over this pin.

- **SEG1 ~ SEG48**
  LCD driving output pins. The reversed phase of the COM signal, which is used to display the data, is output from these pins when SEG1 ~ SEG48 are set at high level, while there is no display on the LCD when these pins are set at low level. The data which was input from the DATA IN pin is output from these pins to the LCD panel. The SEG N pin corresponds to the bit N of the shift register.

- **COM**
  Output terminal for the LCD. It is connected to the common side of the LCD.

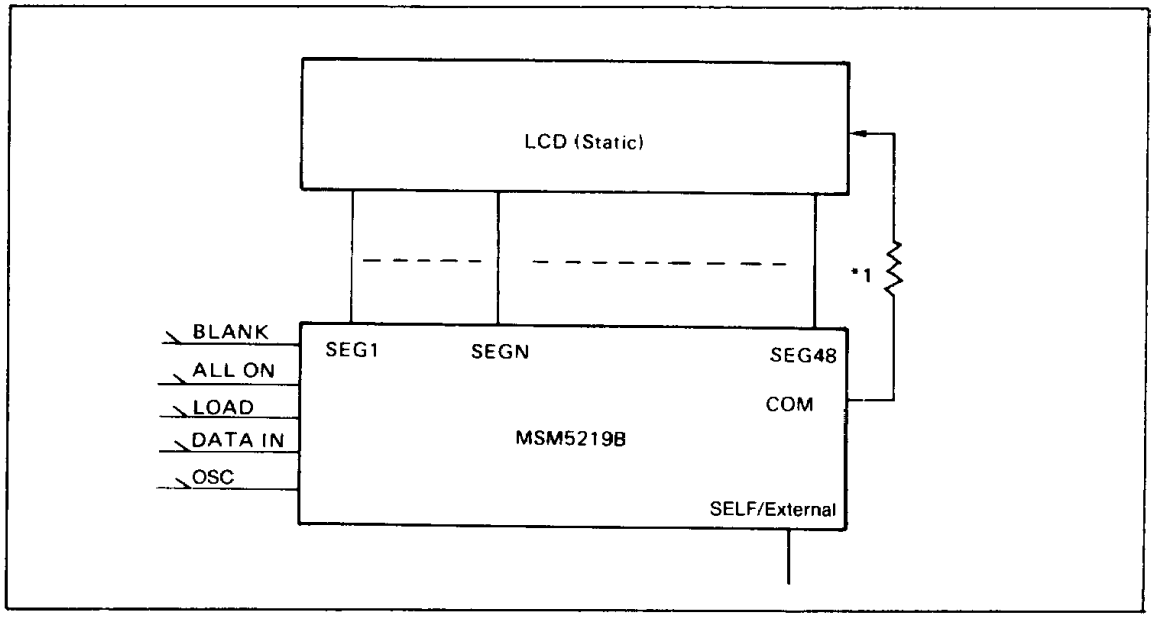
- **DATA OUT 32, DATA OUT 48**
  Output pin of the shift register. It is used when the MSM5219BGS is connected in a series (cascade connection). It is connected to next MSM5219BGS's DATA IN terminal.

- **SELF/EXTERNAL**
  When this pin is set at high level, OSC is self mode. At low level, OSC is external mode.

- **Self-excited/separately-excited terminal**
  This terminal is used to switch over functions of OSC terminal. When "H" level is set, OSC terminal forms an oscillation circuit, and the 1/8 divided frequency is output as COM signal.
  When "L" level is set, the OSC terminal is separated from the oscillation circuit, and its input logical level is used as COM signal without change. When cascade-connecting the IC, the terminal is to be set "H" level at the master and "L" level at the slave.

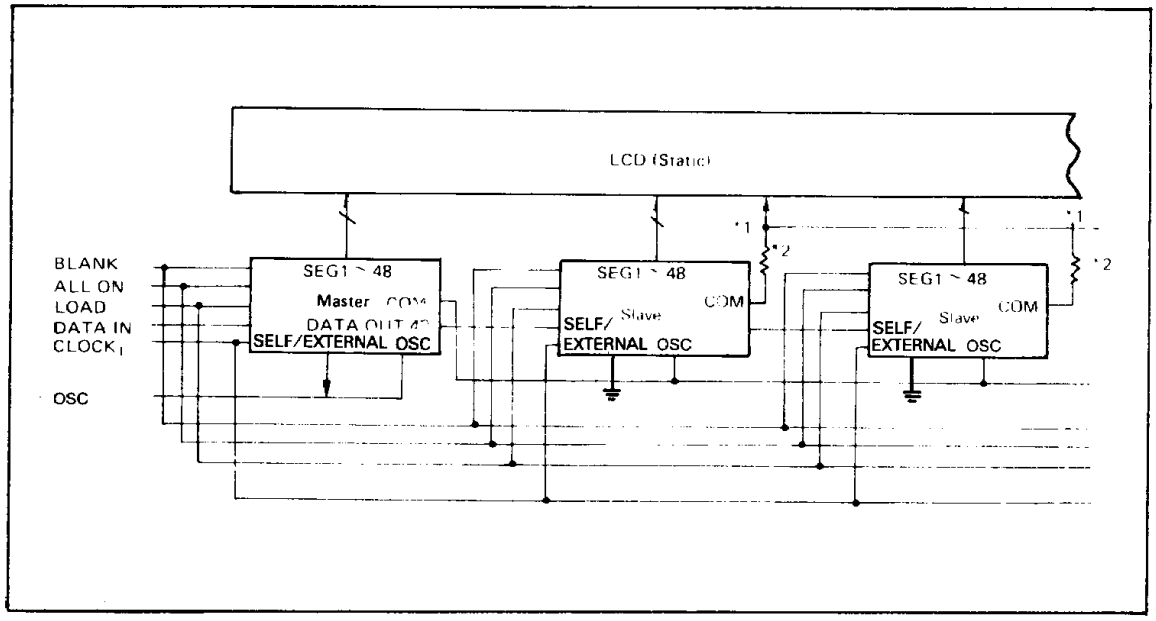
APPLICATION CIRCUIT

- **Single MSM5219BGS**



*1: When this IC is used under a strong external noise or large-capacity LCD load, this resistor prevents latch-up to be caused by a low output impedance of the COM pin.
The resistance is about 100Ω.

- **Cascade connection**

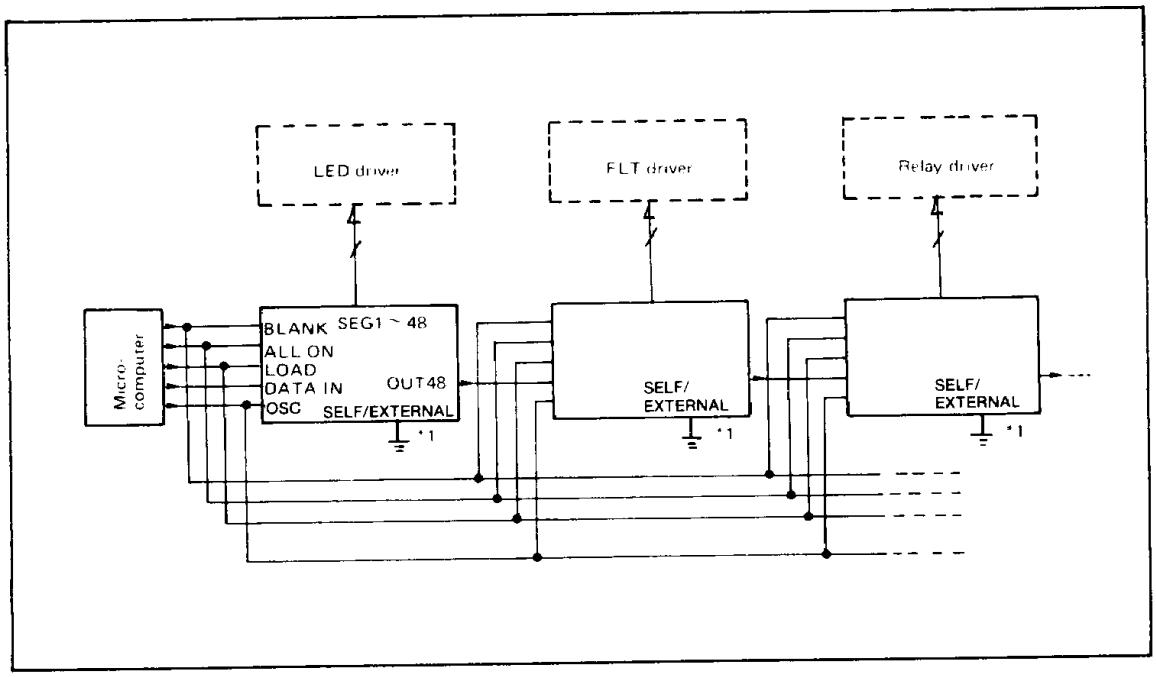


*1: The COM pin of the slave MSM5219BGS can be WIRED OR.

*2: When this IC is used under a strong external noise or large-capacity LCD load, this resistor prevents latch-up to be caused by a low output impedance of the COM pin.
The resistance is about 100Ω.

● **Output Expander**

As explained above, this IC can drive the static LCD with the COM pin. In addition, it can also be used as an output pin expander for a microcomputer with the following connections:



*1: In this example, "H" is output by the positive logic, that is, when "H" is written from DATA IN, "H" is output with a LOAD signal. If the OSC pin is connected to V_{DD}, the output has the negative logic, that is, the logic level input from the DATA IN pin is inverted and output.