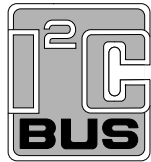


DATA SHEET



SAA7219 MPEG2 Transport RISC processor

Product specification
Supersedes data of 2000 Jun 14
File under Integrated Circuits, IC02

2001 Mar 28

MPEG2 Transport RISC processor**SAA7219**

CONTENTS

1	FEATURES
1.1	External interfaces
1.2	CPU related features
1.3	MPEG2 systems features
2.1	SAA7219 overview
2.2	SAA7219 in a DVB system
3	ORDERING INFORMATION
5	PINNING
6	APPLICATION INFORMATION
6.1	Memory configurations
7	PACKAGE OUTLINE
8.1	Introduction to soldering surface mount packages
8.2	Reflow soldering
8.3	Wave soldering
8.4	Manual soldering
8.5	Suitability of surface mount IC packages for wave and reflow soldering methods
9	DATA SHEET STATUS
10	DEFINITIONS
11	DISCLAIMERS

MPEG2 Transport RISC processor

SAA7219

1 FEATURES

- Conditional access descrambling Digital Video Broadcasting (DVB) compliant and MULTI2 compliant
- Stream demultiplexing: Transport Stream (TS), Packetized Elementary Stream (PES), program and proprietary streams
- Internal 32-bit MIPS RISC based Central Processing Unit (CPU) supporting MIPS16 instruction set and running at 81 MHz
- Low-power sleep modes supported across the chip
- Comprehensive driver software and development tool support
- Package: SQFP208.

1.1 External interfaces

- Versatile compressed stream input at 108 Mbits/s
- A 32-bit microcontroller extension bus supporting DRAM, SDRAM, Flash, (E)PROM and external memory mapped I/O devices. It also supports a synchronous interface to communicate with the integrated MPEG Audio Video Graphics Decoder (AVGD) SAA7215 at 40.5 Mbytes.
- An IEEE 1284 interface (Centronics) supporting master and slave modes. Usable as a general purpose port.
- An interface to IEEE 1394 devices (such as Philips PDI 1394 chip-set)
- Two UART (RS232) data ports with Direct Memory Access (DMA) capabilities (187.5 kbits/s) including hardware flow control signals RXD, TXD, RTS and CTS for modem support
- A Synchronous Serial Interface (SSI) to connect an off-chip modem analog front-end
- An elementary UART with DMA capabilities, dedicated to front panel devices for instance
- Two dedicated smart-card reader interfaces (ISO 7816 compatible) with DMA capabilities
- Two I²C-bus master/slave transceivers with DMA capabilities, supporting the standard (100 kbit/s) and fast (400 kbits/s) I²C-bus modes
- 32 general purpose, bidirectional I/O interface pins, 8 of which may also be used as interrupt inputs
- One Pulse Width Modulated (PWM) output with 8-bit resolution



- A General Purpose/High-Speed (GP/HS) interface supporting stream recording through IEEE 1394 interface IC
- An extended JTAG interface for board test support.

1.2 CPU related features

The SAA7219 contains an embedded RISC CPU, which incorporates the following features:

- A 32-bit PR3930 core running at 81 MHz
- 8-kbyte, 2-way set associative instruction cache
- 4-kbyte, 4-way set associative data cache
- A programmable low-power mode, including wake-up on interrupt
- A memory management unit with 32 odd/even entries and variable page sizes
- Multiply/accumulate/divide unit with fast multiply/accumulate for 16-bit and 32-bit operands
- Two fully independent 24-bit timers and one 24-bit timer including watchdog facilities
- A real-time clock unit (active in Sleep mode)
- Built-in software debug support unit as part of Extended Enhanced JTAG debug interface
- On-chip SRAM of 4 kbytes for storing code which needs fast execution.

1.3 MPEG2 systems features

- Hardware based parsing of Transport Stream (TS), Philips Semiconductors program and proprietary software data streams. Maximum input rate is 108 Mbits/s.
- A real-time descrambler consisting of 3 modules:
 - A control word bank containing 14 pairs (odd, even) of control words and a default control word
 - The DVB descrambler core implementing the stream decipher and block decipher algorithms
 - The MULTI2 descrambler algorithm implementing the CBC and OFB mode descrambling functions.

MPEG2 Transport RISC processor

SAA7219

- Hardware section filtering based on 32 different Packet Identifiers (PIDs) with a flexible number of filter conditions (8 or 4-byte condition plus 8 or 4-byte mask) per PID and a total filter capacity of 40 (8-byte condition checks) or up to 80 (4-byte condition checks) filter conditions:
 - 4 TS/PES filters for retrieval for data at TS or PES level for applications such as subtitling, TXT or retrieval of private data
 - Flexible DMA based storage of the 32 section substreams and 4 TS/PES data substreams in the external memory.
- System time base management with a double counter mechanism for clock control and discontinuity handling, 2 Presentation Time Stamp (PTS)/Decoding Time Stamp (DTS) timers
- A GP/HS filter which can serve as an alternate input from for example IEEE 1394 devices. The IEEE 1394 GP/HS mode supports packet insertion and has an internal SRAM for storing 2 packets. It can also output either scrambled or descrambled TS to IEEE 1394 devices.

2 GENERAL DESCRIPTION

2.1 SAA7219 overview

The device is part of a comprehensive source decoding kit which contains all the hardware and software required to receive and decode MPEG2 transport streams, including descrambling, demultiplexing. In addition, it includes a PR3930 core which is a 32-bit MIPS RISC-based CPU core supporting the MIPS 16 instruction set to reduce memory requirements and several peripheral interfaces such as UARTs, I²C-bus units, an IEC 1883, and an IEEE 1284 (Centronics) interface. The SAA7219 is therefore capable of performing all controller tasks in digital television receiver applications such as set-top boxes. Furthermore, the SAA7219 is compliant to DVB and MULT12 standards.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7219HS/C2	SQFP208	plastic shrink quad flat package; 208 leads (lead length 1.3 mm); body 28 × 28 × 3.4 mm; high stand-off height	SOT316-1

The SAA7219 receives transport streams through a versatile stream input interface capable of handling both byte-parallel and bit-serial streams in various formats, supporting data streams up to and including 13.5 Mbyte/s (108 Mbits/s). The stream data is first applied to an on-chip descrambler incorporating a DVB descrambling algorithm, on the basis of 14 control word pairs stored in on-chip RAM. Demultiplexing is subsequently applied to the stream, to separate up to 32 individual data streams.

The demultiplexer section includes clock recovery and timebase management. Program Specific Information (PSI), Service Information (SI), Conditional Access (CA) messages and private data are selected and stored in external memory, for subsequent off-line processing by the internal PR3930 CPU core.

To support advanced board testing facilities the SAA7219 includes boundary scan test hardware, according to the EJTAG standard. The device features a low-power sleep mode, which is capable of sustaining set-top box standby functionality, thus eliminating the need for a separate front panel controller. The SAA7219 requires a supply voltage of 3.3 V and most devices input and output interfaces are 5 V tolerant except the extension bus which is 3.3 V only. The SAA7219 is mounted in a SQFP208 package.

2.2 SAA7219 in a DVB system

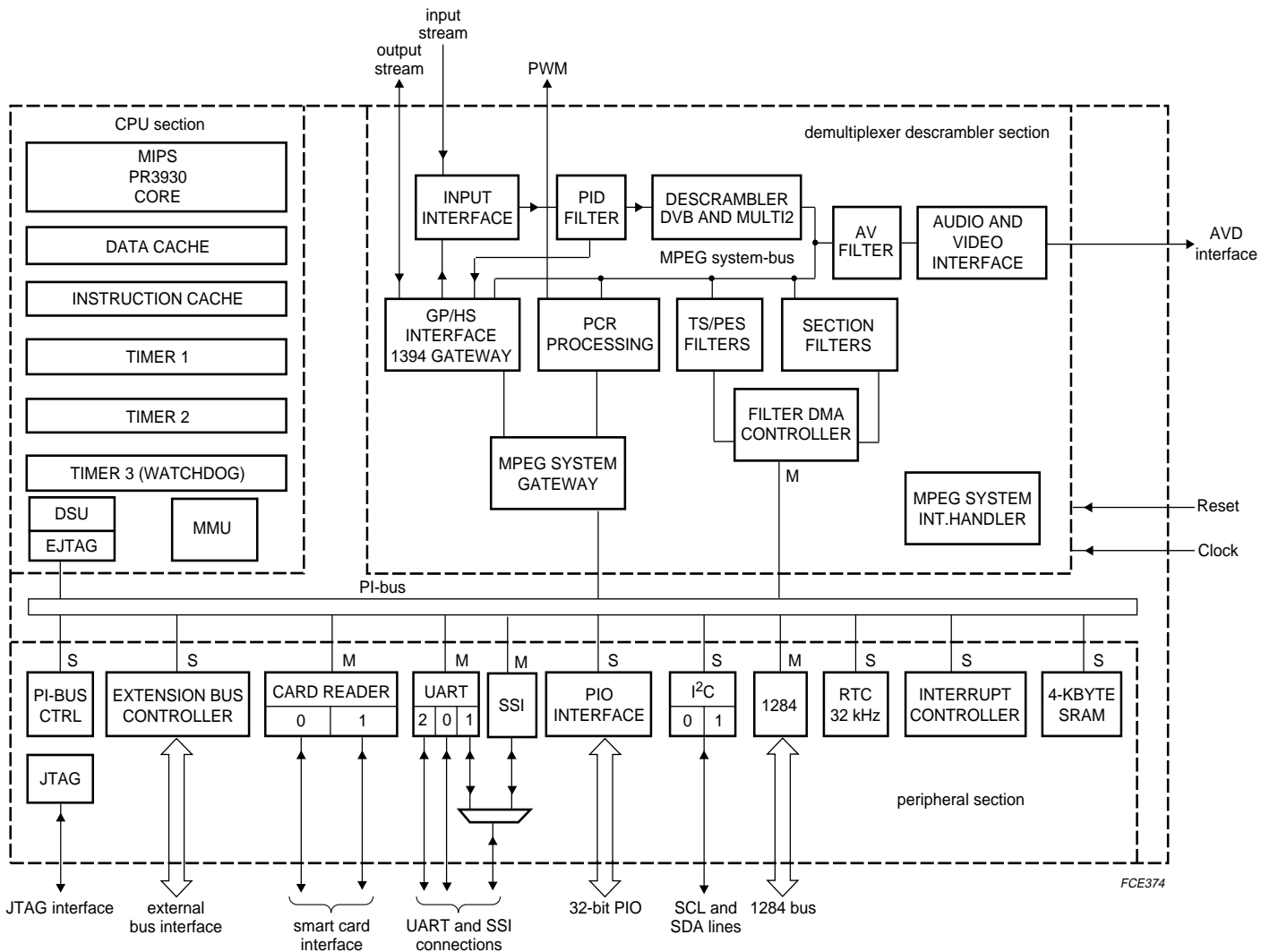
The SAA7219 has been designed to offer optimum performance when used with the SAA7215 for MPEG2 AVG decoding.

- Synchronous bus interface transfer at 40.5 MHz on 16 bits
- SAA7215 has one dedicated SDRAM for MPEG2 audio video handling and one for graphics and CPU data. The second memory offers high bandwidth and low latency to the SAA7219 when accessing it to download graphics or executing some applications. This enables a high level of performance together with a low system cost by having one SDRAM for graphics and CPU data.

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SAA7219

4 BLOCK DIAGRAM



M = master peripheral with embedded DMA channel
 S = slave peripheral

Fig.1 Block diagram.

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5 PINNING

Table 1 SQFP208 package: 179 functional pins and 29 power supply pins

SYMBOL	PIN	I/O	BUFFER TYPE	VOLT ⁽¹⁾	DESCRIPTION
PIO interface (32 pins)					
PIO0 to PIO7	105 to 112	I/O	bidirectional, 3 mA output drive	5 V	usable as interrupt inputs and/or I/O lines
PIO8/BOOTIS32	113	I/O	bidirectional, 3 mA output drive	5 V	PIO bit and PIO-strap. At power-on, it indicates the data bus size of the booting device.
PIO9/BOOTIS16	114	I/O	bidirectional, 3 mA output drive	5 V	PIO bit and PIO-strap. At power-on, if BOOTIS32 is LOW, it indicates if the system should reboot from a 16-bit or 8-bit device.
PIO10 to PIO15	116 to 121	I/O	bidirectional, 3 mA output drive	5 V	PIO bit and PIO-strap
PIO(31:16)/D(31:16)	2, 4 to 9, 11 to 16, 18 to 20	I/O	bidirectional, 6 mA output drive	5 V	I/O lines or upper 16-bit data bus. The data bus width of the booting device is automatically configured at power-on.
Extension bus (58 pins)					
D15 to D0	21, 22, 24, 25, 28 to 30, 33 to 36, 38 to 41	I/O	bidirectional, 8 mA output drive	3.3 V	lower 16-bit data bus
A0 to A21	63 to 65, 67 to 71, 73 to 77, 81 to 85, 87 to 90	O	8 mA output drive	3.3 V	address bus
RAS0N	49	O	8 mA output drive	3.3 V	row access strobe for DRAM and SDRAM Bank 0
RAS1N/DCS1N	48	O	8 mA output drive	3.3 V	row access strobe for DRAM and SDRAM Bank 1
LCASN	46	O	8 mA output drive	3.3 V	column access strobe lower byte
MLCASN	43	O	8 mA output drive	3.3 V	column access strobe mid lower byte
MUCASN	44	O	8 mA output drive	3.3 V	column access strobe mid upper byte
UCASN	42	O	8 mA output drive	3.3 V	column access strobe upper byte
WEN	62	O	8 mA output drive	3.3 V	write enable
DCS0N	47	O	8 mA output drive	3.3 V	chip select for SDRAM Bank 0
CS6N to CS0N	50 to 56	O	8 mA output drive	3.3 V	chip select
OEN	58	O	8 mA output drive	3.3 V	output enable
DTACKN	59	I	TTL input	5 V	Data termination acknowledge. Asserted LOW by the peripheral when the data bus is valid.
CS_SDN	60	O	2 mA output drive	3.3 V	selects the graphics SDRAM memory space of the SAA7215

MPEG2 Transport RISC processor

SAA7219

SYMBOL	PIN	I/O	BUFFER TYPE	VOLT ⁽¹⁾	DESCRIPTION
CS_RGN	61	O	2 mA output drive	3.3 V	selects the control registers of the SAA7215
CLK	91	O	8 mA output drive	3.3 V	40.5 MHz clock
UART 0 interface (4 pins)					
RXD0	141	I	TTL input	5 V	UART 0 receive data line or receive serial data
TXD0	142	O	2 mA output drive	3.3 V	UART 0 transmit data line or transmit serial data
RTSN0	143	O	2 mA output drive	3.3 V	UART 0 request to send
CTSN0	144	I	TTL input	5 V	UART 0 clear to send
UART 1 and SSI interfaces (5 pins)					
RXD1/V34_RXD	137	I	TTL input	5 V	UART 1 receive data line or receive serial data of the SSI interface
TXD1/V34_TXD	138	O	2 mA output drive	3.3 V	UART 1 transmit data line or transmit serial data of the SSI interface
RTSN1/V34_FS	139	I/O	bidirectional, 3 mA output drive	5 V	UART 1 request to send (output) or frame synchronization reference of the SSI interface (input)
CTSN1/V34_CLK	140	I	TTL input	5 V	UART 1 clear to send or serial input interface clock of the SSI interface (up to 3.375 MHz)
MCLK	146	O	2 mA output drive	3.3 V	master clock for the SSI interface (36.684 MHz)
UART 2 interface (2 pins)					
RXD2	135	I	TTL input	5 V	UART 2 receive data line
TXD2	136	O	2 mA output drive	3.3 V	UART 2 transmit data line
I²C-bus 0 interface (2 pins)					
SCL0	149	I/O	bidirectional with open-drain 8 mA output drive	5 V	I ² C-bus 0 clock line
SDA0	150	I/O	bidirectional with open-drain 8 mA output drive	5 V	I ² C-bus 0 data line

MPEG2 Transport RISC processor

SAA7219

SYMBOL	PIN	I/O	BUFFER TYPE	VOLT ⁽¹⁾	DESCRIPTION
I²C-bus 1 interface (2 pins)					
SCL1	147	I/O	bidirectional with open-drain 8 mA output drive	5 V	I ² C-bus 1 clock line
SDA1	148	I/O	bidirectional with open-drain 8 mA output drive	5 V	I ² C-bus 1 data line
Smart card 0 interface (5 pins)					
CLK_CARD0	128	O	2 mA output drive	3.3 V	ISO UART 0 card clock
CMDVCCN0	129	O	2 mA output drive	3.3 V	ISO UART 0 command of the VCC
RSTIN0	132	O	2 mA output drive	3.3 V	ISO UART 0 reset of the card
OFFN0	133	I	TTL input	5 V	ISO UART 0 card presence
SC_I/O0	134	I/O	bidirectional with open-drain 8 mA output drive	5 V	ISO UART 0 I/O line
Smart card 1 interface (5 pins)					
CLK_CARD1	122	O	2 mA output drive	3.3 V	ISO UART 1 card clock
CMDVCCN1	123	O	2 mA output drive	3.3 V	ISO UART 1 command of the VCC
RSTIN1	124	O	2 mA output drive	3.3 V	ISO UART 1 reset of the card
OFFN1	125	I	TTL input	5 V	ISO UART 1 card presence
SC_I/O1	126	I/O	bidirectional with open-drain 8 mA output drive	5 V	ISO UART 1 I/O line
Input Stream interface (11 pins)					
PKTSTROBE	154	I	TTL input	5 V	byte strobe or bit strobe
PKTSYNC	155	I	TTL input	5 V	packet synchronization
PKTVALID	156	I	TTL input	5 V	data valid, or bit stream word select
PKTDATA7 to PKTDATA0	157 to 164	I	TTL input	5 V	8-bit primary TS data input
GP/HS interface (11 pins)					
GPDATA7 to GPDATA0	166 to 169, 171 to 174	I/O	bidirectional, 3 mA output drive	5 V	GP/HS data bus
GPVALID	175	I/O	bidirectional, 3 mA output drive	5 V	GP/HS control lines
GPSYNC	176	I/O	bidirectional, 3 mA output drive	5 V	GP/HS control lines
GPSTROBE	177	I/O	bidirectional, 3 mA output drive	5 V	GP/HS control lines

MPEG2 Transport RISC processor

SAA7219

SYMBOL	PIN	I/O	BUFFER TYPE	VOLT ⁽¹⁾	DESCRIPTION
SAA7215 MPEG interface (11 pins)					
V_STROBE	93	O	2 mA output drive	3.3 V	HIGH-to-LOW transition strobes the video data in the AV_DATA stream
A_STROBE	94	O	2 mA output drive	3.3 V	HIGH-to-LOW transition strobes the audio data in the AV_DATA stream
AV_ERROR	95	O	2 mA output drive	3.3 V	flag for bit stream error (active HIGH)
AV_DATA7 to AV_DATA0	96 to 103	O	2 mA output drive	3.3 V	MPEG audio/video stream output port
IEEE 1284 interface (18 pins)					
GPD0 to GPD7	190 to 197	I/O	bidirectional, 3 mA output drive	5 V	parallel data bus
NSELECTIN	199	I/O	bidirectional, 3 mA output drive	5 V	host to peripheral select line
NINIT	200	I/O	bidirectional, 3 mA output drive	5 V	host to peripheral control line
NSTROBE	201	I/O	bidirectional, 3 mA output drive	5 V	host to peripheral strobe line
NACK	202	I/O	bidirectional, 3 mA output drive	5 V	peripheral acknowledge line
BUSY	203	I/O	bidirectional, 3 mA output drive	5 V	peripheral busy line
PERROR	204	I/O	bidirectional, 3 mA output drive	5 V	peripheral error line
SELECT	205	I/O	bidirectional, 3 mA output drive	5 V	peripheral on-line
NAUTOF	206	I/O	bidirectional, 3 mA output drive	5 V	host to peripheral control line
NFAULT	207	I/O	bidirectional, 3 mA output drive	5 V	peripheral error line
DIR1284	208	O	2 mA output drive	3.3 V	direction control of the external buffers
PWM interface (1 pin)					
PWM0	165	O	open-drain 8 mA output drive	5 V	open-drain 5 V tolerant for VCXO control
System interface (3 pins)					
RESETN	1	I/O	bidirectional with open-drain 8 mA output drive and Schmitt trigger input with high hysteresis	3.3 V	General system reset; active LOW. The pad is bidirectional with an open-drain which is asserted LOW when the internal watchdog time out is detected.
XTAL1	153	I		3.3 V	13.5 MHz crystal input
XTAL2	152	O		3.3 V	13.5 MHz crystal output

MPEG2 Transport RISC processor

SAA7219

SYMBOL	PIN	I/O	BUFFER TYPE	VOLT ⁽¹⁾	DESCRIPTION
JTAG and Test interface (5 pins)					
TDO	178	O	3-state, 2 mA output drive	3.3 V	Test data output/Target PC output. Real-time trace mode off. Serial output data is shifted from JTAG instruction register to the TDO pin on the falling edge of the TCK clock. When no data is shifted out, TDO is 3-stated. Real-time trace mode on. TDO provides non-sequential program counter output at the processor clock speed.
TDI	179	I	TTL input	5 V	Test data input/Debug interrupt. Real-time trace mode off. Serial input data (TDI) is shifted into the JTAG instruction register or data register on the rising edge of the TCK clock, depending of the TAP controller state. Real-time trace mode on. An active LOW level at this input sampled by TCK positive edge, is used as interrupt to switch the real-time trace mode off (standard JTAG).
TMS	180	I	TTL input	5 V	Test mode select. This input is decoded by the TAP controller to control test operation. Sampled on the rising edge of TCK.
TRST	181	I	TTL input	5 V	Test reset. Active LOW level for asynchronous reset of the EJTAG module, independent of the processor logic.
TCK	184	I	TTL input	5 V	Test clock. Input clock used to shift data into or out from the JTAG instruction or data register.
EJTAG extension reserved for PR3930 (4 pins)					
DSU_CLK	185	O	2 mA output drive	3.3 V	DSU clock is equivalent to the processor clock. Captures address and data from pin TDO when PC trace mode is on. Is 3-stated when bit 0 or 15 of the JTAG control register is logic 0.
PCST0 to PCST2	186, 188 and 189	O	2 mA output drive	3.3 V	CPU status: debug mode, pipeline stall, occurrence of exception

MPEG2 Transport RISC processor

SAA7219

SYMBOL	PIN	I/O	BUFFER TYPE	VOLT ⁽¹⁾	DESCRIPTION
Supplies (29 pins)					
V _{DD(P)}	3, 17, 31, 43, 66, 80, 92, 115, 145 and 187	–	–	–	pad supply voltage
V _{SS(P)}	10, 23, 37, 57, 72, 86, 104, 127, 170 and 198	–	–	–	ground supply
V _{DD(C)}	27, 79, 130 and 182	–	–	–	core supply voltage
V _{SS(C)}	26, 78, 131 and 183	–	–	–	ground supply
V _{DD(PLL)}	151	–	–	–	analog supply for the on-chip PLLs

Note

- 5 V tolerant inputs can receive signals swinging between V_{SS} and 3.3 V or V_{SS} and 5 V. 5 V tolerant bidirectional I/O pins can receive signals swinging between V_{SS} and 3.3 V or V_{SS} and 5 V when they are inputs and swing between V_{SS} and V_{DD} when they are outputs.

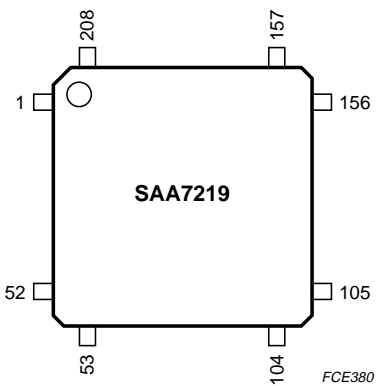


Fig.2 Pin configuration

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SAA7219

6 APPLICATION INFORMATION

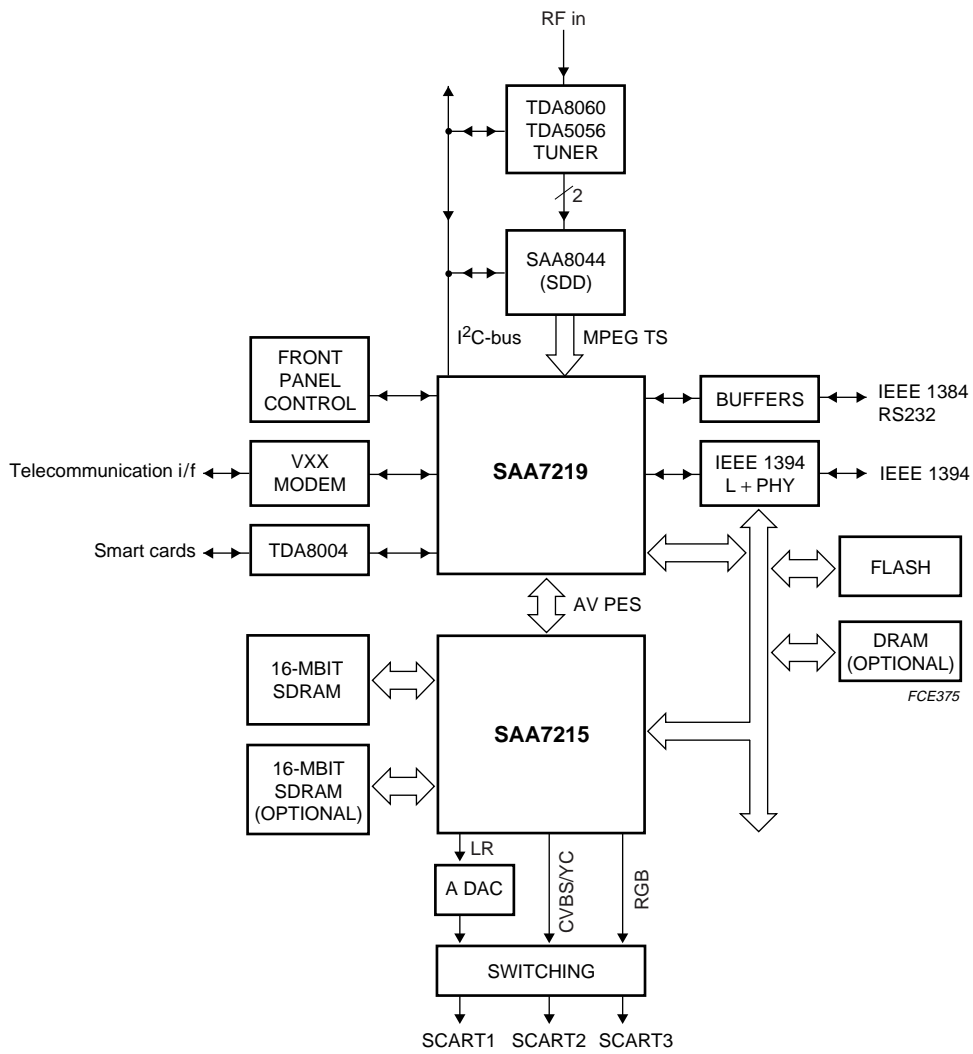


Fig.3 Set-top box example.

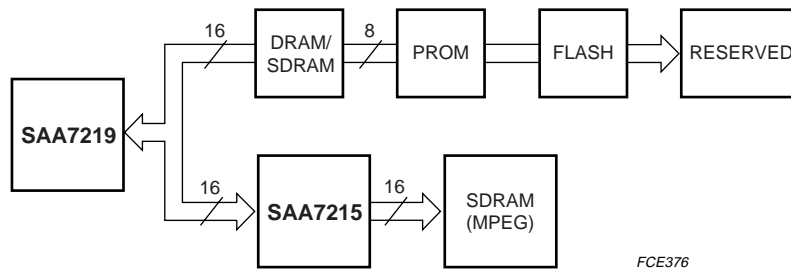
MPEG2 Transport RISC processor

SAA7219

6.1 Memory configurations

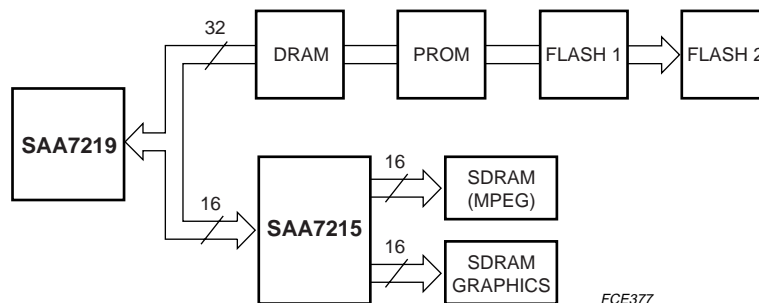
Table 2 Low-end and high-end memory configurations

CONFIGURATION	SDRAM	DRAM	PROM	FLASH PERIPHERALS
Low-end	1M × 16	256K × 16	512K × 8	–
High-end	up to 2 banks of 64 Mbits	up to 2 banks of 4 Mbytes	up to 4 Mbytes	2 to 7 banks of up to 4 Mbytes



FCE376

Fig.4 Typical low-end memory configuration.



FCE377

Fig.5 Typical high-end unified memory configuration.

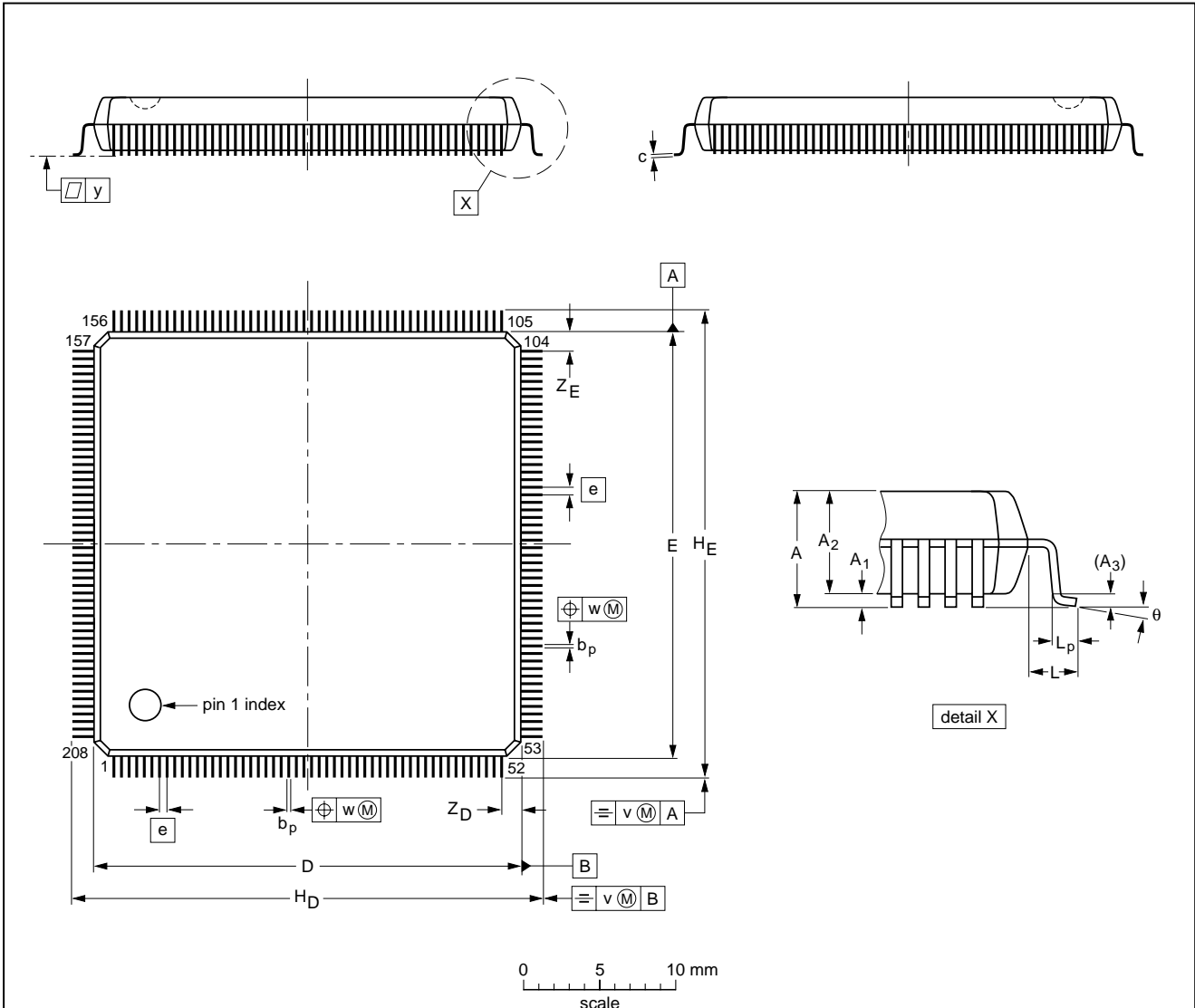
MPEG2 Transport RISC processor

SAA7219

7 PACKAGE OUTLINE

SQFP208: plastic shrink quad flat package;
208 leads (lead length 1.3 mm); body 28 x 28 x 3.4 mm; high stand-off height

SOT316-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _D	H _E	L	L _p	v	w	y	Z _D ⁽¹⁾	Z _E ⁽¹⁾	θ
mm	4.10	0.50 0.25	3.6 3.2	0.25	0.27 0.17	0.20 0.09	28.1 27.9	28.1 27.9	0.5	30.9 30.3	30.9 30.3	1.3	0.75 0.45	0.2	0.08	0.08	1.39 1.11	1.39 1.11	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT316-1		MS-029			99-12-27 00-01-25

MPEG2 Transport RISC processor

SAA7219

8 SOLDERING

8.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

8.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

8.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

8.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

MPEG2 Transport RISC processor

SAA7219

8.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW ⁽¹⁾
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable ⁽²⁾	suitable
PLCC ⁽³⁾ , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended ⁽³⁾⁽⁴⁾	suitable
SSOP, TSSOP, VSO	not recommended ⁽⁵⁾	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

MPEG2 Transport RISC processor

SAA7219

9 DATA SHEET STATUS

DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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Notes

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MPEG2 Transport RISC processor**SAA7219**

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MPEG2 Transport RISC processor

SAA7219

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SCA 72

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