NIPPON PRECISION CIRCUITS INC.

SM8223A/B

FSK Decoder and DTMF Receiver IC

OVERVIEW

The SM8223A/B is a FSK (Frequency shift keying) decoder and DTMF (Dual tone multi-frequency) receiver IC. It is fabricated using a CMOS process and features a power-down function for low power dissipation operation. The FSK decoder and DTMF receiver have the same performance characteristics as dedicated ICs that perform the same functions, with the added benefit of an FSK decoder/DTMF receiver auto-select function[1] using the telephone tip/ring input signal. It also features a ring (call signal) signal detection circuit, making for easy construction of low power dissipation, high-performance analog telephone-related applications.

FEATURES

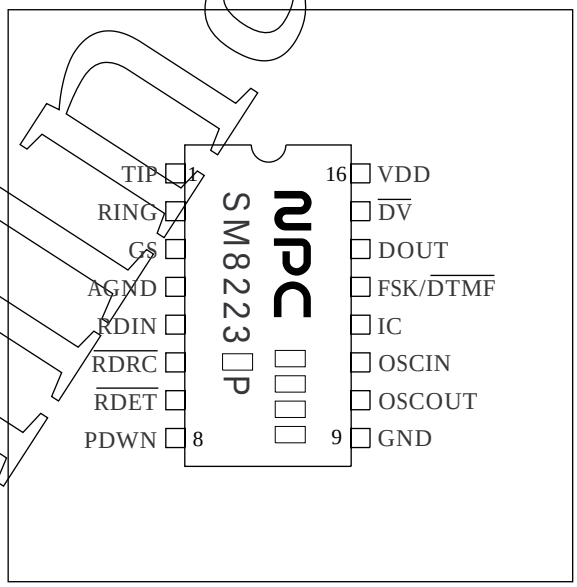
- Both FSK signal caller-ID information services and DTMF signal caller-ID information services supported
- FSK decoder/DTMF receiver auto-select function
- Ring (call signal) signal detection circuit built-in
- Serial I/O
- Input gain adjustment circuit built-in
- Power-down mode
- Single supply operation
  - SM8223A: 3.0V ± 10%
  - SM8223B: 5.0V ± 10%
- 3.579545MHz external crystal oscillator frequency
- Molybdenum-gate CMOS process

APPLICATIONS

- Telephones, fax machines and modems that support caller-ID information services
- Adapters for caller-ID information service functions
- Telephones, fax machines and modems that support remote operation functions

PINOUT

(Unit: mm)



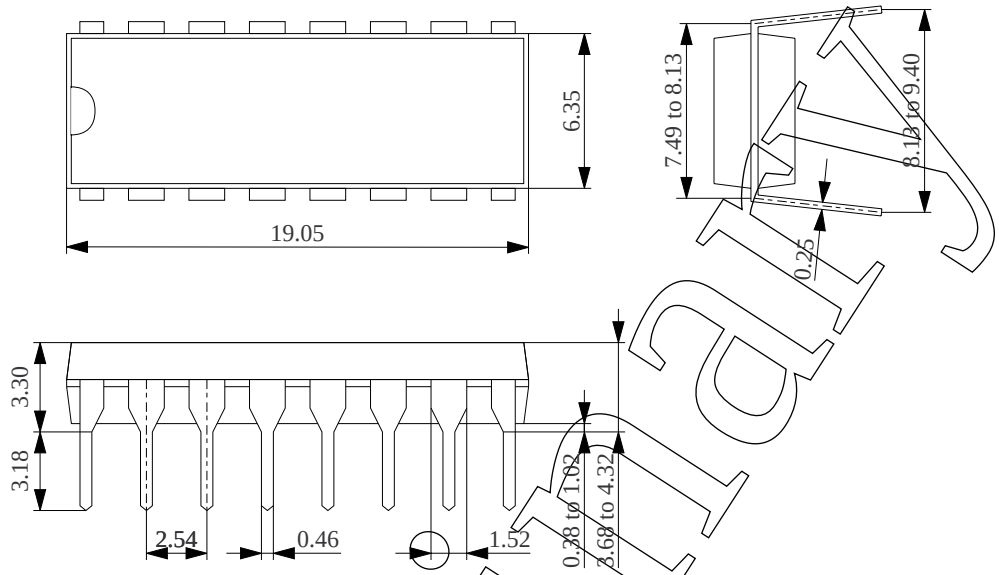
ORDERING INFORMATION

Device	Package
SM8223A/B	16-pin DIP

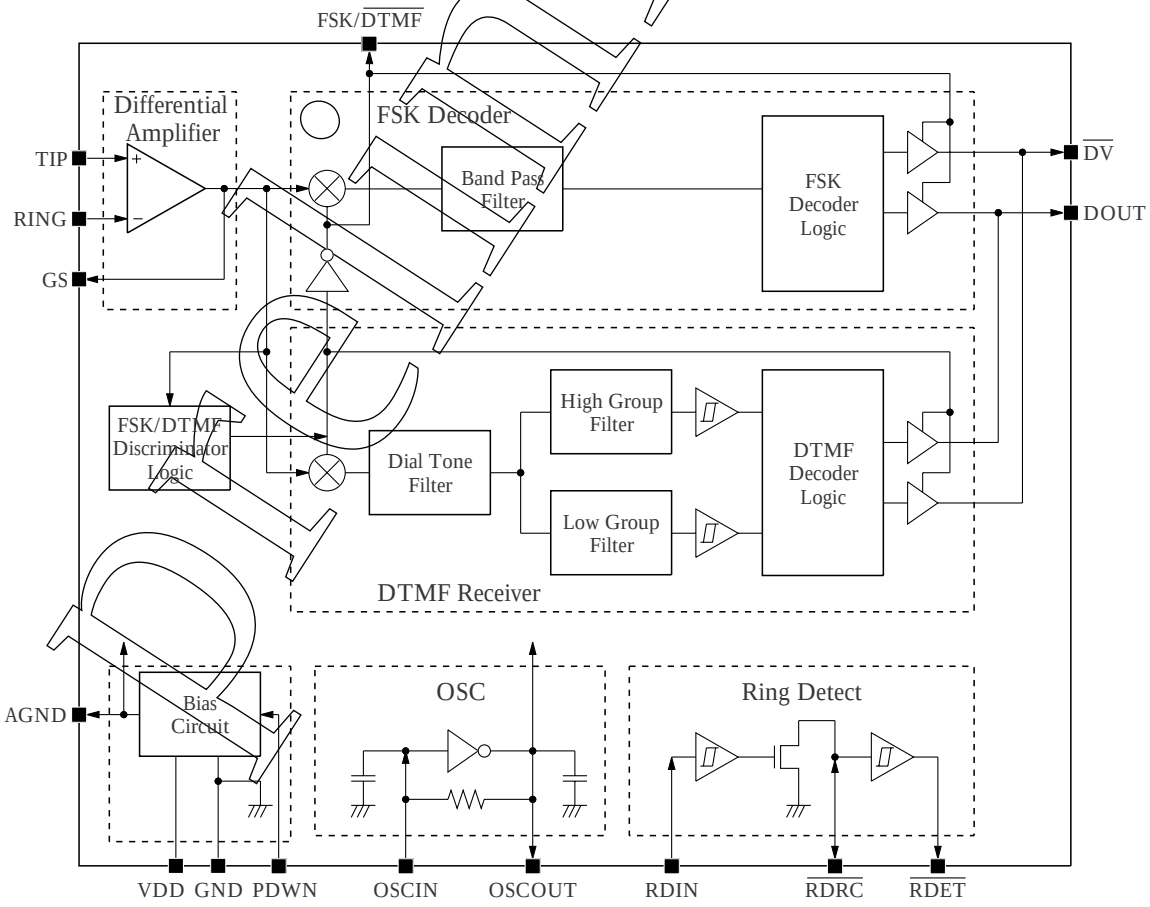
1. Auto-select function operates if the FSK signal conforms to the Bellcore GR-30-CORE standard.

PACKAGE DIMENSIONS

(Unit: mm)



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	I/O	Function
1	TIP	I	Tip input. Connected to the telephone line through a protection circuit
2	RING	I	Ring input. Connected to the telephone line through a protection circuit
3	GS	O	Input-stage amplifier gain-select output. Used to adjust the gain of the input-stage amplifier.
4	AGND	O	Analog ground output. Internal reference voltage (V_{DD}/2) output level
5	RDIN	I	Ring detector input. Used for line reversal and ring signal detection. Connected for ring detection of attenuated ring signals.
6	$\overline{\text{RDRC}}$	I/O	Ring detector RC terminal. Connected to an RC network which sets the ring detector delay time.
7	$\overline{\text{RDET}}$	O	Ring detector output. $\overline{\text{RDRC}}$-input Schmitt-trigger buffer output. LOW-level output when ring signal is detected.
8	PDWN	I	Power-down control input. LOW-level for normal operation, HIGH-level for power-down state. In the power-down state, pins AGND, OSCOUT, DOUT, and $\overline{\text{DV}}$ are HIGH.
9	GND	–	Ground. Connected to the system ground potential.
10	OSCOUT	O	Crystal oscillator output. The crystal oscillator element is connected between this pin and OSCIN.
11	OSCIN	I	Crystal oscillator input. The crystal oscillator element is connected between this pin and OSCOUT.
12	IC	I	Test input. Tied LOW for normal operation.
13	FSK/$\overline{\text{DTMF}}$	O	FSK/DTMF discriminator output. HIGH-level output when receiving FSK signal, and LOW-level output when receiving DTMF signal.
14	DOUT	O	Demodulator output. Demodulated FSK or DTMF signal output. HIGH-level output in power-down state.
15	$\overline{\text{DV}}$	O	Data trigger output. Data is output on DOUT when this pin goes LOW.
16	VDD	–	Supply

SPECIFICATIONS

Absolute Maximum Ratings

GND = 0V

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	–0.5 to 5.0	V
Input voltage range	V_{IN}	– 0.3 to V_{DD} + 0.3	V
Power dissipation	P_D	44	mW
Storage temperature range	T_{stg}	–40 to 125	°C

Recommended Operating Conditions

GND = 0V

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply voltage	V_{DD}		2.7	–	3.3	V
Clock frequency	f_{CLK}		–	3.579545	–	MHz
Clock frequency accuracy	Δf_C		–0.1	–	+0.1	%
Operating temperature	T_a		–40	–	85	°C

DC Electrical Characteristics

V_{DD} = 3.0V ± 0.3V, GND = 0V, f_{CLK} = 3.579545MHz, T_a = –20 to 85°C unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply current consumption	I_{DD}	OSCIN = 0V, PDWN = 0V, RDIN = 0V, $\overline{RDRC}$ = 0V, all other inputs open	–	–	4.5	mA
Power-down state current	I_{DPD}	OSCIN = 0V, PDWN = V_{DD}, RDIN = 0V, $\overline{RDRC}$ = 0V, all other inputs open	–	–	15	µA
PDWN LOW-level input voltage	V_{IL1}		–	–	$0.3V_{DD}$	V
PDWN, FSK/$\overline{DTMF}$ HIGH-level input voltage	V_{IH1}		$0.7V_{DD}$	–	–	V
RDIN, $\overline{RDRC}$ LOW-level input voltage	V_{IL2}		–	–	$0.3V_{DD}$	V
RDIN, $\overline{RDRC}$ HIGH-level input voltage	V_{IH2}		$0.7V_{DD}$	–	–	V
OSCIN LOW-level input voltage	V_{IL3}		–	–	TBD	V
OSCIN HIGH-level input voltage	V_{IH3}		TBD	–	–	V
DOUT, $\overline{DV}$, $\overline{RDET}$, FSK/$\overline{DTMF}$ LOW-level output current	I_{OL}		2	–	–	mA
DOUT, $\overline{DV}$, $\overline{RDET}$, FSK/$\overline{DTMF}$ HIGH-level output current	I_{OH}		–	–	–0.8	mA
OSCIN, PDWN, RDIN input leakage current	I_{IN}		–1	–	1	µA
$\overline{RDRC}$, FSK/$\overline{DTMF}$ output leakage current	I_{OFF}		–	–	1	µA

AC Electrical Characteristics

FSK decoder

V_{DD} = 3.0V ± 0.3V, GND = 0V, f_{CLK} = 3.579545MHz, T_a = –20 to 85°C unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Input sensitivity			–44	–48	–	dBm
Bandpass filter frequency response (gain relative to 1700Hz sine wave input)		60Hz	–	–80	–	dB
		1,200Hz	–	–1	–	
		2,200Hz	–	0	–	
		4,000Hz	–	–43	–	
		≥ 10,000Hz	–	–54	–	

DTMF receiver

V_{DD} = 3.0V ± 0.3V, GND = 0V, f_{CLK} = 3.579545MHz, T_a = –20 to 85°C unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Detection frequency deviation			±1.5% ± 2	–	–	Hz
Non-detection frequency deviation			3.5	–	–	%
Detection sensitivity			–32.0	–	4.0	dBm
Non-detection sensitivity			–	–	–40.0	dBm
Signal level error			–	–	8	dB
High-frequency rejection ratio			–	18	–	dB
Noise rejection ratio			–	12	–	dB
Dial tone rejection ratio			–	20	–	dB

Input-stage amplifier Characteristics

V_{DD} = 3.0V ± 0.3V, GND = 0V, f_{CLK} = 3.579545MHz, T_a = –20 to 85°C unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Input leakage current	I_{IN}		–	–	1	µA
Input resistance	R_{IN}		–	TBD	–	MΩ
DC open-loop voltage gain	A_{VOL}		TBD	–	–	dB
Unity gain frequency	f_C		TBD	–	–	MHz
Maximum load capacitance	C_L		–	–	TBD	pF
Maximum load resistance	R_L		50	–	–	kΩ

Timing Characteristics

Oscillator

V_{DD} = 3.0V ± 0.3V, GND = 0V, T_a = –20 to 85°C unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Clock HIGH-level pulsewidth	t_{WH}		110	–	–	ns
Clock LOW-level pulsewidth	t_{WL}		110	–	–	ns
Clock rise time	t_r		–	–	30	ns
Clock fall time	t_f		–	–	30	ns

FSK decoder

V_{DD} = 3.0V ± 0.3V, GND = 0V, f_{CLK} = 3.579545MHz, T_a = –20 to 85°C unless otherwise noted.

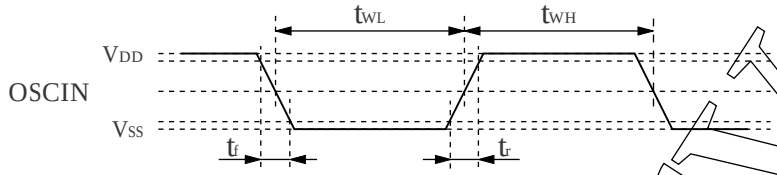
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Power-down release time	t_{DPD}		–	8	–	ms
Oscillator start-up time	t_{DOSC}		–	5	–	ms
Mark signal to $\overline{DV}$ ON time	t_{DED}	$\overline{DV}$ = LOW		–	3.75	ms
FSK flag setup time	t_{AF}		833 (1/1.2kHz)	–	–	ns
FSK flag hold time	t_{AH}		–	–	10	ns
Input to DOUT delay time	t_{ADD}		–	1	5	ms
DOUT rise time	t_{r0}		–	–	TBD	ns
DOUT fall time	t_{f0}		–	–	TBD	ns
Input to DOUT delay time	t_{IDD}		–	–	5	ms
DOUT data rate			1188	1200	1212	baud

DTMF receiver

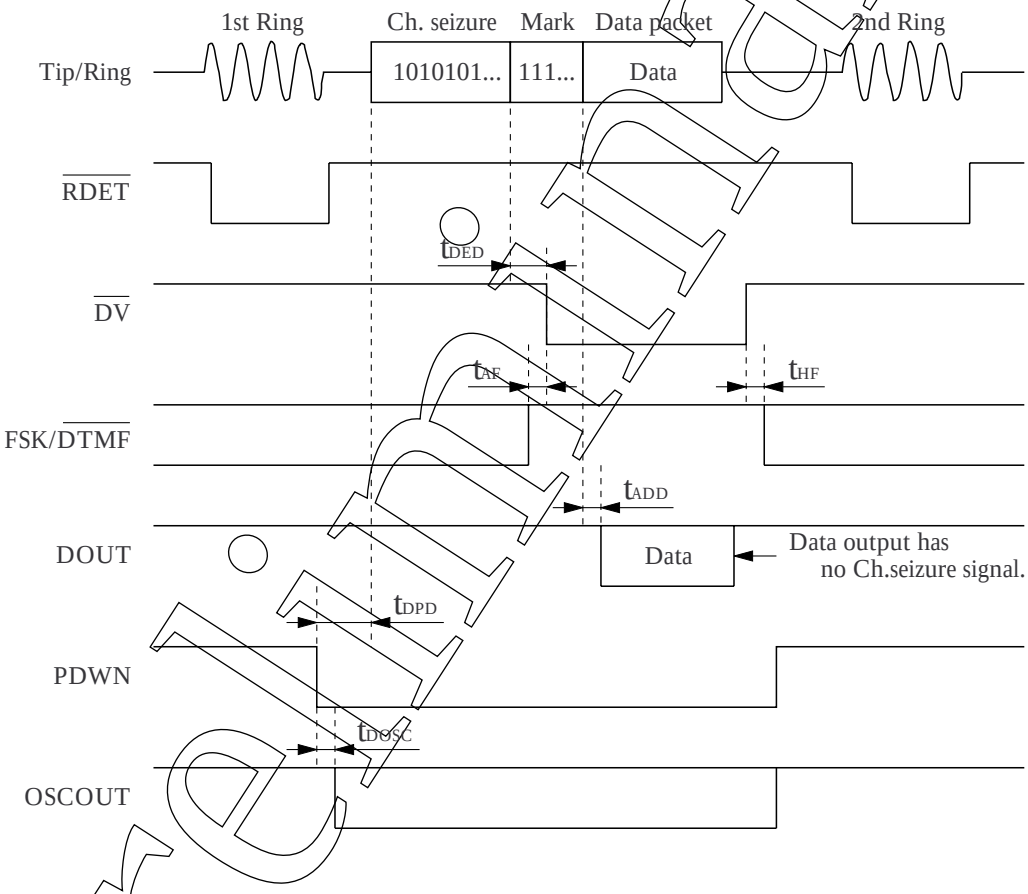
V_{DD} = 3.0V ± 0.3V, GND = 0V, f_{CLK} = 3.579545MHz, T_a = –20 to 85°C unless otherwise noted.

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
DOUT, $\overline{DV}$ rise time	t_{Dr0}	Q_0 to Q_3	–	–	TBD	ns
DOUT, $\overline{DV}$ fall time	t_{Df0}	Q_0 to Q_3	–	–	TBD	ns
Signal detection time	t_{RE}	$\overline{DV}$	–	35	40	ms
Received signal non-detection time	$t_{\overline{RE}}$	$\overline{DV}$	20	–	–	ms
Pause detection time	t_{PA}	$\overline{DV}$	20	–	–	ms
Pause non-detection time	t_{PR}	$\overline{DV}$	–	–	20	ms
$\overline{DV}$ output data delay time	t_{BDD}		–	–	5	ms
Power-down release time	t_{DPD}		–	8	–	ms
Oscillator start-up time	t_{DOSC}		–	5	–	ms
DOUT data rate			1188	1200	1212	baud
DTMF flag setup time	t_{AF}		833 (1/1.2kHz)	–	–	ns

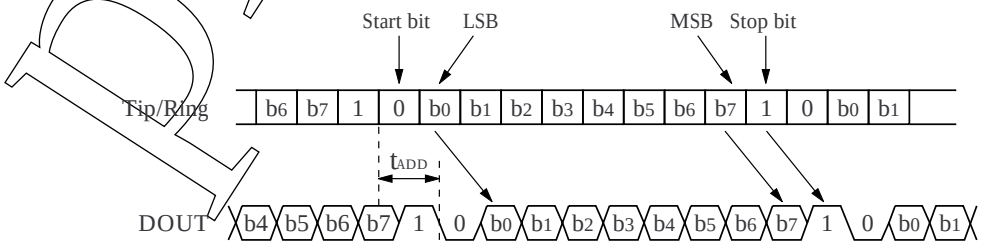
OSCIN input timing



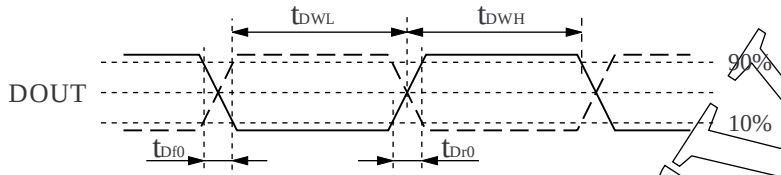
FSK receive timing (1)



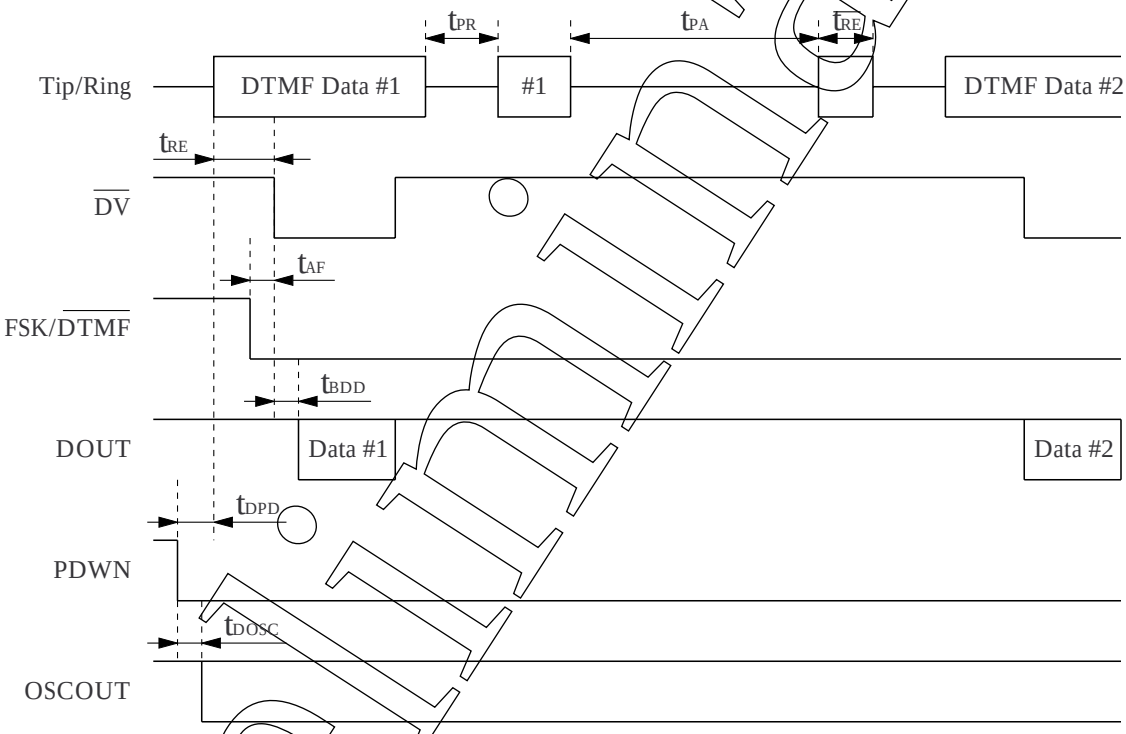
FSK receive timing (2)



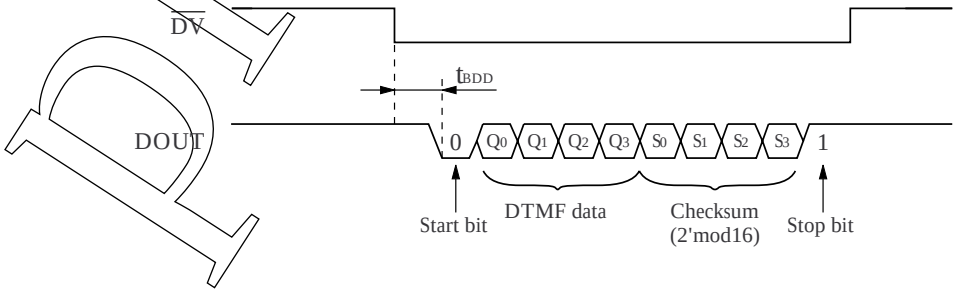
DOUT output timing



DTMF receive timing (1)



DTMF receive timing (2)



FUNCTIONAL DESCRIPTION

Ring Signal Detector

The telephone tip and ring signals pass through a protection circuit and are input to a resistor, capacitor and diode bridge network, shown in figure 1.

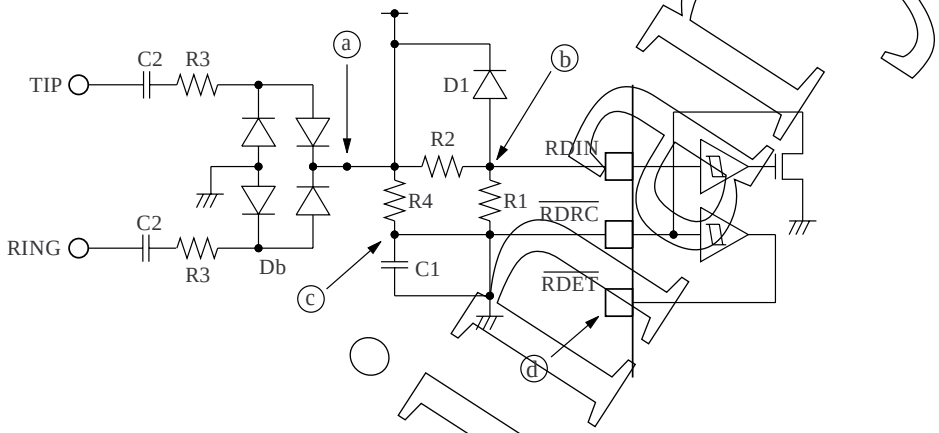


Figure 1. Ring signal detector circuit

The diode bridge full-wave rectified output signal (point a) is reduced in level by a resistor voltage divider comprising R_1 and R_2 (point b), and then input on RDIN. When the ring signal input on RDIN exceeds the Schmitt buffer trigger voltage ($0.7V_{DD}$), the output switches the open-drain $\overline{\text{RDRC}}$ pin. The signal at $\overline{\text{RDRC}}$ (point c) drives a time-constant circuit comprised by resistor R_4 and capacitor C_1 connected to the input of a second Schmitt buffer to generate the detector signal output on $\overline{\text{RDET}}$ (point d). Thus, $\overline{\text{RDET}}$ goes LOW when the ring or tip signal exceeds the level set by the resistor voltage divider.

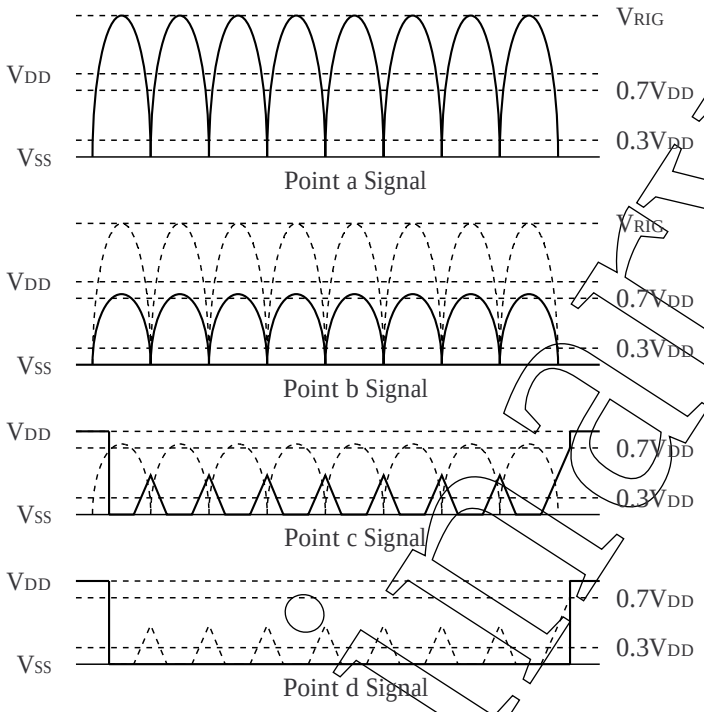


Figure 2. Ring signal detector circuit waveform transitions

The voltage divider level and RC time constant are given by the following equations, respectively.

$$0.7V_{DD} = \frac{R_1 + R_2 + R_3}{R_3} \cdot V_{RIG}$$

$$C_1 R_4 = \frac{t}{\ln\left(\frac{V_{DD}}{V_{DD} - V_T}\right)}$$

where t is the guard time, and the trigger level satisfies the expression $0.3V_{DD} \leq V_T \leq 0.7V_{DD}$.

Input Differential Amplifier

The SM8223A/B uses an input differential amplifier for input gain adjustment of the tip/ring signal input to the FSK detector or DTMF receiver. Differential input configuration and single-ended input configuration circuits are shown in figure 3. A bypass capacitor should be connected between GND and AGND in both circuit configurations.

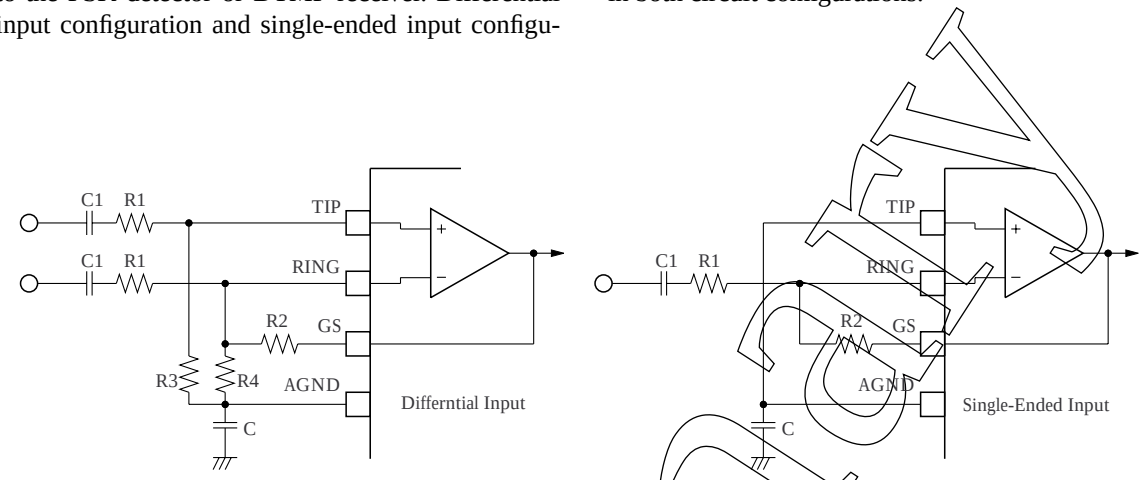


Figure 3. Input circuits

The gain for single-ended configurations is given by the following equation.

$$A_V = \frac{R_2}{R_1}$$

and the input impedance is given by the following equation.

$$Z_i = 2\sqrt{R_1^2 + \left(\frac{1}{\omega C_1}\right)^2}$$

The gain for differential configurations is given by the following equation,

$$A_V = \frac{R_2}{R_1} \text{ where } R_3 = \frac{R_2 R_4}{R_2 + R_4}$$

FSK/DTMF Auto-discriminator

The SM8223A/B examines the tip/ring input signal and determines the nature of the signal, FSK or DTMF, and invokes the corresponding circuits, FSK decoder or DTMF receiver, respectively. It determines whether the input signal is an FSK signal or DTMF signal by the presence or otherwise of the channel seizure information in the FSK signal header. This function automatically discriminates between the input signals if the FSK signal conforms to the Bellcore GR-30-CORE standard.

FSK Demodulator

When an FSK signal is received, the FSK/DTMF signal discriminator circuit sets the FSK/$\overline{\text{DTMF}}$ pin HIGH and connects the input signal to the FSK demodulator circuit. Demodulated data is output on DOUT with the format shown in figure 4. The FSK signal conforms to the following Bellcore standard.

Table 1. FSK signal

Parameter	Description
Modulation type	Continuous-phase binary frequency-shift keying
Logic "1" data (mark)	1200 ± 12 Hz
Logic "0" data (space)	2200 ± 22 Hz
Signal level (mark)	–32 to –12 dBm
Signal level (space)	–36 to –12 dBm
Data transfer rate	1200 ± 12 baud

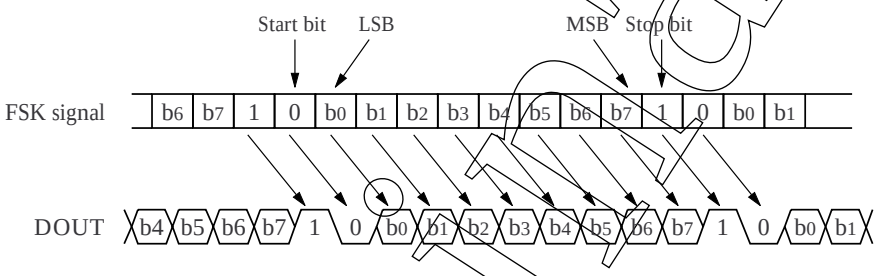


Figure 4. FSK signal to DOUT output

DTMF Demodulator

When a DTMF signal is received, the FSK/DTMF signal discriminator circuit sets the FSK/$\overline{\text{DTMF}}$ pin LOW and connects the input signal to the DTMF demodulator circuit. The DTMF signal is comprised by a high-group frequency and a low-group frequency which, in combination, represent a point in the DTMF matrix.

Table 2. DTMF matrix

Low group	High group			
	1209Hz	1336Hz	1477Hz	1633Hz
697Hz	1	2	3	A
770Hz	4	5	6	B
852Hz	7	8	9	C
941Hz	*	0	#	D

The DTMF receiver demodulates the received DTMF signal and outputs data bits Q_0 to Q_3 and a 4-bit (2-mod-16) checksum S_0 to S_3 in serial format on DOUT.

Table 3. DTMF signal output (DOUT)

Matrix input	DTMF				Checksum			
	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
	Q_0	Q_1	Q_2	Q_3	S_0	S_1	S_2	S_3
1	1	0	0	0	1	1	1	1
2	0	1	0	0	0	1	1	1
3	1	1	0	0	1	0	1	1
4	0	0	1	0	0	0	1	1
5	1	0	1	0	1	1	0	1
6	0	1	1	0	0	1	0	1
7	1	1	1	0	1	0	0	1
8	0	0	0	1	0	0	0	1
9	1	0	0	1	1	1	1	0
0	0	1	0	1	0	1	1	0
*	1	1	0	1	1	0	1	0
#	0	0	1	1	0	0	1	0
A	1	0	1	1	1	1	0	0
B	0	1	1	1	0	1	0	0
C	1	1	1	1	1	0	0	0
D	0	0	0	0	0	0	0	0

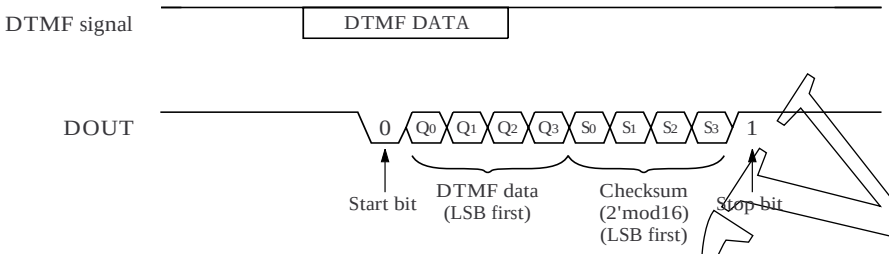
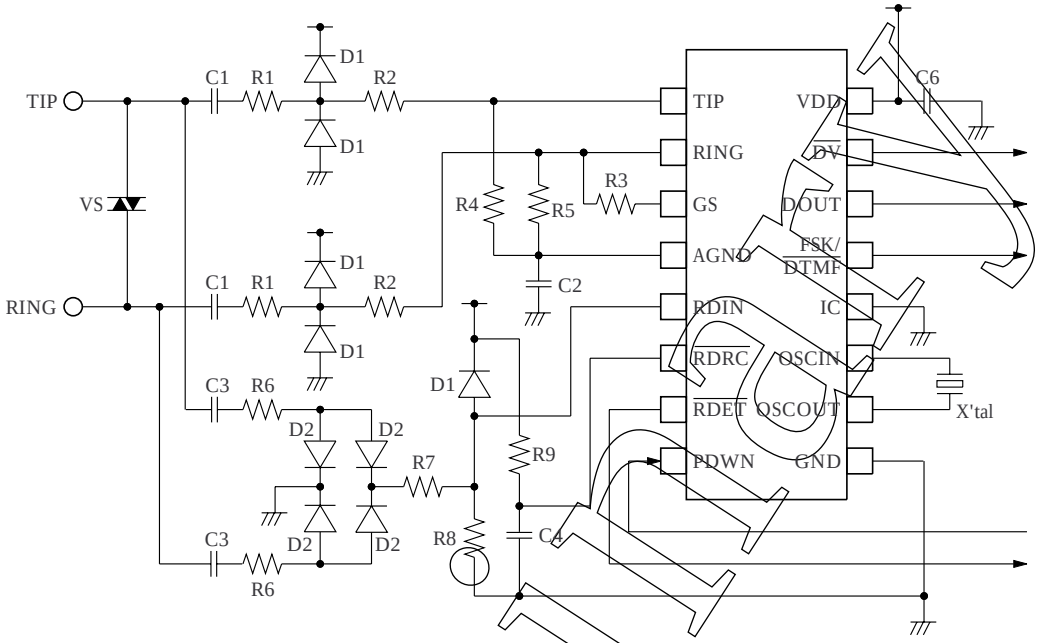


Figure 5. DTMF signal to DOUT output

The DTMF receiver determines whether the received data (DTMF signal) is valid after an interval of $t_{REC} \geq 36$ms stable reception. If valid, $\overline{DV}$ goes LOW and data is output on DOUT. If DTMF data is not detected after an interval $t_{SPA} \geq 20$ms, a data pause is activated and the next DTMF signal is in a wait state (see timing diagrams in AC Electrical Characteristics). The SM8223A/B DTMF receiver can be used as a general-purpose DTMF receiver without the need for the external time constant circuit, in which case the resistor/capacitor/diode network can be omitted.

TYPICAL APPLICATION CIRCUIT



Symbol	Rating	Unit
R_1	TBD	kΩ
R_2	TBD	kΩ
R_3	TBD	kΩ
R_4	TBD	kΩ
R_5	TBD	kΩ
C_1	TBD	µF
C_2	TBD	µF
R_6	TBD	kΩ
R_7	TBD	kΩ
R_8	TBD	kΩ
R_9	TBD	kΩ
C_3	TBD	µF
C_4	TBD	µF
D_2	TBD	–
R_{10}	TBD	kΩ
R_{11}	TBD	kΩ
C_5	TBD	µF
C_6	TBD	µF
D_1	TBD	–
VS	TBD	–
X'tal	3.579545	MHz

NPC
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NP9909AE 1999.09