PM5365

TEMAP

HIGH DENSITY VT/TU MAPPER AND M13 MULTIPLEXER

REGISTER DESCRIPTION

Proprietary and Confidential

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1 NORMAL MODE REGISTER DESCRIPTION

Normal mode registers are used to configure and monitor the operation of the TEMAP. Normal mode registers (as opposed to test mode registers) are selected when TRS (A[13]) is low.

Notes on Normal Mode Register Bits:

1) Writing values into unused register bits typically has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bit must be written with logic 0. Reading back unused bits can produce either a logic 1 or a logic 0; hence unused register bits should be masked off by software when read.

2) All configuration bits that can be written into can also be read back. This allows the processor controlling the TEMAP to determine the programming state of the block.

3) Writeable normal mode register bits are cleared to logic 0 upon reset unless otherwise noted.

4) Writing into read-only normal mode register bit locations does not affect TEMAP operation unless otherwise noted.

5) The TEMAP registers default to a DS3 M13 mux with T1 framers enabled. Default system side access is via the SBI bus without any tributaries enabled. The SONET/SDH blocks are by default in a reset state.

6) In the SONET/SDH register descriptions virtual tribtuaries, VT, and Tributary units, TU, are sometimes used interchangeably. Sometimes TU is only only mentioned but the intention is that the register applies to both TUs and the equivilent VTs.

7) Some configurations of the device will hold certain sections of the TEMAP in reset. For example when in T1 mode, the E1 specific blocks are held in reset and vice versa. The individual register descriptions indicate when certain registers are held in reset.

1.1 Top Level Master Registers

Register 0000H: Global Reset

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	RESET	0

RESET:

The RESET bit implements a software reset for the entire TEMAP. If the RESET bit is a logic 1, the entire TEMAP is held in reset. This bit is not self-clearing; therefore, a logic 0 must be written to bring the TEMAP out of reset. Holding the TEMAP in a reset state effectively puts it into a low power, stand-by mode. A hardware reset clears the RESET bit, thus deasserting the software reset.

Register 0001H: Global Configuration

Bit	Type	Function	Default
Bit 7	R/W	E1/T1B	0
Bit 6	R/W	LINEOPT1	0
Bit 5	R/W	LINEOPT0	0
Bit 4	R/W	SYSOPT2	0
Bit 3	R/W	SYSOPT1	1
Bit 2	R/W	SYSOPT0	0
Bit 1	R/W	OPMODE1	0
Bit 0	R/W	OPMODE0	0

OPMODE[1:0]:

Configures the master operating mode of the TEMAP. The three modes are Mapper/Multiplexer, Transmux or DS3 framer. In mapper/multiplexer mode, all the T1/E1 framer slices are configured to pass unframed data through to the system interface and the TEMAP becomes a SONET/SDH mapper or DS3 multiplexer only. For transmit performance monitoring in SBI mode, OPMODE[0:1] must be set to 01. In Transmux mode unframed T1 streams are passed between the SONET/SDH mapper and the DS3 multiplexer. In DS3 Framer only mode all the T1/E1 framers, the SONET/SDH mapper, the MX23, MX12 and DS2 blocks are disabled and the RDATO, RFPO/RMFPO, RGAPCLK/RSCLK, ROVRHD, TFPO/TMFPO, TFPI/TMFPI, TGAPCLK and TDATI I/O pins are enabled for serial clock and data mode. The following table shows the OPMODE values for each mode:

OPMODE[1:0]	Mode
00	Reserved
01	Mapper/Multiplexer mode
10	Transmux mode
11	DS3 Framer Only mode

Note that in DS3 Framer-only mode, RXMFPO and TXMFPI in Register 1002H must be programmed correctly.

Note that in Transmux mode, the SYSOPT[2:0] bits must be programmed to "010". Also note that the T1/E1 receive jitter attenuators must be used for each tributary. This can be selected by setting RJATBYP to logic 0 for all T1/E1 framers in Register 002H+80H*N: T1/E1 Receive Options.

SYSOPT:

The System Side Options bits, SYSOPT[2:0], configures the system side interface of the TEMAP. The possible system side interface selections are serial clock and data interfaces and Scaleable Bandwidth Interconnect bus interface. The following table shows the SYSOPT[2:0] values for each system side interface configuration:

SYSOPT[2:0]	System Interface Mode
000	Serial Clock and Data Interface
001	Reserved
010	SBI Interface
011	Reserved
1XX	Reserved

Note that in Transmux operating mode(OPMODE[1:0]="10"), the SYSOPT[2:0] bits must be programmed to "010".

LINEOPT[1:0]:

The Line Side Options bits, LINEOPT[1:0], select the line side multiplexing interface of the TEMAP. When the TEMAP is configured for high density T1/E1 framer mode or Mapper/Multiplexer mode the LINEOPT[1:0] bits select between a DS3 multiplexer, DS3 Mapper or T1/E1 mapper. When in DS3 Framer only mode LINEOPT[1:0] selects the DS3 LIU interface or DS3 Mapper. These bits must be left selecting the LIU interface when in Transmux mode. The following table shows the LINEOPT[1:0] values for each line side interface configuration:

LINEOPT[1:0]	Line Interface Mode
00	DS3 Mux with serial LIU interface
01	DS3 Mux with DS3 SONET/SDH Mapper
1X	T1/E1 Mapper

E1/T1B:

The E1/T1B pin configures the T1/E1 framer slices to be configured as either 28 T1 framers or 21 E1 framers. When E1/T1B is a logic 0 the T1/E1 framer slices are configured as 28 T1 framers. When E1/T1B is a logic the T1/E1 framer slices are configured as 21 E1 framers.

Register 0002H: Revision/Global PMON Update

Bit	Type	Function	Default
Bit 7	R	TYPE3	0
Bit 6	R	TYPE2	0
Bit 5	R	TYPE1	0
Bit 4	R	TYPE0	1
Bit 3	R	ID3	0
Bit 2	R	ID2	1
Bit 1	R	ID1	0
Bit 0	R	ID0	1

Writing to this register causes all performance monitoring to be updated simultaneously.

ID[3:0]:

The version identification bits ID[3:0], are set to a fixed value representing the version number of the TEMAP. These bits can be read by software to determine the version number.

TYPE[3:0]:

The type identification bits TYPE[3:0], identify this device from other products in the same Asynchronous Multiplexer family of devices.

Register 003H: Master Recovered Clock#1/Reference Clock Select

Bit	Type	Function	Default
Bit 7	R/W	REFCLK1	0
Bit 6	R/W	REFCLK0	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	RECV1SEL4	0
Bit 3	R/W	RECV1SEL3	0
Bit 2	R/W	RECV1SEL2	0
Bit 1	R/W	RECV1SEL1	0
Bit 0	R/W	RECV1SEL0	0

RECV1SEL[4:0]:

Select the source of the recovered clock which will be output on pin RECVCLK1. When this register is a logic 0 no registers are selected and the RECVCLK1 output will be held at logic 0. Values from 1 to 28 select the recovered clock from one of the 28 T1/E1 framers slices. When in E1 mode the T1/E1 framers slices from 22 through 28 will result in an invalid recovered clock.

Reserved:

This bit must be set to logic 0 for proper operation of the TEMAP.

REFCLK[1:0]:

The Reference clock select bits, REFCLK[1:0], select the source of the clock to be used as the transmit T1/E1 clock. The following table shows the REFCLK[1:0] selections:

REFCLK[1:0]	Clock
00	CTCLK pin
01	RECVCLK1 pin (generated internally)
10	RECVCLK2 pin (generated internally)
11	Unused

Register 0004H: Recovered Clock#2 Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	RECV2SEL4	0
Bit 3	R/W	RECV2SEL3	0
Bit 2	R/W	RECV2SEL2	0
Bit 1	R/W	RECV2SEL1	0
Bit 0	R/W	RECV2SEL0	0

RECV2SEL[4:0]:

Select the source of the recovered clock which will be output on pin RECVCLK2. When this register is a logic 0 no registers are selected and the RECVCLK2 output will be held at logic 0. Values from 1 to 28 select the recovered clock from one of the 28 T1/E1 framers slices. When in E1 mode the T1/E1 framers slices from 22 through 28 will result in an invalid recovered clock.

Register 0010H: Master Clock Monitor #1

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	RCLKA	X
Bit 5	R	TICLKA	X
Bit 4	R	CTCLKA	X
Bit 3	R	XCLKA	X
Bit 2	R	CLK52MA	X
Bit 1	R	LREFCLKA	X
Bit 0	R	SREFCLKA	X

When a monitored clock signal makes a low to high transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point all the bits in this register are cleared. A lack of transitions is indicated by the corresponding register bit reading low. This register should be read at periodic intervals to detect clock failures.

SREFCLKA:

The SREFCLK active, SREFCLKA, bit detects low to high transitions on the SREFCLK input. SREFCLKA is set high on a rising edge of SREFCLK, and is set low when this register is read.

LREFCLKA:

The LREFCLK active, LREFCLKA, bit detects low to high transitions on the LREFCLK input. LREFCLKA is set high on a rising edge of LREFCLK, and is set low when this register is read.

CLK52MA:

The CLK52M active, CLK52MA, bit detects low to high transitions on the CLK52M input. CLK52MA is set high on a rising edge of CLK52M, and is set low when this register is read.

XCLKA:

The XCLK active, XCLKA, bit detects for low to high transitions on the XCLK input. XCLKA is set high on a rising edge of XCLK, and is set low when this register is read.

CTCLKA:

The CTCLK active, CTCLKA, bit detects for low to high transitions on the CTCLK input. CTCLKA is set high on a rising edge of CTCLK, and is set low when this register is read.

TICLKA:

The TICLK active, TICLKA, bit detects for low to high transitions on the TICLK input. TICLKA is set high on a rising edge of TICLK, and is set low when this register is read.

RCLKA:

The RCLK active, RCLKA, bit detects for low to high transitions on the RCLK input. RCLKA is set high on a rising edge of RCLK, and is set low when this register is read.

Register 0011H: Master Clock Monitor #2

Bit	Type	Function	Default
Bit 7	R	ECLKA8	X
Bit 6	R	ECLKA7	X
Bit 5	R	ECLKA6	X
Bit 4	R	ECLKA5	X
Bit 3	R	ECLKA4	X
Bit 2	R	ECLKA3	X
Bit 1	R	ECLKA2	X
Bit 0	R	ECLKA1	X

When a monitored clock signal makes a low to high transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point all the bits in this register are cleared. A lack of transitions is indicated by the corresponding register bit reading low. This register should be read at periodic intervals to detect clock failures.

ECLKA[1:8]:

The ECLK[x] active, ECLKA[x], bit detects low to high transitions on the ECLK inputs when the egress interface is configured for Clock Slave mode. ECLKA[x] is set high on a rising edge of ECLK[x], and is set low when this register is read.

Register 0012H: Master Clock Monitor #3

Bit	Type	Function	Default
Bit 7	R	ECLKA16	X
Bit 6	R	ECLKA15	X
Bit 5	R	ECLKA14	X
Bit 4	R	ECLKA13	X
Bit 3	R	ECLKA12	X
Bit 2	R	ECLKA11	X
Bit 1	R	ECLKA10	X
Bit 0	R	ECLKA9	X

When a monitored clock signal makes a low to high transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point all the bits in this register are cleared. A lack of transitions is indicated by the corresponding register bit reading low. This register should be read at periodic intervals to detect clock failures.

ECLKA[9:16]:

The ECLK[x] active, ECLKA[x], bit detects low to high transitions on the ECLK inputs when the egress interface is configured for Clock Slave mode. ECLKA[x] is set high on a rising edge of ECLK[x], and is set low when this register is read.

Register 0013H: Master Clock Monitor #4

Bit	Type	Function	Default
Bit 7	R	ECLKA24	X
Bit 6	R	ECLKA23	X
Bit 5	R	ECLKA22	X
Bit 4	R	ECLKA21	X
Bit 3	R	ECLKA20	X
Bit 2	R	ECLKA19	X
Bit 1	R	ECLKA18	X
Bit 0	R	ECLKA17	X

When a monitored clock signal makes a low to high transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point all the bits in this register are cleared. A lack of transitions is indicated by the corresponding register bit reading low. This register should be read at periodic intervals to detect clock failures.

ECLKA[17:24]:

The ECLK[x] active, ECLKA[x], bit detects low to high transitions on the ECLK inputs when the egress interface is configured for Clock Slave mode. ECLKA[x] is set high on a rising edge of ECLK[x], and is set low when this register is read.

Register 0014H: Master Clock Monitor #5

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	ECLKA28	X
Bit 2	R	ECLKA27	X
Bit 1	R	ECLKA26	X
Bit 0	R	ECLKA25	X

When a monitored clock signal makes a low to high transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point all the bits in this register are cleared. A lack of transitions is indicated by the corresponding register bit reading low. This register should be read at periodic intervals to detect clock failures.

ECLKA[25:28]:

The ECLK[x] active, ECLKA[x], bit detects low to high transitions on the ECLK inputs when the egress interface is configured for Clock Slave mode. ECLKA[x] is set high on a rising edge of ECLK[x], and is set low when this register is read.

Register 0020H: Master Interrupt Source

Bit	Type	Function	Default
Bit 7	R	T1E1INT1	X
Bit 6	R	T1E1INT2	X
Bit 5	R	T1E1INT3	X
Bit 4	R	T1E1INT4	X
Bit 3	R	SDH/SBIINT	X
Bit 2	R	DS3INT	X
Bit 1	R	DS2INT	X
Bit 0	R	MX12INT	X

MX12INT:

If the MX12INT bit is a logic 1, at least one bit in the Master Interrupt Source MX12 Register is set.

DS2INT:

If the DS2INT bit is a logic 1, at least one bit in the Master Interrupt Source DS2 Register is set.

DS3INT:

If the DS3INT bit is a logic 1, at least one bit in the Master Interrupt Source DS3 Register is set.

SDH/SBIINT:

If the SDH/SBIINT bit is a logic 1, at least one bit in either of the Master Interrupt Source SDH or SBI Registers is set.

T1E1INT4:

If the T1E1INT4 bit is a logic 1, at least one bit in the Master Interrupt Source T1E1#25-28 Register is set, that is, at least one of the fourth group of four T1 framers numbered 25-28 is generating an interrupt.

T1E1INT3:

If the T1E1INT3 bit is a logic 1, at least one bit in the Master Interrupt Source T1E1#17-24 Register is set, that is, at least one of the third group of eight T1/E1 framers numbered 17-24 is generating an interrupt.

T1E1INT2:

If the T1E1INT2 bit is a logic 1, at least one bit in the Master Interrupt Source T1E1#9-16 Register is set, that is, at least one of the second group of eight T1/E1 framers numbered 9-16 is generating an interrupt.

T1E1INT1:

If the T1E1INT1 bit is a logic 1, at least one bit in the Master Interrupt Source T1E1#1-8 Register is set, that is, at least one of the first group of eight T1/E1 framers numbered 1-8 is generating an interrupt.

Register 0021H: Master Interrupt Source T1E1#1-8

Bit	Type	Function	Default
Bit 7	R	T1E1#8	X
Bit 6	R	T1E1#7	X
Bit 5	R	T1E1#6	X
Bit 4	R	T1E1#5	X
Bit 3	R	T1E1#4	X
Bit 2	R	T1E1#3	X
Bit 1	R	T1E1#2	X
Bit 0	R	T1E1#1	X

T1E1#[8:1]:

If the T1E1#[x] bit is a logic 1, an interrupt has been generated by T1/E1 framer slice x. To determine the T1/E1 block generating the interrupt and to clear the interrupt signal, read the T1/E1 Interrupt Source #1 and #2 registers for T1/E1 slice x.

Register 0022H: Master Interrupt Source T1E1#9-16

Bit	Type	Function	Default
Bit 7	R	T1E1#16	X
Bit 6	R	T1E1#15	X
Bit 5	R	T1E1#14	X
Bit 4	R	T1E1#13	X
Bit 3	R	T1E1#12	X
Bit 2	R	T1E1#11	X
Bit 1	R	T1E1#10	X
Bit 0	R	T1E1#9	X

T1E1#[16:9]:

If the T1E1#[x] bit is a logic 1, an interrupt has been generated by T1/E1 framer slice x. To determine the T1/E1 block generating the interrupt and to clear the interrupt signal, read the T1/E1 Interrupt Source #1 and #2 registers for T1/E1 slice x.

Register 0023H: Master Interrupt Source T1E1#17-24

Bit	Type	Function	Default
Bit 7	R	T1E1#24	X
Bit 6	R	T1E1#23	X
Bit 5	R	T1E1#22	X
Bit 4	R	T1E1#21	X
Bit 3	R	T1E1#20	X
Bit 2	R	T1E1#19	X
Bit 1	R	T1E1#18	X
Bit 0	R	T1E1#17	X

T1E1#[24:17]:

If the T1E1#[x] bit is a logic 1, an interrupt has been generated by T1/E1 framer slice x. To determine the T1/E1 block generating the interrupt and to clear the interrupt signal, read the T1/E1 Interrupt Source #1 and #2 registers for T1/E1 slice x.

Register 0024H: Master Interrupt Source T1E1#25-28

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	T1E1#28	X
Bit 2	R	T1E1#27	X
Bit 1	R	T1E1#26	X
Bit 0	R	T1E1#25	X

T1E1#[28:25]:

If the T1E1#[x] bit is a logic 1, an interrupt has been generated by T1/E1 framer slice x. To determine the T1/E1 block is generating the interrupt and to clear the interrupt signal, read the T1/E1 Interrupt Source #1 and #2 registers.

Register 0025H: Master Interrupt Source SDH

Bit	Type	Function	Default
Bit 7	R	Unused	X
Bit 6	R	Unused	X
Bit 5	R	LDPINT	X
Bit 4	R	D3MAINT	X
Bit 3	R	D3MDINT	X
Bit 2	R	EVTPPINT	X
Bit 1	R	IVTPPINT	X
Bit 0	R	RTOPINT	X

RTOPINT:

If the RTOPINT bit is a logic 1, an interrupt has been generated by the RTOP block. The RTOP Interrupt register must be read to clear this interrupt.

IVTPPINT:

If the IVTPPINT bit is a logic 1, an interrupt has been generated by the Ingress VTPP block. The Ingress VTPP Interrupt register must be read to clear this interrupt.

EVTPPINT:

If the EVTPPINT bit is a logic 1, an interrupt has been generated by the egress VTPP block. The egress VTPP Interrupt register must be read to clear this interrupt.

D3MDINT:

If the D3MDINT bit is a logic 1, the D3MD block is generating an interrupt. The D3MD Interrupt register must be read to clear this interrupt.

D3MAINT:

If the D3MAINT bit is a logic 1, the D3MA block is generating an interrupt. The D3MA Interrupt register must be read to clear this interrupt.

LDPINT:

If the LDPINT bit is a logic 1, an interrupt has been generated from a parity error on the Line DROP bus. This is an indication that there may be multiple

devices driving the Line DROP bus simultaneously. This interrupt is enabled with the LDPE bit in the SONET/SDH Master Ingress Configuration register. This Interrupt register will be cleared when read.

Register 0026H: Master Interrupt Source SBI

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	EXSBIINT	X
Bit 4	R	INSBIINT	X
Bit 3	R/W	SDET1E	0
Bit 2	R/W	SDET0E	0
Bit 1	R	SDET1INT	X
Bit 0	R	SDET0INT	X

SDET0INT:

If the SACT0INT bit is a logic 1, an interrupt has been generated by the SBIDET[0] signal high concurrently with this device driving the SBI DROP bus. This is an indication that there are multiple devices driving the SBI DROP bus simultaneously. The TEMAP will not output data when SBIDET[0] is asserted. The SBIDET0 Collision Detect register must be read to determine which tributary was in conflict. This Interrupt register will be cleared when read.

SDET1INT:

If the SDET1INT bit is a logic 1, an interrupt has been generated by the SBIDET[1] signal high concurrently with this device driving the SBI DROP bus. This is an indication that there are multiple devices driving the SBI DROP bus simultaneously. The TEMAP will not output data when SBIDET[1] is asserted. The SBIDET1 Collision Detect register must be read to determine which tributary was in conflict. This Interrupt register will be cleared when read.

SDET0E:

The SBI ADD activity detect interrupt enable bit, SDET0E, enables interrupts to be generated on INTB when the SBIDET[0] signal is asserted concurrently with this device driving the SBI DROP bus. When SDET0E is a logic 1, an interrupt will be generated when SBIDET[0] is active with this device driving the SBI DROP bus. When SBIDET[0] is a logic 0, errors are not generated due to SBIDET[0] concurrent with this device driving the SBI DROP bus.

SDET1E:

The SBI ADD activity detect interrupt enable bit, SDET1E, enables interrupts to be generated on INTB when the SBIDET[1] signal is asserted concurrently with this device driving the SBI DROP bus. When SDET1E is a logic 1, an interrupt will be generated when SBIDET[1] is active with this device driving the SBI DROP bus. When SBIDET[1] is a logic 0, errors are not generated due to SBIDET[1] concurrent with this device driving the SBI DROP bus.

INSBIINT:

If the INSBIINT bit is a logic 1, the INSBI block is generating an interrupt due to a FIFO underrun or overrun. The INSBI Interrupt register must be read to clear this interrupt.

EXSBIINT:

If the EXSBIINT bit is a logic 1, the EXSBI block is generating an interrupt due to a FIFO underrun or overrun. The EXSBI Interrupt register must be read to clear this interrupt.

Register 0028H: Master Interrupt Source DS3

Bit	Type	Function	Default
Bit 7	R	DS3PMON	X
Bit 6	R	DS3RDLC	X
Bit 5	R	DS3RBOC	X
Bit 4	R	DS3FRMR	X
Bit 3	R	DS3TDPR	X
Bit 2	R	DS3XBOC	X
Bit 1	R	MX23	X
Bit 0	R	DS3PRGD	X

DS3PRGD:

If the DS3PRGD bit is a logic 1, the PRGD (Pseudo Random Generator/Receiver) connecting to the DS3 framer is generating an interrupt. Register 1031H must be read to determine the source of the interrupt and to clear this interrupt signal.

MX23:

If the MX23 bit is a logic 1, the MX23 block is generating an interrupt due to the detection of a DS2 loopback request. The MX23 Loopback Request Interrupt register at address 1046H must be read to clear this interrupt.

DS3XBOC:

If the DS3XBOC bit is a logic 1, the DS3 XBOC block is generating an interrupt.

DS3TDPR:

If the DS3TDPR bit is a logic 1, the DS3 TDPR block is generating an interrupt. The DS3 TDPR Interrupt Status register at address 1024H must be read to determine which event in DS3 TDPR has caused the interrupt.

DS3FRMR:

If the DS3FRMR bit is a logic 1, the DS3 FRMR block is generating an interrupt. The DS3 FRMR Interrupt status register at address 100EH must be read to determine which event in DS3 FRMR has caused the interrupt.

DS3RBOC:

If the DS3RBOC bit is a logic 1, the DS3 RBOC block is generating an interrupt. The DS3 RBOC Interrupt Status register at address 104BH must be read to determine which event in DS3 RBOC has caused the interrupt.

DS3RDLC:

If the DS3RDLC bit is a logic 1, the DS3 RDLC block is generating an interrupt. The DS3 RDLC Status register at address 102AH must be read to determine which event in DS3 RDLC has caused the interrupt.

DS3PMON:

If the DS3PMON bit is a logic 1, the DS3 PMON block is generating an interrupt. The DS3 PMON Interrupt Status register at address 1011H must be read to determine which event in DS3 PMON has caused the interrupt.

Register 0029H: Master Interrupt Source DS2

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	DS2 FRMR#7	X
Bit 5	R	DS2 FRMR#6	X
Bit 4	R	DS2 FRMR#5	X
Bit 3	R	DS2 FRMR#4	X
Bit 2	R	DS2 FRMR#3	X
Bit 1	R	DS2 FRMR#2	X
Bit 0	R	DS2 FRMR#1	X

DS2 FRMR#[7:1]:

Any DS2 FRMR#[7:1] bits which are a logic 1 indicate which of the seven DS2 Framers is generating an interrupt on the INTB output pin. The appropriate DS2 FRMR Interrupt Status register must be read to clear the interrupt.

Register 002AH: Master Interrupt Source MX12

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	MX12#7	X
Bit 5	R	MX12#6	X
Bit 4	R	MX12#5	X
Bit 3	R	MX12#4	X
Bit 2	R	MX12#3	X
Bit 1	R	MX12#2	X
Bit 0	R	MX12#1	X

MX12#[7:1]:

Any MX12#[7:1] bits which are a logic 1 indicate a MX12 block that is generating an interrupt on the INTB output pin due to the detection of a DS1 loopback request. The appropriate MX12 Loopback Interrupt register must be read to clear the interrupt.

Register 002CH: Master SBIDET0 Collision Detect LSB

Bit	Type	Function	Default
Bit 7	R	COL7	0
Bit 6	R	COL6	0
Bit 5	R	COL5	0
Bit 4	R	COL4	0
Bit 3	R	COL3	0
Bit 2	R	COL2	0
Bit 1	R	COL1	0
Bit 0	R	COL0	0

Register 002DH: Master SBIDET0 Collision Detect MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	COL8	0

COL[8:0]:

The SBIDET[0] Collision Detection identifier, COL[8:0], identifies the SBI column number of the last collision as indicated by the SDET0INT interrupt. The tributary experiencing contention is calculated from COL[8:0] as follows:
SPE# or DS3# = MOD(COL[8:0]-1,3)+1
T1# or TVT1.5# = SPE#, MOD(TRUNC((COL[8:0]-10)/3-1),28)+1
E1# or TVT2# = SPE#, MOD(TRUNC((COL[8:0]-10)/3-1),21)+1

Register 002EH: Master SBIDET1 Collision Detect LSB

Bit	Type	Function	Default
Bit 7	R	COL7	0
Bit 6	R	COL6	0
Bit 5	R	COL5	0
Bit 4	R	COL4	0
Bit 3	R	COL3	0
Bit 2	R	COL2	0
Bit 1	R	COL1	0
Bit 0	R	COL0	0

Register 002FH: Master SBIDET1 Collision Detect MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	COL8	0

COL[8:0]:

The SBIDET[1] Collision Detection identifier, COL[8:0], identifies the SBI column number of the last collision as indicated by the SDET1INT interrupt. The tributary experiencing contention is calculated from COL[8:0] as follows:
SPE# or DS3# = MOD(COL[8:0]-1,3)+1
T1# or TVT1.5# = SPE#, MOD(TRUNC((COL[8:0]-10)/3-1),28)+1
E1# or TVT2# = SPE#, MOD(TRUNC((COL[8:0]-10)/3-1),21)+1

1.2 T1/E1 Master Configuration Registers (N=1 to 28)

Register 0000H+80H*N: T1/E1 Master Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	PMONRST	0
Bit 4	R/W	TXPMON	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	RESET	0

RESET:

The RESET bit allows software to hold each T1/E1 framer slice in a reset condition. When RESET is a logic 1 the entire T1/E1 slice will be held in a reset state which is also a low power state. This will force all registers to their default state. While in reset the clocks can not be guaranteed accurate or existing. When RESET is a logic 0 the T1/E1 framer slice is in normal operating mode.

When the TEMAP DS3 mux is configured in G.747 mode every forth T1/E1 framer must be held in reset, ie. N=4,8,12,16,20,24,28 in the address calculation for this register.

Reserved:

This bit must be set to logic 0 for proper operation of the TEMAP.

TXPMON:

When in Mapper/Multiplexer mode this bit selects performance monitoring for the transmit path. When TXPMON is a logic 1 performance monitoring is performed on the egress tributary. When TXPMON is a logic 0 performance monitoring is performed on the ingress tributary. In Transmux mode TXPMON set to 1 selects the mapper transmit stream for performance monitoring and TXPMON set to 0 selects the DS3 transmit stream for performance monitoring. The LINEOPT[1:0] bits in the Global Configuration register must be set to “00” when in transmux mode for TXPMON to be active.

TXPMON can be used in High Density Framer mode with clear channel system interfaces enabled by the RCVCLRCH bit in the T1/E1 Receive Options register set to logic 1. TXPMON must be set to logic 0 when RCVCLRCH is logic 0 in High Density Framer mode.

PMONRST:

The performance monitor reset bit, PMONRST, forces the PMON block into reset. When PMONRST is a logic 1 the PMON block will be held in a reset state. When PMONRST is a logic 0 the PMON block is in normal operating mode.

Register 0002H+80H*N: T1/E1 Receive Options

Bit	Type	Function	Default
Bit 7	R/W	RJATBYP	1
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Unused	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	WORDERR	0
Bit 1	R/W	CNTNFAS	0
Bit 0	R/W	CCOFA	0

This register allows software to configure the receive functions of each framer.

CCOFA

The CCOFA bit determines whether the PMON counts Change-Of-Frame Alignment (COFA) events or out-of-frame (OOF) events. When CCOFA is set to logic 1, COFA events are counted by PMON. When CCOFA is set to logic 0, OOF events are counted by PMON. The CCOFA bit is only valid in T1 mode.

CNTNFAS:

In E1 mode, when the CNTNFAS bit is a logic 1, a zero in bit 2 of time slot 0 of non-frame alignment signal (NFAS) frames results in an increment of the framing error count. If WORDERR is also a logic 1, the word is defined as the eight bits consisting of the seven-bit FAS pattern and bit 2 of time slot 0 of the next NFAS frame. When the CNTNFAS bit is a logic 0, only errors in the FAS affect the framing error count.

WORDERR:

In E1 mode, the WORDERR bit determines how frame alignment signal (FAS) errors are reported. When WORDERR is logic 1, one or more errors in the seven bit FAS word results in a single framing error count. When WORDERR is logic 0, each error in a FAS word results in a single framing error count.

Reserved:

This bit must be set to logic 0 for proper operation of the TEMAP.

RJATBYP:

The RJATBYP bit disables jitter attenuation in the receive direction. When receive jitter attenuation is not being used, setting RJATBYP to logic 1 will reduce the latency through the receiver section by typically 40 bits.
The receive jitter attenuator must not be bypassed when receiving T1 tributaries via the DS3 multiplexer.

Register 0003H+80H*N: T1/E1 Alarm Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	TAISEN	0
Bit 2		Unused	X
Bit 1	R/W	Reserved	0
Bit 0	R/W	EALMEN	0

Reserved:

This bit must be set to logic 0 for proper operation of the TEMAP.

TAISEN:

The TAISEN bit enables generation of an all ones AIS alarm in the egress tributary. When TAISEN is a logic 1 the egress data stream is forced to all ones. When TAISEN is a logic 0 the egress tributary operates normally. Note that the diagnostic loopback point is downstream of this AIS insertion point (i.e. AIS will be looped back to the receive side when diagnostic loopback is enabled).

Reserved:

This bit must be set to logic 0 for proper operation of the TEMAP.

EALMEN:

The EALMEN bit enables an egress SBI alarm indication signal to force the transmit data stream into an all ones AIS. When EALMEN is a logic 1 and the SBI bus is selected, an alarm indication from the SBI bus will force the transmit data to the VT/TU mapper and DS3 M13 multiplexer to all ones. When EALMEN is a logic 0, an SBI alarm indication will not affect the transmit data stream.

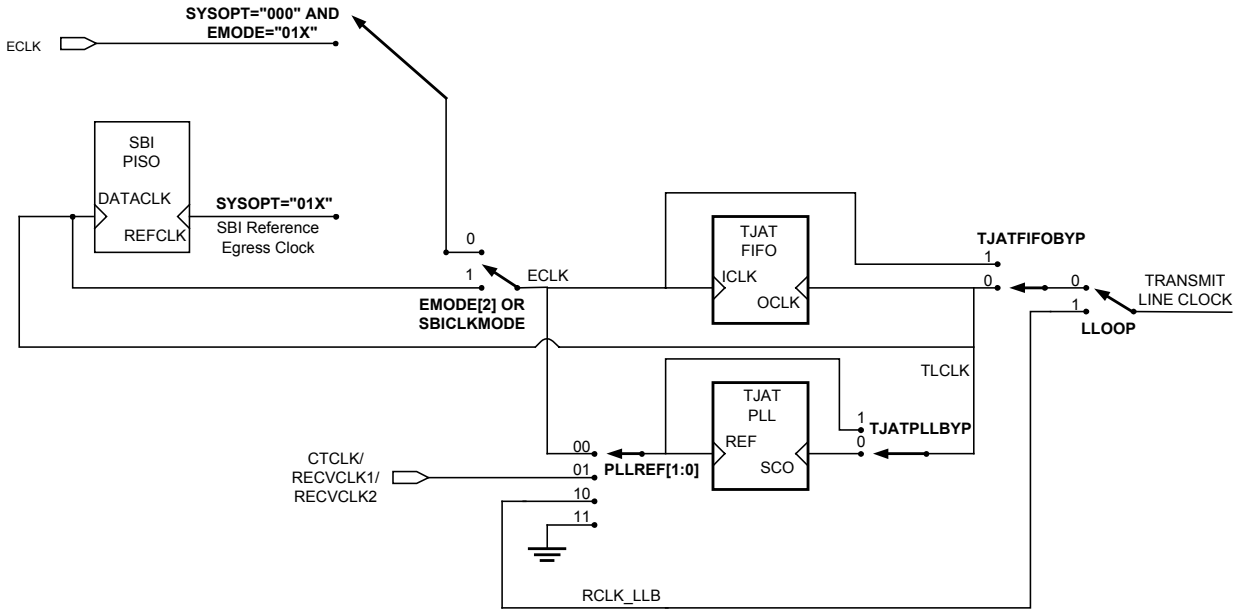
The diagnostic loopback point is upstream of this AIS insertion point.

Register 0004H+80H*N: T1/E1 Egress Line Interface Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	1
Bit 5	R/W	SBICLKMODE	0
Bit 4		Unused	X
Bit 3	R/W	TJATFIFOBYP	0
Bit 2	R/W	TJATPLLBYP	0
Bit 1	R/W	PLLREF1	0
Bit 0	R/W	PLLREF0	0

Figure 1 shows how the transmit jitter attenuator can be configured to be in or out of the transmit path. TXCLK is the TEMAP internal clock that is used for egress timing in Master clock modes and is the data clock to the DS3 M13 mux and SONET/SDH mapper. RCLK is the recovered clock.

Figure 1 – Transmit Timing Options Diagram



PLLREF[1:0]:

The TJAT PLL reference select bits, PLLREF[1:0], select the source of the clock going into the TJAT digital PLL. The PLLREF[1:0] bits are also used to select between the transmit reference clocks and the receive clock, RCLK, in Master mode. **Care must be taken to prevent PLLREF[1:0] from being set to "00" or "11" when EMODE[2:0] selects the master mode configuration.** If EMODE is in master timing mode and PLLREF is set to "00" or "11" a timing loop will be formed and the clock will become unstable. The following table shows the settings for PLLREF[1:0]:

PLLREF[1:0]	Selection
00	Slave clock – do not use with EMODE set to clock Master mode
01	External Transmit reference
10	Recovered Receive clock
11	Reserved

TJATPLLBYP:

The TJATPLLBYP bit disables transmit transmit clock jitter attenuation. Transmit jitter attenuation may be unnecessary when the T1/E1 framer slice is configured for egress Clock Master modes and the reference clock is a line rate clock or when configured for Clock Slave: Clear Channel mode. Jitter attenuation must be used when additional jitter attenuation is required on the external transmit reference clock or when in clock slave mode and the slave clock is not at the line rate or it needs jitter attenuation.

TJATFIFOBYP:

The TJAT fifo bypass bit, TJATFIFOBYP, is used to remove the transmit jitter attenuator FIFO from the transmit data path. When transmit jitter attenuation is not being used as selected by the TJATPLLBYP register bit, setting TJATFIFOBYP to logic 1 will reduce the latency through the transmitter section by typically 40 bits.

SBICLKMODE:

The SBI clock Mode bit, SBICLKMODE, selects the egress clocking mode used over the SBI bus. When SBICLKMODE is a logic 1 and the system interface is configured for the SBI interface, egress tributary clocking is set for Master mode. In this mode the TEMAP T1/E1 transmit clock is used to control the SBI tributary rate for this T1/E1. The CLK_MSTR bit in the

corresponding EXSBI register must also be set to Master mode for correct operation. When SBICLKMODE is a logic 0 and the system interface is configured for the SBI bus, the egress T1/E1 clock is slaved to the T1/E1 rate from the tributary on the SBI bus. The CLK_MSTR bit in the corresponding EXSBI register must also be set to Slave mode for correct operation. When the SBI bus is operating in Synchronous mode as selected by the SYNCSBI bit in the SBI Master Configuration register, this bit must be set to 0 corresponding to slave mode.

SBICLKMODE affects the transmit timing options as shown in Figure 1. When the SBI Add bus is set to master mode, SBICLKMODE is 1, the switch labeled EMODE[2] is in the “1” switch position.

The SBICLKMODE bit must be set before the tributaries within the SBI are enabled.

Reserved:

Bit 7 must be set to logic 0 and bit 6 must be set to logic 1 for proper operation of the TEMAP.

Register 0005H+80H*N: T1/E1 Ingress Serial Interface Mode Select

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	IMODE1	0
Bit 0	R/W	IMODE0	0

IMODE:

The ingress clock mode bits, IMODE[1:0], determine which serial interface mode is being used for this tributary. These bits must be programmed to “11” for proper operation of the TEMAP, selecting the Clock Master: Clear Channel mode.

Table 1 - Ingress Serial Interface Mode Selection

IMODE[1]	IMODE[0]	Operation
0	0	Reserved
0	1	Reserved
1	0	Reserved
1	1	Clock Master: Clear Channel

Reserved:

This bit must be set to logic 0 for proper operation of the TEMAP.

Register 0006H+80H*N: T1/E1 Egress Serial Interface Mode Select

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	EMODE2	0
Bit 1	R/W	EMODE1	0
Bit 0	R/W	EMODE0	0

EMODE:

The egress clock mode, EMODE, bit determines which serial interface mode is being used for this tributary.

The modes are listed in the following table:

Table 2 - Egress Serial Interface Mode Selection

EMODE[2]	EMODE[1]	EMODE[0]	Operation
X	X	1	Reserved
X	0	0	Reserved
0	1	0	Clock Slave: Clear Channel
1	1	0	Clock Master: Clear Channel

Reserved:

This bit must be set to logic 0 for proper operation of the TEMAP.

Register 0009H+80H*N: T1/E1 Serial Interface Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	IDE	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	EDE	1
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

This register only affects the serial clock and data interface signals when enabled as the system interface via the SYSOPT[2:0] bits in the Global Configuration register.

Reserved:

This bit must be set to logic 0 for proper operation of the TEMAP.

EDE:

When EDE is set to logic 1, the ED[x] signal is sampled by the rising ECLK[x] edge. When EDE is set to logic 0, the ED[x] signal is sampled by the falling ECLK[x] edge.

IDE:

When IDE is set to logic 1, the ID[x] signal is updated on the rising edge of ICLK[x]. When IDE is set to logic 0, the ID[x] signal is updated on the falling edge of ICLK[x].

Register 000BH+80H*N: T1/E1 Interrupt Source #1

Bit	Type	Function	Default
Bit 7	R	RJAT	0
Bit 6	R	TJAT	0
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	T1E1FRMR	0
Bit 0	R	PMON	0

This register allows software to determine the block which produced the interrupt on the INTB output pin.

Reading this register does not remove the interrupt indication; the corresponding block's interrupt status register must be read to remove the interrupt indication.

Register 000CH+80H*N: T1/E1 Interrupt Source #2

Bit	Type	Function	Default
Bit 7	R	Reserved	X
Bit 6	R	PRBS	0
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	ALMI	0
Bit 1		Unused	X
Bit 0	R	Reserved	X

This register allows software to determine the block that produced the interrupt on the INTB output pin.

Reading this register does not remove the interrupt indication; the corresponding block's interrupt status register must be read to remove the interrupt indication.

Register 000DH+80H*N: T1/E1 Diagnostics

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	LLOOP	0
Bit 3	R/W	RAIS	0
Bit 2	R/W	DLOOP	0
Bit 1	R/W	Reserved	0
Bit 0		Unused	X

Reserved:

This bit must be set to logic 0 for proper operation of the TEMAP.

DLOOP:

The DLOOP bit selects the digital diagnostic loopback mode, where the TEMAP is configured to internally direct the output of the TJAT to the input of the RJAT. When DLOOP is set to logic 1, the digital diagnostic loopback mode is enabled. When DLOOP is set to logic 0, the digital diagnostic loopback mode is disabled. The RJATBYP or TJATBYP register bits can be used to bypass the ingress and egress jitter attenuators to decrease delay.

RAIS:

When a logic 1, the RAIS bit forces all ones into the ingress data stream. The ingress data stream will freeze at the current valid signaling.

LLOOP:

The LLOOP bit selects the line loopback mode, where the recovered data are internally directed downstream of the FIFO of the transmit jitter attenuator. When LLOOP is set to logic 1, the line loopback mode is enabled. When LLOOP is set to logic 0, the line loopback mode is disabled.

Reserved:

This bit must be set to logic 0 for proper operation of the TEMAP.

Register 000EH+80H*N: T1/E1 PRBS Positioning and Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	RXPATGEN	0
Bit 1	R/W	UNF_GEN	0
Bit 0	R/W	UNF_DET	0

This register modifies the way in which the PRBS generator/checker is used.

UNF_DET

When the Unframed Pattern Detection bit, UNF_DET, is set to logic 1, the PRBS Checker will search for the pattern in all 193 bits/256 bits of the transmit or receive stream, depending on the setting of RXPATGEN. This bit must be set to logic 1 for proper detection of PRBS sequences.

UNF_GEN

When the Unframed Pattern Generation bit, UNF_GEN, is set to logic 1, the PRBS Generator will overwrite all 193 bits/256 bits in every frame in the direction specified by the RXPATGEN bit. . This bit must be set to logic 1 for proper generation of PRBS sequences.

RXPATGEN:

The Receive Pattern Generate, RXPATGEN, bit controls the location of the PRBS generator/detector. When RXPATGEN is set to logic 1, the PRBS generator is inserted in the ingress receive path and the PRBS checker is inserted in the egress transmit path. Payload from the receive line may be overwritten with generated PRBS patterns before appearing on the receive system interface, and timeslots from the transmit system interface may be checked for the generated pattern before appearing on the transmit line. Note that this mode requires an appropriate receive line clock (RCLK when in DS3 LIU mode or LREFCLK when in DS3/T1/E1 mapper mode) for proper insertion of the PRBS sequence. Alternatively, the PRBS generator can clocked by the T1/E1 transmit clock when DLOOP is set to logic 1 in Register

00DH +80H*N - T1/E1 Diagnostics. When inserting framed PRBS from the receiver per channel serial controller, the tributary needs to be in frame.

When RXPATGEN is set to logic 0, the PRBS detector is inserted in the ingress receive path and the PRBS generator is inserted in the egress transmit path. Payload from the transmit system interface may be overwritten with generated PRBS patterns before appearing on the transmit line, and timeslots from the receive line may be checked for the generated pattern before appearing on the receive system interface.

Reserved:

This bit must be set to logic 0 for proper operation of the TEMAP.

1.3 RJAT Receive Jitter Attenuator Registers (N=1 to 28)

Register 0010H+80H*N: RJAT Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	OVRI	X
Bit 0	R	UNDI	X

UNDI:

The UNDI bit is asserted when an attempt is made to read data from the receive FIFO when the FIFO is already empty. When UNDI is a logic 1, an underrun event has occurred. Reading this register will clear the UNDI bit to logic 0.

OVRI:

The OVRI bit is asserted when an attempt is made to write data into the receive FIFO when the FIFO is already full. When OVRI is a logic 1, an overrun event has occurred. Reading this register will clear the OVRI bit to logic 0.

Register 0011H+80H*N: RJAT Reference Clock Divider N1 Control

Bit	Type	Function	Default
Bit 7	R/W	N1[7]	0
Bit 6	R/W	N1[6]	0
Bit 5	R/W	N1[5]	1
Bit 4	R/W	N1[4]	0
Bit 3	R/W	N1[3]	1
Bit 2	R/W	N1[2]	1
Bit 1	R/W	N1[1]	1
Bit 0	R/W	N1[0]	1

This register contains an 8-bit binary number, N1, which is one less than the magnitude of the reference clock divisor. The reference divisor magnitude, (N1+1), is the ratio between the frequency of the recovered clock (or the transmit clock if a diagnostic loopback is enabled) and the frequency at the phase discriminator input.

Writing to this register will reset the PLL.

The default value of N1 after a device reset is 47 = 2FH.

Register 0012H+80H*N: RJAT Output Clock Divider N2 Control

Bit	Type	Function	Default
Bit 7	R/W	N2[7]	0
Bit 6	R/W	N2[6]	0
Bit 5	R/W	N2[5]	1
Bit 4	R/W	N2[4]	0
Bit 3	R/W	N2[3]	1
Bit 2	R/W	N2[2]	1
Bit 1	R/W	N2[1]	1
Bit 0	R/W	N2[0]	1

This register contains an 8-bit binary number, N2, which is one less than the magnitude of the output clock divisor. The output clock divisor magnitude, (N2+1), is the ratio between the frequency of the smooth output clock, ID[x], and the frequency applied to the phase discriminator input.

Writing to this register will reset the PLL.

The default value of N2 after a device reset is 47 = 2FH.

Register 0013H+80H*N: RJAT Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	1
Bit 4	R/W	CENT	0
Bit 3	R/W	UNDE	0
Bit 2	R/W	OVRE	0
Bit 1	R/W	SYNC	1
Bit 0	R/W	LIMIT	1

Please note that the TEMAP start-up procedure in the TEMUX/TEMAP Programmer's Guide should be referenced for correct sequencing of the jitter attenuators.

CENT:

The CENT bit allows the FIFO to self-center its read pointer, maintaining the pointer at least 4 UI away from the FIFO being empty or full. When CENT is set to logic 1, the FIFO is enabled to self-center for the next 384 transmit data bit period, and for the first 384 bit periods following an overrun or underrun event. If an EMPTY or FULL alarm occurs during this 384 UI period, the period will be extended by the number of UI that the EMPTY or FULL alarm persists. During the EMPTY or FULL alarm conditions, data is lost. When CENT is set to logic 0, the self-centering function is disabled, allowing the data to pass through uncorrupted during EMPTY or FULL alarm conditions. It is recommended to set this bit to 1.

The CENT bit can only be set to logic 1 if the SYNC bit is set to logic 0.

UNDE:

Setting the UNDE bit to logic 1 enables an underrun event to assert the INTB output low.

OVRE:

Setting the OVRE bit to logic 1 enables an overrun event to assert the INT output low.

SYNC:

The SYNC bit enables the PLL to synchronize the phase delay between the FIFO input and output data to the phase delay between reference clock input and smooth output clock at the PLL. For example, if the PLL is operating so that the smooth output clock lags the reference clock by 24 UI, then the synchronization pulses that the PLL sends to the FIFO will force its output data to lag its input data by 24 UI. When SYNC is set to logic 1, then the RJAT divisors (N1 and N2) must be set so that N1+1 is a multiple of 48 decimal, and N2+1 is a multiple of 48 decimal.

LIMIT:

Setting the LIMIT bit to logic 1 will limit the PLL jitter attenuation by enabling the FIFO to increase or decrease the frequency of the smooth output clock whenever the FIFO is within one UI of overflowing or underflowing. This limiting of jitter ensures that no data is lost during high phase shift conditions. When LIMIT is set to logic 0, underflows and overflows may occur.

Reserved:

This bit must be programmed to logic 1 for future compatibility.

1.4 TJAT Transmit Jitter Attenuator Registers (N=1 to 28)

Register 0014H+80H*N: TJAT Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	OVRI	X
Bit 0	R	UNDI	X

UNDI:

The UNDI bit is asserted when an attempt is made to read data from the transmit FIFO when the FIFO is already empty. When UNDI is a logic 1, an underrun event has occurred. Reading this register will clear the UNDI bit to logic 0.

OVRI:

The OVRI bit is asserted when an attempt is made to write data into the transmit FIFO when the FIFO is already full. When OVRI is a logic 1, an overrun event has occurred. Reading this register will clear the OVRI bit to logic 0.

Register 0015H+80H*N: TJAT Jitter Attenuator Divider N1 Control

Bit	Type	Function	Default
Bit 7	R/W	N1[7]	0
Bit 6	R/W	N1[6]	0
Bit 5	R/W	N1[5]	1
Bit 4	R/W	N1[4]	0
Bit 3	R/W	N1[3]	1
Bit 2	R/W	N1[2]	1
Bit 1	R/W	N1[1]	1
Bit 0	R/W	N1[0]	1

This register contains an 8-bit binary number, N1, which is one less than the magnitude of the reference clock divisor. The reference divisor magnitude, (N1+1), is the ratio between the frequency of the reference clock (as selected by the PLLREF1 and PLLREF0 bits of the Egress Interface Configuration register) and the frequency at the phase discriminator input.

Writing to this register will reset the PLL.

The default value of N1 after a device reset is 47 = 2FH.

Register 0016H+80H*N: TJAT Divider N2 Control

Bit	Type	Function	Default
Bit 7	R/W	N2[7]	0
Bit 6	R/W	N2[6]	0
Bit 5	R/W	N2[5]	1
Bit 4	R/W	N2[4]	0
Bit 3	R/W	N2[3]	1
Bit 2	R/W	N2[2]	1
Bit 1	R/W	N2[1]	1
Bit 0	R/W	N2[0]	1

This register contains an 8-bit binary number, N2, which is one less than the magnitude of the output clock divisor. The output clock divisor magnitude, (N2+1), is the ratio between the frequency of the smooth output clock and the frequency applied to the phase discriminator input.

Writing to this register will reset the PLL.

The default value of N2 after a device reset is 47 = 2FH.

Register 0017H+80H*N: TJAT Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	1
Bit 4	R/W	CENT	0
Bit 3	R/W	UNDE	0
Bit 2	R/W	OVRE	0
Bit 1	R/W	SYNC	1
Bit 0	R/W	LIMIT	1

CENT:

The CENT bit allows the FIFO to self-center its read pointer, maintaining the pointer at least 4 UI away from the FIFO being empty or full. When CENT is set to logic 1, the FIFO is enabled to self-center for the next 384 transmit data bit period, and for the first 384 bit periods following an overrun or underrun event. If an EMPTY or FULL alarm occurs during this 384 UI period, the period will be extended by the number of UI that the EMPTY or FULL alarm persists. During the EMPTY or FULL alarm conditions, data is lost. When CENT is set to logic 0, the self-centering function is disabled, allowing the data to pass through uncorrupted during EMPTY or FULL alarm conditions. It is recommended to set this bit to 1.

The CENT bit can only be set to logic 1 if the SYNC bit is set to logic 0.

UNDE:

Setting the UNDE bit to logic 1 enables an underrun event to assert the INTB output low.

OVRE:

Setting the OVRE bit to logic 1 enables an overrun event to assert the INT output low.

SYNC:

The SYNC bit enables the PLL to synchronize the phase delay between the FIFO input and output data to the phase delay between reference clock input and smooth output clock at the PLL. For example, if the PLL is operating so

that the smooth output clock lags the reference clock by 24 UI, then the synchronization pulses that the PLL sends to the FIFO will force its output data to lag its input data by 24 UI. When using the 2Mbit/s transmit backplane option, the SYNC bit must be set to logic 0. When SYNC is set to logic 1, then the TJAT divisors (N1 and N2) must be set so that N1+1 is a multiple of 48 decimal, and N2+1 is a multiple of 48 decimal.

SYNC must only be set to logic 1 when The Egress Interface is in a Clock Slave mode (PLLREF[1:0] = 00 in Register 004H+80H*N)

LIMIT:

Setting the LIMIT bit to logic 1 will limit the PLL jitter attenuation by enabling the FIFO to increase or decrease the frequency of the smooth output clock whenever the FIFO is within one UI of overflowing or underflowing. This limiting of jitter ensures that no data is lost during high phase shift conditions. When LIMIT is set to logic 0, underflows and overflows may occur.

Reserved:

The Reserved bit must be programmed to logic 1 for future compatibility.

1.5 PMON Performance Monitor Registers (N=1 to 28)

Register 0038H+80H*N: PMON Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	INTE	0
Bit 1	R	XFER	0
Bit 0	R	OVR	0

This register contains status information indicating when counter data has been transferred into the holding registers and indicating whether the holding registers have been overrun.

INTE:

The INTE bit controls the generation of a microprocessor interrupt when the transfer clock has caused the counter values to be stored in the holding registers. A logic 1 bit in the INTE position enables the generation of an interrupt via the INTB output; a logic 0 bit in the INTE position disables the generation of an interrupt.

XFER:

The XFER bit indicates that a transfer of counter data has occurred. A logic 1 in this bit position indicates that a latch request, initiated by writing to one of the counter register locations or the Global PMON Update register, was received and a transfer of the counter values has occurred. A logic 0 indicates that no transfer has occurred. The XFER bit is cleared (acknowledged) by reading this register.

OVR:

The OVR bit is the overrun status of the holding registers. A logic 1 in this bit position indicates that a previous transfer (indicated by XFER being logic 1) has not been acknowledged before the next transfer clock has been issued and that the contents of the holding registers have been overwritten. A logic 0

indicates that no overrun has occurred. The OVR bit is cleared by reading this register.

Registers 0038H+80H*N –003DH+80H*N: Latching Performance Data

The Performance Data registers for a single framer are updated as a group by writing to any of the PMON count registers (Framing Bit Error count register, OOF/COFA/Fare End Block Error count register or Bit Error/CRCE Error count register). A write to one (and only one) of these locations loads performance data located in the PMON into the internal holding registers. Alternatively, the Performance Data registers are updated by writing to the Revision / Global PMON Update register (address 0002H). The data contained in the holding registers can then be subsequently read by microprocessor accesses into the PMON count register address space. The latching of count data, and subsequent resetting of the counters, is synchronized to the internal event timing so that no events are missed.

The PMON is loaded with new performance data within 3.5 recovered clock periods of the latch performance data register write. With nominal line rates, the PMON registers should not be polled until 2.3 µsec have elapsed from the "latch performance data" register write.

When the TEMAP is reset, the contents of the PMON count registers are unknown until the first latching of performance data is performed.

Register 0039H+80H*N: PMON Framing Bit Error Count

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	FER[6]	X
Bit 5	R	FER[5]	X
Bit 4	R	FER[4]	X
Bit 3	R	FER[3]	X
Bit 2	R	FER[2]	X
Bit 1	R	FER[1]	X
Bit 0	R	FER[0]	X

FER[6:0]:

The FER[6:0] bits indicate the number of framing bit error events that occurred during the previous accumulation interval. The FER counts are suppressed when the framer has lost frame alignment (OOF in the E1-FRMR Framing Status register is logic 1 or INFR in the T1-FRMR Interrupt Status register is logic 0).

In T1 mode, a framing bit error is defined as an F_e-bit error in ESF mode or a framing bit error in SF mode.

In E1 mode, the count is either the number of FAS (frame alignment signal) bits (default) or words in error. As an option, a zero in bit 2 of time slot 0 of non-frame alignment signal (NFAS) frames results in an increment of the framing error count. Refer to the Receive Options register.

Register 003AH+80H*N: PMON OOF/COFA/Far End Block Error Count LSB

Bit	Type	Function	Default
Bit 7	R	OOF/FEBE[7]	X
Bit 6	R	OOF/FEBE[6]	X
Bit 5	R	OOF/FEBE[5]	X
Bit 4	R	OOF/FEBE[4]	X
Bit 3	R	OOF/FEBE[3]	X
Bit 2	R	OOF/FEBE[2]	X
Bit 1	R	OOF/FEBE[1]	X
Bit 0	R	OOF/FEBE[0]	X

Register 003BH+80H*N: PMON OOF/COFA/Far End Block Error Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	OOF/FEBE[9]	X
Bit 0	R	OOF/FEBE[8]	X

OOF/FEBE[9:0]:

In T1 mode, the OOF[9:0] bits indicate the number Out Of Frame or Change Of Frame Alignment events that occurred during the previous accumulation interval, as specified by the CCOFA bit in the Receive Options register. If OOFs are being accumulated, the count is incremented each time a severely errored framing event forces a reframe. IF COFAs are being accumulated, the count is incremented if a new alignment differs from the previous alignment.

In E1 mode, the FEBE[9:0] bits indicate the number of far end block error events that occurred during the previous accumulation interval. The FEBE

counts are suppressed when the E1 FRMR has lost frame alignment (OOF in the FRMR Framing Status register is set).

Register 003CH+80H*N: PMON Bit Error/CRC Error Count LSB

Bit	Type	Function	Default
Bit 7	R	BEE/CRCE[7]	X
Bit 6	R	BEE/CRCE[6]	X
Bit 5	R	BEE/CRCE[5]	X
Bit 4	R	BEE/CRCE[4]	X
Bit 3	R	BEE/CRCE[3]	X
Bit 2	R	BEE/CRCE[2]	X
Bit 1	R	BEE/CRCE[1]	X
Bit 0	R	BEE/CRCE[0]	X

Register 003DH+80H*N: PMON Bit Error/CRC Error Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	BEE/CRCE[9]	X
Bit 0	R	BEE/CRCE[8]	X

BEE/CRCE[9:0]:

In T1 mode, the BEE[9:0] bits contain the number of bit error events that occurred during the previous accumulation interval. A bit error event is defined as a CRC-6 error in ESF mode or a framing bit error in SF mode.

In E1 mode, the CRCE[9:0] bits indicate the number of CRC error events that occurred during the previous accumulation interval. CRC error events are suppressed when the E1 FRMR is out of CRC-4 multiframe alignment (OOCMF bit in the FRMR Framing Status register is set).

1.6 PRBS Generator/Checker Registers (N=1 to 28)

Register 0050H+80H*N: PRBS Generator/Checker Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	QRSS	0
Bit 4		Unused	X
Bit 3	R/W	TINV	0
Bit 2	R/W	RINV	0
Bit 1	R/W	AUTOSYNC	1
Bit 0	R/W	MANSYNC	0

QRSS:

The QRSS bit enables the zero suppression feature required when generating the QRSS sequence. When QRSS is a logic 1, a one is forced in the TDAT stream when the following 14 bit positions are all zeros. When QRSS is a logic 0, the zero suppression feature is disabled. To generate the 2^{20} -1 QRSS pattern, note that the PATSEL[1:0] bits in PRBS Pattern Select Register 0052H+80H*N must be programmed to 01.

TINV:

The TINV bit controls the logical inversion of the generated data stream. When TINV is a logic 1, the data is inverted. When TINV is a logic 0, the data is not inverted.

RINV:

The RINV bit controls the logical inversion of the receive data stream before processing. When RINV is a logic 1, the received data is inverted before being processed by the pattern detector. When RINV is a logic 0, the received data is not inverted.

AUTOSYNC:

The AUTOSYNC bit enables the automatic resynchronization of the pattern detector. The automatic resynchronization is activated when 10 or more bit errors are detected in a fixed 48-bit window. When AUTOSYNC is a logic 1,

the auto resync feature is enabled. When AUTOSYNC is a logic 0, the auto sync feature is disabled, and pattern resynchronization is accomplished using the MANSYNC bit.

MANSYNC:

The MANSYNC bit is used to initiate a manual resynchronization of the pattern detector. A low to high transition on MANSYNC initiates the resynchronization.

Register 0051H+80H*N: PRBS Checker Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7	R/W	SYNCE	0
Bit 6	R/W	BEE	0
Bit 5	R/W	XFERE	0
Bit 4	R	SYNCV	X
Bit 3	R	SYNCI	X
Bit 2	R	BEI	X
Bit 1	R	XFERI	X
Bit 0	R	OVR	X

SYNCE:

The SYNCE bit enables the generation of an interrupt when the PRBS checker changes synchronization state. When SYNCE is set to logic 1, the interrupt is enabled.

BEE:

The BEE bit enables the generation of an interrupt when a bit error is detected in the receive data. When BEE is set to logic 1, the interrupt is enabled.

XFERE:

The XFERE bit enables the generation of an interrupt when an accumulation interval is completed and new values are stored in the error counter holding registers. When XFERE is set to logic 1, the interrupt is enabled.

SYNCV:

The SYNCV bit indicates the synchronization state of the PRBS checker. When SYNCV is a logic 1 the PRBS checker is synchronized (the PRBS checker has observed at least 32 consecutive error free bit periods). When SYNCV is a logic 0, the PRBS checker is out of sync (the PRBS checker has detected 6 or more bit errors in a 64 bit period window).

SYNCI:

The SYNCI bit indicates that the detector has changed synchronization state since the last time this register was read. If SYNCI is logic 1, the pattern

detector has gained or lost synchronization at least once. SYNCI is set to logic 0 when this register is read.

BEI:

The BEI bit indicates that one or more bit errors have been detected since the last time this register was read. When BEI is set to logic 1, at least one bit error has been detected. BEI is set to logic 0 when this register is read.

XFERI:

The XFERI bit indicates that a transfer of the error count has occurred. A logic 1 in this bit position indicates that the error counter holding registers has been updated. This update is initiated by writing to one of the PRBS Error Count register locations, or by writing to the TEMAP Global PMON Update Register. XFERI is set to logic 0 when this register is read.

OVR:

The OVR bit is the overrun status of the Error Count registers. A logic 1 in this bit position indicates that a previous transfer (indicated by XFERI being logic 1) has not been acknowledged before the next accumulation interval has occurred and that the contents of the error counter holding registers have been overwritten. OVR is set to logic 0 when this register is read.

Register 0052H+80H*N: PRBS Pattern Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	PATSEL[1]	0
Bit 0	R/W	PATSEL[0]	0

PATSEL[1:0]:

PATSEL[1:0] determines which of the three PRBS patterns are generated and checked for errors.

PATSEL[1:0]	Pattern
00	2^{15}-1
01	2^{20}-1
10	2^{11}-1
11	Reserved

Register 0054H+80H*N: PRBS Error Count #1

Bit	Type	Function	Default
Bit 7	R/W	ERRCNT [7]	0
Bit 6	R/W	ERRCNT [6]	0
Bit 5	R/W	ERRCNT [5]	0
Bit 4	R/W	ERRCNT [4]	0
Bit 3	R/W	ERRCNT [3]	0
Bit 2	R/W	ERRCNT [2]	0
Bit 1	R/W	ERRCNT [1]	0
Bit 0	R/W	ERRCNT [0]	0

Register 0055H+80H*N: PRBS Error Count #2

Bit	Type	Function	Default
Bit 7	R/W	ERRCNT [15]	0
Bit 6	R/W	ERRCNT [14]	0
Bit 5	R/W	ERRCNT [13]	0
Bit 4	R/W	ERRCNT [12]	0
Bit 3	R/W	ERRCNT [11]	0
Bit 2	R/W	ERRCNT [10]	0
Bit 1	R/W	ERRCNT [9]	0
Bit 0	R/W	ERRCNT [8]	0

Register 0056H+80H*N: PRBS Error Count #3

Bit	Type	Function	Default
Bit 7	R/W	ERRCNT [23]	0
Bit 6	R/W	ERRCNT [22]	0
Bit 5	R/W	ERRCNT [21]	0
Bit 4	R/W	ERRCNT [20]	0
Bit 3	R/W	ERRCNT [19]	0

Bit	Type	Function	Default
Bit 2	R/W	ERRCNT [18]	0
Bit 1	R/W	ERRCNT [17]	0
Bit 0	R/W	ERRCNT [16]	0

ERRCNT[23:0]:

ERRCNT[23:0] contain the error counter holding register. The value in this register represents the number of bit errors that have been accumulated since the last accumulation interval. Note that bit errors are not accumulated while the pattern detector is out of sync.

The Error Count registers for each individual PRBS generator/Checker are updated by writing to any one of the Error count registers. Alternatively, the Error Count registers are updated globally with all other TEMAP counter registers by writing to the Revision / Global PMON Update register (address 0002H).

1.7 ALMI Alarm Integrator Registers (N=1 to 28)

These registers are only accessible when in T1 mode; selected when the E1/T1B mode bit in the TEMAP Global Configuration Register is a logic 0.

Register 0060H+80H*N: T1 ALMI Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	ESF	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1		Unused	X
Bit 0		Unused	X

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

This register allows selection of the framing format and the data rate of the Facility Data Link in ESF to allow operation of the CFA detection algorithms.

ESF:

The ESF bit selects either extended superframe format or regular superframe framing formats. A logic 1 in the ESF bit position selects ESF; a logic 0 in the ESF bit selects SF.

Reserved:

These bits are reserved and must be set to logic 0 for correct operation.

Register 0061H+80H*N: T1 ALMI Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	FASTD	0
Bit 3	R/W	ACCEL	0
Bit 2	R/W	YELE	0
Bit 1	R/W	REDE	0
Bit 0	R/W	AISE	0

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

This register selects which of the three CFA's can generate an interrupt when their logic state changes and enables the "fast" deassertion mode of operation.

FASTD:

The FASTD bit enables the "fast" deassertion of Red and AIS alarms. When FASTD is set to a logic 1, deassertion of Red alarm occurs within 120 ms of going in frame. Deassertion of AIS alarm occurs within 180 ms of either detecting a 60 ms interval containing 127 or more zeros, or going in frame. When FASTD is set to a logic 0, Red and AIS alarm deassertion times remain as defined in the ALMI description.

ACCEL:

The ACCEL bit is used for production test purposes only. THE ACCEL BIT MUST BE PROGRAMMED TO LOGIC 0 FOR NORMAL OPERATION.

YELE, REDE, AISE:

A logic 1 in the enable bit positions (YELE, REDE, AISE) enables a state change in the corresponding CFA to generate an interrupt; a logic 0 in the enable bit positions disables any state changes to generate an interrupt. The enable bits are independent; any combination of Yellow, Red, and AIS CFA's can be enabled to generate an interrupt.

Upon reset of the TEMAP, these bits are cleared to logic 0.

Register 0062H+80H*N: T1 ALMI Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	YELI	0
Bit 4	R	REDI	0
Bit 3	R	AISI	0
Bit 2	R	YEL	0
Bit 1	R	RED	0
Bit 0	R	AIS	0

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

This register indicates which of the three Carry Failure Alarms (CFA's) generated an interrupt when their logic state changed in bit positions 5 through 3, and indicate the current state of each CFA in bit positions 2 through 0. A logic 1 in the status positions (YELI, REDI, AISI) indicate that a state change in the corresponding CFA has generated an interrupt; a logic 0 in the status positions indicates that no state change has occurred. Both the status bit positions (bits 5 through 3) and the interrupt generated because of the change in CFA state are cleared to logic 0 when the register containing then is read.

Register 0063H+80H*N: T1 ALMI Alarm Detection Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	REDD	X
Bit 1	R	YELD	X
Bit 0	R	AISD	X

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

This register indicates the presence or absence of one or more OOF occurrences within the last 40 ms; the presence or absence of the Yellow alarm signal over the last 40 ms; and indicate the presence or absence of the AIS alarm signal over the last 60 ms.

REDD:

When REDD is a logic 1, one or more out of frame events have occurred during the last 40 ms interval. When REDD is a logic 0, no out of frame events have occurred within the last 40 ms interval.

YELD:

When YELD is logic 1, a valid Yellow signal was present during the last 40 ms interval. When YELD is logic 0, the Yellow signal was absent during the last 40 ms interval. For each framing format, a valid Yellow signal is deemed to be present if:

- bit 2 of each channel is not logic 0 for 16 or fewer times during the 40 ms interval for the SF framing format;
- the 16-bit Yellow bit oriented code is received error-free 8 or more times during the interval for ESF framing format with a 4 KHz data link;

AISD:

When AISD is logic 1, a valid AIS signal was present during the last 60 ms interval. When AISD is logic 0, the AIS signal was absent during the last 60 ms interval. A valid AIS signal is deemed to be present during a 60 ms interval if the out of frame condition has persisted for the entire interval and the received PCM data stream is not logic 0 for 126 or fewer times.

1.8 T1-FRMR Framer Registers (N=1 to 28)

These registers are only accessible when in T1 mode; selected when the E1/T1B mode bit in the TEMAP Global Configuration Register is a logic 0.

Register 006CH+80H*N: T1 FRMR Configuration

Bit	Type	Function	Default
Bit 7	R/W	M2O[1]	0
Bit 6	R/W	M2O[0]	0
Bit 5	R/W	ESFFA	0
Bit 4	R/W	ESF	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	JPN	0
Bit 0		Unused	X

When the E1/T1B bit of the Global Configuration register is a logic 1 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

This register selects the framing format and the frame loss criteria used by the T1-FRMR.

M2O[1:0]:

The M2O[1:0] bits select the ratio of errored to total framing bits before declaring out of frame in SF, and ESF framing formats. A logic 00 selects 2 of 4 framing bits in error; a logic 01 selects 2 of 5 bits in error; a logic 10 selects 2 of 6 bits in error. A logic 11 in the M2O[1:0] bits is reserved and must not be used.

ESFFA:

The ESFFA bit selects one of two framing algorithms for ESF frame search in the presence of mimic framing patterns in the incoming data. A logic 0 selects the ESF algorithm where the FRMR does not declare inframe while more than one framing bit candidate is following the framing pattern in the incoming data. A logic 1 selects the ESF algorithm where a CRC-6 calculation is performed on each framing bit candidate, and is compared

against the CRC bits associated with the framing bit candidate to determine the most likely framing bit position.

ESF:

The ESF bit selects either extended superframe format or enables the Frame Mode Select bits to select standard superframe format. A logic 1 in the ESF bit position selects ESF; a logic 0 selects standard superframe.

JPN:

The JPN bit enables Japanese variations of the standard framing formats. If the JPN bit is a logic 1 and the ESF format is selected (ESF bit is logic 1), the T1-FRMR complies to TTC JT-G704. If the JPN bit is a logic 1 and a non-ESF format is selected (ESF bit is logic 0), it is assumed the 12^{th} F-bit of the superframe carries a far end receive failure alarm. The alarm is extracted and the framing is modified to be robust when the alarm is active.

Reserved:

These bits are reserved and must each be set to logic 0 for correct operation.

Register 006DH+80H*N: T1 FRMR Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	Reserved	0
Bit 5	R/W	COFAE	0
Bit 4	R/W	FERE	0
Bit 3	R/W	BEEE	0
Bit 2	R/W	SFEE	0
Bit 1	R/W	MFPE	0
Bit 0	R/W	INFRE	0

When the E1/T1B bit of the Global Configuration register is a logic 1 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

This register selects which of the MFP, COFA, FER, BEE, SFE or INFR events generates an interrupt on the microprocessor INTB pin when their state changes or their event condition is detected.

Reserved:

The Reserved bit is used for production test purposes only. The Reserved bit must be programmed to logic 0 for normal operation.

COFAE:

The COFAE bit enables the generation of an interrupt when the frame find circuitry determines that frame alignment has been achieved and that the new alignment differs from the previous alignment. When COFAE is set to logic 1, the declaration of a change of frame alignment is allowed to generate an interrupt. When COFAE is set to logic 0, a change in the frame alignment does not generate an interrupt on the INTB pin.

FERE:

The FERE bit enables the generation of an interrupt when a framing bit error has been detected. When FERE is set to logic 1, the detection of a framing bit error is allowed to generate an interrupt. When FERE is set to logic 0, any error in the framing bits does not generate an interrupt on the INTB pin.

BEEE:

The BEEE bit enables the generation of an interrupt when a bit error event has been detected. A bit error event is defined as framing bit errors for SF formatted data or CRC-6 mismatch errors for ESF formatted data. When BEEE is set to logic 1, the detection of a bit error event is allowed to generate an interrupt. When BEEE is set to logic 0, bit error events are disabled from generating an interrupt on the INTB pin.

SFEE:

The SFEE bit enables the generation of an interrupt when a severely errored framing event has been detected. A severely errored framing event is defined as 2 or more framing bit errors during the current superframe for SF and ESF formatted data. When SFEE is set to logic 1, the detection of a severely errored framing event is allowed to generate an interrupt. When SFEE is set to logic 0, severely errored framing events are disabled from generating an interrupt on the INTB pin.

MFPE:

The MFPE bit enables the generation of an interrupt when the frame find circuitry detects the presence of framing bit mimics. The occurrence of a mimic is defined as more than one framing bit candidate following the frame alignment pattern. When MFPE is set to logic 1, the assertion or deassertion of the detection of a mimic is allowed to generate an interrupt. When MFPE is set to logic 0, the detection of a mimic framing pattern is disabled from generating an interrupt on the INTB pin.

INFRE:

The INFRE bit enables the generation of an interrupt when the frame find circuitry determines that frame alignment has been achieved and that the framer is now "inframe". When INFRE is set to logic 1, the assertion or deassertion of the "inframe" state is allowed to generate an interrupt. When INFRE is set to logic 0, a change in the "inframe" state is disabled from generating an interrupt on the INTB pin.

Upon reset of the TEMAP, these bits are set to logic 0, disabling the generation of interrupts on the INTB pin.

Register 006EH+80H*N: T1 FRMR Interrupt Status

Bit	Type	Function	Default
Bit 7	R	COFAI	0
Bit 6	R	FERI	0
Bit 5	R	BEEI	0
Bit 4	R	SFEI	0
Bit 3	R	MFPI	0
Bit 2	R	INFRI	0
Bit 1	R	MFP	0
Bit 0	R	INFR	0

When the E1/T1B bit of the Global Configuration register is a logic 1 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

This register indicate whether a change of frame alignment, a framing bit error, a bit error event, or a severely errored framing event generated an interrupt. This register also indicates whether a mimic framing pattern was detected or whether there was a change in the "inframe" state of the frame circuitry.

COFAI, FERI, BEEI, SFEI:

A logic 1 in the status bit positions COFAI, FERI, BEEI and SFEI indicate that the occurrence of the corresponding event generated an interrupt; a logic 0 in the status bit positions COFAI, FERI, BEEI, and SFEI indicate that the corresponding event did not generate an interrupt.

MFPI:

A logic 1 in the MFPI status bit position indicates that the assertion or deassertion of the mimic detection indication has generated an interrupt; a logic 0 in the MFPI bit position indicates that no change in the state of the mimic detection indication occurred.

INFRI:

A logic 1 in the INFRI status bit position indicates that a change in the "inframe" state of the frame alignment circuitry generated an interrupt; a logic 0 in the INFRI status bit position indicates that no state change occurred.

MFP, INFR:

The bit position MFP and INFR indicate the current state of the mimic detection and of the frame alignment circuitry.

The interrupt and the status bit positions (COFAI, FERI, BEEI, SFEI, MFPI, and INFRI) are cleared to logic 0 when this register is read.

1.9 E1-FRMR Framer Registers (N=1 to 21)

These registers are only accessible when in E1 mode; selected when the E1/T1B mode bit in the TEMAP Global Configuration Register is a logic 1.

Register 0060H+80H*N: E1 FRMR Frame Alignment Options

Bit	Type	Function	Default
Bit 7	R/W	CRCEN	1
Bit 6	R/W	CASDIS	0
Bit 5	R/W	C2NCIWCK	0
Bit 4		Unused	X
Bit 3	R/W	Reserved	0
Bit 2	R/W	REFR	0
Bit 1	R/W	REFCRCEN	1
Bit 0	R/W	REFRDIS	0

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

This register selects the various framing formats and framing algorithms supported by the FRMR block.

CRCEN:

The CRCEN bit enables the FRMR to frame to the CRC multiframe. When the CRCEN bit is logic 1, the FRMR searches for CRC multiframe alignment and monitors for errors in the alignment. A logic 0 in the CRCEN bit position disables searching for multiframe and suppresses the OOCMF, CRCE, CMFER, FEBE, CFEBE, RAICCRC, C2NCIW and ICMFPI FRMR status/interrupt bits, forcing them to logic 0.

CASDIS:

The CASDIS bit enables the FRMR to frame to the Channel Associated Signaling multiframe when set to a logic 0. When CAS is enabled, the FRMR searches for signaling multiframe alignment and monitors for errors in the alignment. A logic 1 in the CASDIS bit position disables searching for multiframe and suppresses the OOSMF and the SMFER FRMR outputs, forcing them to logic 0.

C2NCIWCK:

The C2NCIWCK bit enables the continuous checking for CRC multiframe in the CRC to non-CRC interworking mode of the E1 FRMR. If this bit is a logic 0, the E1-FRMR will cease searching for CRC multiframe alignment in CRC to non-CRC interworking mode. If this bit is a logic 1, the E1-FRMR will continue searching for CRC multiframe alignment, even if CRC to non-CRC interworking has been declared.

Reserved:

The Reserved bit must be programmed to logic 0 for normal operation.

REFR:

A transition from logic 0 to logic 1 in the REFR bit position forces the re-synchronization to a new frame alignment. The bit must be cleared to logic 0, then set to logic 1 again to generate subsequent re-synchronization.

REFCRCEN:

The REFCRCEN bit enables excessive CRC errors (≥ 915 errors in one second) to force a re-synchronization to a new frame alignment. Setting the REFCRCEN bit position to logic 1 enables reframe due to excessive CRC errors; setting the REFCRCEN bit to logic 0 disables CRC errors from causing a reframe.

REFRDIS:

The REFRDIS bit disables reframing under any error condition once frame alignment has been found; reframing can be initiated by software via the REFR bit. A logic 1 in the REFRDIS bit position causes the FRMR to remain "locked in frame" once initial frame alignment has been found. A logic 0 allows reframing to occur based on the various error criteria (FER, excessive CRC errors, etc.). Note that while the FRMR remains locked in frame due to REFRDIS=1, a received AIS will not be detected since the FRMR must be out-of-frame to detect AIS.

Register 0061H+80H*N: E1 FRMR Maintenance Mode Options

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	BIT2C	1
Bit 5	R/W	SMFASC	0
Bit 4	R/W	TS16C	0
Bit 3	R/W	RAIC	0
Bit 2		Unused	X
Bit 1	R/W	AISC	0
Bit 0	R	EXCRCERR	X

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

BIT2C:

The BIT2C bit enables the additional criterion that loss of frame is declared when bit 2 in time slot 0 of NFAS frames has been received in error on 3 consecutive occasions: a logic 1 in the BIT2C position enables declaration of loss of frame alignment when bit 2 is received in error; a logic 0 in BIT2C enables declaration of loss of frame alignment based on the absence of FAS frames only.

SMFASC:

The SMFASC bit selects the criterion used to declare loss of signaling multiframe alignment signal: a logic 0 in the SMFASC bit position enables declaration of loss of signaling multiframe alignment when 2 consecutive multiframe alignment patterns have been received in error; a logic 1 in the SMFASC bit position enables declaration of loss of signaling multiframe when 2 consecutive multiframe alignment patterns have been received in error or when time slot 16 contains logic 0 in all bit positions for 1 or 2 multiframes based on the criterion selected by TS16C.

TS16C:

The TS16C bit selects the criterion used to declare loss of signaling multiframe alignment signal when enabled by the SMFASC: a logic 0 in the TS16C bit position enables declaration of loss of signaling multiframe alignment when time slot 16 contains logic 0 in all bit positions for 1

multiframe; a logic 1 in the TS16C bit position enables declaration of loss of signaling multiframe when time slot 16 contains logic 0 in all bit positions for 2 consecutive signaling multiframes.

RAIC:

The RAIC bit selects the criterion used to declare a Remote Alarm Indication (RAI). If RAIC is logic 0, the RAIV indication is asserted upon reception of any A=1 (bit 3 of NFAS frames) and is deasserted upon reception of any A=0. If RAIC is logic 1, the RAIV indication is asserted if A=1 is received on 4 or more consecutive occasions, and is cleared upon reception of any A=0.

AISC :

The AISC bit selects the criterion used for determining AIS alarm indication. If AISC is logic 0, AIS is declared if there is a loss of frame (LOF) indication and a 512-bit period is received with less than 3 zeros. If AISC is a logic 1, AIS is declared if less than 3 zeros are detected in each of 2 consecutive 512-bit periods and is cleared when 3 or more zeros are detected in each of 2 consecutive 512-bit intervals.

EXCRCERR:

The EXCRCERR bit is an active high status bit indicating that excessive CRC evaluation errors (i.e., $\geq$ 915 errors in one second) have occurred, thereby initiating a reframe if enabled by the REFCRCNE bit of the E1 FRMR Frame Alignment Options register. The EXCRCERR bit is reset to logic 0 after the register is read.

Register 0062H+80H*N: E1 FRMR Framing Status Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	C2NCIWE	0
Bit 6	R/W	OOFE	0
Bit 5	R/W	OOSMFE	0
Bit 4	R/W	OOCMFE	0
Bit 3	R/W	COFAE	0
Bit 2	R/W	FERE	0
Bit 1	R/W	SMFERE	0
Bit 0	R/W	CMFERE	0

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

C2NCIWE, OOFE, OOSMFE and OOCMFE:

A logic one in bits C2NCIWE, OOFE, OOSMFE and OOCMFE enables the generation of an interrupt on a change of state of C2NCIWV, OOFV, OOSMFV and OOCMFV bits respectively of the E1 FRMR Framing Status register.

COFAE:

A logic one in the COFAE bit enables the generation of an interrupt when the position of the frame alignment has changed.

FERE:

A logic one in the FERE bit enables the generation of an interrupt when an error has been detected in the frame alignment signal.

SMFERE:

A logic one in the SMFERE bit enables the generation of an interrupt when an error has been detected in the signaling multiframe alignment signal.

CMFERE:

A logic one in the CMFERE bit enables the generation of an interrupt when an error has been detected in the CRC multiframe alignment signal.

Register 0063H+80H*N: E1 FRMR Maintenance/Alarm Status Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	RAIE	0
Bit 6	R/W	RMAIE	0
Bit 5	R/W	AISDE	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	REDE	0
Bit 2	R/W	AISE	0
Bit 1	R/W	FEBEE	0
Bit 0	R/W	CRCEE	0

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

RAIE, RMAIE, AISDE, REDE and AISE:

A logic one in bits RAIE, RMAIE, AISDE, REDE or AISE enables the generation of an interrupt on a change of state of the RAIV, RMAIV, AISD, RED and AIS bits respectively of the E1 FRMR Maintenance/Alarm Status register.

Reserved:

This bit must be set to a logic 0 for correct operation.

FEBEE:

When the FEBEE bit is a logic one, an interrupt is generated when a logic zero is received in the Si bits of frames 13 or 15.

CRCEE:

When the CRCEE bit is a logic one, an interrupt is generated when calculated CRC differs from the received CRC remainder.

Register 0064H+80H*N: E1 FRMR Framing Status Interrupt Indication

Bit	Type	Function	Default
Bit 7	R	C2NCIWI	X
Bit 6	R	OOFI	X
Bit 5	R	OOSMFI	X
Bit 4	R	OOCMFI	X
Bit 3	R	COFAI	X
Bit 2	R	FERI	X
Bit 1	R	SMFERI	X
Bit 0	R	CMFERI	X

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

A logic 1 in any bit position of this register indicates which framing status generated an interrupt by changing state.

C2NCIWI, OOFI, OOSMFI, OOCMFI, and COFAI:

C2NCIWI, OOFI, OOSMFI, OOCMFI, and COFAI indicate when the corresponding status has changed state from logic 0 to logic 1 or vice-versa.

FERI, SMFERI, CMFERI:

FERI, SMFERI, CMFERI indicate when a framing error, signaling multiframe error or CRC multiframe error event has been detected; these bits will be set if one or more errors have occurred since the last register read.

The interrupt indications within this register work independently from the interrupt enable bits, allowing the microprocessor to poll the register to determine the state of the framer. The contents of this register are cleared to logic 0 after the register is read; the interrupt is also cleared if it was generated by any of the Framing Status outputs.

Register 0065H+80H*N: E1 FRMR Maintenance/Alarm Status Interrupt Indication

Bit	Type	Function	Default
Bit 7	R	RAII	X
Bit 6	R	RMAII	X
Bit 5	R	AISDI	X
Bit 4		Unused	X
Bit 3	R	REDI	X
Bit 2	R	AISI	X
Bit 1	R	FEBEI	X
Bit 0	R	CRCEI	X

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

A logic 1 in any bit position of this register indicates which maintenance or alarm status generated an interrupt by changing state.

RAII, RMAII, AISDI, REDI, and AISI:

RAII, RMAII, AISDI, REDI, and AISI indicate when the corresponding FRMR Maintenance/Alarm Status register bit has changed state from logic 0 to logic 1 or vice-versa.

FEBEI:

The FEBEI bit becomes a logic one when a logic zero is received in the Si bits of frames 13 or 15.

CRCEI:

The CRCEI bit becomes a logic one when a calculated CRC differs from the received CRC remainder.

The bits in this register are set by a single error event.

The interrupt indications within this register work independently from the interrupt enable bits, allowing the microprocessor to poll the register to determine the state of the framer. The contents of this register are cleared to logic 0 after the register is read; the interrupt is also cleared if it was generated by one of the Maintenance/Alarm Status events.

Register 0066H+80H*N: E1 FRMR Framing Status

Bit	Type	Function	Default
Bit 7	R	C2NCIWV	X
Bit 6	R	OOFV	X
Bit 5	R	OOSMFV	X
Bit 4	R	OOCMFV	X
Bit 3	R	OOOFV	X
Bit 2	R	RAICCRCV	X
Bit 1	R	CFEBEV	X
Bit 0	R	V52LINKV	X

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

Reading this register returns the current state value of the C2NCIW, OOF, OOSMF, OOCMF, OOOF and RAICCRC FRMR framing statuses.

C2NCIWV:

The C2NCIWV bit is set to logic one while the FRMR is operating in CRC to non-CRC interworking mode. The C2NCIWV bit goes to a logic zero once when the FRMR exits CRC to non-CRC interworking mode.

OOFV:

The OOFV bit is a logic one when basic frame alignment has been lost. The OOFV bit goes to a logic zero once frame alignment has been regained.

OOSMFV:

The OOSMFV bit is a logic one when the signaling multiframe alignment has been lost. The OOSMFV bit becomes a logic zero once signaling multiframe has been regained.

OOCMFV:

The OOCMFV bit is a logic one when the CRC multiframe alignment has been lost. The OOCMFV bit becomes a logic zero once CRC multiframe has been regained.

OOOFV:

This bit indicates the current state of the out of offline frame (OOOF) indicator. OOOFV is asserted when the offline framer in the CRC multiframe find procedure is searching for frame alignment.

RAICCRCV:

This bit indicates the current state of the RAI and continuous CRC (RAICCRC) indicator. RAICCRCV is asserted when the remote alarm (A bit) is set high and the CRC error (E bit) is set low for a period of 10 ms.

CFEBEV:

This bit indicates the current state of the continuous FEBE (CFEBE) indicator. CFEBEV is asserted when the CRC error (E bit) is set high on more than 990 occasions in each second (out of 1000 possible occasions) for the last 5 consecutive seconds.

V52LINKV:

This bit indicates the current state of the V5.2 link (V52LINK) identification signal indicator. V52LINKV is asserted if 2 out of the last 3 received Sa7 bits are a logic 0.

Register 0067H+80H*N: E1 FRMR Maintenance/Alarm Status

Bit	Type	Function	Default
Bit 7	R	RAIV	X
Bit 6	R	RMAIV	X
Bit 5	R	AISD	X
Bit 4		Unused	X
Bit 3	R	RED	X
Bit 2	R	AIS	X
Bit 1		Unused	X
Bit 0		Unused	X

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

Reading this register returns the current state value of the RAI, RMAI, AISD, RED, and AIS maintenance/alarm statuses.

RAIV:

The RAIV bit indicates the remote alarm indication (RAI) value. The RAIV bit is set to logic one when the "A" bit (bit 3 in time slot 0 of the non-frame alignment signal frame) has been logic one for an interval specified by the RAIC bit in the E1 FRMR Maintenance Mode Options register. When RACI is logic 1, RAIV is set when A=1 for 4 or more consecutive intervals, and is cleared upon reception of any A=0. When RACI is logic 0, RAI is set upon reception of any A=1, and is cleared upon reception of any A=0. The RAIV output is updated every two frames.

RMAIV:

The RMAIV bit indicates the remote multiframe alarm indication (RMAI) value. The RMAIV bit is set to logic one when the "Y" bit (bit 6 in time slot 16 in frame 0 of the signaling multiframes) has been a logic one for 3 consecutive signaling multiframes, and is cleared upon reception of any Y=0. The RMAIV bit is updated every 16 frames.

AISD:

The AISD bit indicates the alarm indication signal (AIS) detect value. The AISD bit is set to logic one when the incoming data stream has a low zero-bit

density for an interval specified by the AISC bit in the E1 FRMR Maintenance Mode Options register. When AISC is logic 0, AISD is asserted when 512-bit periods have been received with 2 or fewer zeros. The indication is cleared when a 512-bit period is received with 3 or more zeros. When AISC is logic 1, AISD is asserted when two consecutive 512 bit periods have been received with 2 or fewer zeros. The indication is cleared when 2 consecutive 512-bit periods are received, with each period containing 3 or more zeros. The AISD bit is updated once every 512-bit period.

RED:

The RED bit is a logic one if an out of frame condition has persisted for 100 ms. The RED bit returns to a logic zero when a out of frame condition has been absent for 100 ms.

AIS:

The AIS bit is a logic one when an out of frame all-ones condition has persisted for 100 ms. The AIS bit returns to a logic zero when the AIS condition has been absent for 100 ms.

Register 0068H+80H*N: E1 FRMR Timeslot 0 International/National Bits

Bit	Type	Function	Default
Bit 7	R	Si[1]	X
Bit 6	R	Si[0]	X
Bit 5	R	A	X
Bit 4	R	Sa[4]	X
Bit 3	R	Sa[5]	X
Bit 2	R	Sa[6]	X
Bit 1	R	Sa[7]	X
Bit 0	R	Sa[8]	X

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

This register returns the International and National bits from TS0 of incoming frames. The Si[1:0], A and Sa[4:8] bits map to TS0 frames as shown in Table 3.

Table 3 - Timeslot 0 Bit Position Allocation

Frame	1	2	3	4	5	6	7	8
FAS	Si[1]	0	0	1	1	0	1	1
NFAS	Si[0]	1	A	Sa[4]	Sa[5]	Sa[6]	Sa[7]	Sa[8]

Si [1]:

Reading the Si[1] bit returns the International bit in the last received FAS frame. This bit is updated upon generation of the IFPI interrupt on FAS frames.

Si[0]:

Reading the Si[0] bit returns the International bit in the last received NFAS frame. This bit is updated upon generation of the IFPI interrupt on NFAS frames.

A:

Reading the A bit position returns the Remote Alarm Indication (RAI) bit in the last received NFAS frame. This bit is updated upon generation of the IFPI interrupt on NFAS frames.

Sa[4:8]:

Reading these bits returns the National bit values in the last received NFAS frame. This bit is updated upon generation of the IFPI interrupt on NFAS frames.

Register 0069H+80H*N: E1 FRMR CRC Error Counter - LSB

Bit	Type	Function	Default
Bit 7	R	CRCERR[7]	X
Bit 6	R	CRCERR[6]	X
Bit 5	R	CRCERR [5]	X
Bit 4	R	CRCERR [4]	X
Bit 3	R	CRCERR [3]	X
Bit 2	R	CRCERR [2]	X
Bit 1	R	CRCERR [1]	X
Bit 0	R	CRCERR [0]	X

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

CRCERR[7:0]:

The CRCERR[7:0] register bits contain the least significant byte of the 10-bit CRC error counter value, which is updated every second.

Register 006AH+80H*N: E1 FRMR CRC Error Counter – MSB/Timeslot 16 Extra Bits

Bit	Type	Function	Default
Bit 7	R	OVR	0
Bit 6	R	NEWDATA	0
Bit 5	R	X[3]	X
Bit 4	R	Y	X
Bit 3	R	X[1]	X
Bit 2	R	X[0]	X
Bit 1	R	CRCERR [9]	X
Bit 0	R	CRCERR [8]	X

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

This register contains the most significant two bits of the 10-bit CRC error counter value, updated every second.

NEWDATA:

The NEWDATA flag bit indicates that the CRCERR counter register contents have been updated with a new count value accumulated over the last 1 second interval. It is set to logic 1 when the CRC error counter data is transferred into the counter registers, and is reset to logic 0 when this register is read. This bit can be polled to determine the 1 second timing boundary used by the FRMR.

OVR:

The OVR flag bit indicates that the CRCERR counter register contents have not been read within the last 1 second interval, and therefore have been over-written. It is set to logic 1 if CRC error counter data is transferred into the counter registers before the previous data has been read out, and is reset to logic 0 when this register is read.

X[3], Y, X[1], X[0]:

Reading these bits returns the value of the Extra bits (X[3] and X1:0]) and the Remote Signaling Multiframe Alarm bit (Y) in Frame 0, Timeslot 16 of the last received signaling multiframe. These bits are updated upon generation of the

IFPI interrupt on NFAS frames. They map to timeslot 16 as shown in Table 4. Note that the contents of this register are not updated while the E1-FRMR is out of frame.

Table 4 - Signaling Multiframe Timeslot 16, Frame 0 Bit Positions

Bit	1	2	3	4	5	6	7	8
	0	0	0	0	X[3]	Y	X[1]	X[0]

CRCERR[9:8]:

The CRCERR[9:8] register bits contain the two most significant bits of the 10-bit CRC error counter value, which is updated every second.

This CRC error count is distinct from that of PMON because it is guaranteed to be an accurate count of the number of CRC errors in one second; whereas, PMON relies on externally initiated transfers which may not be one second apart.

Register 006BH+80H*N: E1 FRMR National Bit Codeword Interrupt Enables

Bit	Type	Function	Default
Bit 7	R/W	SaSEL[2]	0
Bit 6	R/W	SaSEL[1]	0
Bit 5	R/W	SaSEL[0]	0
Bit 4	R/W	Sa4E	0
Bit 3	R/W	Sa5E	0
Bit 2	R/W	Sa6E	0
Bit 1	R/W	Sa7E	0
Bit 0	R/W	Sa8E	0

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

SaSEL[2:0]:

The SaSEL[2:0] bits selects which National Bit Codeword appears in the SaX[1:4] bits of the National Bit Codeword register. These bits map to the codeword selection as shown in Table 5:

Table 5 - E1 FRMR Codeword Select

SaSEL[2:0]	National Bit Codeword
001	Undefined
010	Undefined
011	Undefined
100	Sa4
101	Sa5
110	Sa6
111	Sa7
000	Sa8

Sa4E, Sa5E, Sa6E, Sa7E, Sa8E:

The National Use interrupt enables allow changes in Sa code word values to generate an interrupt. If SaXE is a logic 1, a logic 1 in the corresponding SaXI bit of the E1 FRMR National Bit Codeword Interrupts register will result in the assertion low of the INTB output.

The interrupt enable must be logic 0 for any bit receiving a HDLC datalink.

Register 006CH+80H*N: E1 FRMR National Bit Codeword Interrupts

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	Sa4I	X
Bit 3	R	Sa5I	X
Bit 2	R	Sa6I	X
Bit 1	R	Sa7I	X
Bit 0	R	Sa8I	X

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

Sa4I, Sa5I, Sa6I, Sa7I, Sa8I:

The National Use interrupt status bits indicate if the debounced version of the individual bits has changed since the last time this register has been read. A logic 1 in one of the bit positions indicates a new nibble codeword is available in the associated SaX[1:4] bits in the National Bit Codeword registers, where N is 4 through 8. If the associated SaXE bit in the E1 FRMR National Bit Interrupt Enables register is a logic 1, a logic 1 in the SaXI results in the assertion of the INTB output.

Register 006DH+80H*N: E1 FRMR National Bit Codeword

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	SaX[1]	X
Bit 2	R	SaX[2]	X
Bit 1	R	SaX[3]	X
Bit 0	R	SaX[4]	X

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

SaX[1:4]:

Reading these bits returns the SaX nibble code word extracted from the submultiframe, where 'X' corresponds to the National bit selected by the SaSEL[2:0] bits in the E1 FRMR National Bit Codeword Interrupt Enables register. SaX[1] is from the first SaX bit of the submultiframe; SaX[4] is from the last. A change in the codeword values sets the SaI[X] bit of the E1 FRMR National Bits Codeword Interrupts register.

Register 006EH+80H*N: E1 FRMR Frame Pulse/Alarm/V5.2 Link ID Interrupt Enables

Bit	Type	Function	Default
Bit 7	R/W	OOOFE	0
Bit 6	R/W	RAICCRCE	0
Bit 5	R/W	CFEBEE	0
Bit 4	R/W	V52LINKE	0
Bit 3	R/W	IFPE	0
Bit 2	R/W	ICSMFPE	0
Bit 1	R/W	ICMFPE	0
Bit 0	R/W	ISMFPE	0

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

OOOFE:

A logic one in the OOOFE bit enables the generation of an interrupt when the out of offline frame interrupt (OOOFI) is asserted.

RAICCRCE:

A logic one in the RAICCRCE bit enables the generation of an interrupt when a RAI and Continuous CRC condition has been detected in the incoming data stream.

CFEBEE:

A logic one in the CFEBEE bit enables the generation of an interrupt when continuous FEBEs have been detected in the incoming data stream.

V52LINKE:

A logic one in the V52LINKE bit enables the generation of an interrupt when a V5.2 link identification has been detected in the Sa7 bits.

IFPE:

The input frame pulse interrupt enable bit allows interrupts to be generated on each basic frame pulse. If IFPE is a logic 1, a logic 1 in the IFPI bit of the Frame Pulse Interrupts register will result in the assertion low of the INTB output.

ICSMFPE:

The input frame pulse interrupt enable bit allows interrupts to be generated on each CRC submultiframe pulse. If ICSMFPE is a logic 1, a logic 1 in the ICSMFPI bit of the Frame Pulse Interrupts register will result in the assertion low of the INTB output.

ICMFPE:

The input frame pulse interrupt enable bit allows interrupts to be generated on each CRC multiframe pulse. If ISMFPE is a logic 1, a logic 1 in the ISMFPI bit of the Frame Pulse Interrupts register will result in the assertion low of the INTB output.

ISMFPE:

The input frame pulse interrupt enable bit allows interrupts to be generated on each signaling multiframe pulse. If ISMFPE is a logic 1, a logic 1 in the ISMFPI bit of the Frame Pulse Interrupts register will result in the assertion low of the INTB output.

Register 006FH+80H*N: E1 FRMR Frame Pulse/Alarm Interrupts

Bit	Type	Function	Default
Bit 7	R	OOOFI	X
Bit 6	R	RAICCRCI	X
Bit 5	R	CFEBEI	X
Bit 4	R	V52LINKI	X
Bit 3	R	IFPI	X
Bit 2	R	ICSMFPI	X
Bit 1	R	ICMFPI	X
Bit 0	R	ISMFPI	X

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

OOOFI:

The OOOFI bit indicates when the out of offline frame indicator (OOOFV) changes state.

RAICCRCI:

The RAICCRCI bit indicates when a RAI and Continuous CRC condition has been detected in the incoming data stream. This interrupt is triggered when the remote alarm (A bit) is set high and the CRC error (E bit) is set low for a period of 10 ms.

CFEBEI:

The CFEBEI bit indicates when continuous FEBEs have been detected in the incoming data stream. This interrupt is triggered when the CRC error (E bit) is set high on more than 990 occasions in each second (out of 1000 possible occasions) for 5 consecutive seconds.

V52LINKI:

V52LINKI indicates when a V5.2 link identification signal has been detected or lost in the Sa7 bits. This bit will toggle any time the V52LINKV bit changes state.

IFPI:

The input frame pulse interrupt status bit is asserted at timeslot 1, bit position 1 of the frame in the incoming data stream.

ICSMFPI:

The input CRC submultiframe alignment frame pulse interrupt status bit is asserted at timeslot 1, bit position 1 of frame 0 of the CRC submultiframe in the incoming data stream.

ICMFPI:

The input CRC multiframe alignment frame pulse interrupt status bit is asserted at timeslot 1, bit position 1 of frame 0 of the CRC multiframe in the incoming data stream.

ISMFPI:

The input signaling multiframe alignment frame pulse interrupt status bit is asserted at timeslot 17, bit position 1 of frame 0 of the signaling multiframe in the incoming data stream.

1.10 DS3/M13 Master Registers

Register 1000H: DS3 Master Reset

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	PMONRST	0
Bit 0	R/W	RESET	0

RESET:

The RESET bit allows software to hold DS3 M13 Mux in a reset condition. When RESET is a logic 1 the DS3 M13 multiplexer block will be held in a reset state which is also a low power state. This will force all registers to their default state. While in reset the clocks can not be guaranteed accurate or existing. When RESET is a logic 0 the DS3 M13 multiplexer block is in normal operating mode.

PMONRST:

The performance monitor reset bit, PMONRST, forces the PMON block into reset. When PMONRST is a logic 1 the PMON block will be held in a reset state. When PMONRST is a logic 0 the PMON block is in normal operating mode.

Register 1001H: DS3 Master Data Source

Bit	Type	Function	Default
Bit 7	R/W	PLOOP	0
Bit 6	R/W	DLOOP	0
Bit 5	R/W	LLOOP	0
Bit 4	R/W	LOOPT	0
Bit 3	R/W	DLINV	0
Bit 2	R/W	SBICLKMODE	0
Bit 1	R/W	RCVCLR	0
Bit 0		Unused	X

RCVCLR:

The DS3 clear channel bit, RCVCLR, bypasses the DS3 TRAN which selects clear channel DS3 data to be accessed over the SBI bus or the DS3 system interface when the TEMAP is configured for DS3 framer only mode. When RCVCLR is a logic 1 a clear channel DS3 is transmitted from the SBI bus or DS3 system interface. When RCVCLR is a logic 0 the DS3 payload is accessed from the SBI bus or DS3 system interface and DS3 framing is inserted by the TEMAP. This should only be set when the TEMAP is configured for DS3 framer only mode via the Global Configuration register.

SBICLKMODE:

The SBI clock mode bit, SBICLKMODE, selects the egress clocking mode used over the SBI bus. When SBICLKMODE is a logic 1 and the TEMAP is configured for DS3 framer only mode over the SBI system interface via the Global Configuration register, the TEMAP is the egress clock master and the egress clock will be TICLK. When SBICLKMODE is a logic 0 and the TEMAP is configured for DS3 framer only mode over the SBI system interface, the TEMAP is slave to the DS3 clock from the SBI bus. The CLK_MSTR bit for TRIB_TYP[1] in the EXSBI Tributary Control Indirect Access Data must be set to match the setting of SBICLKMODE.

Please note that this bit must be set before any SBI tributary is enabled and must only be changed when tributaries are disabled.

DLINV:

The DLINV bit provides polarity control for the DS3 C-bit Parity path maintenance data link which is located in the 3 C-bits of M-subframe 5. When a logic 1 is written to DLINV, the path maintenance data link is inverted before being processed. The rationale behind this bit is as follows: currently ANSI standard T1.107 specifies that the C-bits (which carry the path maintenance data link) be set to all zeros while the AIS maintenance signal is transmitted. The data link is obviously inactive during AIS transmission, and ideally the HDLC idle sequence (all ones) should be transmitted. By inverting the data link, the all zeros C-bit pattern becomes an idle sequence and the data link is terminated gracefully. Although this inversion is currently not specified in ANSI T1.107a, this bit is provided to safe-guard the TEMAP in case the inversion is required in the future.

LOOPT:

The Transmit Timing Source Select bit selects the transmit timing source. When a logic 1 is written to LOOPT, the transmitter is loop-timed to the receiver. When loop timing is enabled, the receive clock RCLK is used as the transmit timing source. When a logic 0 is written to LOOPT, the transmit clock TICLK is used as the transmit timing source. Setting the LOOPT bit disables the effect of the TICLK bit.

When operating in DS3 Framer Only mode over the SBI bus, LOOPT does not disable TICLK as the reference timing to the SBI bus. If looptiming in DS3 framer mode is required when using the SBI bus, the receive clock from the external phase lock loop (required for de-jittering) should be multiplexed into the TICLK input and used as the reference for TEMAP in this mode.

LLOOP:

The LLOOP bit controls the line loopback. When a logic 0 is written to LLOOP, line loopback is disabled. When a logic 1 is written to LLOOP, the stream received on RPOS/RDAT and RNEG/RLCV is looped to the TPOS/TDAT and TNEG/TMFP outputs. Note that the TPOS, TNEG, and TCLK outputs are referenced to RCLK when LLOOP is logic 1.

DLOOP:

The DLOOP bit controls the diagnostic loopback. When a logic 0 is written to DLOOP, diagnostic loopback is disabled. When a logic 1 is written to DLOOP, the transmit data stream is looped in the receive direction. The DLOOP must not be set to a logic 1 when either the PLOOP, LLOOP, or LOOPT bit is a logic 1. The TUNI register bit in the DS3 Transmit Line

Options register must be set to the same value as the UNI bit in the DS3 FRMR register.

PLOOP:

The PLOOP bit controls the DS3 payload loopback. When a logic 0 is written to PLOOP, DS3 payload loopback is disabled. When a logic 1 is written to PLOOP, the DS3 overhead bits are regenerated and inserted into the received DS3 stream and the resulting stream is transmitted. Setting the PLOOP bit disables the effect of the TICLK bit in the DS3 Transmit Line Options register, thereby forcing flow-through timing. TXGAPEN in Register 1002H must be set to logic 0 when payload loopback is enabled.

It is possible to inadvertently generate C-Bit parity errors in DS3 Payload loopback mode by the way its operation is sequenced. When configuring for DS3 framer mode before payload loopback, C-Bit parity errors can occur. To avoid this, configure the TEMAP for payload loopback before configuring for DS3 framer only mode.

Register 1002H: DS3 Master Unchannelized Interface Options

Bit	Type	Function	Default
Bit 7	R/W	TDATIFALL	0
Bit 6	R/W	TXGAPEN	0
Bit 5	R/W	TXMFPO	0
Bit 4	R/W	TXMFPI	0
Bit 3		Unused	X
Bit 2	R/W	RXMFPO	0
Bit 1	R/W	RXGAPEN	0
Bit 0	R/W	RSCLKR	0

This register controls the framer only system side interface for unchannelized DS3 operation.

RSCLKR:

The RSCLKR bit has effect only when DS3 framer only mode is selected in the Global Configuration register. When RSCLKR is a logic 1, the RDATO, RMFPO, and ROVRHD outputs are updated on the rising edge of RSCLK. When RSCLKR is a logic 0, the RDATO, RMFPO, and ROVRHD outputs are updated on the falling edge of RSCLK. If the RXGAPEN bit is a logic 1, then RSCLKR affects RGAPCLK in the same manner as it affects RSCLK.

RXGAPEN:

The RXGAPEN bit configures the TEMAP to enable the RGAPCLK outputs. When RXGAPEN is a logic 1, then the RGAPCLK output is enabled. When RXGAPEN is a logic 0, then the RSCLK output is enabled. DS3 framer only mode must be selected in the Global Configuration register for RXGAPEN to have affect.

RXMFPO:

The RXMFPO bit controls which of the outputs RMFPO or RFPO is valid. If RXMFPO is a logic 1, then RMFPO will be available. If RXMFPO is a logic 0, then RFPO will be available. This bit has effect only if DS3 framer only mode is selected in the Global Configuration register.

When using the SBI bus in DS3-framer-only mode, RXMFPO must be programmed to 1.

TXMFPI:

The TXMFPI bit controls which of the inputs TMFPI or TFPI is valid. If TXMFPI is a logic 1, then TMFPI will be expected. If TXMFPI is a logic 0, then TFPI will be expected. This bit has effect only if DS3 framer only mode is selected in the Global Configuration register.

When using the SBI bus in DS3-framer-only mode, TXMFPI must be programmed to 1.

TXMFPO:

The TXMFPO bit controls which of the outputs TMFPO or TFPO is valid. If TXMFPO is a logic 1, then TMFPO will be available. If TXMFPO is a logic 0, then TFPO will be available. This bit has effect only if DS3 framer only mode is selected in the Global Configuration register and the TXGAPEN bit is a logic 0.

TXGAPEN:

The TXGAPEN bit configures the TEMAP to enable the TGAPCLK output. When TXGAPEN is a logic 1, then the TGAPCLK output is enabled. When TXGAPEN is a logic 0, then either the TFPO or TMFPO output is enabled, depending on the setting of the TXMFPO register bit. DS3 framer only mode must be selected in the Global Configuration register for TXGAPEN to have affect.

TDATIFALL:

The TDATIFALL bit configures the sampling edge of the DS3 framer transmit data signal, TDATI, the sampling edge of the framer transmit framing pulse input signal TFPI/TMFPI and the updating edge of the framer transmit framing pulse output signal TFPO/TMFPO. When TDATIFALL is a logic 1, TDATI and TFPI/TMFPI will be sampled on the falling edge of TICLK when TXGAPEN is a logic zero, and will be sampled on the falling edge of TGAPCLK when TXGAPEN is a logic 1. When TDATIFALL is a logic 0, TDATI and TFPI/TMFPI will be sampled on the rising edge of either TICLK or TGAPCLK. TFPO/TMFPO will be updated on the falling edge of TICLK when TDATIFALL is a logic 0 and on the rising edge when TDATIFALL is a logic 1.

Register 1003H: DS3 Master Transmit Line Options

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	PRGD_EN	0
Bit 4	R/W	TICLK	0
Bit 3	R/W	TNEGINV	0
Bit 2	R/W	TPOSINV	0
Bit 1	R/W	TRISE	0
Bit 0	R/W	TUNI	0

TICLK:

The Transmit Clocking Select bit selects the transmit clock used to update the TPOS/TDAT and TNEG/TMFP outputs. When a logic 0 is written to TICLK, the buffered version of the input transmit clock, TCLK, is used to update TPOS/TDAT and TNEG/TMFP on the edge selected by the TRISE bit. When a logic 1 is written to TICLK, TPOS/TDAT and TNEG/TMFP are updated by TICLK on the edge selected by the TRISE bit, eliminating the flow-through TCLK signal. The TICLK bit has no effect if the LOOPT bit in the DS3 Master Data Source register is a logic 1.

TNEGINV:

The TNEGINV bit provides polarity control for outputs TNEG/TMFP. When a logic 0 is written to TNEGINV, the TNEG/ TMFP output is not inverted. When a logic 1 is written to TNEGINV, the TNEG/ TMFP output is inverted. The TNEGINV bit setting does not affect the loopback data in diagnostic loopback.
TNEGINV must be a logic 0 when mapping the DS3 signal into the SONET/SDH line interface through the D3MA block.

TPOSINV:

The TPOSINV bit provides polarity control for outputs TPOS/TDAT. When a logic 0 is written to TPOSINV , the TPOS/TDAT output is not inverted. When a logic 1 is written to TPOSINV , the TPOS/TDAT output is inverted. The TPOSINV bit setting does not affect the loopback data in diagnostic loopback. TPOSINV must be a logic 0 when mapping the DS3 signal into the SONET/SDH line interface through the D3MA block.

TRISE:

The TRISE bit provides clock edge control for the outputs TPOS/TDAT and TNEG/TMFP. When a logic 0 is written to TRISE, TPOS/TDAT and TNEG/TMFP are updated on the falling edge of TCLK or TICLK as selected by the TICLK bit. When a logic 1 is written to TRISE, TPOS/TDAT and TNEG/TMFP are updated on the rising edge of TCLK or TICLK.
TRISE must be a logic 0 when mapping the DS3 signal into the SONET/SDH line interface through the D3MA block.

TUNI:

The transmit unipolar bit configures the DS3 transmit interface for unipolar or dual rail operation. When TUNI is a logic 1, the transmit interface is configured as TDAT and TMFP. When TUNI is a logic 0, the transmit interface is configured as TPOS and TNEG.
TUNI must be a logic 1 when mapping the DS3 signal into the SONET/SDH line interface through the D3MA block.

PRGD_EN:

The PRGD enable bit, PRGD_EN, controls the insertion of the PRGD pattern generator in the transmit DS3 path. When PRGD_EN is a logic 1 the PRGD pattern is inserted in the transmit DS3 payload and will overwrite everything except the DS3 framing bits. When PRGD_EN is a logic 0 the PRGD pattern generator is removed from the transmit path.

Register 1004H: DS3 Master Receive Line Options

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	RNEGINV	0
Bit 1	R/W	RPOSINV	0
Bit 0	R/W	RFALL	0

RNEGINV:

The RNEGINV bit provides polarity control for input RNEG/RLCV. When a logic 0 is written to RNEGINV, the input RNEG/RLCV is not inverted. When a logic 1 is written to RNEGINV, the input RNEG/RLCV is inverted. The RNEGINV bit setting does not affect the loopback data in diagnostic loopback.
RNEGINV must be a logic 0 when demapping the DS3 signal from the SONET/SDH line interface through the D3MD block.

RPOSINV:

The RPOSINV bit provides polarity control for input RPOS/RDAT. When a logic 0 is written to RPOSINV , the input RPOS/RDAT is not inverted. When a logic 1 is written to RPOSINV , the input RPOS/RDAT is inverted. The RPOSINV bit setting does not affect the loopback data in diagnostic loopback.
RPOSINV must be a logic 0 when demapping the DS3 signal from the SONET/SDH line interface through the D3MD block.

RFALL:

The RFALL bit provides polarity control for input RCLK. When a logic 0 is written to RFALL, RPOS/RDAT and RNEG/RLCV are sampled on the rising edge of RCLK. When a logic 1 is written to RFALL, RPOS/RDAT and RNEG/RLCV are sampled on the falling edge of RCLK.
RFALL must be a logic 0 when demapping the DS3 signal from the SONET/SDH line interface through the D3MD block.

Register 1005H: DS3 Master Alarm Enable

Bit	Type	Function	Default
Bit 7	R/W	FEBEEN	0
Bit 6	R/W	ALTFEBE	0
Bit 5	R/W	DS3REDEN	0
Bit 4	R/W	DS3AISEN	0
Bit 3	R/W	DS3OOFEN	0
Bit 2	R/W	DS3LOSEN	0
Bit 1	R/W	RED3ALME	0
Bit 0	R/W	DS3ALME	0

FEBEEN:

The Far End Block Error Enable bit enables the automatic generation of the transmit DS3 FEBE during all receive frame conditions. When FEBEEN is a logic 1, a FEBE will be generated in the C-bit Parity DS3 transmit stream during a receive OOF condition. When FEBEEN is a logic 0, transmit FEBE indications will not be generated during receive OOF.

ALTFEBE:

The Alternate Far End Block Error bit selects the error conditions detected to define a FEBE indication. If ALTFEBE is a logic 1, a FEBE indication is generated if either one or more framing bit errors or a C-bit parity error has occurred in the last received M-frame. If no framing bit errors nor C-bit parity errors have occurred, then no FEBE is generated. If ALTFEBE is a logic 0, a FEBE indication is generated in the outgoing C-bit Parity DS3 transmit stream if a C-bit parity error occurred in the last received M-frame. If no C-bit parity error occurred, no FEBE is generated.

DS3REDEN:

The DS3REDEN bit enables the receive RED alarm (persistent out of frame) indication to automatically generate a FERF indication in the DS3 transmit stream. When DS3REDEN is logic 1, assertion of the RED indication by the DS3 framer causes a FERF to be transmitted by DS3 transmitter for the duration of the RED assertion. Also the DS3OOFEN bit is internally forced to logic 0 when DS3REDEN is logic 1. When DS3REDEN is logic 0, assertion of the RED indication does not cause transmission of a FERF.

DS3AISEN:

The DS3AISEN bit enables the receive alarm indication signal to automatically generate a FERF indication in the DS3 transmit stream. When DS3AISEN is logic 1, assertion of the AIS indication by the DS3 framer causes a FERF to be transmitted by TRAN for the duration of the AIS assertion. When DS3AISEN is logic 0, assertion of the AIS indication does not cause transmission of a FERF.

DS3OOFEN:

The DS3OOFEN bit enables the receive out of frame indication to automatically generate a FERF indication in the DS3 transmit stream. This bit only operates when the DS3REDEN bit is logic 0. When DS3OOFEN is logic 1, assertion of the OOF indication by the framer causes a FERF to be transmitted by TRAN for the duration of the OOF assertion. When DS3OOFEN is logic 0, assertion of the OOF indication does not cause transmission of a FERF.

DS3LOSEN:

The DS3LOSEN bit enables the receive loss of signal indication to automatically generate a FERF in the DS3 transmit stream. When DS3LOSEN is logic 1, assertion of the LOS indication by the DS3 framer causes a FERF to be transmitted by TRAN for the duration of the LOS assertion. When LOSEN is logic 0, assertion of the LOS indication does not cause transmission of a FERF.

RED3ALME:

The RED DS3 Alarm Enable bit works in conjunction with the DS3ALME and enables detection of DS3 RED condition to be used in place of DS3 loss of signal and DS3 out-of-frame in the above criteria for demultiplexed AIS generation. When DS3ALME is set to logic 1 and REDALME is set to logic 1, the occurrence of LOS or OOF for 127 consecutive M-frames (or 21 consecutive M-frames, if FDET is set to logic 1 in the DS3 FRMR configuration register) causes a DS3 RED alarm condition and generates the DS2 AIS. When DS3ALME is set to logic 1 and REDALME is set to logic 0, any occurrence of LOS or OOF generates the DS2 AIS. If DS3ALME is a logic 0, the REDALME bit is ignored.

DS3ALME:

The DS3 Alarm Enable bit allows the automatic generation of AIS in all of the demultiplexed DS2s upon a DS3 alarm condition. If DS3ALME is a logic 1, a DS3 loss of signal (>175 zeros), a DS3 out-of-frame (OOF) condition (i.e. immediately after 3-of-n F-bit errors where n is 8 or 16, or 3-of-4 M-frames containing M-bit errors), DS3 idle code detection or DS3 AIS detection

causes all of the DS2s to be replaced by an unframed all ones pattern immediately. Generation of AIS continues while the detected alarm condition persists. If DS3ALME is a logic 0, AIS can still be generated in the demultiplexed DS2s under software control by setting the bits in the MX23 Demux AIS Insert Register.

In DS3 framer only mode, a DS3 AIS will be generated in the ingress path when DS3ALME is set to logic 1 and an OOF or LOF alarm occurs.

Register 1006H: DS2 Master Alarm Enable / DS3 Network Requirement Bit

Bit	Type	Function	Default
Bit 7	R/W	TNR	1
Bit 6	R	RNR	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	RED2ALME	0
Bit 0	R/W	DS2ALME	0

TNR:

The Transmit Network Requirement (TNR) bit determines the value inserted into the Network Requirement (N_r) bit transmitted in the second C-bit in M-subframe 1 when in DS3 C-bit parity mode. A logic 1 in the TNR bit causes a one to be transmitted in the N_r overhead bit timeslot. The TNR bit is set to a logic 1 upon either a hardware or software reset. If C-bit parity is not selected, the TNR bit has no effect.

When the TEMAP is set for transmission of DS3 AIS via the DS3 TRAN Configuration register Bit 6 in C-bit parity mode, all C-bits are forced to 0 except for the network requirement bit which is forced to the TNR register bit value. The TNR bit must be cleared when TRAN is enabled to generate AIS in C-bit parity mode.

RNR:

The Receive Network Requirement bit reflects the real time value of the Network Requirement (N_r) bit presented in the second C-bit in M-subframe 1 when in DS3 C-bit parity mode. The RNR bit is a logic 1 if a logic one occurs in the N_r overhead bit timeslot. If C-bit parity is not selected, the value of RNR is meaningless and random.

RED2ALME:

The RED DS2 Alarm Enable (RED2ALME) bit works in conjunction with the DS2ALME and enables detection of DS2 RED condition to be used in place of DS2/G.747 out-of-frame in the above criteria for demultiplexed AIS generation. When DS2ALME is set to logic 1 and RED2ALME is set to logic 1, the occurrence of OOF for 53 consecutive DS2/G.747 "M-frames" causes a

DS2 RED alarm condition and generates the DS1 AIS. When DS2ALME is set to logic 1 and RED2ALME is set to logic 0, any occurrence of OOF generates the DS1 AIS. If DS2ALME is a logic 0, the RED2ALME bit is ignored.

DS2ALME:

The DS2 Alarm Enable (DS2ALME) bit allows the automatic generation of AIS in the DS1s demultiplexed from a DS2 or G.747 stream which is in an alarm condition. If DS2ALME is a logic 1,a DS2 or G.747 out-of-frame (OOF) condition (i.e. immediately after 2-of-n F-bit errors where n is 4 or 5, or 3-of-4 M-frames containing M-bit errors for DS2, or immediately after 4 consecutive framing word errors for G.747) or detection of DS2 or G.747 AIS causes each of the associated DS1s to be replaced by an unframed all ones pattern immediately. If DS2ALME is a logic 0, AIS can still be generated in the demultiplexed DS1s under software control by setting the bits in the appropriate MX12 AIS Insert Register. Note that the removal of the auto all-ones insertion is performed upon the first DS2 M-frame or G.747 frame pulse after the DS2 FRMR has found frame alignment.

1.11 DS3 TRAN Transmitter Registers

Register 1008H: DS3 TRAN Configuration

Bit	Type	Function	Default
Bit 7	R/W	CBTRAN	0
Bit 6	R/W	AIS	0
Bit 5	R/W	IDL	0
Bit 4	R/W	FERF	0
Bit 3	R/W	Reserved	0
Bit 2		Unused	X
Bit 1	R/W	TSIG	0
Bit 0	R/W	CBIT	0

CBIT:

The CBIT bit enables the DS3 C-bit parity application. When CBIT is written with a logic 1, C-bit parity is enabled, and the TEMAP modifies the C-bits as required to include the path maintenance data link, the FEAC channel, the far end block error indication, and the path parity. When CBIT is written with a logic 0, the M23 application is selected, and the C-bits are passed transparently through the DS3 TRAN.

TSIG:

The TSIG bit forces a 100… pattern on TDAT, or the corresponding encoded 100… signal on the B3ZS outputs, TPOS and TNEG. The test signal is inserted when TSIG is logic 1, and disabled when TSIG is logic 0. The signal insertion is provided for test purposes, and will overwrite any input data stream. The signal provides a minimum number of transitions on the encoded B3ZS output signal to allow pulse mask testing.

FERF:

The FERF bit enables insertion of the far end receive failure maintenance signal in the DS3 stream. When FERF is written with a logic 1, the X1 and X2 overhead bit positions are set to logic 0. When FERF is written with a logic 0, the X1 and X2 overhead bit positions in the DS3 stream are set to logic 1.

IDL:

The IDL bit enables the transmission of the DS3 Idle signal. When IDL is logic 1, the incoming DS3 data stream is overwritten with the pattern 1100… When CBTRAN is logic 0 and IDL is logic 1, the C-bits in the third M-subframe are set to 0. When CBTRAN is logic 1, all C-bits are passed transparently.

AIS:

The AIS bit enables the transmission of the DS3 alarm indication signal. When AIS is logic 1, the incoming DS3 data stream is overwritten with the pattern 1010... When CBTRAN is logic 0 and AIS is logic 1, the C-bits are all set to 0 with the exception of the network requirement bit which is forced to the TNR register bit value. When CBTRAN is logic 1, all C-bits are passed transparently.

CBTRAN:

The CBTRAN bit controls the C-bits during AIS and IDLE transmission. When CBTRAN is a logic 0, the C-bits are overwritten with zeros during AIS transmission (as is currently specified in ANSI T1.107a Section 8.1.3.1). The only exception is the network requirement bit in C-bit parity mode, which is forced to the TNR register bit value as specified in the DS3 Network Requirement Bit register. During IDLE transmission and CBTRAN is a logic 0 the C-bits in the third M-subframe are overwritten with zeros. When CBTRAN is a logic 1 and the M23 application is enabled, the C-bits pass through transparently during AIS and IDLE transmission. When CBTRAN is a logic 1, and the C-bit parity application is enabled, the C-bits are overwritten with the appropriate C-bit parity functions during AIS and IDLE transmission.

Reserved:

The reserved bit must be programmed to logic 0 for proper operation.

Register 1009H: DS3 TRAN Diagnostic

Bit	Type	Function	Default
Bit 7	R/W	DLOS	0
Bit 6	R/W	DLCV	0
Bit 5		Unused	X
Bit 4	R/W	DFERR	0
Bit 3	R/W	DMERR	0
Bit 2	R/W	DCPERR	0
Bit 1	R/W	DPERR	0
Bit 0	R/W	DFEBE	0

DFEBE:

The DFEBE bit controls the insertion of far end block errors in the DS3 stream. When DFEBE is written with a logic 1, and the C-bit parity application is enabled, the three C-bits in M-subframe 4 are set to a logic 0. When DFEBE is written with a logic 0, FEBEs are indicated based on receive framing bit errors and path parity errors.

DPERR:

The DPERR bit controls the insertion of parity errors (P-bit errors) in the DS3 stream. When DPERR is written with a logic 1, the P-bits are inverted before insertion. When DPERR is written with a logic 0, the parity is calculated and inserted normally.

DCPERR:

The DCPERR bit controls the insertion of path parity errors in the DS3 stream. When DCPERR is written with a logic 1 and the C-bit parity application is enabled, the three C-bits in M-subframe 3 are inverted before insertion. When DCPERR is written with a logic 0, the path parity is calculated and inserted normally.

DMERR:

The DMERR bit controls the insertion of M-bit framing errors in the DS3 stream. When DMERR is written with a logic 1, the M-bits are inverted before insertion. When DMERR is written with a logic 0, the M-bits are inserted normally.

DFERR:

The DFERR bit controls the insertion of F-bit framing errors in the DS3 stream. When DFERR is written with a logic 1, the F-bits are inverted before insertion. When DFERR is written with a logic 0, the F-bits are inserted normally.

DLCV:

The DLCV bit controls the insertion of a single line code violation in the DS3 stream. When DLCV is written with a logic 1, a line code violation is inserted by generating an incorrect polarity of violation in the next B3ZS signature. The data being transmitted must therefore contain periods of three consecutive zeros in order for the line code violation to be inserted. For example, line code violations may not be inserted when transmitting AIS, but may be inserted when transmitting the idle signal. DLCV is automatically cleared upon insertion of the line code violation.

DLOS:

The DLOS bit controls the insertion of loss of signal in the DS3 stream. When DLOS is written with a logic 1, the data on outputs TPOS/TDAT and TNEG/TMFP is forced to continuous zeros.

1.12 DS3 FRMR Receive Framer Registers

Register 100CH: DS3 FRMR Configuration

Bit	Type	Function	Default
Bit 7	R/W	AISPAT	1
Bit 6	R/W	FDET	0
Bit 5	R/W	MBDIS	0
Bit 4	R/W	M3O8	0
Bit 3	R/W	UNI	0
Bit 2	R/W	REFR	0
Bit 1	R/W	AISC	0
Bit 0	R/W	CBE	0

CBE:

The CBE bit enables the DS3 C-bit parity application. When a logic 1 is written to CBE, C-bit parity mode is enabled. When a logic 0 is written to CBE, the DS3 M23 format is selected. While the C-bit parity application is enabled, C-bit parity error events, far end block errors are accumulated.

AISC:

The AISC bit controls the algorithm used to detect the alarm indication signal (AIS). When a logic 1 is written to AISC, the algorithm checks that a framed DS3 signal with all C-bits set to logic 0 is observed for a period of time before declaring AIS. The payload contents are checked to the pattern selected by the AISPAT bit. When a logic 0 is written to AISC, the AIS detection algorithm is determined solely by the settings of AISPAT and AISONES register bits (see bit mapping table in the Additional Configuration Register description).

REFR:

The REFR bit initiates a DS3 reframe. When a logic 1 is written to REFR, the TEMAP is forced out-of-frame, and a new search for frame alignment is initiated. Note that only a low to high transition of the REFR bit triggers reframing; multiple write operations are required to ensure such a transition.

UNI:

The UNI bit configures the TEMAP to accept either dual-rail or single-rail receive DS3 streams. When a logic 1 is written to UNI, the TEMAP accepts a single-rail DS3 stream on RDAT. The TEMAP accumulates line code violations on the RLCV input. When a logic 0 is written to UNI, the TEMAP accepts B3ZS-encoded dual-rail data on RPOS and RNEG. UNI must be set to a logic 1 when demapping the DS3 signal from the SONET/SDH interface through the D3MD block.

M3O8:

The M3O8 bit controls the DS3 out of frame decision criteria. When a logic 1 is written to M3O8, DS3 out of frame is declared when 3 of 8 framing bits (F-bits) are in error. When a logic 0 is written to M3O8, the 3 of 16 framing bits in error criteria is used, as recommended in ANSI T1.107

MBDIS:

The MBDIS bit disables the use of M-bit errors as a criteria for losing frame alignment. When MBDIS is set to logic 1, M-bit errors are disabled from causing an OOF; the loss of frame criteria is based solely on the number of F-bit errors selected by the M3O8 bit. When MBDIS is set to logic 0, errors in either M-bits or F-bits are enabled to cause an OOF. When MBDIS is logic 0, an OOF can occur when one or more M-bit errors occur in 3 out of 4 consecutive M-frames, or when the F-bit error ratio selected by the M3O8 bit is exceeded.

FDET:

The FDET bit selects the fast detection timing for AIS, IDLE and RED. When FDET is set to logic 1, the AIS, IDLE, and RED detection time is 2.23 ms; when FDET is set to logic 0, the detection time is 13.5 ms.

AISPAT:

The AISPAT bit controls the pattern used to detect the alarm indication signal (AIS). When a logic 1 is written to AISPAT, the AIS detection algorithm checks that a framed DS3 signal containing the repeating pattern 1010... is present. The C-bits are checked for the value specified by the AISC bit setting. When a logic 0 is written to AISPAT, the AIS detection algorithm is determined solely by the settings of AISC and AISONES register bits (see bit mapping table in the Additional Configuration Register description).

Register 100DH: DS3 FRMR Interrupt Enable (ACE=0)

Bit	Type	Function	Default
Bit 7	R/W	COFAE	0
Bit 6	R/W	REDE	0
Bit 5	R/W	CBITE	0
Bit 4	R/W	FERFE	0
Bit 3	R/W	IDLE	0
Bit 2	R/W	AISE	0
Bit 1	R/W	OOFE	0
Bit 0	R/W	LOSE	0

LOSE:

The LOSE bit enables interrupt generation when a DS3 loss of signal defect is declared or removed. The interrupt is enabled when a logic 1 is written.

OOFE:

The OOFE bit enables interrupt generation when a DS3 out of frame defect is declared or removed. The interrupt is enabled when a logic 1 is written.

AISE:

The AISE bit enables interrupt generation when the DS3 AIS maintenance signal is detected or removed. The interrupt is enabled when a logic 1 is written.

IDLE:

The IDLE bit enables interrupt generation when the DS3 IDLE maintenance signal is detected or removed. The interrupt is enabled when a logic 1 is written.

FERFE:

The FERFE bit enables interrupt generation when a DS3 far end receive failure defect is declared or removed. The interrupt is enabled when a logic 1 is written.

CBITE:

The CBITE bit enables interrupt generation when the TEMAP detects a change of state in the DS3 application identification channel. The interrupt is enabled when a logic 1 is written.

REDE:

The REDE bit enables an interrupt to be generated when a change of state of the DS3 RED indication occurs. The DS3 RED indication is visible in the REDV bit location of the DS3 FRMR Status register. When REDE is set to logic 1, the interrupt output, INTB, is set low when the state of the RED indication changes.

COFAE:

The COFAE bit enables interrupt generation when the TEMAP detects a DS3 change of frame alignment. The interrupt is enabled when a logic 1 is written.

Register 100DH: DS3 FRMR Additional Configuration (ACE=1)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	AISONES	0
Bit 4	R/W	BPVO	0
Bit 3	R/W	EXZSO	0
Bit 2	R/W	EXZDET	0
Bit 1	R/W	SALGO	0
Bit 0	R/W	DALGO	0

DALGO:

The DALGO bit determines the criteria used to decode a valid B3ZS signature. When DALGO is set to logic 1, a valid B3ZS signature is declared and 3 zeros substituted whenever a zero followed by a bipolar violation of the opposite polarity to the last observed BPV is seen. When the DALGO bit is set to logic 0, a valid B3ZS signature is declared and the 3 zeros are substituted whenever a zero followed by a bipolar violation is observed.

SALGO:

The SALGO bit determines the criteria used to establish a valid B3ZS signature used to map BPVs to line code violation indications. Any BPV that is not part of a valid B3ZS signature is indicated as an LCV. When the SALGO bit is set to logic 1, a valid B3ZS signature is declared whenever a zero followed by a bipolar violation is observed. When SALGO is set to logic 0, a valid B3ZS signature is declared whenever a zero followed by a bipolar violation of the opposite polarity to the last observed BPV is seen.

EXZDET:

The EXZDET bit determines the type of zero occurrences to be included in the LCV indication. When EXZDET is set to logic 1, the occurrence of an excessive zero generates a single pulse indication that is used to indicate an LCV. When EXZDET is set to logic 0, every occurrence of 3 consecutive zeros generates a pulse indication that is used to indicate an LCV. For example, if a sequence of 15 consecutive zeros were received, with EXZDET=1 only a single LCV would be indicated for this string of excessive

zeros; with EXZDET=0, five LCVs would be indicated for this string (i.e. one LCV for every 3 consecutive zeros).

EXZSO:

The EXZSO bit enables only summed zero occurrences to be accumulated in the PMON EXZS Count Registers. When EXZSO is set to logic 1, any excessive zeros occurrences over an 85 bit period increments the PMON EXZS counter by one. When EXZSO is set to logic 0, summed LCVs are accumulated in the PMON EXZS Count Registers. A summed LCV is defined as the occurrence of either BPVs not part of a valid B3ZS signature or 3 consecutive zeros (or excessive zeros if EXZDET=1) occurring over an 85 bit period; each summed LCV occurrence increment the PMON EXZS counter by one.

BPVO:

The BPVO bit enables only bipolar violations to indicate line code violations and be accumulated in the PMON LCV Count Registers. When BPVO is set to logic 1, only BPVs not part of a valid B3ZS signature generate an LCV indication and increment the PMON LCV counter. When BPVO is set to logic 0, both BPVs not part of a valid B3ZS signature, and either 3 consecutive zeros or excessive zeros generate an LCV indication and increment the PMON LCV counter.

AISONES:

The AISONES bit controls the pattern used to detect the alarm indication signal (AIS) when both AISPAT and AISC bits in DS3 FRMR Configuration register are logic 0; if either AISPAT or AISC are logic 1, the AISONES bit is ignored. When a logic 0 is written to AISONES, the algorithm checks that a framed all-ones payload pattern (1111...) signal is observed for a period of time before declaring AIS. Only the payload bits are observed to follow an all-ones pattern, the overhead bits (X, P, M, F, C) are ignored. When a logic 1 is written to AISONES, the algorithm checks that an unframed all-ones pattern (1111...) signal is observed for a period of time before declaring AIS. In this case all the bits, including the overhead, are observed to follow an all-ones pattern. The valid combinations of AISPAT, AISC, and AISONES bits are summarized below:

AISPAT	AISC	AISONES	AIS Detected
1	0	X	Framed DS3 stream containing repeating 1010… pattern; overhead bits ignored.

0	1	X	Framed DS3 stream containing C-bits all logic 0; payload bits ignored.
1	1	X	Framed DS3 stream containing repeating 1010… pattern and C-bits all logic 0.
0	0	0	Framed DS3 stream containing all-ones payload pattern; overhead bits ignored.
0	0	1	Unframed all-ones DS3 stream.

Register 100EH: DS3 FRMR Interrupt Status

Bit	Type	Function	Default
Bit 7	R	COFAI	X
Bit 6	R	REDI	X
Bit 5	R	CBITI	X
Bit 4	R	FERFI	X
Bit 3	R	IDLI	X
Bit 2	R	AISI	X
Bit 1	R	OOFI	X
Bit 0	R	LOSI	X

LOSI:

The LOSI bit is set to logic 1 when a loss of signal defect is detected or removed. The LOSI bit position is set to logic 0 when this register is read.

OOFI:

The OOFI bit is set to logic 1 when an out of frame defect is detected or removed. The OOFI bit position is set to logic 0 when this register is read.

AISI:

The AISI bit is set to logic 1 when the DS3 AIS maintenance signal is detected or removed. The AISI bit position is set to logic 0 when this register is read.

IDLI:

The IDLI bit is set to logic 1 when the DS3 IDLE maintenance signal is detected or removed. The IDLI bit position is set to logic 0 when this register is read.

FERFI:

The FERFI bit is set to logic 1 when a FERF defect is detected or removed. The FERFI bit position is set to logic 0 when this register is read.

CBITI:

The CBITI bit is set to logic 1 when a change of state is detected in the DS3 application identification channel. The CBITI bit position is set to logic 0 when this register is read.

REDI:

The REDI bit indicates that a change of state of the DS3 RED indication has occurred. The DS3 RED indication is visible in the REDV bit location of the DS3 FRMR Status register. When the REDI bit is a logic 1, a change in the RED state has occurred. When the REDI bit is logic 0, no change in the RED state has occurred.

COFAI:

The COFAI bit is set to logic 1 when a change of frame alignment is detected. A COFA is generated when a new DS3 frame alignment is determined that differs from the last known frame alignment. The COFAI bit position is set to logic 0 when this register is read.

Register 100FH: DS3 FRMR Status

Bit	Type	Function	Default
Bit 7	R/W	ACE	0
Bit 6	R	REDV	X
Bit 5	R	CBITV	X
Bit 4	R	FERFV	X
Bit 3	R	IDLV	X
Bit 2	R	AISV	X
Bit 1	R	OOFV	X
Bit 0	R	LOSV	X

LOSV:

The LOSV bit indicates the current loss of signal defect state. LOSV is a logic 1 when a sequence of 175 zeros is detected on the B3ZS encoded DS3 receive stream. LOSV is a logic 0 when a signal with a ones density greater than 33% for 175 ± 1 bit periods is detected.

OOFV:

The OOFV bit indicates the current DS3 out of frame defect state. When the TEMAP has lost frame alignment and is searching for the new alignment, OOFV is set to logic 1. When the TEMAP has found frame alignment, the OOFV bit is set to logic 0.

AISV:

The AISV bit indicates the alarm indication signal state. When the TEMAP detects the AIS maintenance signal, AISV is set to logic 1. The FERFV bit should also be checked to ensure it is a logic 0 when AIS is declared.

IDLV:

The IDLV bit indicates the IDLE signal state. When the TEMAP detects the IDLE maintenance signal, IDLV is set to logic 1.

FERFV:

The FERFV bit indicates the current far end receive failure defect state. When the TEMAP detects an M-frame with the X1 and X2 bits both set to

zero, FERFV is set to logic 1. When the TEMAP detects an M-frame with the X1 and X2 bits both set to one, FERFV is set to logic 0.

CBITV:

The CBITV bit indicates the application identification channel (AIC) state. CBITV is set to logic 1 (indicating the presence of the C-bit parity application) when the AIC bit is set high for 63 consecutive M-frames. CBITV is set to logic 0 (indicating the presence of the M23 or SYNTRAN applications) when AIC is set low for 2 or more M-frames in the last 15.

REDV:

The REDV bit indicates the current state of the DS3 RED indication. When the REDV bit is a logic 1, the DS3 FRMR frame alignment acquisition circuitry has been out of frame for 2.23ms (or for 13.5ms when FDET is logic 0). When the REDV bit is logic 0, the frame alignment circuitry has found frame (i.e. OOFV=0) for 2.23ms (or 13.5ms if FDET=0).

ACE:

The ACE bit selects the Additional Configuration Register. This register is located at address 075H, and is only accessible when the ACE bit is set to logic 1. When ACE is set to logic 0, the Interrupt Enable register is accessible at address 075H.

1.13 DS3 Performance Monitoring Registers

Register 1010H: DS3 PMON Performance Meters

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	LCVCH	X
Bit 4	R	FERRCH	X
Bit 3	R	EXZS_IECCH	X
Bit 2	R	PERRCH	X
Bit 1	R	CPERRCH	X
Bit 0	R	FEBECH	X

FEBECH:

The FEBECH bit is set to logic 1 if one or more FEBE events have occurred during the latest PMON accumulation interval.

CPERRCH:

The CPERRCH bit is set to logic 1 if one or more path parity error events have occurred during the latest PMON accumulation interval.

PERRCH:

The PERRCH bit is set to logic 1 if one or more parity error events have occurred during the latest PMON accumulation interval.

EXZS_IECCH:

The EXZS_IECCH bit is set to logic 1 if one or more summed line code violation events in DS3 mode have occurred during the latest PMON accumulation interval.

FERRCH:

The FERRCH bit is set to logic 1 if one or more F-bit or M-bit error events have occurred during the latest PMON accumulation interval.

LCVCH:

The LCVCH bit is set to logic 1 if one or more line code violation events have occurred during the latest PMON accumulation interval.

Register 1011H: DS3 PMON Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	INTE	0
Bit 1	R	INTR	X
Bit 0	R	OVR	X

OVR:

The OVR bit indicates the overrun status of the PMON holding registers. A logic 1 in this bit position indicates that a previous interrupt has not been cleared before the end of the next accumulation interval, and that the contents of the holding registers have been overwritten. A logic 0 indicates that no overrun has occurred. This bit is reset to logic 0 when this register is read.

INTR:

The INTR bit indicates the current status of the interrupt signal. A logic 1 in this bit position indicates that a transfer of counter values to the holding registers has occurred; a logic 0 indicates that no transfer has occurred. The INTR bit is set to logic 0 when this register is read.

INTE:

The INTE bit enables the generation of an interrupt when the PMON counter values are transferred to the holding registers. When a logic 1 is written to INTE, the interrupt generation is enabled.

Register 1014H: DS3 PMON Line Code Violation Event Count LSB

Bit	Type	Function	Default
Bit 7	R	LCV[7]	X
Bit 6	R	LCV[6]	X
Bit 5	R	LCV[5]	X
Bit 4	R	LCV[4]	X
Bit 3	R	LCV[3]	X
Bit 2	R	LCV[2]	X
Bit 1	R	LCV[1]	X
Bit 0	R	LCV[0]	X

Register 1015H: DS3 PMON Line Code Violation Event Count MSB

Bit	Type	Function	Default
Bit 7	R	LCV[15]	X
Bit 6	R	LCV[14]	X
Bit 5	R	LCV[13]	X
Bit 4	R	LCV[12]	X
Bit 3	R	LCV[11]	X
Bit 2	R	LCV[10]	X
Bit 1	R	LCV[9]	X
Bit 0	R	LCV[8]	X

LCV[15:0]:

LCV[15:0] represents the number of DS3 line code violation errors that have been detected since the last time the LCV counter was polled.
This counter (and all other counters in the PMON) is polled by writing to any of the PMON register addresses (024H to 2FH), (034H to 37H) or to the TEMAP Master Revision/Global PMON update register (01H). Such a write transfers the internally accumulated count to the LCV Error Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost. The transfer takes 3 RCLK cycles to complete.

Register 1016H: DS3 PMON Framing Bit Error Event Count LSB

Bit	Type	Function	Default
Bit 7	R	FERR[7]	X
Bit 6	R	FERR[6]	X
Bit 5	R	FERR[5]	X
Bit 4	R	FERR[4]	X
Bit 3	R	FERR[3]	X
Bit 2	R	FERR[2]	X
Bit 1	R	FERR[1]	X
Bit 0	R	FERR[0]	X

Register 1017H: DS3 PMON Framing Bit Error Event Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	FERR[9]	X
Bit 0	R	FERR[8]	X

FERR[9:0]:

FERR[9:0] represents the number of DS3 F-bit and M-bit errors that have been detected since the last time the framing error counter was polled. The counter (and all other counters in the PMON) is polled by writing to any of the PMON register addresses (024H to 02FH), (034H to 037H) or to the TEMAP Master Revision/Global PMON update register (01H). Such a write transfers the internally accumulated count to the FERR Error Event Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost. The transfer takes 3 RCLK cycles to complete.

Register 1018H: DS3 PMON Excessive Zeros LSB

Bit	Type	Function	Default
Bit 7	R	EXZS/IEC[7]	X
Bit 6	R	EXZS/IEC[6]	X
Bit 5	R	EXZS/IEC[5]	X
Bit 4	R	EXZS/IEC[4]	X
Bit 3	R	EXZS/IEC[3]	X
Bit 2	R	EXZS/IEC[2]	X
Bit 1	R	EXZS/IEC[1]	X
Bit 0	R	EXZS/IEC[0]	X

Register 1019H: DS3 PMON Excessive Zeros MSB

Bit	Type	Function	Default
Bit 7	R	EXZS/IEC[15]	X
Bit 6	R	EXZS/IEC[14]	X
Bit 5	R	EXZS/IEC[13]	X
Bit 4	R	EXZS/IEC[12]	X
Bit 3	R	EXZS/IEC[11]	X
Bit 2	R	EXZS/IEC[10]	X
Bit 1	R	EXZS/IEC[9]	X
Bit 0	R	EXZS/IEC[8]	X

EXZS/IEC[15:0]:

In DS3 mode, EXZS/IEC[15:0] represents the number of summed Excessive Zeros (EXZS) that occurred during the previous accumulation interval. One or more excessive zeros occurrences within an 85 bit DS3 information block is counted as one summed excessive zero. Excessive zeros are accumulated by this register only when the EXZSO and EXZDET are logic 1 in the DS3 FRMR Additional Configuration Register. This register accumulates summed line code violations when the EXZSO is logic 0. The count of summed line code violations is defined as the number of DS3 information blocks (85 bits) that contain one or more line code violations

since the last time the summed LCV counter was polled.

The counter (and all other counters in the PMON) is polled by writing to any of the PMON register addresses (024H to 02FH), (034H to 037H) or to the TEMAP Master Revision/Global PMON update register (01H). Such a write transfers the internally accumulated count to the EXZS/IEC Event Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost. The transfer takes 3 RCLK cycles to complete.

Register 101AH: DS3 PMON Parity Error Event Count LSB

Bit	Type	Function	Default
Bit 7	R	PERR[7]	X
Bit 6	R	PERR[6]	X
Bit 5	R	PERR[5]	X
Bit 4	R	PERR[4]	X
Bit 3	R	PERR[3]	X
Bit 2	R	PERR[2]	X
Bit 1	R	PERR[1]	X
Bit 0	R	PERR[0]	X

Register 101BH: DS3 PMON Parity Error Event Count MSB

Bit	Type	Function	Default
Bit 7	R	PERR[15]	X
Bit 6	R	PERR[14]	X
Bit 5	R	PERR[13]	X
Bit 4	R	PERR[12]	X
Bit 3	R	PERR[11]	X
Bit 2	R	PERR[10]	X
Bit 1	R	PERR[9]	X
Bit 0	R	PERR[8]	X

PERR[15:0]:

PERR[15:0] represents the number of DS3 P-bit errors.
The counter (and all other counters in the PMON) is polled by writing to any of the PMON register addresses (024H to 02FH), (034H to 037H) or to the TEMAP Master Revision/Global PMON update register (01H). Such a write transfers the internally accumulated count to the PERR Error Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that coincident events are not lost. The transfer takes 3 RCLK cycles to complete.

Register 101CH: DS3 PMON Path Parity Error Event Count LSB

Bit	Type	Function	Default
Bit 7	R	CPERR[7]	X
Bit 6	R	CPERR[6]	X
Bit 5	R	CPERR[5]	X
Bit 4	R	CPERR[4]	X
Bit 3	R	CPERR[3]	X
Bit 2	R	CPERR[2]	X
Bit 1	R	CPERR[1]	X
Bit 0	R	CPERR[0]	X

Register 101DH: DS3 PMON Path Parity Error Event Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	CPERR[13]	X
Bit 4	R	CPERR[12]	X
Bit 3	R	CPERR[11]	X
Bit 2	R	CPERR[10]	X
Bit 1	R	CPERR[9]	X
Bit 0	R	CPERR[8]	X

CPERR[13:0]:

When configured for DS3 applications, CPERR[13:0] represents the number of DS3 path parity errors that have been detected since the last time the DS3 path parity error counter was polled.

The counter (and all other counters in the PMON) is polled by writing to any of the PMON register addresses (024H to 02FH), (034H to 037H) or to the TEMAP Master Revision/Global PMON update register (01H). Such a write transfers the internally accumulated count to the CPERR Error Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that

coincident events are not lost. The transfer takes 3 RCLK cycles to complete.

Register 101EH: DS3 PMON FEBE Event Count LSB

Bit	Type	Function	Default
Bit 7	R	FEBE[7]	X
Bit 6	R	FEBE[6]	X
Bit 5	R	FEBE[5]	X
Bit 4	R	FEBE[4]	X
Bit 3	R	FEBE[3]	X
Bit 2	R	FEBE[2]	X
Bit 1	R	FEBE[1]	X
Bit 0	R	FEBE[0]	X

Register 101FH: DS3 PMON FEBE Event Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	FEBE[13]	X
Bit 4	R	FEBE[12]	X
Bit 3	R	FEBE[11]	X
Bit 2	R	FEBE[10]	X
Bit 1	R	FEBE[9]	X
Bit 0	R	FEBE[8]	X

FEBE[13:0]:

FEBE[13:0] represents the number of DS3 far end block errors that have been detected since the last time the FEBE error counter was polled.

The counter (and all other counters in the PMON) is polled by writing to any of the PMON register addresses (024H to 02FH), (034H to 037H) or to the TEMAP Master Revision/Global PMON update register (01H). Such a write transfers the internally accumulated count to the FEBE Event Count Registers and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that

coincident events are not lost. The transfer takes 3 RCLK cycles to complete.

1.14 DS3 Transmit HDLC Controller Registers

Register 1020H: DS3 TDPR Configuration

Bit	Type	Function	Default
Bit 7	R/W	FLGSHARE	1
Bit 6	R/W	FIFOCLR	0
Bit 5	R/W	Reserved	0
Bit 4		Unused	X
Bit 3	R/W	EOM	0
Bit 2	R/W	ABT	0
Bit 1	R/W	CRC	1
Bit 0	R/W	EN	0

Consecutive writes to the TDPR Configuration, TDPR Interrupt Status/UDR Clear, and TDPR Transmit Data register and reads of the TDPR Interrupt Status/UDR Clear register should not occur at rates greater than 1/8th that of the line rate clock, thus consecutive reads and writes should not occur at greater than 5.5 MHz in DS3 mode.

EN:

The EN bit enables the TDPR functions. When EN is set to logic 1, the TDPR is enabled and flag sequences are sent until data is written into the TDPR Transmit Data register. When the EN bit is set to logic 0, the TDPR is disabled and an all 1's Idle sequence is transmitted on the datalink.

CRC:

The CRC enable bit controls the generation of the CCITT_CRC frame check sequence (FCS). Setting the CRC bit to logic 1 enables the CCITT-CRC generator and appends the 16-bit FCS to the end of each message. When the CRC bit is set to logic 0, the FCS is not appended to the end of the message. The CRC type used is the CCITT-CRC with generator polynomial $x^{16} + x^{12} + x^5 + 1$. The high order bit of the FCS word is transmitted first.

ABT:

The Abort (ABT) bit controls the sending of the 7 consecutive ones HDLC abort code. Setting the ABT bit to a logic 1 causes the 01111111 code (the 0

is transmitted first) to be transmitted after the current byte from the TDPR FIFO is transmitted. The TDPR FIFO is then reset. All data in the TDPR FIFO will be lost. Aborts are continuously sent and the FIFO is held in reset until this bit is reset to a logic 0. At least one Abort sequence will be sent when the ABT bit transitions from logic 0 to logic 1.

EOM:

The EOM bit indicates that the last byte of data written in the Transmit Data register is the end of the present data packet. If the CRC bit is set then the 16-bit FCS word is appended to the last data byte transmitted and a continuous stream of flags is generated. The EOM bit is automatically cleared upon a write to the TDPR Transmit Data register.

Reserved:

This bit must be set to logic 0 for proper operation.

FIFOCLR:

The FIFOCLR bit resets the TDPR FIFO. When set to logic 1, FIFOCLR will cause the TDPR FIFO to be cleared.

FLGSHARE:

The FLGSHARE bit configures the TDPR to share the opening and closing flags between successive frames. If FLGSHARE is logic 1, then the opening and closing flags between successive frames are shared. If FLGSHARE is logic 0, then separate closing and opening flags are inserted between successive frames.

Register 1021H: DS3 TDPR Upper Transmit Threshold

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	UTHR[6]	1
Bit 5	R/W	UTHR[5]	0
Bit 4	R/W	UTHR[4]	0
Bit 3	R/W	UTHR[3]	0
Bit 2	R/W	UTHR[2]	0
Bit 1	R/W	UTHR[1]	0
Bit 0	R/W	UTHR[0]	0

UTHR[6:0]:

The UTHR[6:0] bits define the TDPR FIFO fill level which will automatically cause the bytes stored in the TDPR FIFO to be transmitted. Once the fill level exceeds the UTHR[6:0] value, transmission will begin. Transmission will not stop until the last complete packet is transmitted and the TDPR FIFO fill level is below UTHR[6:0] + 1.

The value of UTHR[6:0] must always be greater than the value of LINT[6:0] unless both values are equal to 00H.

Register 1022H: DS3 TDPR Lower Interrupt Threshold

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	LINT[6]	0
Bit 5	R/W	LINT[5]	0
Bit 4	R/W	LINT[4]	0
Bit 3	R/W	LINT[3]	0
Bit 2	R/W	LINT[2]	1
Bit 1	R/W	LINT[1]	1
Bit 0	R/W	LINT[0]	1

LINT[6:0]:

The LINT[6:0] bits define the TDPR FIFO fill level which causes an internal interrupt (LFILLI) to be generated. Once the TDPR FIFO level decrements to empty or to a value less than LINT[6:0], LFILLI and BLFILL register bits will be set to logic 1. LFILLI will cause an interrupt on INTB if LFILLE is set to logic 1.

The value of LINT[6:0] must always be less than the value of UTHR[6:0] unless both values are equal to 00H.

Register 1023H: DS3 TDPR Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	Reserved	0
Bit 3	R/W	FULLE	0
Bit 2	R/W	OVRE	0
Bit 1	R/W	UDRE	0
Bit 0	R/W	LFILLE	0

LFILLE:

The LFILLE enables a transition to logic 1 on LFILLI to generate an interrupt on INTB. If LFILLE is a logic 1, a transition to logic 1 on LFILLI will generate an interrupt on INTB. If LFILLE is a logic 0, a transition to logic 1 on LFILLI will not generate an interrupt on INTB.

UDRE:

The UDRE enables a transition to logic 1 on UDRI to generate an interrupt on INTB. If UDRE is a logic 1, a transition to logic 1 on UDRI will generate an interrupt on INTB. If UDRE is a logic 0, a transition to logic 1 on UDRI will not generate an interrupt on INTB.

OVRE:

The OVRE enables a transition to logic 1 on OVRI to generate an interrupt on INTB. If OVRE is a logic 1, a transition to logic 1 on OVRI will generate an interrupt on INTB. If OVRE is a logic 0, a transition to logic 1 on OVRI will not generate an interrupt on INTB.

FULLE:

The FULLE enables a transition to logic 1 on FULLI to generate an interrupt on INTB. If FULLE is a logic 1, a transition to logic 1 on FULLI will generate an interrupt on INTB. If FULLE is a logic 0, a transition to logic 1 on FULLI will not generate an interrupt on INTB.

Reserved:

This bit must be set to logic 0 for proper operation.

Register 1024H: DS3 TDPR Interrupt Status/UDR Clear

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	FULL	X
Bit 5	R	BLFILL	X
Bit 4	R	Reserved	X
Bit 3	R	FULLI	X
Bit 2	R	OVR	X
Bit 1	R	UDRI	X
Bit 0	R	LFILLI	X

Consecutive writes to the TDPR Configuration, TDPR Interrupt Status/UDR Clear, and TDPR Transmit Data register and reads of the TDPR Interrupt Status/UDR Clear register should not occur at rates greater than 1/8th that of the line rate clock, thus consecutive reads and writes should not occur at greater than 5.5 MHz in DS3 mode.

LFILLI:

The LFILLI bit will transition to logic 1 when the TDPR FIFO level transitions to empty or falls below the value of LINT[6:0] programmed in the TDPR Lower Interrupt Threshold register. LFILLI will assert INTB if it is a logic 1 and LFILLE is programmed to logic 1. LFILLI is cleared when this register is read.

UDRI:

The UDRI bit will transition to 1 when the TDPR FIFO underruns. That is, the TDPR was in the process of transmitting a packet when it ran out of data to transmit. UDRI will assert INTB if it is a logic 1 and UDRE is programmed to logic 1. UDRI is cleared when this register is read.

OVRI:

The OVRI bit will transition to 1 when the TDPR FIFO overruns. That is, the TDPR FIFO was already full when another data byte was written to the TDPR Transmit Data register. OVRI will assert INTB if it is a logic 1 and OVRE is programmed to logic 1. OVRI is cleared when this register is read.

FULLI:

The FULLI bit will transition to logic 1 when the TDPR FIFO is full. FULLI will assert INTB if it is a logic 1 and FULLE is programmed to logic 1. FULLI is cleared when this register is read.

Reserved:

This bit is not used in TEMAP applications.

BLFILL:

The BLFILL bit is set to logic 1 if the current FIFO fill level is below the LINT[7:0] level or is empty.

FULL:

The FULL bit reflects the current condition of the TDPR FIFO. If FULL is a logic 1, the TDPR FIFO already contains 128-bytes of data and can accept no more.

Register 1025H: DS3 TDPR Transmit Data

Bit	Type	Function	Default
Bit 7	R/W	TD[7]	X
Bit 6	R/W	TD[6]	X
Bit 5	R/W	TD[5]	X
Bit 4	R/W	TD[4]	X
Bit 3	R/W	TD[3]	X
Bit 2	R/W	TD[2]	X
Bit 1	R/W	TD[1]	X
Bit 0	R/W	TD[0]	X

Consecutive writes to the TDPR Configuration, TDPR Interrupt Status/UDR Clear, and TDPR Transmit Data register and reads of the TDPR Interrupt Status/UDR Clear register should not occur at rates greater than 1/8th that of the line rate clock, thus consecutive reads and writes should not occur at greater than 5.5 MHz in DS3 mode.

TD[7:0]:

The TD[7:0] bits contain the data to be transmitted on the data link. Data written to this register is serialized and transmitted (TD[0] is transmitted first).

1.15 DS3 Receive HDLC Controller Registers

Register 1028H: DS3 RDLC Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	Reserved	0
Bit 3	R/W	MEN	0
Bit 2	R/W	MM	0
Bit 1	R/W	TR	0
Bit 0	R/W	EN	0

EN:

The EN bit controls the overall operation of the RDLC. When EN is set to logic 1, RDLC is enabled; when set to logic 0, RDLC is disabled. When RDLC is disabled, the RDLC FIFO buffer and interrupts are all cleared. When RDLC is enabled, it will immediately begin looking for flags.

TR:

Setting the terminate reception (TR) bit to logic 1 forces the RDLC to immediately terminate the reception of the current data frame, empty the RDLC FIFO buffer, clear the interrupts, and begin searching for a new flag sequence. The RDLC handles a terminate reception event in the same manner as it would the toggling of the EN bit from logic 1 to logic 0 and back to logic 1. Thus, the RDLC state machine will begin searching for flags. An interrupt will be generated when the first flag is detected. The TR bit will reset itself to logic 0 after the register write operation is completed and a rising and falling edge occurs on the internal datalink clock input. If the RDLC Configuration Register is read after this time, the TR bit value returned will be logic 0.

MEN:

Setting the Match Enable (MEN) bit to logic 1 enables the detection and storage in the RDLC FIFO of only those packets whose first data byte matches either of the bytes written to the Primary or Secondary Match

Address Registers, or the universal all ones address. When the MEN bit is logic 0, all packets received are written into the RDLC FIFO.

MM:

Setting the Match Mask (MM) bit to logic 1 ignores the PA[1:0] bits of the Primary Address Match Register, the SA[1:0] bits of the Secondary Address Match Register, and the two least significant bits of the universal all ones address when performing the address comparison.

Reserved:

This register bit must be set to logic 0 for proper operation.

Register 1029H: DS3 RDLC Interrupt Control

Bit	Type	Function	Default
Bit 7	R/W	INTE	0
Bit 6	R/W	INTC[6]	0
Bit 5	R/W	INTC[5]	0
Bit 4	R/W	INTC[4]	0
Bit 3	R/W	INTC[3]	0
Bit 2	R/W	INTC[2]	0
Bit 1	R/W	INTC[1]	0
Bit 0	R/W	INTC[0]	0

INTC[6:0]:

The INTC[6:0] bits control the assertion of FIFO fill level set point interrupts.

INTE:

The Interrupt Enable bit (INTE) must set to logic 1 to allow the internal interrupt status to be propagated to the INTB output. When the INTE bit is logic 0 the RDLC will not assert INTB.

The contents of the Interrupt Control Register must only be changed when the EN bit in the RDLC Configuration Register is logic 0. This prevents any erroneous interrupt generation.

Register 102AH: DS3 RDLC Status

Bit	Type	Function	Default
Bit 7	R	FE	X
Bit 6	R	OVR	X
Bit 5	R	COLS	X
Bit 4	R	PKIN	X
Bit 3	R	PBS[2]	X
Bit 2	R	PBS[1]	X
Bit 1	R	PBS[0]	X
Bit 0	R	INTR	X

Consecutive reads of the RDLC Status and Data registers should not occur at rates greater than 1/10 that of the line rate clock, thus consecutive reads should not occur at greater than 4.4 MHz in DS3 mode.

INTR:

The interrupt (INTR) bit reflects the status of the internal RDLC interrupt. If the INTE bit in the RDLC Interrupt Control Register is set to logic 1, a RDLC interrupt (INTR is a logic 1) will cause INTB to be asserted low. The INTR register bit will be set to logic 1 when one of the following conditions occurs:

1. the number of bytes specified in the RDLC Interrupt Control register have been received on the data link and written into the FIFO
2. RDLC FIFO buffer overrun has been detected
3. the last byte of a packet has been written into the RDLC FIFO
4. the last byte of an aborted packet has been written into the RDLC FIFO
5. transition of receiving all ones to receiving flags has been detected.

PBS[2:0]:

The packet byte status (PBS[2:0]) bits indicate the status of the data last read from the FIFO as indicated in the following table:

PBS[2:0]	Data Status
000	The data byte read from the FIFO is not special.
001	The data byte read from the FIFO is the dummy byte that was written into the FIFO when the first HDLC flag sequence (01111110) was detected. This indicates that the data link became active.
010	The data byte read from the FIFO is the dummy byte that was written into the FIFO when the HDLC abort sequence (01111111) was detected. This indicates that the data link became inactive.
011	Unused.
100	The data byte read from the FIFO is the last byte of a normally terminated packet with no CRC error and the packet received had an integer number of bytes.
101	The data byte read from the FIFO must be discarded because there was a non-integer number of bytes in the packet.
110	The data byte read from the FIFO is the last byte of a normally terminated packet with a CRC error. The packet was received in error.
111	The data byte read from the FIFO is the last byte of a normally terminated packet with a CRC error and a non-integer number of bytes. The packet was received in error.

PKIN:

The Packet In (PKIN) bit is logic 1 when the last byte of a non-aborted packet is written into the FIFO. The PKIN bit is cleared to logic 0 after the RDLC Status Register is read.

COLS:

The Change of Link Status (COLS) bit is set to logic 1 if the RDLC has detected the HDLC flag sequence (01111110) or HDLC abort sequence

(01111111) in the data. This indicates that there has been a change in the data link status. The COLS bit is cleared to logic 0 by reading this register or by clearing the EN bit in the RDLC Configuration Register. For each change in link status, a byte is written into the FIFO. If the COLS bit is found to be logic 1 then the RDLC FIFO must be read until empty. The status of the data link is determined by the PBS[2:0] bits associated with the data read from the RDLC FIFO.

OVR:

The overrun (OVR) bit is set to logic 1 when data is written over unread data in the RDLC FIFO buffer. This bit is not reset to logic 0 until after the Status Register is read. While the OVR bit is logic 1, the RDLC and RDLC FIFO buffer are held in the reset state, causing the COLS and PKIN bits to be reset to logic 0.

FE:

The FIFO buffer empty (FE) bit is set to logic 1 when the last RDLC FIFO buffer entry is read. The FE bit goes to logic 0 when the FIFO is loaded with new data.

Register 102BH: DS3 RDLC Data

Bit	Type	Function	Default
Bit 7	R	RD[7]	X
Bit 6	R	RD[6]	X
Bit 5	R	RD[5]	X
Bit 4	R	RD[4]	X
Bit 3	R	RD[3]	X
Bit 2	R	RD[2]	X
Bit 1	R	RD[1]	X
Bit 0	R	RD[0]	X

Consecutive reads of the RDLC Status and Data registers should not occur at rates greater than 1/10 that of the line rate clock, thus consecutive reads should not occur at greater than 4.4 MHz in DS3 mode.

RD[7:0]:

RD[7:0] contains the received data link information. RD[0] corresponds to the first received bit of the data link message.
This register reads from the RDLC 128-byte FIFO buffer. If data is available, the FE bit in the FIFO Input Status Register is logic 0.
When an overrun is detected, an interrupt is generated and the FIFO buffer is held cleared until the RDLC Status Register is read.

Register 102CH: DS3 RDLC Primary Address Match

Bit	Type	Function	Default
Bit 7	R/W	PA[7]	1
Bit 6	R/W	PA[6]	1
Bit 5	R/W	PA[5]	1
Bit 4	R/W	PA[4]	1
Bit 3	R/W	PA[3]	1
Bit 2	R/W	PA[2]	1
Bit 1	R/W	PA[1]	1
Bit 0	R/W	PA[0]	1

PA[7:0]:

The first byte received after a flag character is compared against the contents of this register. If a match occurs, the packet data, including the matching first byte, is written into the FIFO. PA[0] corresponds to the first received bit of the data link message. The MM bit in the Configuration Register is used mask off PA[1:0] during the address comparison.

Register 102DH: DS3 RDLC Secondary Address Match

Bit	Type	Function	Default
Bit 7	R/W	SA[7]	1
Bit 6	R/W	SA[6]	1
Bit 5	R/W	SA[5]	1
Bit 4	R/W	SA[4]	1
Bit 3	R/W	SA[3]	1
Bit 2	R/W	SA[2]	1
Bit 1	R/W	SA[1]	1
Bit 0	R/W	SA[0]	1

SA[7:0]:

The first byte received after a flag character is compared against the contents of this register. If a match occurs, the packet data, including the matching first byte, is written into the FIFO. SA[0] corresponds to the first received bit data link message. The MM bit in the Configuration Register is used mask off SA[1:0] during the address comparison.

1.16 PRGD Pseudo Random Pattern Generator and Detector Registers

Register 1030H: PRGD Control

Bit	Type	Function	Default
Bit 7	R/W	PDR[1]	0
Bit 6	R/W	PDR[0]	0
Bit 5	R/W	QRSS	0
Bit 4	R/W	PS	0
Bit 3	R/W	TINV	0
Bit 2	R/W	RINV	0
Bit 1	R/W	AUTOSYNC	1
Bit 0	R/W	MANSYNC	0

PDR[1:0]:

The PDR[1:0] bits select the content of the four pattern detector registers (at addresses 103CH-103FH) to be any one of the pattern receive registers, the error count holding registers, or the bit count holding registers. The selection is shown in the following table:

PDR[1:0]	PDR#1	PDR#2	PDR#3	PDR#4
00, 01	Pattern Receive (LSB)	Pattern Receive	Pattern Receive	Pattern Receive (MSB)
10	Error Count (LSB)	Error Count	Error Count	Error Count (MSB)
11	Bit Count (LSB)	Bit Count	Bit Count	Bit Count (MSB)

QRSS:

The QRSS bit enables the zero suppression feature required when generating the QRSS sequence. When QRSS is a logic 1, a one is forced in the TDAT stream when the following 14 bit positions are all zeros. When QRSS is a logic 0, the zero suppression feature is disabled.

PS:

The PS bit selects the generated pattern. When PS is a logic 1, a repetitive pattern is generated. When PS is a logic 0, a pseudo-random pattern is generated.

TINV:

The TINV bit controls the logical inversion of the generated data stream. When TINV is a logic 1, the data is inverted. When TINV is a logic 0, the data is not inverted.

RINV:

The RINV bit controls the logical inversion of the receive data stream before processing. When RINV is a logic 1, the received data is inverted before being processed by the pattern detector. When RINV is a logic 0, the received data is not inverted.

AUTOSYNC:

The AUTOSYNC bit enables the automatic resynchronization of the pattern detector. The automatic resynchronization is activated when 6 or more bit errors are detected in the last 64 bit periods. When AUTOSYNC is a logic 1, the auto resync feature is enabled. When AUTO SYNC is a logic 0, the auto sync feature is disabled, and pattern resynchronization is accomplished using the MANSYNC bit.

MANSYNC:

The MANSYNC bit is used to initiate a manual resynchronization of the pattern detector. A low to high transition on MANSYNC initiates the resynchronization.

Register 1031H: PRGD Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7	R/W	SYNCE	0
Bit 6	R/W	BEE	0
Bit 5	R/W	XFERE	0
Bit 4	R	SYNCV	X
Bit 3	R	SYNCI	X
Bit 2	R	BEI	X
Bit 1	R	XFERI	X
Bit 0	R	OVR	X

SYNCE:

The SYNCE bit enables the generation of an interrupt when the pattern detector changes synchronization state. When SYNCE is set to logic 1, the interrupt is enabled.

BEE:

The BEE bit enables the generation of an interrupt when a bit error is detected in the receive data. When BEE is set to logic 1, the interrupt is enabled.

XFERE:

The XFERE bit enables the generation of an interrupt when an accumulation interval is completed and new values are stored in the receive pattern registers, the bit counter holding registers, and the error counter holding registers. When XFERE is set to logic 1, the interrupt is enabled.

SYNCV:

The SYNCV bit indicates the synchronization state of the pattern detector. When SYNCV is a logic 1 the pattern detector is synchronized (the pattern detector has observed at least 32 consecutive error free bit periods). When SYNCV is a logic 0, the pattern detector is out of sync (the pattern detector has detected 6 or more bit errors in a 64 bit period window).

SYNCI:

The SYNCI bit indicates that the detector has changed synchronization state since the last time this register was read. If SYNCI is logic 1, the pattern detector has gained or lost synchronization at least once. SYNCI is set to logic 0 when this register is read.

BEI:

The BEI bit indicates that one or more bit errors have been detected since the last time this register was read. When BEI is set to logic 1, at least one bit error has been detected. BEI is set to logic 0 when this register is read.

XFERI:

The XFERI bit indicates that a transfer of pattern detector data has occurred. A logic 1 in this bit position indicates that the pattern receive registers, the bit counter holding registers and the error counter holding registers have been updated. This update is initiated by writing to one of the pattern detector register locations, or by writing to the TEMAP Revision / Global Monitor Update Register (0002H). XFERI is set to logic 0 when this register is read.

OVR:

The OVR bit is the overrun status of the pattern detector registers. A logic 1 in this bit position indicates that a previous transfer (indicated by XFERI being logic 1) has not been acknowledged before the next accumulation interval has occurred and that the contents of the pattern receive registers, the bit counter holding registers and the error counter holding registers have been overwritten. OVR is set to logic 0 when this register is read.

Register 1032H: PRGD Length

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	PL[4]	0
Bit 3	R/W	PL[3]	0
Bit 2	R/W	PL[2]	0
Bit 1	R/W	PL[1]	0
Bit 0	R/W	PL[0]	0

PL[4:0]:

PL[4:0] determine the length of the generated pseudo random or repetitive pattern. The pattern length is equal to the value of PL[4:0] + 1.

Register 1033H: PRGD Tap

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	PT[4]	0
Bit 3	R/W	PT[3]	0
Bit 2	R/W	PT[2]	0
Bit 1	R/W	PT[1]	0
Bit 0	R/W	PT[0]	0

PT[4:0]:

PT[4:0] determine the feedback tap position of the generated pseudo random pattern. The feedback tap position is equal to the value of PT[4:0] + 1.

Register 1034H: PRGD Error Insertion

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	EVENT	0
Bit 2	R/W	EIR[2]	0
Bit 1	R/W	EIR[1]	0
Bit 0	R/W	EIR[0]	0

EVENT:

A low to high transition on the EVENT bit causes a single bit error to be inserted in the generated pattern. This bit must be cleared and set again for a subsequent error to be inserted.

EIR[2:0]:

The EIR[2:0] bits control the insertion of a programmable bit error rate as indicated in the following table:

EIR[2:0]	Generated Bit Error Rate
000	No errors inserted
001	10^{-1}
010	10^{-2}
011	10^{-3}
100	10^{-4}
101	10^{-5}
110	10^{-6}
111	10^{-7}

Register 1038H: PRGD Pattern Insertion #1

Bit	Type	Function	Default
Bit 7	R/W	PI[7]	0
Bit 6	R/W	PI[6]	0
Bit 5	R/W	PI[5]	0
Bit 4	R/W	PI[4]	0
Bit 3	R/W	PI[3]	0
Bit 2	R/W	PI[2]	0
Bit 1	R/W	PI[1]	0
Bit 0	R/W	PI[0]	0

Register 1039H: PRGD Pattern Insertion #2

Bit	Type	Function	Default
Bit 7	R/W	PI[15]	0
Bit 6	R/W	PI[14]	0
Bit 5	R/W	PI[13]	0
Bit 4	R/W	PI[12]	0
Bit 3	R/W	PI[11]	0
Bit 2	R/W	PI[10]	0
Bit 1	R/W	PI[9]	0
Bit 0	R/W	PI[8]	0

Register 103AH: PRGD Pattern Insertion #3

Bit	Type	Function	Default
Bit 7	R/W	PI[23]	0
Bit 6	R/W	PI[22]	0
Bit 5	R/W	PI[21]	0
Bit 4	R/W	PI[20]	0
Bit 3	R/W	PI[19]	0

Bit	Type	Function	Default
Bit 2	R/W	PI[18]	0
Bit 1	R/W	PI[17]	0
Bit 0	R/W	PI[16]	0

Register 103BH: PRGD Pattern Insertion #4

Bit	Type	Function	Default
Bit 7	R/W	PI[31]	0
Bit 6	R/W	PI[30]	0
Bit 5	R/W	PI[29]	0
Bit 4	R/W	PI[28]	0
Bit 3	R/W	PI[27]	0
Bit 2	R/W	PI[26]	0
Bit 1	R/W	PI[25]	0
Bit 0	R/W	PI[24]	0

PI[31:0]:

PI[31:0] contain the data that is loaded in the pattern generator each time a new pattern (pseudo random or repetitive) is to be generated. When a pseudo random pattern is to be generated, PI[31:0] must be set to 0xFFFFFFFF. The data is loaded each time pattern insertion register #4 is written. Pattern insertion registers #1 - #3 should be loaded with the desired data before pattern register #4 is written. When a repetitive pattern is transmitted, PI[31], the MSB, contains the first bit transmitted, PI[0], the LSB, contains the last bit transmitted.

Register 103CH: PRGD Pattern Detector #1

Bit	Type	Function	Default
Bit 7	R/W	PD[7]	0
Bit 6	R/W	PD[6]	0
Bit 5	R/W	PD[5]	0
Bit 4	R/W	PD[4]	0
Bit 3	R/W	PD[3]	0
Bit 2	R/W	PD[2]	0
Bit 1	R/W	PD[1]	0
Bit 0	R/W	PD[0]	0

Register 103DH: PRGD Pattern Detector #2

Bit	Type	Function	Default
Bit 7	R/W	PD[15]	0
Bit 6	R/W	PD[14]	0
Bit 5	R/W	PD[13]	0
Bit 4	R/W	PD[12]	0
Bit 3	R/W	PD[11]	0
Bit 2	R/W	PD[10]	0
Bit 1	R/W	PD[9]	0
Bit 0	R/W	PD[8]	0

Register 103EH: PRGD Pattern Detector #3

Bit	Type	Function	Default
Bit 7	R/W	PD[23]	0
Bit 6	R/W	PD[22]	0
Bit 5	R/W	PD[21]	0
Bit 4	R/W	PD[20]	0
Bit 3	R/W	PD[19]	0

Bit	Type	Function	Default
Bit 2	R/W	PD[18]	0
Bit 1	R/W	PD[17]	0
Bit 0	R/W	PD[16]	0

Register 103FH: PRGD Pattern Detector #4

Bit	Type	Function	Default
Bit 7	R/W	PD[31]	0
Bit 6	R/W	PD[30]	0
Bit 5	R/W	PD[29]	0
Bit 4	R/W	PD[28]	0
Bit 3	R/W	PD[27]	0
Bit 2	R/W	PD[26]	0
Bit 1	R/W	PD[25]	0
Bit 0	R/W	PD[24]	0

PD[31:0]:

PD[31:0] contain the pattern detector data. The values contained in these registers are determined by the PDR[1:0] bits in the PRGD Control register.

When PDR[1:0] is set to 00 or 01, PD[31:0] contain the pattern receive register. The 32 bits received immediately before the last accumulation interval are present on PD[31:0]. PD[31] contains the first of the 32 received bits, PD[0] contains the last of the 32 received bits.

When PDR[1:0] is set to 10, PD[31:0] contain the error counter holding register. The value in this register represents the number of bit errors that have been accumulated since the last accumulation interval. Note that bit errors are not accumulated while the pattern detector is out of sync.

When PDR[1:0] is set to 11, PD[31:0] contain the bit counter holding register. The value in this register represents the total number of bits that have been received since the last accumulation interval.

The PRGD Pattern Detect registers are updated by writing to any one of the Pattern Detect registers. Alternatively, the Pattern Detect registers are

updated globally with all other TEMAP counter registers by writing to the Revision / Global PMON Update register (address 0002H).

1.17 MX23 Multiplexer Registers

Register 1040H: MX23 Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	LBCODE[1]	0
Bit 2	R/W	LBCODE[0]	0
Bit 1	R/W	CBE	0
Bit 0	R/W	INTE	0

INTE:

When set high, the INTE bit enables the MX23 to activate the interrupt output, INTB, whenever any of the LBRI[7:1] bits are set high in the MX23 Loopback Request Interrupt register. MX23 interrupts are masked when INTE is cleared low.

CBE:

When set high, the CBE bit enables C-bit parity operation. When CBE is low, M23 operation is enabled. While in C-bit parity mode, loopback request detection and loopback request insertion are disabled. The generated DS2 clock, GD2CLK, is nominally 6.3062723 MHz while in C-bit parity mode, received C bits are ignored, and transmitted C bits are set to 1. While in M23 mode, the generated DS2 clock, GD2CLK, is nominally 6.311993 MHz and C bit decoding and encoding is fully operational.

LBCODE[1:0]:

The LBCODE[1:0] bits select the valid state for a loopback request coded in the C-bits of the DS3 signals. Transmit and receive are not independent; the same code is expected in the receive DS3 as is inserted in the transmitted DS3. The following table gives the correspondence between LBCODE[1:0] bits and the valid codes:

LBCODE[1:0]	Loopback Code
00	C1 = C2 and C1 = $\overline{C3}$
01	C1 = C3 and C1 = $\overline{C2}$
10	C2 = C3 and C1 = $\overline{C2}$
11	C1 = C2 and C1 = $\overline{C3}$

If LBCODE[1:0] is 'b00 or 'b11, the loopback code is as per ANSI T1.107a Section 8.2.1 and TR-TSY-000009 Section 3.7. Because TR-TSY-000233 Section 5.3.14.1 recommends compatibility with non-compliant existing equipment, the two other loopback command possibilities are also supported. The LBCODE[1:0] bits become logical 0 upon either a hardware or software reset.

Register 1041H: MX23 Demux AIS Insert

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	DAIS[7]	0
Bit 5	R/W	DAIS[6]	0
Bit 4	R/W	DAIS[5]	0
Bit 3	R/W	DAIS[4]	0
Bit 2	R/W	DAIS[3]	0
Bit 1	R/W	DAIS[2]	0
Bit 0	R/W	DAIS[1]	0

DAIS[7:1]:

Setting any of the DAIS[7:1] bits activates insertion of the alarm indication signal (all ones) into the corresponding DS2 stream demultiplexed from the DS3 signal input on RDAT. Demux AIS insertion takes place after the point where per DS2 loopback may be invoked using the Loopback Activate register thus allowing demux AIS to be inserted into the through path while a DS2 loopback is activated.

Register 1042H: MX23 Mux AIS Insert

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	MAIS[7]	0
Bit 5	R/W	MAIS[6]	0
Bit 4	R/W	MAIS[5]	0
Bit 3	R/W	MAIS[4]	0
Bit 2	R/W	MAIS[3]	0
Bit 1	R/W	MAIS[2]	0
Bit 0	R/W	MAIS[1]	0

MAIS[7:1]:

Setting any of the MAIS[7:1] bits activates insertion of the alarm indication signal (all ones) into the corresponding DS2 stream multiplexed into the DS3 signal output on TDAT. Mux AIS insertion takes place before the point where per DS2 loopback may be invoked using the Loopback Activate register and thus mux AIS cannot be inserted while a DS2 loopback is activated.

Register 1043H: MX23 Loopback Activate

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	LBA[7]	0
Bit 5	R/W	LBA[6]	0
Bit 4	R/W	LBA[5]	0
Bit 3	R/W	LBA[4]	0
Bit 2	R/W	LBA[3]	0
Bit 1	R/W	LBA[2]	0
Bit 0	R/W	LBA[1]	0

LBA[7:1]:

Setting any of the LBA[7:1] bits activates loopback of the corresponding DS2 stream from the input DS3 signal to the output DS3 signal.
The demultiplexed DS2 signals continue to present valid payloads while loopbacks are activated. The MX23 Demux AIS Insert Register allows insertion of DS2 AIS if required.

Register 1044H: MX23 Loopback Request Insert

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	ILBR[7]	0
Bit 5	R/W	ILBR[6]	0
Bit 4	R/W	ILBR[5]	0
Bit 3	R/W	ILBR[4]	0
Bit 2	R/W	ILBR[3]	0
Bit 1	R/W	ILBR[2]	0
Bit 0	R/W	ILBR[1]	0

ILBR[7:1]:

Setting any of the ILBR[7:1] bits enables the insertion of a loopback request in the corresponding DS2 stream in the output DS3 signal. The format of the loopback request is determined by the LBCODE[1:0] bits in the MX23 Configuration Register.

Register 1045H: MX23 Loopback Request Detect

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	LBRD[7]	X
Bit 5	R	LBRD[6]	X
Bit 4	R	LBRD[5]	X
Bit 3	R	LBRD[4]	X
Bit 2	R	LBRD[3]	X
Bit 1	R	LBRD[2]	X
Bit 0	R	LBRD[1]	X

LBRD[7:1]:

The LBRD[7:1] bits are set high while a loopback request is detected for the corresponding DS2 stream in the input DS3 signal. The LBRD[7:1] bits are set low otherwise.

The format of the loopback request expected is determined by the LBCODE[1:0] bits in the MX23 Configuration Register. As per TR-TSY-000009 Section 3.7, the loopback request must be present for five successive M-frames before declaration of detection. Removal of the loopback request is declared when it has been absent for five successive M-frames.

Register 1046H: MX23 Loopback Request Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	LBRI[7]	X
Bit 5	R	LBRI[6]	X
Bit 4	R	LBRI[5]	X
Bit 3	R	LBRI[4]	X
Bit 2	R	LBRI[3]	X
Bit 1	R	LBRI[2]	X
Bit 0	R	LBRI[1]	X

LBRI[7:1]:

The LBRI[7:1] bits are set high when a loopback request is asserted or deasserted for the corresponding DS2 stream in the input DS3 signal. The LBRI[7:1] bits are set high whenever the corresponding LBRD[7:1] bits change state. If interrupts are enabled using the INTE bit in the Configuration register then the interrupt output, INTB, is activated. The LBRI[7:1] bits are SET to logic 0 immediately following a read of the register, acknowledging the interrupt and deactivating the INTB output.

1.18 FEAC Transmit Bit Oriented Code Registers

Register 1048H: FEAC XBOC Control

Bit	Type	Function	Default
Bit 7	R	FEACSMPI	X
Bit 6	R/W	FEACSMPE	0
Bit 5	R	RDY	X
Bit 4		Unused	X
Bit 3	R/W	RPT[3]	0
Bit 2	R/W	RPT[2]	0
Bit 1	R/W	RPT[1]	0
Bit 0	R/W	RPT[0]	0

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

FEACSMPI:

The FEACSMPI bit is set high when the FEAC XBOC Code register and RPT[3:0] are sampled by the FEAC XBOC, indicating that the Code Register is ready to be updated with a new FEAC code. If interrupts are enabled via FEACSMPE, the INTB output will be cleared whenever this register is read. FEACSMPI will not change while a Control Register read is in process. Instead, FEACSMPI will hold its initial value – its value at the start of a Control Register read cycle, when RDB falls – until the Control Register read cycle is complete, when RDB rises. After RDB rises, FEACSMPI will be cleared to 0 if it was logic 1 during the read, otherwise FEACSMPI will not be cleared.

FEACSMPE:

Setting FEACSMPE to logic 1 enables a hardware interrupt on the TEMAP INTB output pin when FEACSMPI is logic 1.

RDY:

The RDY bit is set high when the Code Register and RPT[3:0] are sampled by the FEAC XBOC, indicating that the XBOC is ready to be updated with a new FEAC code. Whenever a new FEAC code is written, RDY goes low, indicating that the code has not yet been accepted by the XBOC state

machine. Note that if the FEAC XBOC code register is written with a new value, causing RDY to fall, and then written with its original value, RDY will rise immediately, indicating that the code has been sampled previously.

RPT[3:0]:

These bits contain the 4 bit repeat count used to determine the number (RPT[3:0] + 1) of consecutive, identical, 16-bit bit-oriented code patterns to be transmitted before sampling the FEAC XBOC Code Register, and FEAC XBOC Control Register again. In the event that the Code Register values do not change, the same FEAC code pattern will be repeated continuously. The RPT[3:0] bits can be changed at any time, and are sampled at the same time as the bit oriented code patterns. To obtain the maximum FEAC code modification rate, RPT[3:0] should be updated and stable within N*16 - 3 bit periods of the INTB interrupt pin going high, where N is the number of times the FEAC code is to be repeated.

Register 1049H: FEAC XBOC Code

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	FEAC[5]	1
Bit 4	R/W	FEAC[4]	1
Bit 3	R/W	FEAC[3]	1
Bit 2	R/W	FEAC[2]	1
Bit 1	R/W	FEAC[1]	1
Bit 0	R/W	FEAC[0]	1

FEAC[5:0]:

FEAC[5:0] contains the six bit code that is transmitted on the DS3 far end alarm and control channel (FEAC). The transmitted code consists of a sixteen bit sequence that is repeated continuously. The sequence consists of 8 ones followed by a zero, followed by the six bit code sequence transmitted in order FEAC0, FEAC1, ..., FEAC5, followed by a zero. The all ones sequence is inserted in the FEAC channel when FEAC[5:0] is written with all ones.

1.19 FEAC Receive Bit Oriented Code Registers

Register 104AH: FEAC RBOC Configuration/Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	IDLE	0
Bit 1	R/W	AVC	0
Bit 0	R/W	FEACE	0

FEACE:

The FEACE bit enables the generation of an interrupt when a valid far end alarm and control (FEAC) code is detected. When a logic 1 is written to FEACE, the interrupt generation is enabled.

AVC:

The AVC bit position selects the validation criterion used in determining a valid FEAC code. When a logic 0 is written to AVC, a FEAC code is validated when 8 out of the last 10 received codes are identical. The FEAC code is removed when 2 out of the last 10 received codes do not match the validated code.

When a logic 1 is written to AVC, a FEAC code is validated when 4 out of the last 5 received codes are identical. The FEAC code is removed when a single received FEACs does not match the validated code.

IDLE:

The IDLE bit enables the generation of an interrupt when a validated FEAC is removed. When a logic 1 is written to IDLE, the interrupt generation is enabled.

Register 104BH: FEAC RBOC Interrupt Status

Bit	Type	Function	Default
Bit 7	R	IDLI	X
Bit 6	R	FEACI	X
Bit 5	R	FEAC[5]	X
Bit 4	R	FEAC[4]	X
Bit 3	R	FEAC[3]	X
Bit 2	R	FEAC[2]	X
Bit 1	R	FEAC[1]	X
Bit 0	R	FEAC[0]	X

FEAC[5:0]:

The FEAC[5:0] bits contain the received far end alarm and control channel codes. The FEAC[5:0] bits are set to all ones ("111111") when no code has been validated.

FEACI:

The FEACI bit is set to logic 1 when a new FEAC code is validated. The FEAC code value is contained in the FEAC[5:0] bits. The FEACI bit position is set to logic 0 when this register is read.

IDLI:

The IDLI bit is set to logic 1 when a validated FEAC code is removed. The FEAC[5:0] bits are set to all ones when the code is removed. The IDLI bit position is set to logic 0 when this register is read.

1.20 DS2 Framer Registers (N=1 to 7)

Registers 1040H+20H*N: DS2 FRMR #1-#7 Configuration

Bit	Type	Function	Default
Bit 7	R/W	G747	0
Bit 6		Unused	X
Bit 5	R/W	WORD	0
Bit 4	R/W	M2O5	0
Bit 3	R/W	MBDIS	0
Bit 2	R/W	REFR	0
Bit 1		Unused	X
Bit 0		Unused	X

REFR:

The REFR bit is used to trigger reframing. If a logic 1 is written to REFR when it was previously logic 0, the FRMR is forced out-of-frame, and a new search for frame alignment is initiated. Note that only a low-to-high transition of the REFR bit triggers reframing; multiple write operations are required to ensure such a transition.

MBDIS:

The MBDIS bit disables the declaration of out-of-frame upon excessive M-bit errors. If MBDIS is a logic 0, out-of-frame is declared when one or more M-bit errors are detected in 3 out of 4 consecutive M-frames. If MBDIS is a logic 1, the state of the M-bits is ignored once in frame. Regardless of the state of the MBDIS bit, the F-bits are always monitored for invalid framing.

M2O5:

The M2O5 bit selects the error ratio for declaring out-of-frame (OOF) when in DS2 mode only. When a 1 is written to M2O5, the framer declares OOF when 2 F-bit errors out of 5 consecutive F-bits are observed. When a 0 is written, the framer declares OOF when 2 F-bit errors out of 4 consecutive F-bits are observed. (These two ratios are recommended in TR-TSY-000009 Section 4.1.2) When the FRMR is configured for G.747 operation (the G747 bit is set to logic 1), the OOF status is declared when 4 consecutive framing word errors occur (as per CCITT Rec. G747 Section 4), regardless of the M2O5 bit setting.

WORD:

The WORD bit determines the method of accumulating G.747 framing errors. If the WORD bit is a logic 0, each frame alignment signal (FAS) bit error results in a single FERR count. If the WORD bit is a logic 1, one or more bit errors in a FAS word result in a single FERR count.

G747:

The G747 bit configures the FRMR for G.747 operation. If the G747 bit is a logic 1, the FRMR will process a G.747 signal. If the G747 bit is a logic 0, the FRMR will process a DS2 signal as defined in ANSI T1.107 Section 7.

Registers 1041H+20H*N: DS2 FRMR #1-#7 Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	COFAE	0
Bit 6		Unused	X
Bit 5	R/W	REDE	0
Bit 4	R/W	FERFE	0
Bit 3	R/W	RESE	0
Bit 2	R/W	AISE	0
Bit 1	R/W	OOFE	0
Bit 0		Unused	X

OOFE:

The OOFE bit enables interrupt generation when a DS2 out of frame defect is declared or removed. The interrupt is enabled when a logic 1 is written.

AISE:

The AISE bit enables interrupt generation when the DS2 AIS maintenance signal is detected or removed. The interrupt is enabled when a logic 1 is written.

RESE:

The RESE bit enables interrupt generation when a change is detected in the debounced value of the reserved bit in Set II when in G.747 mode. The interrupt is enabled when the RESE bit is written with a logic 1. The debounced value of the reserved bit only changes when the reserved bit is the same for two consecutive frames. The RESE bit has no effect in DS2 mode.

FERFE:

The FERFE bit enables interrupt generation when a DS2 far end receive failure defect is declared or removed. The interrupt is enabled when a logic 1 is written.

REDE:

The REDE bit enables an interrupt to be generated when a change of state of the DS2 RED indication occurs. The DS2 RED indication is visible in the

REDV bit location of the DS2 FRMR Status register. When REDE is set to logic 1, the interrupt output, INTB, is set low when the state of the RED indication changes.

COFAE:

The COFAE bit enables interrupt generation when the TEMAP detects a DS2 change of frame alignment. The interrupt is enabled when a logic 1 is written.

Registers 1042H+20H*N: DS2 FRMR #1-#7 Interrupt Status

Bit	Type	Function	Default
Bit 7	R	COFAI	X
Bit 6		Unused	X
Bit 5	R	REDI	X
Bit 4	R	FERFI	X
Bit 3	R	RESI	X
Bit 2	R	AISI	X
Bit 1	R	OOFI	X
Bit 0		Unused	X

OOFI:

The OOFI bit is set to logic 1 when an out of frame defect is detected or removed. The OOFI bit position is set to logic 0 when this register is read.

AISI:

The AISI bit is set to logic 1 when the DS2 AIS maintenance signal is detected or removed. The AISI bit position is set to logic 0 when this register is read.

RESI:

The RESI bit is set to logic 1 when the debounced value of the reserved bit in Set II in G.747 mode changes. The debounced value of the reserved bit only changes when the reserved bit is the same for two consecutive frames. This bit has no effect in DS2 mode.

FERFI:

The FERFI bit is set to logic 1 when a FERF defect is detected or removed. The FERFI bit position is set to logic 0 when this register is read.

REDI:

The REDI bit indicates that a change of state of the DS2 RED indication has occurred. The DS2 RED indication is visible in the REDV bit location of the DS2 FRMR Status register. When the REDI bit is a logic 1, a change in the RED state has occurred. When the REDI bit is logic 0, no change in the RED state has occurred.

COFAI:

The COFAI bit is set to logic 1 when a change of frame alignment is detected. A COFA is generated when a new DS2 frame alignment is determined that differs from the last known frame alignment. The COFAI bit position is set to logic 0 when this register is read.

Registers 1043H+20H*N: DS2 FRMR #1-#7 Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	REDV	X
Bit 4	R	FERFV	X
Bit 3	R	RESV	X
Bit 2	R	AISV	X
Bit 1	R	OOFV	X
Bit 0		Unused	X

OOFV:

The OOFV bit indicates the current DS2 out of frame defect state. When the TEMAP has lost frame alignment and is searching for the new alignment, OOFV is set to logic 1. When the TEMAP has found DS2 frame alignment, the OOFV bit is set to logic 0.

AISV:

The AISV bit indicates the alarm indication signal state. When the TEMAP detects the AIS maintenance signal, AISV is set to logic 1.

RESV:

The RESV bit reflects the debounced state of the reserved bit in Set II when in G.747 mode. The debounced value of the reserved bit only changes when the reserved bit is the same for two consecutive frames.

FERFV:

The FERFV bit indicates the current far end receive failure defect state.
In DS2 mode, the FERFV bit reflects the debounced state of the X bit (first bit of the M4-Subframe). If the X-bit has been a zero for two consecutive M-frames, the FERFV bit becomes a logic 1. If the X-bit has been a one for two consecutive M-frames, the FERFV bit becomes a logic 0.
In G.747 mode, FERFV bit reflects the debounced state of the Remote Alarm Indication (RAI, bit 1 of Set II) bit. If the RAI bit has been a one for two consecutive frames, the FERFV bit becomes a logic 1. If the RAI bit has been a zero for two consecutive frames, the FERFV bit becomes a logic 0.

A six frame latency of the FERFV status ensures a virtually 100% probability of freezing correctly in DS2 mode upon an out-of-frame condition and a better than 99.9% probability of freezing correctly in G.747 mode.

REDV:

The REDV bit indicates the current state of the DS2 RED indication. The REDV bit is a logic 1 if an out-of-frame condition has persisted for 9.9 ms (6.9ms in G.747 mode). This is less than 1.5 times the maximum average reframe time allowed. The REDV status will remain asserted for 9.9 ms (6.9ms in G.747 mode) after frame alignment has been declare and then become logic 0.

Registers 1044H+20H*N: DS2 FRMR #1-#7 Monitor Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	INTE	0
Bit 1	R	INTR	0
Bit 0	R	OVR	0

INTE:

The INTE bit allows the generation of an interrupt, assertion of interrupt output signal INTB, upon transfer of the DS2 error counts into holding registers. A logic 1 in the INTE bit position enables the DS2 FRMR to generate an interrupt when the counter values are transferred to the Holding Registers. A logic 0 in the INTE bit position disables the DS2 FRMR from generating an interrupt. The interrupt is cleared when this register is read if its assertion was a result a transfer operation. A write to the Global PMON Update Register is required to generate a transfer of the counters to the holding registers.

INTR:

The INTR bit indicates the current status of the internal interrupt signal. A logic 1 in this bit position indicates that a transfer of counter values to the Holding Registers has occurred; a logic 0 indicates that no transfer has occurred. This bit is set to logic 0 when this register is read. The value of the INTR bit is not affected by the value of the INTE bit. A write to the Global PMON Update Register is required to generate a transfer of the counters to the holding registers.

OVR:

The OVR bit indicates the overrun status of the Holding Registers. A logic 1 in this bit position indicates that a previous interrupt has not been cleared before the end of the next accumulation interval, and that the contents of the Holding Registers have been overwritten. A logic 0 indicates that no overrun has occurred. This bit is reset to logic 0 when this register is read.

Registers 1045H+20H*N: DS2 FRMR #1-#7 FERR Count

Bit	Type	Function	Default
Bit 7	R	FERR[7]	X
Bit 6	R	FERR[6]	X
Bit 5	R	FERR[5]	X
Bit 4	R	FERR[4]	X
Bit 3	R	FERR[3]	X
Bit 2	R	FERR[2]	X
Bit 1	R	FERR[1]	X
Bit 0	R	FERR[0]	X

FERR[7:0]:

This register indicates the number of DS2 framing bit error events or G.747 framing word errors that occurred during the previous accumulation interval. A DS2 framing bit error event is either an M-bit or and F-bit error. One or more bit errors in a G.747 frame alignment signal results in a single framing word error.

A transfer to the holding register can be triggered by writing to the Global PMON Update Register.

Registers 1046H+20H*N: DS2 FRMR #1-#7 PERR Count (LSB)

Bit	Type	Function	Default
Bit 7	R	PERR[7]	X
Bit 6	R	PERR[6]	X
Bit 5	R	PERR[5]	X
Bit 4	R	PERR[4]	X
Bit 3	R	PERR[3]	X
Bit 2	R	PERR[2]	X
Bit 1	R	PERR[1]	X
Bit 0	R	PERR[0]	X

Registers 1047H+20H*N: DS2 FRMR #1-#7 PERR Count (MSB)

Bit	Type	Function	Default
Bit 7	R	Unused	X
Bit 6	R	Unused	X
Bit 5	R	Unused	X
Bit 4	R	PERR[12]	X
Bit 3	R	PERR[11]	X
Bit 2	R	PERR[10]	X
Bit 1	R	PERR[9]	X
Bit 0	R	PERR[8]	X

PERR[12:0]:

These two registers indicate the number of G.747 parity error events that occurred during the previous accumulation interval.
A transfer operation can be triggered by writing to the Global PMON Update Register.

1.21 MX12 Multiplexer Registers (N=1 to 7)

Registers 1050H+20H*N: MX12 #1-#7Configuration and Control

Bit	Type	Function	Default
Bit 7	R/W	G747	0
Bit 6	R/W	PINV	0
Bit 5	R/W	MINV	0
Bit 4	R/W	FINV	0
Bit 3	R/W	XAIS	0
Bit 2	R/W	XFERF	0
Bit 1	R/W	XRES	0
Bit 0	R/W	INTE	0

INTE:

When set high, the INTE bit enables the MX12 to activate the interrupt output, INTB, whenever any of the LBRI[4:1] bits are set high in the MX12 Loopback Request Interrupt register. MX12 interrupts are masked when INTE is cleared low.

XRES:

The XRES bit only has effect in G.747 mode. When XRES is set high and AIS is not being transmitted, the reserved bit (Set II, bit 3) is set to 0; otherwise, the transmitted reserved bit is set to 1.

XFERF:

When set high, the XFERF bit enables the transmission of the far end receive failure (FERF) signal in the DS2 output stream when in DS2 mode (i.e. G747 bit low). When XFERF is set high, the transmitted X bit is set to 0, provided that AIS is not being transmitted; otherwise the transmitted X bit is set to 1. When in G.747 mode (i.e. G747 bit high), the remote alarm indication (RAI) is set to 1 when XFERF is set high; otherwise, the transmitted RAI bit is set to 0 unless AIS is being transmitted.

XAIS:

When set to a logic 1, the XAIS bit enables the transmission of the alarm indication signal (AIS) in the DS2 stream output on TDAT. When XAIS is set

high, the transmitted data is set to all ones; otherwise the transmitted data is not affected.

FINV:

When FINV is set high and G747 is low, all the transmitted F bits in the DS2 output stream are logically inverted for diagnostic purposes. If G747 is high when FINV is set high, the nine bit frame alignment signal (111010000) is logically inverted (i.e. 000101111).

MINV:

When MINV is set to a logic 1, the transmitted M bits in the DS2 stream output on TDAT are inverted for diagnostic purposes. This only has effect when the G747 bit is low.

PINV:

When PINV is set high, the transmitted parity bit in the G.747 formatted output stream is inverted for diagnostic purposes. This only has effect when the G747 bit is high.

G747:

When G747 is high, the MX12 supports CCITT Recommendation G.747. In this mode, three 2048 kbit/s tributaries are multiplexed into and demultiplex out of an 840-bit frame. If G747 is low, the frame format is compatible with DS2 as specified in the ANSI T1.107 Standard. When G.747 mode is enable every forth T1/E1 framer must be held in reset by setting the RESET bit in the T1/E1 Master Configuration Registers.

Registers 1051H+20H*N: MX12 #1-#7 Loopback Code Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	LBCODE[1]	0
Bit 0	R/W	LBCODE[0]	0

LBCODE[1:0]:

The LBCODE[1:0] bits select the valid state for a loopback request coded in the C-bits of the DS2 signals. Transmit and receive are not independent; the same code is expected in the receive DS2 as is inserted in the transmitted DS2. The following table gives the correspondence between LBCODE[1:0] bits and the valid codes:

LBCODE[1:0]	Loopback Code
00	C1 = C2 and C1 = $\overline{C3}$
01	C1 = C3 and C1 = $\overline{C2}$
10	C2 = C3 and C1 = $\overline{C2}$
11	C1 = C2 and C1 = $\overline{C3}$

If LBCODE[1:0] is 'b00 or 'b11, the loopback code is as per ANSI T1.107a Section 8.2.1 and TR-TSY-000009 Section 3.7

The LBCODE[1:0] bits become logical 0 upon either a hardware or software reset.

The LBCODE[1:0] bits will also select the valid state for a loopback request coded in the C-bits of the G.747 formatted signal. Again, the transmit and receive are not independent; the same code is expected in the demultiplexed G.747 stream as is inserted in the G.747 stream to be multiplexed. The valid codes are the same as those for the DS2 formatted stream given in the table above.

Register 1052H+20H*N: MX12 #1-#7 Mux/Demux AIS Insert

Bit	Type	Function	Default
Bit 7	R/W	MAIS[4]	0
Bit 6	R/W	MAIS[3]	0
Bit 5	R/W	MAIS[2]	0
Bit 4	R/W	MAIS[1]	0
Bit 3	R/W	DAIS[4]	0
Bit 2	R/W	DAIS[3]	0
Bit 1	R/W	DAIS[2]	0
Bit 0	R/W	DAIS[1]	0

DAIS[4:1]:

Setting any of the DAIS[4:1] bits activates insertion of the alarm indication signal (all ones) into the corresponding DS1 stream demultiplexed from the DS2 signal. Demux AIS insertion takes place after the point where remote loopback may be invoked using the Loopback Activate register, thus allowing demux AIS to be inserted into the through path while a loopback is activated.

MAIS[4:1]:

Setting any of the MAIS[4:1] bits activates insertion of the alarm indication signal (all ones) into the corresponding DS1 stream multiplexed into the DS2 signal. Mux AIS insertion takes place before the point where remote loopback may be invoked using the Loopback Activate register and thus mux AIS cannot be inserted while a loopback is activated.

Registers 1053H+20H*N: MX12 #1-#7 Loopback Activate

Bit	Type	Function	Default
Bit 7	R/W	ILBR[4]	0
Bit 6	R/W	ILBR[3]	0
Bit 5	R/W	ILBR[2]	0
Bit 4	R/W	ILBR[1]	0
Bit 3	R/W	LBA[4]	0
Bit 2	R/W	LBA[3]	0
Bit 1	R/W	LBA[2]	0
Bit 0	R/W	LBA[1]	0

LBA[4:1]:

Setting any of the LBA[4:1] bits activates loopback of the corresponding stream from the DS2 signal received to the DS2 signal transmitted. The demultiplexed DS1 streams continue to present valid payloads while loopbacks are activated. The AIS Insert Register allows insertion of AIS if required. LBA[4] has no effect in G.747 mode, but LBA[3:1] activates the loopback of the corresponding 2048 kbit/s signal.

ILBR[4:1]:

Setting any of the ILBR[4:1] bits enables the insertion of a loopback request in the corresponding DS1 streams in the DS2 output signal. The loopback is indicated by inverting the C_{j1}, C_{j2} or C_{j3} bits according to the format of the loopback request is determined by the LBCODE[1:0] bits in the Loopback Code Select Register. In G.747 mode, ILBR[j] inverts bit C_{j1}, C_{j2} or C_{j3} in the G.747 frame in an analogous fashion.

Register 1054H+20H*N: MX12 #1-#7 Loopback Interrupt

Bit	Type	Function	Default
Bit 7	R	LBRI[4]	0
Bit 6	R	LBRI[3]	0
Bit 5	R	LBRI[2]	0
Bit 4	R	LBRI[1]	0
Bit 3	R	LBRD[4]	0
Bit 2	R	LBRD[3]	0
Bit 1	R	LBRD[2]	0
Bit 0	R	LBRD[1]	0

LBRD[4:1]:

The LBRD[4:1] bits are a logic 1 while a loopback request is detected for the corresponding DS1 stream in the received DS2 signal. The LBRD[4:1] bits are a logic 0 otherwise. The format of the loopback request expected is determined by the LBCODE[1:0] bits in the Loopback Code Select Register. As per TR-TSY-000009 Section 3.7, the loopback request must be present for five successive M-frames before declaration of detection. Removal of the loopback request is declared when it has been absent for five successive M-frames. LBRD[4] is not used in G747 mode.

LBRI[4:1]:

The LBRI[4:1] bits are a logic 1 when a loopback request is asserted or deasserted for the corresponding DS1 stream in the received DS2 signal. The LBRI[4:1] bits are set to a logic 1 whenever the corresponding LBRD[4:1] bits change state. If interrupts are enabled using the INTE bit in the Configuration register then the interrupt output, INTB, is activated. The LBRI[4:1] bits are set to a logic 0 immediately following a read of this register, acknowledging the interrupt and deactivating the INT output. LBRI[4] is not used in G747 mode.

1.22 SONET/SDH Mapper Master Configuration Registers

Register 1200H: SONET/SDH Master Configuration

Bit	Type	Function	Default
Bit 7	R/W	VTMPRST	0
Bit 6	R/W	DS3MPRST	0
Bit 5	R/W	LADDOE	0
Bit 4	R/W	LADDSEL1	0
Bit 3	R/W	LADDSEL0	0
Bit 2	R/W	LDROPSEL1	0
Bit 1	R/W	LDROPSEL0	0
Bit 0	R/W	RESET	0

RESET:

The RESET bit allows software to hold the SONET/SDH mapper in a reset condition. When RESET is a logic 1 the SONET/SDH mapper will be held in a reset state which is also a low power state. This will force all registers to their default state with the exception of this register, 1200H, which is not reset when this RESET bit is a logic 1. While in reset the clocks can not be guaranteed accurate or existing. When RESET is a logic 0 the SONET/SDH mapper is in normal operating mode. The SONET/SDH mapper is by default in the operational state. This register is only reset by the hardware device reset and not by this RESET register bit.

LDROPSEL[1:0]:

The Line DROP Bus select bits, LDROPSEL[1:0], determine where in the SONET/SDH Line side drop interface the tributaries will be demapped. When LDROPSEL[1:0] is set to logic 0 the line side interface demapper, RTDM, will have access to all tributaries in the STS-3/STM-1 and will receive a subset of these links as determined by tributaries selected in the RTDM mapping registers. When dropping tributaries from the full STS-3/STM-1 the VTPP must be bypassed with the IVTPPBYP bit in the SONET/SDH Master Ingress Configuration register. All non-zero values in LDROPSEL[1:0] limit the selection of tributaries within the telecom drop bus SPE as shown in the following table:

LDROPSEL[1:0]	Telecom Drop Bus Interface SPE Selection
00	Full STS-3/STM-1
01	SPE #1
10	SPE #2
11	SPE #3

LADDSEL[1:0]:

The Line ADD Bus select bits, LADDSEL[1:0], determine which SPE the Line side interface will insert its tributaries. When LADDSEL[1:0] is set to logic 0 the line side interface will drive selected tributaries on the telecom add bus as determined by tributaries selected in the TTMP mapping registers. When adding tributaries into the full STS-3/STM-1 the egress VTPP must be bypassed with the EVTPPBYP bit in the SONET/SDH Master Egress VTPP Configuration register. All non-zero values in LADDSEL[1:0] will only allow the TEMAP to drive the telecom add bus during the selected SPE as shown in the following table:

LADDSEL[1:0]	Telecom Add Bus Interface SPE Selection
00	Full STS-3/STM-1 (bypass VTPP)
01	SPE #1
10	SPE #2
11	SPE #3

To avoid contention on the Telecom Add bus the LADDSEL[1:0] should only be changed after a LAC1 frame pulse has been received. The reason for this is that on power up the TEMAP assumes an arbitrary LAC1 alignment. In systems with multiple TEMAPs which have all assumed some arbitrary alignment, SPE #1 in one device may contend with SPE #2 in another device. In order to avoid bus cnotention when all Add bus devices are synchronized by LAC1, no two devices should be assigned the same SPE number at the same time. During reconfigurations setting LADDSEL[1:0] to “00” with all tributaries disabled via the TTMP LAOE register bits will ensure that a device is removed from the bus and therefore prevent bus contention.

LADDOE:

The Line ADD Bus output enable signal, LADDOE, enables the Line ADD bus for use with an external multiplexer to merge the ADD busses from multiple TEMAPs. When LADDOE is a logic 1 the Line ADD Bus signals are driven permanently and the LAOE signal is driven whenever the data on the line

ADD bus is valid. When LADDOE is a logic 0 the Line ADD Bus signals are driven only during valid data and are otherwise tristated. In DS3 mapping mode, LADDOE must be set to logic 1.

DS3MPRST:

The DS3 mapper reset bit allows independent reset control over the DS3 mappers. The reset to the DS3 mapper blocks is the OR of this bit and the RESET bit in this register. This bit is useful for putting the DS3 mappers in a low power reset mode when the VT/TU mappers are being used. When DS3MPRST is a logic 1 the DS3 mapper blocks are held in reset. When DS3MPRST is a logic 0 the DS3 mapper blocks are in normal operating mode.

VTMPRST:

The VT/TU mapper reset bit allows independent reset control over the VT/TU mapper blocks. The reset to the VT/TU mapper blocks is the OR of this bit and the RESET bit in this register. This bit is useful for putting the VT/TU mapper blocks in a low power reset mode when the DS3 mappers are being used. When VTMPRST is a logic 1 the VT/TU mapper blocks are held in reset. When VTMPRST is a logic 0 the VT/TU mapper blocks are in normal operating mode.

Register 1201H: SONET/SDH Master Ingress Configuration

Bit	Type	Function	Default
Bit 7	R/W	LDPE	0
Bit 6	R/W	ITMFEN	0
Bit 5	R/W	IVTPPBYP	0
Bit 4	R/W	ITSEN	0
Bit 3	R/W	INCLDPL	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	LDOP	0
Bit 0	R/W	ICONCAT	0

This register configures the TEMAP functionality that are related to the ingress SONET/SDH data stream.

ICONCAT:

When set high, the ICONCAT bit configures the telecom drop bus of the TEMAP to operate in AU4 mode. When the ICONCAT bit is set to 0, the telecom drop bus operates in AU3 mode (or equivalently, STS-1 mode) and the LDC1J1V1 input is expected to mark every J1 byte of each SPE. When ICONCAT is set to 1, the telecom drop bus operates in AU4 mode and the LDC1J1V1 input is expected to mark the J1 of the VC4. The J1 is stretched to provide a J1 to the VTPP whether it is configured for TUG3 #1, 2 or 3. When ICONCAT is set to AU4 mode the ingress VTPP must be configured for TUG3 operation via the ITUG3 bit in the SONET/SDH Master Ingress VTPP Configuration register.

LDOP:

The LDOP bit controls the expected parity on the incoming parity signal LDDP. When LDOP is set high, the parity of the parity signal set, together with LDDP is expected to be odd. When LDOP is set low, the expected parity is even. Membership of the parity signal set always includes LDDATA[7:0], and may include input signals LDPL as controlled by the INCLDPL bit..

Reserved:

This bit is reserved and must be left at logic 0 for proper operation.

INCLDPL:

The INCLDPL bit controls the whether the LDPL input signal participates in the incoming parity calculations. When INCLDPL is set high, the parity signal set includes the LDPL input. When INCLDPL is set low, parity is calculated without regard to the state of LDPL. Selection of odd or even parity is controlled by the LDOP bit.

ITSEN:

The Ingress Time Switch Enable register bit, ITSEN, controls the time switch function in the RTDM block. When ITSEN is a logic 0 the RTDM is not enabled to perform switching of the tributaries and all tributaries are fixed in a one-to-one mapping from a single STS-1 SPE, STM-1 VC3 or STM-1 TUG-3. This is necessary when the ingress tributaries are being processed by the VTPP block as controlled by the IVTPPBYP register bit. When ITSEN is a logic 1 the RTDM is enabled to select up to 28 T1 or 21 E1 tributaries from the entire STM-1 AU4 or STS-3 arriving on the Line Drop Side Telecom bus. This requires the VTPP to be bypassed using the IVTPPBYP register bit.

IVTPPBYP:

The Ingress VTPP bypass select bit, IVTPPBYP, configures the Line Side Telecom Drop bus to bypass the ingress VTPP and go directly into the RTDM. This is possible only when the Line Side Telecom Drop bus is processed outside the TEMAP, such as when connecting through an external TUPP-PLUS. When IVTPPBYP is a logic 1 the ingress VTPP will be bypassed. The data on the telecom bus must be preprocessed such that the J1 octet is in a fixed location and the LDV5, LDPL and LDTPL signals are valid. When IVTPPBYP is a logic 0 the ingress VTPP will perform pointer processing on a single STS-1 SPE, STM-1 VC3 or STM-1 TUG-3. When using the ingress VTPP the Line Side Telecom Drop bus has no restrictions on any pointer alignments. When the ingress VTPP is bypassed the RTOP is also bypassed. When the Ingress VTPP is bypassed, the OTUG3 bit in the SONET/SDH Master Ingress VTPP Configuration register must match the external telecom bus interface.

ITMFEN:

When set high, the ITMFEN bit enables the TEMAP to use the corresponding LDC1J1V1 input to locate tributary multiframe boundaries. When ITMFEN is set to 1 the H4 bytes in the incoming data stream are ignored by the VTPP. When ITMFEN is set to 0, the ingress VTPP processes the H4 bytes to locate the multiframe boundaries and the V1 indication is ignored.

LDPE:

The LDPE bit is an active high interrupt enable. When LDPE is set high, the occurrence of a parity error on the Line Side Drop Telecom bus parity signal set will cause an interrupt to be asserted on the interrupt (INTB) output. When LDPE is set low, incoming parity errors will not cause an interrupt.

Register 1202H: SONET/SDH Master Egress Configuration

Bit	Type	Function	Default
Bit 7	R/W	LOCK0	0
Bit 6	R/W	ETSEN	0
Bit 5	R/W	LAJ1EN	0
Bit 4	R/W	LAV1EN	0
Bit 3	R/W	INCLAPL	0
Bit 2	R/W	INCLAC1J1V1	0
Bit 1	R/W	LAOP	0
Bit 0	R/W	ECONCAT	0

This register configures the TEMAP functionality that are related to the egress data stream.

ECONCAT:

When set high, the ECONCAT bit configures the telecom add bus of the TEMAP to operate in AU4 mode. When the ECONCAT bit is set to 0, the telecom add bus operates in AU3 mode (or equivalently, STS-1 mode) and the LAC1J1V1 input marks every J1 byte of each SPE. When ECONCAT is set to 1, the telecom add bus operates in AU4 mode and the LAC1J1V1 input is marks the J1 of the VC4. The J1 is stretched to provide a J1 for TUG3 #1, 2 and 3.
When ECONCAT is set to AU4 mode the egress VTPP must be configured for TUG3 operation via the OTUG3 bit in the SONET/SDH Master Egress VTPP Configuration register.

LAOP:

The LAOP bit controls the parity placed on the egress parity signal LADP. When LAOP is set low, the parity of outgoing data stream LADATA[7:0], together with LADP is even. When LAOP is set high, the parity is odd.

INCLAC1J1V1:

The INCLAC1J1V1 bit controls whether the LAC1J1V1 signal participates in the egress parity calculations. When INCLAC1J1V1 is set high, the parity signal set includes the LAC1J1V1 output. When INCLAC1J1V1 is set low, parity is calculated without regard to the state of LAC1J1V1. Selection of odd or even parity is controlled by the LAOP bit.

INCLAPL:

The INCLAPL bit controls the whether the LAPL signal participates in the egress parity calculations. When INCLAPL is set high, the parity signal set includes the LAPL output. When INCLAPL is set low, parity is calculated without regard to the state of LAPL. Selection of odd or even parity is controlled by the LAOP bit.

LAV1EN:

The Line Side Telecom Add bus V1 enable bit, LAV1EN, controls the identification of the third byte after J1. When LAV1EN is set low, the LAC1J1V1 output only indicates the C1 and optionally J1 bytes. The third byte after J1 is not indicated. When LAV1EN is set high, the LAC1J1V1 output indicates the C1, optionally J1 and the third byte after J1.

LAJ1EN:

The Line Side Telecom Add bus J1 enable bit, LAJ1EN, controls the identification of the J1 byte in addition to the C1 byte. When LAJ1EN is set low, the LAC1J1V1 output only indicates the C1 byte and optionally the third byte after the J1 if LAV1EN is set high. When LAJ1EN is set high, the LAC1J1V1 output indicates the C1, J1 and optionally the third byte after J1.

ETSEN:

The Egress Time Switch Enable register bit, ETSEN, overrides the time switch function in the TTMP block. When ETSEN is a logic 0 the TTMP is not enabled to perform switching of the tributaries and all tributaries are fixed in a one-to-one mapping from a single STS-1 SPE, STM-1 VC3 or STM-1 TUG-3. This is necessary when the egress tributaries are being processed by the egress VTPP block as controlled by the EVTPPBYP register bit. When ETSEN is a logic 1 the TTMP is enabled to generate up to 28 T1 or 21 E1 tributaries across the entire STM-1 AU4 or STS-3 on the Line Add Side Telecom bus. This requires the egress VTPP to be bypassed using the EVTPPBYP register bit.

LOCK0:

The LOCK0 bit controls the SPE payload offset of the line side Telecom Add bus when the egress VTPP is not bypassed. When LOCK0 is logic 1 the H1,H2 pointer is set to zero and the first byte of the SPE (J1) will occur immediately after H3. When LOCK0 is a logic 0 the H1,H2 pointer is set to 522 and the first byte of the SPE will occur immediately after C1.
When using the TEMAP with Transparent VTs between the SBI bus and the line side telecom bus LOCK0 must be set to 0 such that J1 immediately follows C1.

Register 1203H: SONET/SDH Master Ingress VTPP Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	SOS	0
Bit 5	R/W	MONIS	0
Bit 4	R/W	ICODE	0
Bit 3	R/W	NOFILT	0
Bit 2		Unused	X
Bit 1	R/W	ITUG3	0
Bit 0	R/W	OTUG3	0

This register is used to enable the processing of a STS-1 (TUG3) and configure the major operational modes of the ingress VTPP.

OTUG3:

When set high, the OTUG3 bit configures the ingress tributary payload processor, ingress VTPP, to process TUG2s that have been mapped into a TUG3 in the outgoing data stream connecting to the internal SONET/SDH blocks. When low, the tributary payload processor defaults to processing TUG2s that have been mapped into a VC3, or equivalently, VT groups that have been mapped into an STS-1. When passing transparent VTs between the line side Telecom bus and the system side SBI bus, OTUG3 must be configured for TUG2s mapped into a TUG3 by setting this bit high. When the ingress VTPP is bypassed this bit must be set to match the format of the external telecom drop bus.

ITUG3:

When set high, the ITUG3 bit configures the ingress tributary payload processor to process TUG2s that have been mapped into a TUG3 in the incoming data stream. When low, the tributary payload processor defaults to processing TUG2s that have been mapped into a VC3, or equivalently, VT groups that have been mapped into an STS-1. When processing a TUG3 the ICONCAT bit must also be set high. When the ingress VTPP is not bypassed this bit must be set to match the format of the external telecom drop bus.

NOFILT:

The NOFILT bit controls the processing of incoming tributary pointers. When a logic 0 is written to this location, illegal variations from normal tributary pointer value (i.e. changes which do not correspond to pointer justification events, and are not accompanied by a new data flag) are ignored unless a consistent new value is received three times consecutively. When a logic 1 is written to this location, variations take effect immediately and are passed through the payload buffer unfiltered.

ICODE:

The ICODE bit controls the value inserted into tributary bytes when idle insertion is enabled. When a logic 0 is written to this location, the idle code is chosen to be all zeros. Setting ICODE to 1 sets the idle code to all ones. Idle insertion only affects the tributary payload bytes which are overwritten with the selected idle pattern. The outgoing pointer remains a function of the incoming pointer and the relative multiframe alignment of the incoming and outgoing streams. ICODE has no effect on pointer processing.

MONIS:

The MONIS bit controls the source of pointer justification interrupts. When MONIS is set high, the incoming stream is monitored for tributary pointer justification events. When MONIS is set low, the outgoing stream is monitored for pointer justification events. Interrupts can be optionally generated upon a pointer justification event in the monitored stream.

SOS:

The SOS bit controls the spacing between consecutive pointer justification events on the incoming stream. When SOS is set high, the definition of inc_ind and dec_ind indications includes the requirement that active offset changes have occurred at least three frames ago. When SOS is set low, pointer justification indications in the incoming stream are followed without regard to the proximity of previous active offset change.

Register 1204H: SONET/SDH Master Egress VTPP Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	EVTPPBYP	0
Bit 2	R/W	EPTRBYP	0
Bit 1	R/W	ITUG3	0
Bit 0	R/W	OTUG3	0

This register configures additional TEMAP functionality that are related to the egress data stream.

OTUG3:

When set high, the OTUG3 bit configures the egress tributary payload processor, egress VTPP, to process TUG2s that have been mapped into a TUG3 in the outgoing data stream on the telecom add bus. When low, the tributary payload processor defaults to processing TUG2s that have been mapped into a VC3, or equivalently, VT groups that have been mapped into an STS-1. When the egress VTPP is not bypassed this bit must be set to match the format of the external telecom add bus.

ITUG3:

When set high, the ITUG3 bit configures the egress tributary payload processor to process TUG2s that have been mapped into a TUG3 in the incoming data stream. When low, the tributary payload processor defaults to processing TUG2s that have been mapped into a VC3, or equivalently, VT groups that have been mapped into an STS-1. When passing transparent VTs between the system side SBI bus and the line side Telecom bus, ITUG3 must be configured for TUG2s mapped into a TUG3 by setting this bit high. When the egress VTPP is bypassed this bit must be set to match the format of the external telecom add bus.

EPTRBYP:

When set high, the EPTRBYP bit configures the egress VTPP to bypass pointer interpretation for all transparent virtual tributaries. Pointer

interpretation bypass is necessary for transparent VTs which do not have valid V1,V2 pointers. Two types of transparent VTs are possible, those without pointers but with V5 indications and those with pointers and no V5 indications. When EPTRBYP is a logic 0 the transparent VTs entering the egress VTPP must have valid pointers. When EPTRBYP is a logic 1 the transparent VTs entering the egress VTPP do not need valid pointers but must have a valid V5 indication. In either pointer bypass configuration, tributaries from the TTMP tributary bit asynchronous mapper will be able to pass through the VTPP. For individual tributary control of egress VTPP pointer bypass the ETVTPTRDIS bits should be set in the TTMP Control registers.

EVTPPBYP:

The egress VTPP bypass select bit, EVTPPBYP, configures the TEMAP to bypass the egress VTPP and connect directly to the Line Side Telecom Add bus. When EVTPPBYP is a logic 1 the egress VTPP will be bypassed. When bypassing the egress VTPP the Line Side Telecom Add bus must be able to accept a J1 at a pointer offset of either 0 or 522. When EVTPPBYP is a logic 0 the egress VTPP will perform pointer processing on a single STS-1 SPE, STM-1 VC3 or STM-1 TUG-3. When using the egress VTPP the Line Side Telecom Add bus has no restrictions on any pointer alignments. When the egress VTPP is bypassed the ITUG3 bit in this register must be set to match the format of the external telecom add bus.

Register 1205H: SONET/SDH Master RTOP Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	RDI10	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	1

This register configures the operation of RTOP.

Reserved:

These bit are reserved and must be set to their default values.

RDI10:

The RDI10 bit controls the number of times the tributary path RDI, RFI or the extended RDI code is filtered before being accepted. When RDI10 is set high, the RDI bit, the RFI bit or the extended RDI code is filtered for ten occurrences. When RDI10 is set low, the RDI bit, the RFI bit or the extended RDI code is filtered for five occurrences.

Register 1206H: SONET/SDH Master Tributary Alarm AIS Control

Bit	Type	Function	Default
Bit 7	R/W	LOMAIS	0
Bit 6	R/W	LOPAIS	0
Bit 5		Unused	X
Bit 4	R/W	UNEQAIS	0
Bit 3	R/W	PSLMAIS	0
Bit 2	R/W	PSLUAIS	0
Bit 1		Unused	X
Bit 0	R/W	Reserved	0

This register controls the insertion of ingress tributary path AIS as a result of tributary path signal label alarms and tributary multiframe alarms. It also controls the insertion of egress tributary alarms as a result of SBI bus alarm indications.

Reserved:

This bit is reserved and must be set to logic 0 for proper operation.

PSLUAIS:

The PSLUAIS bit is an active high AIS insertion enable. When PSLUAIS is set high, AIS is automatically generated on the ingress data stream for all tributaries that are in path signal label unstable state. When PSLUAIS is set low, the generation of AIS on the ingress data stream is inhibited. The negation of AIS occurs at tributary multiframe boundaries.

PSLMAIS:

The PSLMAIS bit is an active high AIS insertion enable. When PSLMAIS is set high, AIS is automatically generated on the ingress data stream for all tributaries that are in path signal label mismatch state. When PSLMAIS is set low, the generation of AIS on the ingress data stream is inhibited. The negation of AIS occurs at tributary multiframe boundaries. Note that the generation of AIS is inhibited in the unequipped state (i.e. when UNEQ is “active”), regardless of the PSLM state.

UNEQAIS:

The UNEQAIS bit is an active high AIS insertion enable. When UNEQAIS is set high, AIS is automatically generated on the ingress data stream for all

tributaries that are unequipped. When UNEQAIS is set low, the generation of AIS on the outgoing data stream is inhibited. The negation of AIS occurs at tributary multiframe boundaries.

LOPAIS:

The LOPAIS bit is an active high AIS insertion enable. When LOPAIS is set high, AIS is automatically generated on the ingress data stream for all tributaries that are in loss of pointer state. When LOPAIS is set low, the generation of AIS on the ingress data stream is inhibited. The negation of AIS occurs at tributary multiframe boundaries.

LOMAIS:

The LOMAIS bit is an active high AIS insertion enable. When LOMAIS is set high, AIS is automatically generated on the ingress data stream for all tributaries that are in loss of tributary multiframe state. When LOMAIS is set low, the generation of AIS on the ingress data stream is inhibited.

Register 1207H: SONET/SDH Master Tributary Remote Defect Indication Control

Bit	Type	Function	Default
Bit 7	R/W	LOMRDI	0
Bit 6	R/W	LOPRDI	0
Bit 5	R/W	AISRDI	0
Bit 4	R/W	UNEQRDI	0
Bit 3	R/W	PSLMRDI	0
Bit 2	R/W	PSLURDI	0
Bit 1		Unused	X
Bit 0		Unused	X

This register controls the insertion of tributary path RDI to the egress Tributary Alarm Processor, TRAP, and optionally on the Ingress V5 byte, as a result of tributary pointer alarms, tributary path signal label alarms and tributary multiframe alarms. The Egress AIS registers in the TRAP module must be set correctly, in addition to setting this register, for RDI insertion.

PSLURDI:

The PSLURDI bit is an active high RDI insertion enable. When PSLURDI is set high, RDI is reported to TRAP and optionally in the V5 byte of the ingress data stream for all tributaries that are in path signal label unstable state. When PSLURDI is set low, reporting of RDI due to PSLU is inhibited.

PSLMRDI:

The PSLMRDI bit is an active high RDI insertion enable. When PSLMRDI is set high, RDI is reported to TRAP and optionally in the V5 byte of the ingress data stream for all tributaries that are in path signal label mismatch state. When PSLMRDI is set low, reporting of RDI due to PSLM is inhibited. Note that the generation of RDI is inhibited in the unequipped state (i.e. when UNEQ is “active”), regardless of the PSLM state.

UNEQRDI:

The UNEQRDI bit is an active high RDI insertion enable. When UNEQRDI is set high, RDI is reported to TRAP and optionally in the V5 byte of the ingress data stream for all tributaries that are in unequipped state. When UNEQRDI is set low, reporting of RDI due to UNEQ is inhibited. When there is a match

of 000 between the expected PSL and the accepted PSL an AIS cannot be inserted, even if the UNEQRDI bit is set high.

AISRDI:

The AISRDI bit is an active high RDI insertion enable. When AISRDI is set high, RDI is reported to TRAP and optionally the V5 byte of the outgoing data stream for all tributaries that are in incoming AIS state. When AISRDI is set low, reporting of RDI due to AIS is inhibited.

LOPRDI:

The LOPRDI bit is an active high RDI insertion enable. When LOPRDI is set high, RDI is reported to TRAP and optionally the V5 byte of the outgoing data stream for all tributaries that are in loss of pointer state. When LOPRDI is set low, reporting of RDI due to LOP is inhibited.

LOMRDI:

The LOMRDI bit is an active high RDI insertion enable. When LOMRDI is set high, RDI is reported to TRAP and optionally in the V5 byte of the outgoing data stream for all tributaries that are in loss of multiframe state. When LOMRDI is set low, reporting of RDI due to LOM is inhibited.

Register 1208H: SONET/SDH Master Tributary Auxiliary Remote Defect Indication Control

Bit	Type	Function	Default
Bit 7	R/W	NOLOMARDI	1
Bit 6	R/W	NOLOPARDI	1
Bit 5	R/W	NOAISARDI	1
Bit 4	R/W	UNEQARDI	0
Bit 3	R/W	PSLMARDI	0
Bit 2	R/W	PSLUARDI	0
Bit 1		Unused	X
Bit 0		Unused	X

This register controls the insertion of tributary path auxiliary RDI to the egress Tributary Alarm Processor, TRAP, and optionally on the V5 byte as a result of tributary pointer alarms, tributary path signal label alarms and tributary multiframe alarms. The Egress AIS registers in the TRAP module must be set correctly, in addition to setting this register, for auxiliary RDI insertion.

PSLUARDI:

The PSLUARDI bit is an active high auxiliary RDI insertion enable. When PSLUARDI is set high, ARDI is reported to TRAP and optionally in the V5 byte of the outgoing data stream for all tributaries that are in path signal label unstable state. When PSLUARDI is set low, reporting of auxiliary RDI due to PSLU is inhibited.

PSLMARDI:

The PSLMARDI bit is an active high auxiliary RDI insertion enable. When PSLMARDI is set high, ARDI is reported to TRAP and optionally in the V5 byte of the outgoing data stream for all tributaries that are in path signal label mismatch state. When PSLMARDI is set low, reporting of auxiliary RDI due to PSLM is inhibited. Note that the generation of ARDI is inhibited in the unequipped state (i.e. when UNEQ is “active”), regardless of the PSLM state.

UNEQARDI:

The UNEQARDI bit is an active high auxiliary RDI insertion enable. When UNEQARDI is set high, ARDI is reported to TRAP and optionally in the V5 byte of the outgoing data stream for all tributaries that are in unequipped

state. When UNEQARDI is set low, the reporting of auxiliary RDI for unequipped tributaries is inhibited.

NOLOPARDI:

The NOLOPARDI bit is an active high auxiliary RDI insertion disable. When NOLOPARDI is set high, ARDI is not reported to TRAP nor in the V5 of the outgoing data stream for all tributaries that are in loss of pointer state. NOLOPARDI has precedence over UNEQARDI, PSLUARDI and PSLMARDI. When NOLOPARDI is set low, reporting of RDI is according to UNEQARDI, PSLUARDI and PSLMARDI and the associated alarm states.

NOAISARDI:

The NOAISARDI bit is an active high auxiliary RDI insertion disable. When NOAISARDI is set high, auxiliary RDI is not reported to TRAP nor in the V5 byte of the outgoing data stream for all tributaries that are in incoming AIS state. NOAISARDI has precedence over UNEQARDI, PSLUARDI and PSLMARDI. When NOAISARDI is set low, reporting of RDI is according to UNEQARDI, PSLUARDI and PSLMARDI and the associated alarm states.

NOLOMARDI:

The NOLOMARDI bit is an active high auxiliary RDI insertion disable. When NOLOMARDI is set high, ARDI is not reported to TRAP nor in the V5 byte of the outgoing data stream for all tributaries that are in loss of multiframe state. When NOLOMARDI is set low, reporting of RDI is according to UNEQARDI, PSLUARDI and PSLMARDI and the associated alarm states.

Register 1209H: SONET/SDH Master DS3 Clock Generation Control

Bit	Type	Function	Default
Bit 7	R/W	FASTCLKFREQ	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	SC1FPEN	0

FASTCLKFREQ:

The Fast Clock Frequency select bit indicates the frequency of the CLK52M reference clock connected to the TEMAP DS3 mappers. When FASTCLKFREQ is set high the CLK52M reference clock is selected to be 51.84MHz. When FASTCLKFREQ is set low the CLK52M reference clock is selected to be 44.928MHz. This setting must match the FASTCLKFREQ bit in the SBI Master Configuration register.

SC1FPEN:

The SC1FP enable bit controls whether the internal VT/TU mapper blocks use the SBI bus SC1FP frame pulse for synchronization or the line side telecom bus LAC1 and LDC1J1V1 signals for frame synchronization. When SC1FPEN is '0', SC1FP is not used by the VT/TU mapper. When SC1FPEN is '1', SC1FP is used by the VT/TU mapper blocks and SREFCLK must be the same as LREFCLK.

Normally the VT/TU blocks are synchronized to the telecom bus frame signals but when Transparent VT's are enabled between the SBI bus and the line side telecom bus, SREFCLK must be the same as LREFCLK and SC1FPEN must be set to “1”. This is required so that the VT/TU mapped tributaries align with the SBI bus transparent VTs.

When transparent VTs are enabled within a single SPE identified by LADDSEL[1:0] and LDROPSEL[1:0] and the VTPPs are enabled to re-align the tributaries, there is no assumed relationship between LDC1J1V1, SC1FP and LAC1. In this case SC1FPEN must be set to “1”, the external frame alignment pulses can occur anywhere and the VTPPs will align the SC1FP frame alignment with LAC1 and LDC1J1V1 frame alignment.

When transparent VTs are enabled across the entire STS-3 (LADDSEL[1:0] and LDROPSEL[1:0] are set to “00”) or the VTPPs are bypassed, then there is a relationship between LDC1J1V1, SC1FP and LAC1. In this case there must be a fixed offset of four LREFCLK/SREFCLK cycles from LDC1J1V1 to SC1FP, a fixed offset of 13 clock cycles from SC1FP to LAC1, and SC1FPEN can be configured either way since the external frame alignment signals are already forced to synchronized offsets.

When there are no transparent VTs enabled, then SREFCLK and LREFCLK do not need to be the same. When SREFCLK and LREFCLK are not the same clock then SC1FPEN must be set to “0”.

Register 120AH: SONET/SDH Master Loopback Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	DLOOP	0
Bit 0	R/W	LLOOP	0

LLOOP:

The LLOOP bit puts the Telecom Bus interface into Line Loopback mode. When LLOOP is a logic 1 the selected ingress STS-1 SPE, STM-1/VC4 TUG-3 or STM-1/VC3 will be looped back out the egress telecom bus. When LLOOP is a logic 0 no line loopback will be preformed.

DLOOP:

The DLOOP enables a diagnostic loopback at the telecom bus interface. When DLOOP is a logic 1 then entire egress STS-3 or STM-1 is looped back to the ingress data path. When DLOOP is a logic 0 no diagnostic loopback will be performed.

Reserved:

This bit must be set to a logic 0 for correct operation of the TEMAP.

Register 120BH: SONET/SDH Telecom Bus Signal Monitor, Accumulation Trigger

Bit	Type	Function	Default
Bit 7	R	RADWESTA	X
Bit 6	R	RADEASTA	X
Bit 5	R	LAC1	X
Bit 4	R	LDDA	X
Bit 3	R	LDV5	X
Bit 2	R	LDTPLA	X
Bit 1	R	LDPLA	X
Bit 0	R	LDC1J1V1A	X

When a monitored Telecom Bus signal makes a low to high transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point all the bits in this register are cleared. A lack of transitions is indicated by the corresponding register bit reading low. This register should be read at periodic intervals to detect clock failures.

Writing to this register delimits the accumulation intervals in the RTOP accumulation registers. Counts accumulated in those registers are transferred to holding registers where they can be read. The counters themselves are then cleared to begin accumulating events for a new accumulation interval. To prevent loss of data, accumulation intervals must be 0.5 second or shorter. The bits in this register are not affected by write accesses.

LDC1J1V1A:

The LDC1J1V1 active, LDC1J1V1A, bit monitors for low to high transitions on the LDC1J1V1 input. LDC1J1V1A is set high on a rising edge of LDC1J1V1, and is set low when this register is read.

LDPLA:

The LDPL active, LDPLA, bit monitors for low to high transitions on the LDPL input. LDPLA is set high on a rising edge of LDPL, and is set low when this register is read.

LDTPLA:

The LDTPL active, LDTPLA, bit monitors for low to high transitions on the LDTPL input. LDTPLA is set high on a rising edge of LDTPL, and is set low when this register is read.

LDV5A:

The LDV5 active, LDV5A, bit monitors for low to high transitions on the LDV5 input. LDV5A is set high on a rising edge of LDV5, and is set low when this register is read.

LDDA:

The LDDATA bus active, LDDA, bit monitors for low to high transitions on the LDDATA[7:0] bus. LDDA is set high when a rising edge has been observed on each signal on the LDDATA [7:0] bus with no interveaning reads of this regiater. LDDA is set low when this register is read.

LAC1A:

The LAC1 active, LAC1A, bit monitors for low to high transitions on the LAC1 input. LAC1A is set high on a rising edge of LAC1, and is set low when this register is read.

RADEASTA:

The RADEASTCK active, RADEASTA, bit detects low to high transitions on the RADEASTCK input. RADEASTA is set high on a rising edge of RADEASTCK, and is set low when this register is read.

RADWESTA:

The RADWESTCK active, RADWESTA, bit detects low to high transitions on the RADWESTCK input. RADWESTA is set high on a rising edge of RADWESTCK, and is set low when this register is read.

1.23 VTPP Ingress Tributary Payload Processor Registers

Register 1240H: VTPP Ingress, TU #1 in TUG2 #1, Configuration and Status

Bit	Type	Function	Default
Bit 7	R/W	Reserved	1
Bit 6	R/W	TU11	1
Bit 5	R/W	PF	0
Bit 4	R	LOPV	X
Bit 3	R/W	ALARME	0
Bit 2	R/W	DLOP	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	IPAIS	0

This register reports the status and configures the operational modes of TU #1 in TUG2 #1.

IPAIS:

The IPAIS bit enables the insertion of path AIS for tributary TU #1 in TUG2 #1. Tributary path AIS is inserted by forcing all ones into all tributary bytes.

DLOP:

The DLOP bit allows downstream pointer processing elements to be diagnosed. When DLOP is set high, the new data flag (NDF) field of the outgoing payload pointer in tributary TU #1 in TUG2 #1 is inverted to cause downstream pointer processing elements to enter a loss of pointer state. Insertion of an inverted new data flag can occur in concert with the insertion of a normal idle (unequipped) indication. The DLOP bit has no effect when the IPAIS bit is set high.

ALARME:

The ALARME bit enables loss of pointer and path AIS interrupts for tributary TU #1 in TUG2 #1. When ALARME is set high, an interrupt is generated upon entry to and exit from the LOP and AIS state of the pointer interpreter state diagram. Interrupts due to AIS and LOP status change are masked when ALARME is set low.

LOPV:

The LOPV bit indicates the loss of pointer status of tributary TU #1 in TUG2 #1.

PF:

The PF bit enables pointer follower mode for tributary TU #1 in TUG2 #1. In pointer follower mode, the tributary FIFO dead-zone is collapsed so that any variation in FIFO depth will result in an outgoing pointer justification event. Any TU pointer justification event on the corresponding incoming tributary, or an AU pointer justification event affecting this tributary will cause an outgoing pointer justification event.

TU11:

The TU11 bit specifies the tributary configuration of tributary group TUG2 #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

Bit 7 must be kept at a logic 1 for proper operation of the TEMAP while bit 1 must be kept to logic 0.

Register 1241H: VTPP Ingress, TU #1 in TUG2 #1, Alarm Status

Bit	Type	Function	Default
Bit 7	R	SS[1]	X
Bit 6	R	SS[0]	X
Bit 5	R	NJEI	X
Bit 4	R	PJEI	X
Bit 3	R	ESEI	X
Bit 2	R/W	PEE	0
Bit 1	R	AISV	X
Bit 0	R/W	RELAYAIS	0

This register reports the alarm status of TU #1 in TUG2 #1.

RELAYAIS:

The RELAYAIS bit controls the number of consecutive AIS_ind indications required to enter the AIS state for tributary TU #1 in TUG2 #1. When RELAYAIS is set high, AIS is declared upon receipt of a single AIS_ind indication. When RELAYAIS is set low, AIS is declared after 3 consecutive AIS_ind indications.

AISV:

The AISV bit indicates the tributary path AIS status of tributary TU #1 in TUG2 #1.

PEE:

The PEE bit enables pointer event interrupts for tributary TU #1 in TUG2 #1. When PEE is set high, an interrupt is generated upon detection of FIFO underflows and overflows, upon detection of incoming pointer justification events when the MONIS bit is set high and upon detection of outgoing pointer justification events when the MONIS bit is set low. Interrupts due to elastic store errors and pointer justification events are masked when PEE is set low.

ESEI:

The ESEI bit reports and acknowledges the status of elastic store error interrupts for tributary TU #1 in TUG2 #1. Interrupts are generated upon FIFO underflows and overflows. ESEI is set high when an elastic store error occurs and is cleared immediately following a read of this register, which also

acknowledges and clears the interrupt. ESEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect elastic store error events.

PJEI:

The PJEI bit reports and acknowledges the status of the positive pointer justification event interrupts for tributary TU #1 in TUG2 #1. When the MONIS bit is set high, interrupts are generated upon reception of a positive pointer justification event in the incoming stream. When the MONIS bit is set low, interrupts are generated upon generation of a positive pointer justification event in the outgoing stream. PJEI is set high when a positive pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PJEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect positive pointer justification events.

NJEI:

The NJEI bit reports and acknowledges the status of the negative pointer justification event interrupts for tributary TU #1 in TUG2 #1. When the MONIS bit is set high, interrupts are generated upon reception of a negative pointer justification event in the incoming stream. When the MONIS bit is set low, interrupts are generated upon generation of a negative pointer justification event in the outgoing stream. NJEI is set high when a negative pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. NJEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect negative pointer justification events.

SS[1:0]:

The SS[1:0] bits reports the value of the size bits in the V1 byte of tributary TU #1 in TUG2 #1. The SS[1:0] bits are not filtered and must be software de-bounced.

Register 1242H, 1244H, 1246H, 1248H, 124AH, 124CH: VTPP Ingress, TU #1 in TUG2 #2 to TUG2 #7, Configuration and Status

Bit	Type	Function	Default
Bit 7	R/W	Reserved	1
Bit 6	R/W	TU11	1
Bit 5	R/W	PF	0
Bit 4	R	LOPV	X
Bit 3	R/W	ALARME	0
Bit 2	R/W	DLOP	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	IPAIS	0

This set of registers reports the status and configures the operational modes of TU #1 in TUG2 #2 to TUG2 #7.

IPAIS:

The IPAIS bit enables the insertion of path AIS for tributary TU #1 in the corresponding TUG2. Tributary path AIS is inserted by forcing all ones into all tributary bytes.

DLOP:

The DLOP bit allows downstream pointer processing elements to be diagnosed. When DLOP is set high, the new data flag (NDF) field of the outgoing payload pointer in tributary TU #1 in the corresponding TUG2 is inverted to cause downstream pointer processing elements to enter a loss of pointer state. Insertion of an inverted new data flag can occur in concert with the insertion of a normal idle (unequipped) indication. The DLOP bit has no effect when the IPAIS bit is set high.

ALARME:

The ALARME bit enables loss of pointer and path AIS interrupts for tributary TU #1 in the corresponding TUG2. When ALARME is set high, an interrupt is generated upon entry to and exit from the LOP and AIS state of the pointer interpreter state diagram. Interrupts due to AIS and LOP status change are masked when ALARME is set low.

LOPV:

The LOPV bit indicates the loss of pointer status of tributary TU #1 in the corresponding TUG2.

PF:

The PF bit enables pointer follower mode for tributary TU #1 in the corresponding TUG2. In pointer follower mode, the tributary FIFO dead-zone is collapsed so that any variation in FIFO depth will result in an outgoing pointer justification event. Any TU pointer justification event on the corresponding incoming tributary, or an AU pointer justification event affecting this tributary will cause an outgoing pointer justification event.

TU11:

The TU11 bit specifies the tributary configuration of tributary group TUG2 #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

Bit 7 must be kept at a logic 1 for proper operation of the TEMAP while bit 1 must be kept to logic 0.

Register 1243H, 1245H, 1247H, 1249H, 124BH, 124DH: VTPP Ingress, TU #1 in TUG2 #2 to TUG2 #7, Alarm Status

Bit	Type	Function	Default
Bit 7	R	SS[1]	X
Bit 6	R	SS[0]	X
Bit 5	R	NJEI	X
Bit 4	R	PJEI	X
Bit 3	R	ESEI	X
Bit 2	R/W	PEE	0
Bit 1	R	AISV	X
Bit 0	R/W	RELAYAIS	0

This set of registers reports the alarm status of TU #1 in TUG2 #2 to TUG2 #7.

RELAYAIS:

The RELAYAIS bit controls the number of consecutive AIS_ind indications required to enter the AIS state for tributary TU #1 in the corresponding TUG2. When RELAYAIS is set high, AIS is declared upon receipt of a single AIS_ind indication. When RELAYAIS is set low, AIS is declared after 3 consecutive AIS_ind indications.

AISV:

The AISV bit indicates the tributary path AIS status of tributary TU #1 in the corresponding TUG2.

PEE:

The PEE bit enables pointer event interrupts for tributary TU #1 in the corresponding TUG2. When PEE is set high, an interrupt is generated upon detection of FIFO underflows and overflows, upon detection of incoming pointer justification events when the MONIS bit is set high and upon detection of outgoing pointer justification events when the MONIS bit is set low. Interrupts due to elastic store errors and pointer justification events are masked when PEE is set low.

ESEI:

The ESEI bit reports and acknowledges the status of elastic store error interrupts for tributary TU #1 in the corresponding TUG2. Interrupts are

generated upon FIFO underflows and overflows. ESEI is set high when an elastic store error occurs and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. ESEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect elastic store error events.

PJEI:

The PJEI bit reports and acknowledges the status of the positive pointer justification event interrupts for tributary TU #1 in the corresponding TUG2. When the MONIS bit is set high, interrupts are generated upon reception of a positive pointer justification event in the incoming stream. When the MONIS bit is set low, interrupts are generated upon generation of a positive pointer justification event in the outgoing stream. PJEI is set high when a positive pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PJEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect positive pointer justification events.

NJEI:

The NJEI bit reports and acknowledges the status of the negative pointer justification event interrupts for tributary TU #1 in the corresponding TUG2. When the MONIS bit is set high, interrupts are generated upon reception of a negative pointer justification event in the incoming stream. When the MONIS bit is set low, interrupts are generated upon generation of a negative pointer justification event in the outgoing stream. NJEI is set high when a negative pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. NJEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect negative pointer justification events.

SS[1:0]:

The SS[1:0] bits reports the value of the size bits in the V1 byte of tributary TU #1 in the corresponding TUG2. The SS[1:0] bits are not filtered and must be software de-bounced.

Register 124EH: VTPP Ingress, TU #1 in TUG2 #1 to TUG2 #7, LOP Interrupt

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R	LOP7I	0
Bit 5	R	LOP6I	0
Bit 4	R	LOP5I	0
Bit 3	R	LOP4I	0
Bit 2	R	LOP3I	0
Bit 1	R	LOP2I	0
Bit 0	R	LOP1I	0

This register is used to identify and acknowledge loss of pointer interrupts for the tributaries TU #1 in TUG2 #1 to TUG2 #7.

LOP1I:

The LOP1I bit identifies the source of loss of pointer interrupts. The LOP1I bit reports and acknowledges LOP interrupt of TU #1 in TUG2 #1. Interrupts are generated upon loss of pointer and upon re-acquisition. LOP1I is set high when the corresponding loss of pointer event occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. LOP1I remains valid when interrupts are not enabled (ALARME set low) and may be polled to detect loss of pointer events.

LOP2I-LOP7I:

The LOP2I to LOP7I bits identify the source of loss of pointer interrupts. The LOP2I to LOP7I bits report and acknowledge LOP interrupt of TU #1 in TUG2 #2 to TUG2 #7, respectively. Interrupts are generated upon loss of pointer and upon re-acquisition. An LOP*x*I bit is set high when a loss of pointer event on the associated tributary (TU #1 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. LOP*x*I remains valid when interrupts are not enabled (ALARME set low) and may be polled to detect loss of pointer events.

Reserved:

The Reserved bit must be written with a logic 0 for proper operation of the TEMAP.

Register 124FH: VTPP Ingress, TU #1 in TUG2 #1 to TUG2 #7, AIS Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	AIS7I	0
Bit 5	R	AIS6I	0
Bit 4	R	AIS5I	0
Bit 3	R	AIS4I	0
Bit 2	R	AIS3I	0
Bit 1	R	AIS2I	0
Bit 0	R	AIS1I	0

This register is used to identify and acknowledge alarm indication signal interrupts for the tributaries TU #1 in TUG2 #1 to TUG2 #7.

AIS1I:

The AIS1I bit identifies the source of tributary path AIS interrupts. The AIS1I bit reports and acknowledges AIS interrupt of TU #1 in TUG2 #1. Interrupts are generated upon detection and removal of tributary path AIS alarm. AIS1I is set high when the corresponding tributary path AIS event occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. AIS1I remains valid when interrupts are not enabled (ALARME set low) and may be polled to detect tributary path AIS events.

AIS2I-AIS7I:

The AIS2I to AIS7I bits identify the source of tributary path AIS interrupts. The AIS2I to AIS7I bits report and acknowledge AIS interrupt of TU #1 in TUG2 #2 to TUG2 #7, respectively. Interrupts are generated upon detection and removal of tributary path AIS. An AIS*x*I bit is set high when a tributary path AIS event on the associated tributary (TU #1 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. AIS*x*I remains valid when interrupts are not enabled (ALARME set low) and may be polled to detect tributary path AIS events.

Register 1250H, 1252H, 1254H, 1256H, 1258H, 125AH, 125CH: VTPP Ingress, TU #2 in TUG2 #1 to TUG2 #7, Configuration and Status

Bit	Type	Function	Default
Bit 7	R	Reserved	1
Bit 6	R	TU11	1
Bit 5	R/W	PF	0
Bit 4	R	LOPV	X
Bit 3	R/W	ALARME	0
Bit 2	R/W	DLOP	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	IPAIS	0

This set of registers reports the status and configures the operational modes of TU #2 in TUG2 #1 to TUG2 #7.

IPAIS:

The IPAIS bit enables the insertion of path AIS for tributary TU #2 in the corresponding TUG2. Tributary path AIS is inserted by forcing all ones into all tributary bytes.

DLOP:

The DLOP bit allows downstream pointer processing elements to be diagnosed. When DLOP is set high, the new data flag (NDF) field of the outgoing payload pointer in tributary TU #2 in the corresponding TUG2 is inverted, causing downstream pointer processing elements to enter a loss of pointer state. Insertion of an inverted new data flag can occur in concert with the insertion of a normal idle (unequipped) indication. The DLOP bit has no effect when the IPAIS bit is set high.

ALARME:

The ALARME bit enables loss of pointer and path AIS interrupts for tributary TU #2 in the corresponding TUG2. When ALARME is set high, an interrupt is generated upon entry to and exit from the LOP and AIS state of the pointer interpreter state diagram. Interrupts due to AIS and LOP status change are masked when ALARME is set low.

LOPV:

The LOPV bit indicates the loss of pointer status of tributary TU #2 in the corresponding TUG2.

PF:

The PF bit enables pointer follower mode for tributary TU #2 in the corresponding TUG2. In pointer follower mode, the tributary FIFO dead-zone is collapsed so that any variation in FIFO depth will result in an outgoing pointer justification event. Any TU pointer justification event on the corresponding incoming tributary, or an AU pointer justification event affecting this tributary will cause an outgoing pointer justification event.

TU11:

The TU11 bit is read-only and reflect the values written into the corresponding register of TU #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

Bit 7 must be kept at a logic 1 for proper operation of the TEMAP while bit 1 must be kept to logic 0.

Register 1251H, 1253H, 1255H, 1257H, 1259H, 125BH, 125DH: VTPP Ingress, TU #2 in TUG2 #1 to TUG2 #7, Alarm Status

Bit	Type	Function	Default
Bit 7	R	SS[1]	X
Bit 6	R	SS[0]	X
Bit 5	R	NJEI	X
Bit 4	R	PJEI	X
Bit 3	R	ESEI	X
Bit 2	R/W	PEE	0
Bit 1	R	AISV	X
Bit 0	R/W	RELAYAIS	0

This set of registers reports the alarm status of TU #2 in TUG2 #1 to TUG2 #7.

RELAYAIS:

The RELAYAIS bit controls the number of consecutive AIS_ind indications required to enter the AIS state for tributary TU #2 in the corresponding TUG2. When RELAYAIS is set high, AIS is declared upon receipt of a single AIS_ind indication. When RELAYAIS is set low, AIS is declared after 3 consecutive AIS_ind indications.

AISV:

The AISV bit indicates the tributary path AIS status of tributary TU #2 in the corresponding TUG2.

PEE:

The PEE bit enables pointer event interrupts for tributary TU #2 in the corresponding TUG2. When PEE is set high, an interrupt is generated upon detection of FIFO underflows and overflows, upon detection of incoming pointer justification events when the MONIS bit is set high and upon detection of outgoing pointer justification events when the MONIS bit is set low. Interrupts due to elastic store errors and pointer justification events are masked when PEE is set low.

ESEI:

The ESEI bit reports and acknowledges the status of elastic store error interrupts for tributary TU #2 in the corresponding TUG2. Interrupts are

generated upon FIFO underflows and overflows. ESEI is set high when an elastic store error occurs and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. ESEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect elastic store error events.

PJEI:

The PJEI bit reports and acknowledges the status of the positive pointer justification event interrupts for tributary TU #2 in the corresponding TUG2. When the MONIS bit is set high, interrupts are generated upon reception of a positive pointer justification event in the incoming stream. When the MONIS bit is set low, interrupts are generated upon generation of a positive pointer justification event in the outgoing stream. PJEI is set high when a positive pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PJEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect positive pointer justification events.

NJEI:

The NJEI bit reports and acknowledges the status of the negative pointer justification event interrupts for tributary TU #2 in the corresponding TUG2. When the MONIS bit is set high, interrupts are generated upon reception of a negative pointer justification event in the incoming stream. When the MONIS bit is set low, interrupts are generated upon generation of a negative pointer justification event in the outgoing stream. NJEI is set high when a negative pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. NJEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect negative pointer justification events.

SS[1:0]:

The SS[1:0] bits reports the value of the size bits in the V1 byte of tributary TU #2 in the corresponding TUG2. The SS[1:0] bits are not filtered and must be software de-bounced.

Register 125EH: VTPP Ingress, TU #2 in TUG2 #1 to TUG2 #7, LOP Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	LOP7I	0
Bit 5	R	LOP6I	0
Bit 4	R	LOP5I	0
Bit 3	R	LOP4I	0
Bit 2	R	LOP3I	0
Bit 1	R	LOP2I	0
Bit 0	R	LOP1I	0

This register is used to identify and acknowledge loss of pointer interrupts for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

LOP1I-LOP7I:

The LOP1I to LOP7I bits identify the source of loss of pointer interrupts. When operational, the LOP1I to LOP7I bits report and acknowledge LOP interrupts of TU #2 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon loss of pointer and upon re-acquisition. An LOP*x*I bit is set high when a loss of pointer event on the associated tributary occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. LOP*x*I remains valid when interrupts are not enabled (ALARME set low) and may be polled to detect loss of pointer events.

Register 125FH: VTPP Ingress, TU #2 in TUG2 #1 to TUG2 #7 AIS Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	AIS7I	0
Bit 5	R	AIS6I	0
Bit 4	R	AIS5I	0
Bit 3	R	AIS4I	0
Bit 2	R	AIS3I	0
Bit 1	R	AIS2I	0
Bit 0	R	AIS1I	0

This register is used to identify and acknowledge tributary path AIS interrupts for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

AIS1I-AIS7I:

The AIS1I to AIS7I bits identify the source of tributary path AIS interrupts. When operational, the AIS1I to AIS7I bits report and acknowledge AIS interrupt of TU #2 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon detection and removal of tributary path AIS alarm. An AIS*x*I bit is set high when a tributary path AIS event on the associated tributary occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. AIS*x*I remains valid when interrupts are not enabled (ALARME set low) and may be polled to detect tributary path AIS events.

Register 1260H, 1262H, 1264H, 1266H, 1268H, 126AH, 126CH: VTPP Ingress, TU #3 in TUG2 #1 to TUG2 #7, Configuration and Status

Bit	Type	Function	Default
Bit 7	R	Reserved	1
Bit 6	R	TU11	1
Bit 5	R/W	PF	0
Bit 4	R	LOPV	X
Bit 3	R/W	ALARME	0
Bit 2	R/W	DLOP	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	IPAIS	0

This set of registers reports the status and configures the operational modes of TU #3 in TUG2 #1 to TUG2 #7.

IPAIS:

The IPAIS bit enables the insertion of path AIS for tributary TU #3 in the corresponding TUG2. Tributary path AIS is inserted by forcing all ones into all tributary bytes.

DLOP:

The DLOP bit allows downstream pointer processing elements to be diagnosed. When DLOP is set high, the new data flag (NDF) field of the outgoing payload pointer in tributary TU #3 in the corresponding TUG2 is inverted, causing downstream pointer processing elements to enter a loss of pointer state. Insertion of an inverted new data flag can occur in concert with the insertion of a normal idle (unequipped) indication. The DLOP bit has no effect when the IPAIS bit is set high.

ALARME:

The ALARME bit enables loss of pointer and path AIS interrupts for tributary TU #3 in the corresponding TUG2. When ALARME is set high, an interrupt is generated upon entry to and exit from the LOP and AIS state of the pointer interpreter state diagram. Interrupts due to AIS and LOP status change are masked when ALARME is set low.

LOPV:

The LOPV bit indicates the loss of pointer status of tributary TU #3 in the corresponding TUG2.

PF:

The PF bit enables pointer follower mode for tributary TU #3 in the corresponding TUG2. In pointer follower mode, the tributary FIFO dead-zone is collapsed so that any variation in FIFO depth will result in an outgoing pointer justification event. Any TU pointer justification event on the corresponding incoming tributary, or an AU pointer justification event affecting this tributary will cause an outgoing pointer justification event.

TU11:

The TU11 bit is read-only and reflect the values written into the corresponding register of TU #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

Bit 7 must be kept at a logic 1 for proper operation of the TEMAP while bit 1 must be kept to logic 0.

Register 1261H, 1263H, 1265H, 1267H, 1269H, 126BH, 126DH: VTPP Ingress, TU #3 in TUG2 #1 to TUG2 #7, Alarm Status

Bit	Type	Function	Default
Bit 7	R	SS[1]	X
Bit 6	R	SS[0]	X
Bit 5	R	NJEI	X
Bit 4	R	PJEI	X
Bit 3	R	ESEI	X
Bit 2	R/W	PEE	0
Bit 1	R	AISV	X
Bit 0	R/W	RELAYAIS	0

This set of registers reports the status and configures the operational modes of TU #3 in TUG2 #1 to TUG2 #7.

RELAYAIS:

The RELAYAIS bit controls the number of consecutive AIS_ind indications required to enter the AIS state for tributary TU #3 in the corresponding TUG2. When RELAYAIS is set high, AIS is declared upon receipt of a single AIS_ind indication. When RELAYAIS is set low, AIS is declared after 3 consecutive AIS_ind indications.

AISV:

The AISV bit indicates the tributary path AIS status of tributary TU #3 in the corresponding TUG2.

PEE:

The PEE bit enables pointer event interrupts for tributary TU #3 in the corresponding TUG2. When PEE is set high, an interrupt is generated upon detection of FIFO underflows and overflows, upon detection of incoming pointer justification events when the MONIS bit is set high and upon detection of outgoing pointer justification events when the MONIS bit is set low. Interrupts due to elastic store errors and pointer justification events are masked when PEE is set low.

ESEI:

The ESEI bit reports and acknowledges the status of elastic store error interrupts for tributary TU #3 in the corresponding TUG2. Interrupts are generated upon FIFO underflows and overflows. ESEI is set high when an elastic store error occurs and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. ESEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect elastic store error events.

PJEI:

The PJEI bit reports and acknowledges the status of the positive pointer justification event interrupts for tributary TU #3 in the corresponding TUG2. When the MONIS bit is set high, interrupts are generated upon reception of a positive pointer justification event in the incoming stream. When the MONIS bit is set low, interrupts are generated upon generation of a positive pointer justification event in the outgoing stream. PJEI is set high when a positive pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PJEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect positive pointer justification events.

NJEI:

The NJEI bit reports and acknowledges the status of the negative pointer justification event interrupts for tributary TU #3 in the corresponding TUG2. When the MONIS bit is set high, interrupts are generated upon reception of a negative pointer justification event in the incoming stream. When the MONIS bit is set low, interrupts are generated upon generation of a negative pointer justification event in the outgoing stream. NJEI is set high when a negative pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. NJEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect negative pointer justification events.

SS[1:0]:

The SS[1:0] bits reports the value of the size bits in the V1 byte of tributary TU #3 in the corresponding TUG2. The SS[1:0] bits are not filtered and must be software de-bounced.

Register 126EH: VTPP Ingress, TU #3 in TUG2 #1 to TUG2 #7, LOP Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	LOP7I	0
Bit 5	R	LOP6I	0
Bit 4	R	LOP5I	0
Bit 3	R	LOP4I	0
Bit 2	R	LOP3I	0
Bit 1	R	LOP2I	0
Bit 0	R	LOP1I	0

This register is used to identify and acknowledge loss of pointer interrupts for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

LOP1I-LOP7I:

The LOP1I to LOP7I bits identify the source of loss of pointer interrupts. When operational, the LOP1I to LOP7I bits report and acknowledge LOP interrupts of TU #3 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon loss of pointer and upon re-acquisition. An LOP*x*I bit is set high when a loss of pointer event on the associated tributary occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. LOP*x*I remains valid when interrupts are not enabled (ALARME set low) and may be polled to detect loss of pointer events.

Register 126FH: VTPP Ingress, TU #3 in TUG2 #1 to TUG2 #7, AIS Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	AIS7I	0
Bit 5	R	AIS6I	0
Bit 4	R	AIS5I	0
Bit 3	R	AIS4I	0
Bit 2	R	AIS3I	0
Bit 1	R	AIS2I	0
Bit 0	R	AIS1I	0

This register is used to identify and acknowledge tributary path AIS interrupts for the tributaries TU #3 in TUG2 #1 to TUG2 #7.

AIS1I-AIS7I:

The AIS1I to AIS7I bits identify the source of tributary path AIS interrupts. When operational, the AIS1I to AIS7I bits report and acknowledge AIS interrupt of TU #3 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon detection and removal of tributary path AIS alarm. An AIS*x*I bit is set high when a tributary path AIS event on the associated tributary occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. AIS*x*I remains valid when interrupts are not enabled (ALARME set low) and may be polled to detect tributary path AIS events.

Register 1270H, 1272H, 1274H, 1276H, 1278H, 127AH, 127CH: VTPP Ingress, TU #4 in TUG2 #1 to TUG2 #7, Configuration and Status

Bit	Type	Function	Default
Bit 7	R	Reserved	1
Bit 6	R	TU11	1
Bit 5	R/W	PF	0
Bit 4	R	LOPV	X
Bit 3	R/W	ALARME	0
Bit 2	R/W	DLOP	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	IPAIS	0

This set of registers reports the status and configures the operational modes of TU #4 in TUG2 #1 to TUG2 #7. When the corresponding TUG2 tributary group is configured to TU12 (VT2) mode, the associated register in this set has no effect.

IPAIS:

The IPAIS bit enables the insertion of path AIS for tributary TU #4 in the corresponding TUG2. Tributary path AIS is inserted by forcing all ones into all tributary bytes.

DLOP:

The DLOP bit allows downstream pointer processing elements to be diagnosed. When DLOP is set high, the new data flag (NDF) field of the outgoing payload pointer in tributary TU #4 in the corresponding TUG2 is inverted, causing downstream pointer processing elements to enter a loss of pointer state. Insertion of an inverted new data flag can occur in concert with the insertion of a normal idle (unequipped) indication. The DLOP bit has no effect when the IPAIS bit is set high.

ALARME:

The ALARME bit enables loss of pointer and path AIS interrupts for tributary TU #4 in the corresponding TUG2. When ALARME is set high, an interrupt is generated upon entry to and exit from the LOP and AIS state of the pointer interpreter state diagram. Interrupts due to AIS and LOP status change are masked when ALARME is set low.

LOPV:

The LOPV bit indicates the loss of pointer status of tributary TU #4 in the corresponding TUG2.

PF:

The PF bit enables pointer follower mode for tributary TU #4 in the corresponding TUG2. In pointer follower mode, the tributary FIFO dead-zone is collapsed so that any variation is FIFO depth will result in an outgoing pointer justification event. Any TU pointer justification event on the corresponding incoming tributary, or an AU pointer justification event affecting this tributary will cause an outgoing pointer justification event.

TU11:

The TU11 bit is read-only and reflect the values written into the corresponding register of TU #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

Bit 7 must be kept at a logic 1 for proper operation of the TEMAP while bit 1 must be kept to logic 0.

Register 1271H, 1273H, 1275H, 1277H, 1279H, 127BH, 127DH: VTPP Ingress, TU #4 in TUG2 #1 to TUG2 #7, Alarm Status

Bit	Type	Function	Default
Bit 7	R	SS[1]	X
Bit 6	R	SS[0]	X
Bit 5	R	NJEI	X
Bit 4	R	PJEI	X
Bit 3	R	ESEI	X
Bit 2	R/W	PEE	0
Bit 1	R	AISV	X
Bit 0	R/W	RELAYAIS	0

This set of registers reports the alarm status of TU #4 in TUG2 #1 to TUG2 #7. When the corresponding TUG2 tributary group is configured to TU12 (VT2) mode, the associated register in this set has no effect.

RELAYAIS:

The RELAYAIS bit controls the number of consecutive AIS_ind indications required to enter the AIS state for tributary TU #4 in the corresponding TUG2. When RELAYAIS is set high, AIS is declared upon receipt of a single AIS_ind indication. When RELAYAIS is set low, AIS is declared after 3 consecutive AIS_ind indications.

AISV:

The AISV bit indicates the tributary path AIS status of tributary TU #4 in the corresponding TUG2.

PEE:

The PEE bit enables pointer event interrupts for tributary TU #4 in the corresponding TUG2. When PEE is set high, an interrupt is generated upon detection of FIFO underflows and overflows, upon detection of incoming pointer justification events when the MONIS bit is set high and upon detection of outgoing pointer justification events when the MONIS bit is set low. Interrupts due to elastic store errors and pointer justification events are masked when PEE is set low.

ESEI:

The ESEI bit reports and acknowledges the status of elastic store error interrupts for tributary TU #4 in the corresponding TUG2. Interrupts are generated upon FIFO underflows and overflows. ESEI is set high when an elastic store error occurs and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. ESEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect elastic store error events.

PJEI:

The PJEI bit reports and acknowledges the status of the positive pointer justification event interrupts for tributary TU #4 in the corresponding TUG2. When the MONIS bit is set high, interrupts are generated upon reception of a positive pointer justification event in the incoming stream. When the MONIS bit is set low, interrupts are generated upon generation of a positive pointer justification event in the outgoing stream. PJEI is set high when a positive pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PJEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect positive pointer justification events.

NJEI:

The NJEI bit reports and acknowledges the status of the negative pointer justification event interrupts for tributary TU #4 in the corresponding TUG2. When the MONIS bit is set high, interrupts are generated upon reception of a negative pointer justification event in the incoming stream. When the MONIS bit is set low, interrupts are generated upon generation of a negative pointer justification event in the outgoing stream. NJEI is set high when a negative pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. NJEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect negative pointer justification events.

SS[1:0]:

The SS[1:0] bits reports the value of the size bits in the V1 byte of tributary TU #4 in the corresponding TUG2. The SS[1:0] bits are not filtered and must be software de-bounced.

Register 127EH: VTPP Ingress, TU #4 in TUG2 #1 to TUG2 #7, LOP Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	LOP7I	0
Bit 5	R	LOP6I	0
Bit 4	R	LOP5I	0
Bit 3	R	LOP4I	0
Bit 2	R	LOP3I	0
Bit 1	R	LOP2I	0
Bit 0	R	LOP1I	0

This register is used to identify and acknowledge loss of pointer interrupts for the tributaries TU #4 in TUG2 #1 to TUG2 #7.

LOP1I-LOP7I:

The LOP1I to LOP7I bits identify the source of loss of pointer interrupts. When the corresponding TUG2 tributary group is configured TU12 (VT2) mode, the associated LOP*x*I bit is unused and will return a logic 0 when read. When operational, the LOP1I to LOP7I bits report and acknowledge LOP interrupt of TU #4 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon loss of pointer and upon re-acquisition. An LOP*x*I bit is set high when a loss of pointer event on the associated tributary occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. LOP*x*I remains valid when interrupts are not enabled (ALARME set low) and may be polled to detect loss of pointer events.

Register 127FH: VTPP Ingress, TU #4 in TUG2 #1 to TUG2 #7, AIS Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	AIS7I	0
Bit 5	R	AIS6I	0
Bit 4	R	AIS5I	0
Bit 3	R	AIS4I	0
Bit 2	R	AIS3I	0
Bit 1	R	AIS2I	0
Bit 0	R	AIS1I	0

This register is used to identify and acknowledge tributary path AIS interrupts for the tributaries TU #4 in TUG2 #1 to TUG2 #7.

AIS1I-AIS7I:

The AIS1I to AIS7I bits identify the source of tributary path AIS interrupts. When the corresponding TUG2 tributary group is configured for TU12 (VT2) mode, the associated AIS*x*I bit is unused and will return a logic 0 when read. When operational, the AIS1I to AIS7I bits report and acknowledge AIS interrupt of TU #4 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon detection and removal of tributary path AIS alarm. An AIS*x*I bit is set high when a tributary path AIS event on the associated tributary occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. AIS*x*I remains valid when interrupts are not enabled (ALARME set low) and may be polled to detect tributary path AIS events.

1.24 RTDM Receive Tributary Demapper Registers

Register 1280H: RTDM TU #1 in TUG2 #1 of TUG3 #1, Control

Bit	Type	Function	Default
Bit 7	R/W	TU11	1
Bit 6	R/W	T1	1
Bit 5	R/W	PROV	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	AIS	0

This register configures the operating mode for TU #1 in TUG2 #1 of TUG3 #1.

AIS:

The AIS bit enables the insertion of AIS on the de-mapped T1 or E1 stream derived from tributary TU #1 in TUG2 #1 of TUG3 #1. The AIS bit is logically ORed with the AIS state of this tributary signaled by the AIS pin. When AIS is set high, all payload bits of the de-mapped T1 or E1 stream are set high and the stream clock rate is set to the nominal value (1.544 MHz for T1 and 2.048 MHz for E1). When AIS is set low, AIS insertion is controlled by the AIS pin.

PROV:

The PROV bit enables processing of tributary TU #1 in TUG2 #1 of TUG3 #1. When PROV is set high, tributary TU #1 in TUG2 #1 of TUG3 #1 is de-mapped normally into either a T1 or an E1 stream as controlled by the TU11 and T1 bits. When PROV is set low, tributary TU #1 in TUG2 #1 of TUG3 #1 is not processed.

TU11 and T1 Bits:

The TU11 and T1 bits specify the tributary configuration of TU #1 in tributary group TUG2 #1 of TUG3 #1.

When the TU11 bit is set high, the tributary is defined as a TU-11 (or VT1.5 in SONET) and contains a T1 stream. When the TU11 bit is set low, the tributary is defined as a TU-12 (or VT2 in SONET) and contains either a T1 or

an E1 stream as determined by the T1 bit. For TU11 low, the TU#4 in the current TUG2 group is meaningless and its configuration is ignored.

When the TU11 bit is set high, the T1 bit is ignored. However, when the TU11 bit is set low, the T1 bit selects whether the tributary contains a T1 stream (if the T1 bit is set high) or an E1 stream (if the T1 bit is set high).

NOTE: All tributaries in each TUG2 must be configured to the same tributary type (i.e., either TU-11 or TU-12). In fact, for each TUG2, all tributaries reference the TU11 bit of the first tributary in the group (TU #1). The TU11 bit of all other tributaries in the group are read-only. The T1 bit must be configured the same for all tributaries.

The configuration specified by the TU11 and T1 bits is summarized as follows:

TU11	T1	Configuration	Active TU (VT)
0	0	E1 in TU-12 (VT2)	#1, #2, #3
0	1	T1 in TU-12	#1, #2, #3
1	0	Not a Valid Setting	
1	1	T1 in TU-11 (VT1.5)	#1, #2, #3, #4

Register 1281H, 1282H, 1283H, 1284H, 1285H, 1286H: RTDM TU #1 in TUG2 #2 to TUG2 #7 of TUG3 #1, Control

Bit	Type	Function	Default
Bit 7	R/W	TU11	1
Bit 6	R/W	T1	1
Bit 5	R/W	PROV	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	AIS	0

This register configures the operational modes of TU #1 in TUG2 #2 of TUG3 #1 to TU #1 in TUG2 #7 of TUG3 #1.

AIS:

The AIS bit enables the insertion of AIS on the de-mapped T1 or E1 stream derived from tributary TU #1 in the corresponding TUG2 of TUG3 #1. The AIS bit is logically ORed with the AIS state of this tributary signaled by the AIS pin. When AIS is set high, all payload bits of the de-mapped T1 or E1 stream are set high and the stream clock rate is set to the nominal value (1.544 MHz for T1 and 2.048 MHz for E1). When AIS is set low, AIS insertion is controlled by the AIS pin.

PROV:

The PROV bit enables processing of tributary TU #1 in the corresponding TUG2 of TUG3 #1. When PROV is set high, tributary TU #1 in the corresponding TUG2 of TUG3 #1 is de-mapped normally into either a T1 or an E1 stream as controlled by the TU11 and T1 bits. When PROV is set low, tributary TU #1 in the corresponding TUG2 of TUG3 #1 is not processed.

TU11 and T1 Bits:

The TU11 and T1 bits specify the tributary configuration of TU #1 in the corresponding TUG2 of TUG3 #1.

When the TU11 bit is set high, the tributary is defined as a TU-11 (or VT1.5 in SONET) and contains a T1 stream. When the TU11 bit is set low, the tributary is defined as a TU-12 (or VT2 in SONET) and contains either a T1 or

an E1 stream as determined by the T1 bit. For TU11 low, the TU#4 in the current TUG2 group is meaningless and its configuration is ignored.

When the TU11 bit is set high, the T1 bit is ignored. However, when the TU11 bit is set low, the T1 bit selects whether the tributary contains a T1 stream (if the T1 bit is set high) or an E1 stream (if the T1 bit is set low).

NOTE: All tributaries in each TUG2 must be configured to the same tributary type (i.e., either TU-11 or TU-12). In fact, for each TUG2, all tributaries reference the TU11 bit of the first tributary in the group (TU #1). The TU11 bit of all other tributaries in the group are read-only. The T1 bit must be configured the same for all tributaries.

The configuration specified by the TU11 and T1 bits is summarized as follows:

TU11	T1	Configuration	Active TU (VT)
0	0	E1 in TU-12 (VT2)	#1, #2, #3
0	1	T1 in TU-12	#1, #2, #3
1	0	Not a Valid Setting	
1	1	T1 in TU-11 (VT1.5)	#1, #2, #3, #4

Register 1288H, 1289H, 128AH, 128BH, 128CH, 128DH,128EH: RTDM TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #1, Control

Bit	Type	Function	Default
Bit 7	R	TU11	1
Bit 6	R/W	T1	1
Bit 5	R/W	PROV	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	AIS	0

This register configures the operational modes of TU #2 in TUG2 #1 of TUG3 #1 to TU #2 in TUG2 #7 of TUG3 #1.

AIS:

The AIS bit enables the insertion of AIS on the de-mapped T1 or E1 stream derived from tributary TU #2 in the corresponding TUG2 of TUG3 #1. The AIS bit is logically ORed with the AIS state of this tributary signaled by the AIS pin. When AIS is set high, all payload bits of the de-mapped T1 or E1 stream are set high and the stream clock rate is set to the nominal value (1.544 MHz for T1 and 2.048 MHz for E1). When AIS is set low, AIS insertion is controlled by the AIS pin.

PROV:

The PROV bit enables processing of tributary TU #2 in the corresponding TUG2 of TUG3 #1. When PROV is set high, tributary TU #2 in the corresponding TUG2 of TUG3 #1 is de-mapped normally into either a T1 or an E1 stream as controlled by the TU11 and T1 bits. When PROV is set low, tributary TU #2 in the corresponding TUG2 of TUG3 #1 is not processed.

TU11 and T1 Bits:

The TU11 and T1 bits specify the tributary configuration of TU #2 in the corresponding TUG2 of TUG3 #1.

When the TU11 bit is set high, the tributary is defined as a TU-11 (or VT1.5 in SONET) and contains a T1 stream. When the TU11 bit is set low, the tributary is defined as a TU-12 (or VT2 in SONET) and contains either a T1 or

an E1 stream as determined by the T1 bit. For TU11 low, the TU#4 in the current TUG2 group is meaningless and its configuration is ignored.

When the TU11 bit is set high, the T1 bit is ignored. However, when the TU11 bit is set low, the T1 bit selects whether the tributary contains a T1 stream (if the T1 bit is set high) or an E1 stream (if the T1 bit is set low).

NOTE: All tributaries in each TUG2 must be configured to the same tributary type (i.e., either TU-11 or TU-12). In fact, for each TUG2, all tributaries reference the TU11 bit of the first tributary in the group (TU #1). The TU11 bit of all other tributaries in the group are read-only. The T1 bit must be configured the same for all tributaries.

The configuration specified by the TU11 and T1 bits is summarized as follows:

TU11	T1	Configuration	Active TU (VT)
0	0	E1 in TU-12 (VT2)	#1, #2, #3
0	1	T1 in TU-12	#1, #2, #3
1	0	Not a Valid Setting	
1	1	T1 in TU-11 (VT1.5)	#1, #2, #3, #4

Register 1290H, 1291H, 1292H, 1293H, 1294H, 1295H, 1296H: RTDM TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #1, Control

Bit	Type	Function	Default
Bit 7	R	TU11	1
Bit 6	R/W	T1	1
Bit 5	R/W	PROV	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	AIS	0

This register configures the operational modes of TU #3 in TUG2 #1 of TUG3 #1 to TU #3 in TUG2 #7 of TUG3 #1.

AIS:

The AIS bit enables the insertion of AIS on the de-mapped T1 or E1 stream derived from tributary TU #3 in the corresponding TUG2 of TUG3 #1. The AIS bit is logically ORed with the AIS state of this tributary signaled by the AIS pin. When AIS is set high, all payload bits of the de-mapped T1 or E1 stream are set high and the stream clock rate is set to the nominal value (1.544 MHz for T1 and 2.048 MHz for E1). When AIS is set low, AIS insertion is controlled by the AIS pin.

PROV:

The PROV bit enables processing of tributary TU #3 in the corresponding TUG2 of TUG3 #1. When PROV is set high, tributary TU #3 in the corresponding TUG2 of TUG3 #1 is de-mapped normally into either a T1 or an E1 stream as controlled by the TU11 and T1 bits. When PROV is set low, tributary TU #3 in the corresponding TUG2 of TUG3 #1 is not processed.

TU11 and T1 Bits:

The TU11 and T1 bits specify the tributary configuration of TU #3 in the corresponding TUG2 of TUG3 #1.

When the TU11 bit is set high, the tributary is defined as a TU-11 (or VT1.5 in SONET) and contains a T1 stream. When the TU11 bit is set low, the tributary is defined as a TU-12 (or VT2 in SONET) and contains either a T1 or

an E1 stream as determined by the T1 bit. For TU11 low, the TU#4 in the current TUG2 group is meaningless and its configuration is ignored.

When the TU11 bit is set high, the T1 bit is ignored. However, when the TU11 bit is set low, the T1 bit selects whether the tributary contains a T1 stream (if the T1 bit is set high) or an E1 stream (if the T1 bit is set low).

NOTE: All tributaries in each TUG2 must be configured to the same tributary type (i.e., either TU-11 or TU-12). In fact, for each TUG2, all tributaries reference the TU11 bit of the first tributary in the group (TU #1). The TU11 bit of all other tributaries in the group are read-only. The T1 bit must be configured the same for all tributaries.

The configuration specified by the TU11 and T1 bits is summarized as follows:

TU11	T1	Configuration	Active TU (VT)
0	0	E1 in TU-12 (VT2)	#1, #2, #3
0	1	T1 in TU-12	#1, #2, #3
1	0	Not a Valid Setting	
1	1	T1 in TU-11 (VT1.5)	#1, #2, #3, #4

Register 1298H, 1299H, 129AH, 129BH, 129CH, 129DH, 129EH: RTDM TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #1, Control

Bit	Type	Function	Default
Bit 7	R	TU11	1
Bit 6	R/W	T1	1
Bit 5	R/W	PROV	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	AIS	0

This register configures the operational modes of TU #4 in TUG2 #1 of TUG3 #1 to TU #4 in TUG2 #7 of TUG3 #1. When the corresponding TUG2 tributary group is configured to TU-12 (VT2) mode, the associated register in this set has no effect.

AIS:

The AIS bit enables the insertion of AIS on the de-mapped T1 or E1 stream derived from tributary TU #4 in the corresponding TUG2 of TUG3 #1. The AIS bit is logically ORed with the AIS state of this tributary signaled by the AIS pin. When AIS is set high, all payload bits of the de-mapped T1 or E1 stream are set high and the stream clock rate is set to the nominal value (1.544 MHz for T1 and 2.048 MHz for E1). When AIS is set low, AIS insertion is controlled by the AIS pin.

PROV:

The PROV bit enables processing of tributary TU #4 in the corresponding TUG2 of TUG3 #1. When PROV is set high, tributary TU #4 in the corresponding TUG2 of TUG3 #1 is de-mapped normally into either a T1 or an E1 stream as controlled by the TU11 and T1 bits. When PROV is set low, tributary TU #4 in the corresponding TUG2 of TUG3 #1 is not processed.

TU11 and T1 Bits:

The TU11 and T1 bits specify the tributary configuration of TU #4 in the corresponding TUG2 of TUG3 #1.

When the TU11 bit is set high, the tributary is defined as a TU-11 (or VT1.5 in SONET) and contains a T1 stream. When the TU11 bit is set low, the tributary is defined as a TU-12 (or VT2 in SONET) and contains either a T1 or an E1 stream as determined by the T1 bit. For TU11 low, the TU#4 in the current TUG2 group is meaningless and its configuration is ignored.

When the TU11 bit is set high, the T1 bit is ignored. However, when the TU11 bit is set low, the T1 bit selects whether the tributary contains a T1 stream (if the T1 bit is set high) or an E1 stream (if the T1 bit is set low).

NOTE: All tributaries in each TUG2 must be configured to the same tributary type (i.e., either TU-11 or TU-12). In fact, for each TUG2, all tributaries reference the TU11 bit of the first tributary in the group (TU #1). The T1 bit must be configured the same for all tributaries.

The configuration specified by the TU11 and T1 bits is summarized as follows:

TU11	T1	Configuration	Active TU (VT)
0	0	E1 in TU-12 (VT2)	#1, #2, #3
0	1	T1 in TU-12	#1, #2, #3
1	0	Not a Valid Setting	
1	1	T1 in TU-11 (VT1.5)	#1, #2, #3, #4

Register 12A0H, 12A1H, 12A2H, 12A3H, 12A4H, 12A5H,12A6H: RTDM TU #1 in TUG2 #1 to TUG2 #7 of TUG3 #2, Control

Bit	Type	Function	Default
Bit 7	R/W	TU11	1
Bit 6	R/W	T1	1
Bit 5	R/W	PROV	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	AIS	0

This register configures the operational modes of TU #1 in TUG2 #2 of TUG3 #2 to TU #1 in TUG2 #7 of TUG3 #2.

AIS:

The AIS bit enables the insertion of AIS on the de-mapped T1 or E1 stream derived from tributary TU #1 in the corresponding TUG2 of TUG3 #2. The AIS bit is logically ORed with the AIS state of this tributary signaled by the AIS pin. When AIS is set high, all payload bits of the de-mapped T1 or E1 stream are set high and the stream clock rate is set to the nominal value (1.544 MHz for T1 and 2.048 MHz for E1). When AIS is set low, AIS insertion is controlled by the AIS pin.

PROV:

The PROV bit enables processing of tributary TU #1 in the corresponding TUG2 of TUG3 #2. When PROV is set high, tributary TU #1 in the corresponding TUG2 of TUG3 #2 is de-mapped normally into either a T1 or an E1 stream as controlled by the TU11 and T1 bits. When PROV is set low, tributary TU #1 in the corresponding TUG2 of TUG3 #2 is not processed.

TU11 and T1 Bits:

The TU11 and T1 bits specify the tributary configuration of TU #1 in the corresponding TUG2 of TUG3 #2.

When the TU11 bit is set high, the tributary is defined as a TU-11 (or VT1.5 in SONET) and contains a T1 stream. When the TU11 bit is set low, the tributary is defined as a TU-12 (or VT2 in SONET) and contains either a T1 or

an E1 stream as determined by the T1 bit. For TU11 low, the TU#4 in the current TUG2 group is meaningless and its configuration is ignored.

When the TU11 bit is set high, the T1 bit is ignored. However, when the TU11 bit is set low, the T1 bit selects whether the tributary contains a T1 stream (if the T1 bit is set high) or an E1 stream (if the T1 bit is set low).

NOTE: All tributaries in each TUG2 must be configured to the same tributary type (i.e., either TU-11 or TU-12). In fact, for each TUG2, all tributaries reference the TU11 bit of the first tributary in the group (TU #1). The T1 bit must be configured the same for all tributaries.

The configuration specified by the TU11 and T1 bits is summarized as follows:

TU11	T1	Configuration	Active TU (VT)
0	0	E1 in TU-12 (VT2)	#1, #2, #3
0	1	T1 in TU-12	#1, #2, #3
1	0	Not a Valid Setting	
1	1	T1 in TU-11 (VT1.5)	#1, #2, #3, #4

Register 12A8H, 12A9H, 12AAH, 12ABH, 12ACH, 12ADH, 12AEH: RTDM TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #2, Control

Bit	Type	Function	Default
Bit 7	R	TU11	1
Bit 6	R/W	T1	1
Bit 5	R/W	PROV	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	AIS	0

This register configures the operational modes of TU #2 in TUG2 #1 of TUG3 #2 to TU #2 in TUG2 #7 of TUG3 #2.

AIS:

The AIS bit enables the insertion of AIS on the de-mapped T1 or E1 stream derived from tributary TU #2 in the corresponding TUG2 of TUG3 #2. The AIS bit is logically ORed with the AIS state of this tributary signaled by the AIS pin. When AIS is set high, all payload bits of the de-mapped T1 or E1 stream are set high and the stream clock rate is set to the nominal value (1.544 MHz for T1 and 2.048 MHz for E1). When AIS is set low, AIS insertion is controlled by the AIS pin.

PROV:

The PROV bit enables processing of tributary TU #2 in the corresponding TUG2 of TUG3 #2. When PROV is set high, tributary TU #2 in the corresponding TUG2 of TUG3 #2 is de-mapped normally into either a T1 or an E1 stream as controlled by the TU11 and T1 bits. When PROV is set low, tributary TU #2 in the corresponding TUG2 of TUG3 #2 is not processed.

TU11 and T1 Bits:

The TU11 and T1 bits specify the tributary configuration of TU #2 in the corresponding TUG2 of TUG3 #2.

When the TU11 bit is set high, the tributary is defined as a TU-11 (or VT1.5 in SONET) and contains a T1 stream. When the TU11 bit is set low, the tributary is defined as a TU-12 (or VT2 in SONET) and contains either a T1 or

an E1 stream as determined by the T1 bit. For TU11 low, the TU#4 in the current TUG2 group is meaningless and its configuration is ignored.

When the TU11 bit is set high, the T1 bit is ignored. However, when the TU11 bit is set low, the T1 bit selects whether the tributary contains a T1 stream (if the T1 bit is set high) or an E1 stream (if the T1 bit is set low).

NOTE: All tributaries in each TUG2 must be configured to the same tributary type (i.e., either TU-11 or TU-12). In fact, for each TUG2, all tributaries reference the TU11 bit of the first tributary in the group (TU #1). The T1 bit must be configured the same for all tributaries.

The configuration specified by the TU11 and T1 bits is summarized as follows:

TU11	T1	Configuration	Active TU (VT)
0	0	E1 in TU-12 (VT2)	#1, #2, #3
0	1	T1 in TU-12	#1, #2, #3
1	0	Not a Valid Setting	
1	1	T1 in TU-11 (VT1.5)	#1, #2, #3, #4

Register 12B0H, 12B1H, 12B2H, 12B3H, 12B4H, 12B5H, 12B6H: RTDM TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #2, Control

Bit	Type	Function	Default
Bit 7	R	TU11	1
Bit 6	R/W	T1	1
Bit 5	R/W	PROV	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	AIS	0

This register configures the operational modes of TU #3 in TUG2 #1 of TUG3 #2 to TU #3 in TUG2 #7 of TUG3 #2.

AIS:

The AIS bit enables the insertion of AIS on the de-mapped T1 or E1 stream derived from tributary TU #3 in the corresponding TUG2 of TUG3 #2. The AIS bit is logically ORed with the AIS state of this tributary signaled by the AIS pin. When AIS is set high, all payload bits of the de-mapped T1 or E1 stream are set high and the stream clock rate is set to the nominal value (1.544 MHz for T1 and 2.048 MHz for E1). When AIS is set low, AIS insertion is controlled by the AIS pin.

PROV:

The PROV bit enables processing of tributary TU #3 in the corresponding TUG2 of TUG3 #2. When PROV is set high, tributary TU #3 in the corresponding TUG2 of TUG3 #2 is de-mapped normally into either a T1 or an E1 stream as controlled by the TU11 and T1 bits. When PROV is set low, tributary TU #3 in the corresponding TUG2 of TUG3 #2 is not processed.

TU11 and T1 Bits:

The TU11 and T1 bits specify the tributary configuration of TU #3 in the corresponding TUG2 of TUG3 #2.

When the TU11 bit is set high, the tributary is defined as a TU-11 (or VT1.5 in SONET) and contains a T1 stream. When the TU11 bit is set low, the tributary is defined as a TU-12 (or VT2 in SONET) and contains either a T1 or

an E1 stream as determined by the T1 bit. For TU11 low, the TU#4 in the current TUG2 group is meaningless and its configuration is ignored.

When the TU11 bit is set high, the T1 bit is ignored. However, when the TU11 bit is set low, the T1 bit selects whether the tributary contains a T1 stream (if the T1 bit is set high) or an E1 stream (if the T1 bit is set low).

NOTE: All tributaries in each TUG2 must be configured to the same tributary type (i.e., either TU-11 or TU-12). In fact, for each TUG2, all tributaries reference the TU11 bit of the first tributary in the group (TU #1). The T1 bit must be configured the same for all tributaries.

The configuration specified by the TU11 and T1 bits is summarized as follows:

TU11	T1	Configuration	Active TU (VT)
0	0	E1 in TU-12 (VT2)	#1, #2, #3
0	1	T1 in TU-12	#1, #2, #3
1	0	Not a Valid Setting	
1	1	T1 in TU-11 (VT1.5)	#1, #2, #3, #4

Register 12B8H, 12B9H, 12BAH, 12BBH, 12BCH, 12BDH, 12BEH: RTDM TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #2, Control

Bit	Type	Function	Default
Bit 7	R	TU11	1
Bit 6	R/W	T1	1
Bit 5	R/W	PROV	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	AIS	0

This register configures the operational modes of TU #4 in TUG2 #1 of TUG3 #2 to TU #4 in TUG2 #7 of TUG3 #2. When the corresponding TUG2 tributary group is configured to TU-12 (VT2) mode, the associated register in this set has no effect.

AIS:

The AIS bit enables the insertion of AIS on the de-mapped T1 or E1 stream derived from tributary TU #4 in the corresponding TUG2 of TUG3 #2. The AIS bit is logically ORed with the AIS state of this tributary signaled by the AIS pin. When AIS is set high, all payload bits of the de-mapped T1 or E1 stream are set high and the stream clock rate is set to the nominal value (1.544 MHz for T1 and 2.048 MHz for E1). When AIS is set low, AIS insertion is controlled by the AIS pin.

PROV:

The PROV bit enables processing of tributary TU #4 in the corresponding TUG2 of TUG3 #2. When PROV is set high, tributary TU #4 in the corresponding TUG2 of TUG3 #2 is de-mapped normally into either a T1 or an E1 stream as controlled by the TU11 and T1 bits. When PROV is set low, tributary TU #4 in the corresponding TUG2 of TUG3 #2 is not processed.

TU11 and T1 Bits:

The TU11 and T1 bits specify the tributary configuration of TU #4 in the corresponding TUG2 of TUG3 #2.

When the TU11 bit is set high, the tributary is defined as a TU-11 (or VT1.5 in SONET) and contains a T1 stream. When the TU11 bit is set low, the tributary is defined as a TU-12 (or VT2 in SONET) and contains either a T1 or an E1 stream as determined by the T1 bit. For TU11 low, the TU#4 in the current TUG2 group is meaningless and its configuration is ignored.

When the TU11 bit is set high, the T1 bit is ignored. However, when the TU11 bit is set low, the T1 bit selects whether the tributary contains a T1 stream (if the T1 bit is set high) or an E1 stream (if the T1 bit is set low).

NOTE: All tributaries in each TUG2 must be configured to the same tributary type (i.e., either TU-11 or TU-12). In fact, for each TUG2, all tributaries reference the TU11 bit of the first tributary in the group (TU #1). The T1 bit must be configured the same for all tributaries.

The configuration specified by the TU11 and T1 bits is summarized as follows:

TU11	T1	Configuration	Active TU (VT)
0	0	E1 in TU-12 (VT2)	#1, #2, #3
0	1	T1 in TU-12	#1, #2, #3
1	0	Not a Valid Setting	
1	1	T1 in TU-11 (VT1.5)	#1, #2, #3, #4

Register 12C0H, 12C1H, 12C2H, 12C3H, 12C4H, 12C5H, 12C6H: RTDM TU #1 in TUG2 #1 to TUG2 #7 of TUG3 #3, Control

Bit	Type	Function	Default
Bit 7	R/W	TU11	1
Bit 6	R/W	T1	1
Bit 5	R/W	PROV	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	AIS	0

This register configures the operational modes of TU #1 in TUG2 #2 of TUG3 #3 to TU #1 in TUG2 #7 of TUG3 #3.

AIS:

The AIS bit enables the insertion of AIS on the de-mapped T1 or E1 stream derived from tributary TU #1 in the corresponding TUG2 of TUG3 #3. The AIS bit is logically ORed with the AIS state of this tributary signaled by the AIS pin. When AIS is set high, all payload bits of the de-mapped T1 or E1 stream are set high and the stream clock rate is set to the nominal value (1.544 MHz for T1 and 2.048 MHz for E1). When AIS is set low, AIS insertion is controlled by the AIS pin.

PROV:

The PROV bit enables processing of tributary TU #1 in the corresponding TUG2 of TUG3 #3. When PROV is set high, tributary TU #1 in the corresponding TUG2 of TUG3 #3 is de-mapped normally into either a T1 or an E1 stream as controlled by the TU11 and T1 bits. When PROV is set low, tributary TU #1 in the corresponding TUG2 of TUG3 #3 is not processed.

TU11 and T1 Bits:

The TU11 and T1 bits specify the tributary configuration of TU #1 in the corresponding TUG2 of TUG3 #3.

When the TU11 bit is set high, the tributary is defined as a TU-11 (or VT1.5 in SONET) and contains a T1 stream. When the TU11 bit is set low, the tributary is defined as a TU-12 (or VT2 in SONET) and contains either a T1 or

an E1 stream as determined by the T1 bit. For TU11 low, the TU#4 in the current TUG2 group is meaningless and its configuration is ignored.

When the TU11 bit is set high, the T1 bit is ignored. However, when the TU11 bit is set low, the T1 bit selects whether the tributary contains a T1 stream (if the T1 bit is set high) or an E1 stream (if the T1 bit is set low).

NOTE: All tributaries in each TUG2 must be configured to the same tributary type (i.e., either TU-11 or TU-12). In fact, for each TUG2, all tributaries reference the TU11 bit of the first tributary in the group (TU #1). The T1 bit must be configured the same for all tributaries.

The configuration specified by the TU11 and T1 bits is summarized as follows:

TU11	T1	Configuration	Active TU (VT)
0	0	E1 in TU-12 (VT2)	#1, #2, #3
0	1	T1 in TU-12	#1, #2, #3
1	0	Not a Valid Setting	
1	1	T1 in TU-11 (VT1.5)	#1, #2, #3, #4

Register 12C8H, 12C9H, 12CAH, 12CBH, 12CCH, 12CDH, 12CEH: RTDM TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #3, Control

Bit	Type	Function	Default
Bit 7	R	TU11	1
Bit 6	R/W	T1	1
Bit 5	R/W	PROV	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	AIS	0

This register configures the operational modes of TU #2 in TUG2 #1 of TUG3 #3 to TU #2 in TUG2 #7 of TUG3 #3.

AIS:

The AIS bit enables the insertion of AIS on the de-mapped T1 or E1 stream derived from tributary TU #2 in the corresponding TUG2 of TUG3 #3. The AIS bit is logically ORed with the AIS state of this tributary signaled by the AIS pin. When AIS is set high, all payload bits of the de-mapped T1 or E1 stream are set high and the stream clock rate is set to the nominal value (1.544 MHz for T1 and 2.048 MHz for E1). When AIS is set low, AIS insertion is controlled by the AIS pin.

PROV:

The PROV bit enables processing of tributary TU #2 in the corresponding TUG2 of TUG3 #3. When PROV is set high, tributary TU #2 in the corresponding TUG2 of TUG3 #3 is de-mapped normally into either a T1 or an E1 stream as controlled by the TU11 and T1 bits. When PROV is set low, tributary TU #2 in the corresponding TUG2 of TUG3 #3 is not processed.

TU11 and T1 Bits:

The TU11 and T1 bits specify the tributary configuration of TU #2 in the corresponding TUG2 of TUG3 #3.

When the TU11 bit is set high, the tributary is defined as a TU-11 (or VT1.5 in SONET) and contains a T1 stream. When the TU11 bit is set low, the tributary is defined as a TU-12 (or VT2 in SONET) and contains either a T1 or

an E1 stream as determined by the T1 bit. For TU11 low, the TU#4 in the current TUG2 group is meaningless and its configuration is ignored.

When the TU11 bit is set high, the T1 bit is ignored. However, when the TU11 bit is set low, the T1 bit selects whether the tributary contains a T1 stream (if the T1 bit is set high) or an E1 stream (if the T1 bit is set low).

NOTE: All tributaries in each TUG2 must be configured to the same tributary type (i.e., either TU-11 or TU-12). In fact, for each TUG2, all tributaries reference the TU11 bit of the first tributary in the group (TU #1). The TU11 bit of all other tributaries in the group are read-only. The T1 bit must be configured the same for all tributaries.

The configuration specified by the TU11 and T1 bits is summarized as follows:

TU11	T1	Configuration	Active TU (VT)
0	0	E1 in TU-12 (VT2)	#1, #2, #3
0	1	T1 in TU-12	#1, #2, #3
1	0	Not a Valid Setting	
1	1	T1 in TU-11 (VT1.5)	#1, #2, #3, #4

Register 12D0H, 12D1H, 12D2H, 12D3H, 12D4H, 12D5H, 12D6H: RTDM TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #3, Control

Bit	Type	Function	Default
Bit 7	R	TU11	1
Bit 6	R/W	T1	1
Bit 5	R/W	PROV	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	AIS	0

This register configures the operational modes of TU #3 in TUG2 #1 of TUG3 #3 to TU #3 in TUG2 #7 of TUG3 #3.

AIS:

The AIS bit enables the insertion of AIS on the de-mapped T1 or E1 stream derived from tributary TU #3 in the corresponding TUG2 of TUG3 #3. The AIS bit is logically ORed with the AIS state of this tributary signaled by the AIS pin. When AIS is set high, all payload bits of the de-mapped T1 or E1 stream are set high and the stream clock rate is set to the nominal value (1.544 MHz for T1 and 2.048 MHz for E1). When AIS is set low, AIS insertion is controlled by the AIS pin.

PROV:

The PROV bit enables processing of tributary TU #3 in the corresponding TUG2 of TUG3 #3. When PROV is set high, tributary TU #3 in the corresponding TUG2 of TUG3 #3 is de-mapped normally into either a T1 or an E1 stream as controlled by the TU11 and T1 bits. When PROV is set low, tributary TU #3 in the corresponding TUG2 of TUG3 #3 is not processed.

TU11 and T1 Bits:

The TU11 and T1 bits specify the tributary configuration of TU #3 in the corresponding TUG2 of TUG3 #3.

When the TU11 bit is set high, the tributary is defined as a TU-11 (or VT1.5 in SONET) and contains a T1 stream. When the TU11 bit is set low, the tributary is defined as a TU-12 (or VT2 in SONET) and contains either a T1 or

an E1 stream as determined by the T1 bit. For TU11 low, the TU#4 in the current TUG2 group is meaningless and its configuration is ignored.

When the TU11 bit is set high, the T1 bit is ignored. However, when the TU11 bit is set low, the T1 bit selects whether the tributary contains a T1 stream (if the T1 bit is set high) or an E1 stream (if the T1 bit is set low).

NOTE: All tributaries in each TUG2 must be configured to the same tributary type (i.e., either TU-11 or TU-12). In fact, for each TUG2, all tributaries reference the TU11 bit of the first tributary in the group (TU #1). The TU11 bit of all other tributaries in the group are read-only. The T1 bit must be configured the same for all tributaries.

The configuration specified by the TU11 and T1 bits is summarized as follows:

TU11	T1	Configuration	Active TU (VT)
0	0	E1 in TU-12 (VT2)	#1, #2, #3
0	1	T1 in TU-12	#1, #2, #3
1	0	Not a Valid Setting	
1	1	T1 in TU-11 (VT1.5)	#1, #2, #3, #4

Register 12D8H, 12D9H, 12DAH, 12DBH, 12DCH, 12DDH, 12DEH: RTDM TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #3,Control

Bit	Type	Function	Default
Bit 7	R	TU11	1
Bit 6	R/W	T1	1
Bit 5	R/W	PROV	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	AIS	0

This register configures the operational modes of TU #4 in TUG2 #1 of TUG3 #3 to TU #4 in TUG2 #7 of TUG3 #3. When the corresponding TUG2 tributary group is configured to TU-12 (VT2) mode, the associated register in this set has no effect.

AIS:

The AIS bit enables the insertion of AIS on the de-mapped T1 or E1 stream derived from tributary TU #4 in the corresponding TUG2 of TUG3 #3. The AIS bit is logically ORed with the AIS state of this tributary signaled by the AIS pin. When AIS is set high, all payload bits of the de-mapped T1 or E1 stream are set high and the stream clock rate is set to the nominal value (1.544 MHz for T1 and 2.048 MHz for E1). When AIS is set low, AIS insertion is controlled by the AIS pin.

PROV:

The PROV bit enables processing of tributary TU #4 in the corresponding TUG2 of TUG3 #3. When PROV is set high, tributary TU #4 in the corresponding TUG2 of TUG3 #3 is de-mapped normally into either a T1 or an E1 stream as controlled by the TU11 and T1 bits. When PROV is set low, tributary TU #4 in the corresponding TUG2 of TUG3 #3 is not processed.

TU11 and T1 Bits:

The TU11 and T1 bits specify the tributary configuration of TU #4 in the corresponding TUG2 of TUG3 #3.

When the TU11 bit is set high, the tributary is defined as a TU-11 (or VT1.5 in SONET) and contains a T1 stream. When the TU11 bit is set low, the tributary is defined as a TU-12 (or VT2 in SONET) and contains either a T1 or an E1 stream as determined by the T1 bit. For TU11 low, the TU#4 in the current TUG2 group is meaningless and its configuration is ignored.

When the TU11 bit is set high, the T1 bit is ignored. However, when the TU11 bit is set low, the T1 bit selects whether the tributary contains a T1 stream (if the T1 bit is set high) or an E1 stream (if the T1 bit is set low).

NOTE: All tributaries in each TUG2 must be configured to the same tributary type (i.e., either TU-11 or TU-12). In fact, for each TUG2, all tributaries reference the TU11 bit of the first tributary in the group (TU #1). The T1 bit must be configured the same for all tributaries.

The configuration specified by the TU11 and T1 bits is summarized as follows:

TU11	T1	Configuration	Active TU (VT)
0	0	E1 in TU-12 (VT2)	#1, #2, #3
0	1	T1 in TU-12	#1, #2, #3
1	0	Not a Valid Setting	
1	1	T1 in TU-11 (VT1.5)	#1, #2, #3, #4

Register 12E0H: RTDM Pointer Justification Rate Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	E1RATE[1]	0
Bit 3	R/W	E1RATE[0]	0
Bit 2		Unused	X
Bit 1	R/W	T1RATE[1]	0
Bit 0	R/W	T1RATE[0]	0

This register configures the rate at which incoming tributary pointer justifications are leaked out.

T1RATE[1:0]:

The T1RATE[1:0] bits control the base rate at which an incoming tributary pointer justification is leaked out for tributaries carrying a T1 stream. The available base rates are as follows:

T1RATE[1]	T1RATE[0]	Base Rate Period (T1 in TU-11)	Base Rate Period (T1 in TU-12)
0	0	1.20 seconds	0.89 second
0	1	0.94 second	0.69 second
1	0	0.67 second	0.50 second
1	1	Reserved	

* The Reserved selection must not be used for proper operation of the TEMAP.

E1RATE[1:0]:

The E1RATE[1:0] bits control the base rate at which an incoming tributary pointer justification is leaked out for tributaries carrying an E1 stream. The available base rates are as follows:

E1RATE[1]	E1RATE[0]	Rate
0	0	1.09 seconds
0	1	0.89 second
1	0	0.59 second
1	1	*Reserved

* The Reserved selection must not be used for proper operation of the TEMAP.

Register 12E2H: RTDM Time Switch Page Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	APAGE	0

This register allows selection of one of two pages in the time switch configuration RAM to be the active page. Neither time switch page is active when the Ingress Time Switch Enable register bit, ITSEN, in the Master SONET/SDH Ingress Configuration register is a logic 0.

APAGE:

The time switch configuration RAM active page select bit, APAGE, controls the selection of one of two pages in the time switch configuration RAM to be the active page. When APAGE is set high, the configuration in page 1 of the time switch configuration RAM is used to associate incoming tributaries to logical FIFOs in the payload buffer. When APAGE is set low, the configuration in page 0 of the time switch configuration RAM is used to associate incoming tributaries to logical FIFOs in the payload buffer.

Register 12E3H: RTDM Indirect Time Switch Tributary RAM Status and Control

Bit	Type	Function	Default
Bit 7	R	BUSY	X
Bit 6	R/W	RWB	1
Bit 5	R/W	PAGE	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register provides control and status for the indirect RAM containing time switch tributary information. Writing to this register triggers an indirect time switch configuration register access. The BUSY bit will immediately be set high and will remain high until the write is complete. The write will only physically occur during transport overhead cycles such that writes can be safely made to the active page as well. Note that when an indirect write access is to be performed, the RTDM Indirect Ingress Tributary Data register and the RTDM Indirect Time Switch Internal Link Address register must first be setup before writing to this register. This time switch settings configured via this register are inactive when the Ingress Time Switch Enable register bit, ITSEN, in the Master SONET/SDH Ingress Configuration register is a logic 0.

PAGE:

The indirect page select bit, PAGE, selects between accesses to the two pages in the time switch configuration RAM. When PAGE is set high, page 1 of the time switch configuration RAM is accessed. When PAGE is set low, page 0 of the RAM is accessed. The PAGE bit should be different than the APAGE bit (register 12E2H) when writing to the RAM as writing to the active page is not recommended.

RWB:

The indirect access control bit, RWB, selects between a configure (write) or interrogate (read) access to the time switch configuration RAM. Writing a logic zero to RWB triggers an indirect write operation. Data to be written is taken from the Indirect Time Switch Tributary register. Writing a logic one to

RWB triggers an indirect read operation. The read can be found in the Indirect Tributary Data register.

BUSY:

The BUSY bit reports the status of the prevailing indirect access operation. BUSY is set high when a write to the Indirect Time Switch Tributary Address register triggers an indirect access and remains high until the access is complete. The BUSY bit should be polled until it is low to determine when data from an indirect read operation is available in the Indirect Tributary Data register or when a new indirect write operation may commence. If LREFCLK disappears during an access, the BUSY bit can stay high.

Register 12E4H: RTDM Indirect Time Switch Internal Link

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	INT_SPE[1]	0
Bit 5	R/W	INT_SPE[0]	1
Bit 4	R/W	INT_LINK[4]	0
Bit 3	R/W	INT_LINK[3]	0
Bit 2	R/W	INT_LINK[2]	0
Bit 1	R/W	INT_LINK[1]	0
Bit 0	R/W	INT_LINK[0]	1

This address specified by this register is the TEMAP internal link number that ingress tributaries to the TEMAP will be switched to when the Ingress Time Switch Enable register bit, ITSEN, in the Master SONET/SDH Ingress Configuration register is a logic 1. The ingress tributary that will be mapped to this internal link number is the Ingress tributary number specified via the RTDM Indirect Ingress Tributary Data register and is contained in the time switch RAM at the address specified by this register.

When switching tributaries via the ingress time switch, the LDROPSEL[1:0] bits in the SONET/SDH Mapper Master Configuration register must be set to “00” for switched access to all tributaries within the STS-3/STM-1.

INT_LINK [4:0]:

The indirect internal link number bits (INT_LINK[4:0]) associate the specified T1 or E1 stream internal to the TEMAP and matching the system side interface with the ingress tributary specified in the Indirect Ingress Tributary Data register. The internal link number that an ingress tributary will be switched to, must be set up in this register before triggering the indirect write or read via the RTDM Indirect Ingress Tributary Data register. INT_LINK [4:0] ranges from 00001b to 10101b (1 to 21) for E1 streams and from 00001b to 11100b (1 to 28) for T1 streams.

INT_SPE[1:0]:

The indirect internal synchronous payload envelope bits, SPE[1:0], associate the specified T1 or E1 stream internal to the TEMAP and matching the system side interface with the ingress tributary specified in the Indirect Ingress Tributary Data register. Before triggering the indirect write operation,

the internal SPE number must be set up in this register. SPE[1:0] must always be set to 01b (SPE number 1) for correct operation of the TEMAP.

Register 12E5H: RTDM Indirect Time Switch Tributary

Bit	Type	Function	Default
Bit 7	R/W	ING_TUG3[1]	X
Bit 6	R/W	ING_TUG3[0]	X
Bit 5	R/W	ING_TUG2[2]	X
Bit 4	R/W	ING_TUG2[1]	X
Bit 3	R/W	ING_TUG2[0]	X
Bit 2	R/W	ING_TU[2]	X
Bit 1	R/W	ING_TU[1]	X
Bit 0	R/W	ING_TU[0]	X

This register identifies an ingress tributary that will be switched to an internal link number through the time switch configuration RAM. An indirect access to the time switch configuration RAM, associates the ingress link specified in this register with the internal link number forming the RAM address as specified in the RTDM Indirect Time Switch Internal Link Address register. The time switch selection configured via this indirect data register are inactive when the Ingress Time Switch Enable register bit, ITSEN, in the Master SONET/SDH Ingress Configuration register is a logic 0.

ING_TU[2:0]:

The indirect ingress tributary unit bits (ING_TU[2:0]) indicate the tributary unit to be switched to the internal link identified in the RTDM Indirect Time Switch Internal Link Address register. Legal ING_TU[2:0] ranges are ‘b001 to ‘b100.

ING_TUG2[2:0]:

The indirect ingress tributary unit group 2 bits (ING_TUG2[2:0]) indicate the tributary unit group 2 to be switched to the internal link identified in the RTDM Indirect Time Switch Internal Link Address register. Legal ING_TUG2[2:0] ranges are ‘b001 to ‘b111.

ING_TUG3[1:0]:

The indirect ingress tributary unit group 3 bits (ING_TUG2[1:0]) indicate the tributary unit group 3 to be switched to the internal link identified in the RTDM Indirect Time Switch Internal Link Address register. Legal ING_TUG3[1:0] ranges are ‘b01 to ‘b11.

Register 12E6H: RTDM Demap State Vector RAM Address

Bit	Type	Function	Default
Bit 7	R/W	TUG-3[1]	0
Bit 6	R/W	TUG-3[0]	1
Bit 5	R/W	TUG-2[2]	0
Bit 4	R/W	TUG-2[1]	0
Bit 3	R/W	TUG-2[0]	1
Bit 2	R/W	TU[2]	0
Bit 1	R/W	TU[1]	0
Bit 0	R/W	TU[0]	1

This register contains the demap block state vector RAM debug address bits. Please note that the TEMAP start-up procedure in the PMC-1991268 TEMAP Programmer's Guide should be referenced for correct usage of the de-mapping state vectors.

TUG-3[1:0]:

The TUG-3[1:0] address bits contain the Telecom side tributary TUG-3 location. The valid rage of TUG-3 is 01b to 11b.

TUG-2[2:0]:

The TUG-2[2:0] address bits contain the Telecom side tributary TUG-2 location. The valid range of TUG-2 is 001b to 111b.

TU[2:0]:

The TU[2:0] address bits contain the Telecom side tributary TU location. The valid range of TU is 001b to 100b for TU-11 tributaries and 001b to 011b for TU-12 tributaries.

Register 12E7H: RTDM Demap State Vector RAM Control and Data

Bit	Type	Function	Default
Bit 7	R/W	CAPTURE_EN	0
Bit 6	R/W	READ_NEW	1
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	D[33]	0

This register contains the demap block state vector RAM control and data bit(s). Please note that the TEMAP start-up procedure in the PMC-1991268 TEMAP Programmer's Guide should be referenced for correct usage of the de-mapping state vectors.

CAPTURE_EN:

The CAPTURE_EN bit enables the continuous capturing of state vectors for the tributary identified in register Register 12E6H: Demap State Vector RAM Address. When CAPTURE_EN is low, capturing is disabled and the last two state vectors are held for reading. When CAPTURE_EN is high, the state vector for the tributary identified in register 12E6H will be captured each time the tributary is serviced. Both an old (previous) and new (current) state vector are held in flops. The values read in D[33:0] are only valid if CAPTURE_EN has been held high at least once since reset for enough time for the selected tributary to be serviced twice. Otherwise, the storage registers will contain zeroes.

READ_NEW:

The READ_NEW bit selects which of the two stored vectors to retrieve when reading D[33:0]. When READ_NEW is high, the new state vector is selected; when low, the old state vector is selected.

D[33]:

The D[33] data bit is the most significant data bit in the state vector selected by READ_NEW when CAPTURE_EN has been asserted for long enough to capture 2 state vectors for the selected tributary.

Register 12E8H: RTDM Demap Debug State Vector RAM Data

Bit	Type	Function	Default
Bit 7	R	D[31]	0
Bit 6	R	D[30]	0
Bit 5	R	D[29]	0
Bit 4	R	D[28]	0
Bit 3	R	D[27]	0
Bit 2	R	D[26]	0
Bit 1	R	D[25]	0
Bit 0	R	D[24]	0

This register contains the demap block state vector RAM data bits. Please note that the TEMAP start-up procedure in the PMC-1991268 TEMAP Programmer's Guide should be referenced for correct usage of the de-mapping state vectors.

D[31:24]:

The D[31:24] data bits contain a portion of the state vector selected by READ_NEW (register 12E7H) when CAPTURE_EN (register 12E7H) has been asserted for long enough to capture 2 state vectors for the selected tributary.

Register 12E9H: RTDM Demap State Vector RAM Data

Bit	Type	Function	Default
Bit 7	R	D[23]	0
Bit 6	R	D[22]	0
Bit 5	R	D[21]	0
Bit 4	R	D[20]	0
Bit 3	R	D[19]	0
Bit 2	R	D[18]	0
Bit 1	R	D[17]	0
Bit 0	R	D[16]	0

This register contains the demap block state vector RAM data bits. Please note that the TEMAP start-up procedure in the PMC-1991268 TEMAP Programmer's Guide should be referenced for correct usage of the de-mapping state vectors.

D[23:16]:

The D[23:16] data bits contain a portion of the state vector selected by READ_NEW (register 12E7H) when CAPTURE_EN (register 12E7H) has been asserted for long enough to capture 2 state vectors for the selected tributary.

Register 12EAH: RTDM Demap State Vector RAM Data

Bit	Type	Function	Default
Bit 7	R	D[15]	0
Bit 6	R	D[14]	0
Bit 5	R	D[13]	0
Bit 4	R	D[12]	0
Bit 3	R	D[11]	0
Bit 2	R	D[10]	0
Bit 1	R	D[9]	0
Bit 0	R	D[8]	0

This register contains the demap block state vector RAM data bits. Please note that the TEMAP start-up procedure in the PMC-1991268 TEMAP Programmer's Guide should be referenced for correct usage of the de-mapping state vectors.

D[15:8]:

The D[15:8] data bits contain a portion of the state vector selected by READ_NEW (register 12E7H) when CAPTURE_EN (register 12E7H) has been asserted for long enough to capture 2 state vectors for the selected tributary.

Register 12EBH: RTDM Demap State Vector RAM Data

Bit	Type	Function	Default
Bit 7	R	D[7]	0
Bit 6	R	D[6]	0
Bit 5	R	D[5]	0
Bit 4	R	D[4]	0
Bit 3	R	D[3]	0
Bit 2	R	D[2]	0
Bit 1	R	D[1]	0
Bit 0	R	D[0]	0

This register contains the demap block state vector RAM data bits. Please note that the TEMAP start-up procedure in the PMC-1991268 TEMAP Programmer's Guide should be referenced for correct usage of the de-mapping state vectors.

D[7:0]:

The D[7:0] data bits contain the least significant portion of the state vector selected by READ_NEW (register 12E7H) when CAPTURE_EN (register 12E7H) has been asserted for long enough to capture 2 state vectors for the selected tributary.

1.25 RTOP Receive Tributary Path Overhead Processor Registers

Register 1300H: RTOP, TU #1 in TUG2 #1, Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	1
Bit 6	R/W	TU11	1
Bit 5	R/W	BLKBIP	0
Bit 4	R/W	PSLUE	0
Bit 3	R/W	PSLME	0
Bit 2	R/W	COPSLE	0
Bit 1	R/W	RFIE	0
Bit 0	R/W	RDIE	0

This register reports the status and configures the operational modes of TU #1 in TUG2 #1.

RDIE:

The RDIE bit enables the remote defect indication interrupt for tributary TU #1 in TUG2 #1. When RDIE is set high, an interrupt is generated upon changes of RDI status. Interrupts due to RDI status change are masked when RDIE is set low. The RDI status is derived from bit 8 of the V5 byte when RDIZ7EN is set low and from bits 5 to 7 of the Z7 byte when RDIZ7EN is set high.

RFIE:

The RFIE bit enables the remote failure indication interrupt for tributary TU #1 in TUG2 #1. When RDIZ7EN is set low, an interrupt is generated upon assertion and negation events of the RFIV bit when RFIE is set high. Interrupts due to RFIV status change are masked when RFIE is set low. When RDIZ7EN is set high, RFIE is ignored.

COPSLE:

The COPSLE bit enables the change of tributary path signal label interrupt for tributary TU #1 in TUG2 #1. When COPSLE is set high, an interrupt is generated when the accepted path signal label changes. Interrupts due to change of PSL are masked when COPSLE is set low.

PSLME:

The PSLME bit enables the tributary path signal label mismatch interrupt for tributary TU #1 in TUG2 #1. When PSLME is set high, an interrupt is generated when the accepted path signal label changes from mismatching the provisioned PSL to matching the provisioned value, or vice versa. Interrupts due to PSL mismatch status change are masked when PSLME is set low.

PSLUE:

The PSLUE bit enables the tributary path signal label unstable interrupt for tributary TU #1 in TUG2 #1. When PSLUE is set high, an interrupt is generated when the received path signal label becomes unstable or returns to stable. Interrupts due to PSL unstable status change are masked when PSLUE is set low.

BLKBIP:

The BLKBIP bit controls the accumulation of tributary BIP-2 errors for the tributary TU #1 in TUG2 #1. When BLKBIP is set high, BIP-2 errors are counted on a block basis; the BIP error count is incremented by one when one or both of the BIP-2 bits are in error. When BLKBIP is set low, BIP-2 two errors are counted on a nibble basis; the BIP error count is incremented once for each BIP-2 bit that is in error.

TU11:

The TU11 bit specifies the tributary configuration of tributary group TUG2 #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMAP.

Register 1301H: RTOP, TU #1 in TUG2 #1, Configuration and Alarm Status

Bit	Type	Function	Default
Bit 7	R/W	RDIZ7EN	0
Bit 6	R/W	TUPTE	0
Bit 5	R/W	Reserved	0
Bit 4	R	PSLUV	X
Bit 3	R	PSLMV	X
Bit 2	R	ERDIV[2]	X
Bit 1	R	ERDIV[1]/RFIV	X
Bit 0	R	ERDIV[0]/RDIV	X

This register reports alarm status and configures TU #1 in TUG2 #1.

RDIV:

The RDIV bit indicates the remote defect indication status of tributary TU #1 in TUG2 #1 when RDIZ7EN is low. RDIV is set high when the RDI bit in the V5 byte is set high for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP Configuration register (addresses 1205H). RDIV is set low when the RDI bit is set low for five or ten consecutive multiframes as determined by the RDI10 bit.

RFIV:

The RFIV bit indicates the remote failure indication status of tributary TU #1 in TUG2 #1 when RDIZ7EN is set low. RFIV is set high when the RFI bit in the V5 byte is set high for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP Configuration register (addresses 1205H). RFIV is set low when the RFI bit is set low for five or ten consecutive multiframes as determined by the RDI10 bit.

ERDIV[2:0]:

The ERDIV[2:0] bits indicates the extended remote defect indication status of tributary TU #1 in TUG2 #1 when RDIZ7EN is set high. The ERDIV[2:0] bits are set to a new code when the same code in the extended RDI bits of the Z7 byte is seen for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP Configuration (addresses 1205H).

PSLMV:

The PSLMV bit indicates the path signal mismatch status of tributary TU #1 in TUG2 #1. PSLMV is set high when the accepted PSL differs from the provisioned value. PSLMV is set low when the accepted PSL has the same value as the provisioned one.

PSLUV:

The PSLUV bit indicates the path signal unstable status of tributary TU #1 in TUG2 #1. The PSL unstable counter is incremented if the PSL of the current multiframe differs from that in the previous multiframe. The counter is cleared to zero when the same PSL is received for five consecutive multiframes. The tributary PSL unstable alarm is asserted and PSLUV set high when the unstable counter reaches five. The PSL unstable alarm is negated and PSLUV set low when the unstable counter is cleared.

Reserved:

The Reserved bit must be programmed to logic 0 for normal operation.

TUPTE:

The TUPTE bit determines the alarm conditions under which AIS is inserted for tributary TU #1 in TUG2 #1 mapped in TUG3. TUPTE is set high if tributary TU #1 is to be terminated in the network element containing this TEMAP device. In this case, tributary AIS is automatically inserted based on the contents of the Ingress Tributary Alarm AIS Control register (address 1206H). TUPTE is set low if tributary TU #1 is part of the through traffic in the network element containing this TEMAP device. In this case, tributary AIS is only inserted when a loss of pointer (LOP) or a loss of multiframe (LOM) alarm is detected (as determined by the Ingress Tributary Alarm AIS Control register).

RDIZ7EN:

The RDIZ7EN indicates which tributary path overhead byte is used for controlling the ERDI[2:0] or RDI/RFI bits. When RDIZ7EN is set low, the RDI and RFI bits in the V5 byte are used to control the RDIV and RFIV register bits. When RDIZ7EN is set high, the three bit extended RDI code in the Z7 byte is used to control the ERDIV[2:0] register bits.

Register 1302H: RTOP, TU #1 in TUG2 #1, Expected Path Signal Label

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	EPSL[2]	0
Bit 1	R/W	EPSL[1]	0
Bit 0	R/W	EPSL[0]	0

This register configures the expected path signal label of TU #1 in TUG2 #1.

EPSL[2:0]:

EPSL[2:0] specifies the expected path signal label of tributary TU #1 in TUG2 #1. The expected PSL is compared with the accepted PSL to determine the PSLM state.

Register 1303H: RTOP, TU3 or TU #1 in TUG2 #1, Accepted Path Signal Label

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	APSL[2]	0
Bit 1	R	APSL[1]	0
Bit 0	R	APSL[0]	0

This register reports the accepted path signal label of TU #1 in TUG2 #1.

APSL[2:0]:

APSL[2:0] specifies the accepted path signal label of tributary TU #1 in TUG2 #1. The expected PSL is compared with the accepted PSL to determine the PSLM state.

Register 1304H: RTOP, TU #1 in TUG2 #1, BIP-2 Error Count LSB

Bit	Type	Function	Default
Bit 7	R	BIP[7]	X
Bit 6	R	BIP[6]	X
Bit 5	R	BIP[5]	X
Bit 4	R	BIP[4]	X
Bit 3	R	BIP[3]	X
Bit 2	R	BIP[2]	X
Bit 1	R	BIP[1]	X
Bit 0	R	BIP[0]	X

Register 1305H: RTOP, TU #1 in TUG2 #1, BIP-2 Error Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	BIP[10]	X
Bit 1	R	BIP[9]	X
Bit 0	R	BIP[8]	X

This register reports the number of block interleave parity (BIP-2) errors detected in TU #1 in TUG2 #1. These registers do not saturate.

BIP[10:0]:

The BIP[10:0] bits reports the number of tributary path bit-interleaved parity errors that have been detected since the last time the BIP-2 registers were polled. The BIP-2 registers are polled by writing to the Master SONET/SDH Accumulate Trigger register which transfers the internally accumulated error count to the BIP-2 registers within 10 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation. BIP-2 errors may

be accumulated on a nibble/bit basis or block basis as controlled by the BLKBIP register bit.

Register 1306H: RTOP TU #1 in TUG2 #1, FEBE Error Count LSB

Bit	Type	Function	Default
Bit 7	R	FEBE[7]	X
Bit 6	R	FEBE[6]	X
Bit 5	R	FEBE[5]	X
Bit 4	R	FEBE[4]	X
Bit 3	R	FEBE[3]	X
Bit 2	R	FEBE[2]	X
Bit 1	R	FEBE[1]	X
Bit 0	R	FEBE[0]	X

Register 1307H: RTOP TU #1 in TUG2 #1, FEBE Error Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	FEBE[10]	X
Bit 1	R	FEBE[9]	X
Bit 0	R	FEBE[8]	X

This register reports the number of far end block errors (FEBE) detected in TU #1 in TUG2 #1.

FEBE[10:0]:

The FEBE[10:0] bits reports the number of tributary path far end block errors that have been detected since the last time the FEBE registers were polled. The FEBE registers are polled by writing to the Master SONET/SDH Accumulate Trigger register. The write access transfers the internally accumulated error counts to the FEBE registers within 10 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation.

Register 1308H, 1310H, 1318H, 1320H, 1328H, 1330H: RTOP, TU #1 in TUG2 #2 to TUG2 #7, Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	1
Bit 6	R/W	TU11	1
Bit 5	R/W	BLKBIP	0
Bit 4	R/W	PSLUE	0
Bit 3	R/W	PSLME	0
Bit 2	R/W	COPSLE	0
Bit 1	R/W	RFIE	0
Bit 0	R/W	RDIE	0

This set of registers configures the operational modes of TU #1 in TUG2 #2 to TUG2 #7.

RDIE:

The RDIE bit enables the remote defect indication interrupt for tributary TU #1 in the corresponding TUG2. When RDIE is set high, an interrupt is generated upon changes of RDI status. Interrupts due to RDI status change are masked when RDIE is set low. The RDI status is derived from bit 8 of the V5 byte when RDIZ7EN is set low and from bits 5 to 7 of the Z7 byte when RDIZ7EN is set high.

RFIE:

The RFIE bit enables the remote failure indication interrupt for tributary TU #1 in the corresponding TUG2. When RDIZ7EN is set low, an interrupt is generated upon assertion and negation events of the RFIV bit when RFIE is set high. Interrupts due to RFIV status change are masked when RFIE is set low. When RDIZ7EN is set high, RFIE is ignored.

COPSLE:

The COPSLE bit enables the change of tributary path signal label interrupt for tributary TU #1 in the corresponding TUG2. When COPSLE is set high, an interrupt is generated when the accepted path signal label changes. Interrupts due to change of PSL are masked when COPSLE is set low.

PSLME:

The PSLME bit enables the tributary path signal label mismatch interrupt for tributary TU #1 in the corresponding TUG2. When PSLME is set high, an interrupt is generated when the accepted path signal label changes from mismatching the provisioned PSL to matching the provisioned value, or vice versa. Interrupts due to PSL mismatch status change are masked when PSLME is set low.

PSLUE:

The PSLUE bit enables the tributary path signal label unstable interrupt for tributary TU #1 in the corresponding TUG2. When PSLUE is set high, an interrupt is generated when the received path signal label becomes unstable or returns to stable. Interrupts due to PSL unstable status change are masked when PSLUE is set low.

BLKBIP:

The BLKBIP bit controls the accumulation of tributary BIP-2 errors for the tributary TU #1 in the corresponding TUG2. When BLKBIP is set high, BIP-2 errors are counted on a block basis; the BIP error count is incremented by one when one or both of the BIP-2 bits are in error. When BLKBIP is set low, the BIP error count is incremented once for each BIP-2 bit that is in error.

TU11:

The TU11 bit specifies the tributary configuration of the corresponding TUG2. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMAP.

Register 1309H, 1311H, 1319H, 1321H, 1329H, 1331H: RTOP, TU #1 in TUG2 #2 to TUG2 #7, Configuration and Alarm Status

Bit	Type	Function	Default
Bit 7	R/W	RDIZ7EN	0
Bit 6	R/W	TUPTE	0
Bit 5	R/W	Reserved	0
Bit 4	R	PSLUV	X
Bit 3	R	PSLMV	X
Bit 2	R	ERDIV[2]	X
Bit 1	R	ERDIV[1]/RFIV	X
Bit 0	R	ERDIV[0]/RDIV	X

This set of registers reports alarm status and configures TU #1 in TUG2 #2 to TUG2 #7.

RDIV:

The RDIV bit indicates the remote defect indication status of tributary TU #1 in the corresponding TUG2 when RDIZ7EN is low. RDIV is set high when the RDI bit in the V5 byte is set high for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP Configuration register (addresses 1205H). RDIV is set low when the RDI bit is set low for five or ten consecutive multiframes as determined by the RDI10 bit

RFIV:

The RFIV bit indicates the remote failure indication status of tributary TU #1 in the corresponding TUG2 when RDIZ7EN is set low. RFIV is set high when the RFI bit in the V5 byte is set high for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP Configuration register (addresses 1205H). RFIV is set low when the RFI bit is set low for five or ten consecutive multiframes as determined by the RDI10 bit.

ERDIV[2:0]:

The ERDIV[2:0] bits indicates the extended remote defect indication status of tributary TU #1 in the corresponding TUG2 when RDIZ7EN is set high. The ERDIV[2:0] bits are set to a new code when the same code in the extended RDI bits of the Z7 byte is seen for five or ten consecutive multiframes as

determined by the RDI10 bit in the RTOP Configuration register (addresses 1205H).

PSLMV:

The PSLMV bit indicates the path signal mismatch status of tributary TU #1 in the corresponding TUG2. PSLMV is set high when the accepted PSL differs from the provisioned value. PSLMV is set low when the accepted PSL has the same value as the provisioned one.

PSLUV:

The PSLUV bit indicates the path signal unstable status of tributary TU #1 in the corresponding TUG2. The PSL unstable counter is incremented if the PSL of the current multiframe differs form that in the previous multiframe. The counter is cleared to zero when the same PSL is received for five consecutive multiframes. The tributary PSL unstable alarm is asserted and PSLUV set high when the unstable counter reaches five. The PSL unstable alarm is negated and PSLUV set low when the unstable counter is cleared.

Reserved:

The Reserved bit must be programmed to logic 0 for normal operation.

TUPTE:

The TUPTE bit determines the alarm conditions under which AIS is inserted for tributary TU #1 in the corresponding TUG2. TUPTE is set high if tributary TU #1 is to be terminated in the network element containing this TEMAP device. In this case, tributary AIS is automatically inserted based on the contents of the Master SONET/SDH Tributary Alarm AIS Control register (address 1206H). TUPTE is set low if tributary TU #1 is part of the through traffic in the network element containing this TEMAP device. In this case, tributary AIS is only inserted when a loss of pointer (LOP) or a loss of multiframe (LOM) alarm is detected (as determined by the global Tributary Alarm AIS Control register).

RDIZ7EN:

The RDIZ7EN indicates which tributary path overhead byte is used for controlling the ERDI[2:0] or RDI/RFI bits of tributary TU #1 in the corresponding TUG2 . When RDIZ7EN is set low, the RDI and RFI bits in the V5 byte are used to control the RDIV and RFIV register bits. When RDIZ7EN is set high, the three bit extended RDI code in the Z7 byte is used to control the ERDIV[2:0] register bits.

Register 130AH, 1312H, 131AH, 1322H, 132AH, 1332H: RTOP, TU #1 in TUG2 #2 to TUG2 #7, Expected Path Signal Label

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	EPSL[2]	0
Bit 1	R/W	EPSL[1]	0
Bit 0	R/W	EPSL[0]	0

This set of registers configures the expected path signal label of TU #1 in TUG2 #2 to TUG2 #7.

EPSL[2:0]:

The EPSL[2:0] bits specifies the expected path signal label of tributary TU #1 in the corresponding TUG2. The expected PSL is compared with the accepted PSL to determine the PSLM state.

Register 130BH, 1313H, 131BH, 1323H, 132BH, 1333H: RTOP, TU #1 in TUG2 #2 to TUG2 #7, Accepted Path Signal Label

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	APSL[2]	0
Bit 1	R	APSL[1]	0
Bit 0	R	APSL[0]	0

This set of registers reports the accepted path signal label of TU #1 in TUG2 #2 to TUG2 #7.

APSL[2:0]:

The APSL[2:0] bits reports the accepted path signal label of tributary TU #1 in the corresponding TUG2. An incoming PSL is accepted when the same value is received for five consecutive multiframes.

Register 130CH, 1314H, 131CH, 1324H, 132CH, 1334H: RTOP, TU #1 in TUG2 #2 to TUG2 #7, BIP-2 Error Count LSB

Bit	Type	Function	Default
Bit 7	R	BIP[7]	X
Bit 6	R	BIP[6]	X
Bit 5	R	BIP[5]	X
Bit 4	R	BIP[4]	X
Bit 3	R	BIP[3]	X
Bit 2	R	BIP[2]	X
Bit 1	R	BIP[1]	X
Bit 0	R	BIP[0]	X

Register 130DH, 1315H, 131DH, 1325H, 132DH, 1335H: RTOP, TU #1 in TUG2 #2 to TUG2 #7, BIP-2 Error Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	BIP[10]	X
Bit 1	R	BIP[9]	X
Bit 0	R	BIP[8]	X

These sets of registers report the number of block interleave parity (BIP-2) errors detected in TU #1 in TUG2 #2 to TUG2 #7 in the previous accumulation interval. These registers do not saturate.

BIP[10:0]:

The BIP[10:0] bits reports the number of tributary path bit-interleaved parity errors that have been detected since the last time the BIP-2 registers were polled. The BIP-2 registers are polled by writing to any of the Master SONET/SDH Accumulate Trigger register. The write access transfers the

internally accumulated error count to the BIP-2 registers within 10 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation. BIP-2 errors may be accumulated on a nibble basis or block basis as controlled by the BLKBIP register bit.

Register 130EH, 1316H, 131EH, 1326H, 132EH, 1336H: TU #1 in TUG2 #2 to TUG2 #7, FEBE Error Count LSB

Bit	Type	Function	Default
Bit 7	R	FEBE[7]	X
Bit 6	R	FEBE[6]	X
Bit 5	R	FEBE[5]	X
Bit 4	R	FEBE[4]	X
Bit 3	R	FEBE[3]	X
Bit 2	R	FEBE[2]	X
Bit 1	R	FEBE[1]	X
Bit 0	R	FEBE[0]	X

Register 130FH, 1317H, 131FH, 1327H, 132FH, 1337H: TU #1 in TUG2 #2 to TUG2 #7, FEBE Error Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	FEBE[10]	X
Bit 1	R	FEBE[9]	X
Bit 0	R	FEBE[8]	X

These registers reports the number of far end block errors (FEBE) detected in TU #1 in TUG2 #2 to TUG2 #7 in the previous accumulation interval.

FEBE[10:0]:

The FEBE[10:0] bits reports the number of tributary path far end block errors that have been detected since the last time the FEBE registers were polled. The FEBE registers are polled by applying by writing to the Master SONET/SDH Accumulate Trigger register. The write access transfers the internally accumulated error count to the FEBE registers within 10 µs and

simultaneously resets the internal counter to begin a new cycle of error accumulation.

Register 1338H: RTOP, TU #1 in TUG2 #1 to TUG2 #7, COPSL Interrupt

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R	COPSL7I	0
Bit 5	R	COPSL6I	0
Bit 4	R	COPSL5I	0
Bit 3	R	COPSL4I	0
Bit 2	R	COPSL3I	0
Bit 1	R	COPSL2I	0
Bit 0	R	COPSL1I	0

This register is used to identify and acknowledge change of path signal label interrupts for the tributaries TU #1 in TUG2 #1 to TUG2 #7.

COPSL1I-COPSL7I:

The COPSL1I to COPSL7I bits identify the source of change of path signal label interrupts. The COPSL1I to COPSL7I bits report and acknowledge COPSL interrupt of TU #1 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the accepted PSL changes. An COPSL*x*I bit is set high when a change of PSL event on the associated tributary (TU #1 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. COPSL*x*I remains valid when interrupts are not enabled (COPSLE set low) and may be polled to detect change of path signal label events.

Reserved:

The Reserved bit must be written with a logic 0 for proper operation of the TEMAP.

Register 1339H: RTOP, TU #1 in TUG2 #1 to TUG2 #7, PSLM Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	PSLM7I	0
Bit 5	R	PSLM6I	0
Bit 4	R	PSLM5I	0
Bit 3	R	PSLM4I	0
Bit 2	R	PSLM3I	0
Bit 1	R	PSLM2I	0
Bit 0	R	PSLM1I	0

This register is used to identify and acknowledge path signal label mismatch interrupts for the tributaries TU #1 in TUG2 #1 to TUG2 #7.

PSLM1I-PSLM7I:

The PSLM1I to PSLM7I bits identify the source of path signal label mismatch interrupts. The PSLM2I to PSLM7I bits report and acknowledge PSLM interrupt of TU #1 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the accepted PSL becomes matched to the expected PSL or becomes mismatched to the expected PSL. An PSLM*x*I bit is set high when a change of PSL matched state on the associated tributary (TU #1 in TUG2 #*x*) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PSLM*x*I remains valid when interrupts are not enabled (PSLME set low) and may be polled to detect path signal label match/mismatch events.

Register 133AH: RTOP, TU #1 in TUG2 #1 to TUG2 #7, PSLU Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	PSLU7I	0
Bit 5	R	PSLU6I	0
Bit 4	R	PSLU5I	0
Bit 3	R	PSLU4I	0
Bit 2	R	PSLU3I	0
Bit 1	R	PSLU2I	0
Bit 0	R	PSLU1I	0

This register is used to identify and acknowledge path signal label unstable interrupts for the tributaries TU #1 in TUG2 #1 to TUG2 #7.

PSLU1I-PSLU7I:

The PSLU1I to PSLU7I bits identify the source of path signal label mismatch interrupts. PSLU1I to PSLU7I bits report and acknowledge PSLU interrupt of TU #1 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the received PSL becomes unstable or returns to stable. An PSLU*x*I bit is set high when a change of PSL unstable state on the associated tributary (TU #1 in TUG2 #*x*) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PSLU*x*I remains valid when interrupts are not enabled (PSLUE set low) and may be polled to detect path signal label stable/unstable events.

Register 133BH: RTOP, TU #1 in TUG2 #1 to TUG2 #7, RDI Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	RDI7I	0
Bit 5	R	RDI6I	0
Bit 4	R	RDI5I	0
Bit 3	R	RDI4I	0
Bit 2	R	RDI3I	0
Bit 1	R	RDI2I	0
Bit 0	R	RDI1I	0

This register is used to identify and acknowledge remote defect indication interrupts for the tributaries TU #1 in TUG2 #1 to TUG2 #7.

RDI1I-RDI7I:

The RDI1I to RDI7I bits identify the source of remote defect indication interrupts. The RDI2I to RDI7I bits report and acknowledge RDI interrupt of TU #1 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the received RDI state changes. An RDI*x*I bit is set high when a change of RDI state on the associated tributary (TU #1 in TUG2 #*x*) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. RDI*x*I remains valid when interrupts are not enabled (RDIE set low) and may be polled to detect change of remote defect indication events.

Register 133CH: RTOP, TU #1 in TUG2 #1 to TUG2 #7 RFI Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	RFI7I	0
Bit 5	R	RFI6I	0
Bit 4	R	RFI5I	0
Bit 3	R	RFI4I	0
Bit 2	R	RFI3I	0
Bit 1	R	RFI2I	0
Bit 0	R	RFI1I	0

This register is used to identify and acknowledge remote failure indication interrupts for the tributaries TU #1 in TUG2 #1 to TUG2 #7.

RFI1I-RFI7I:

The RFI1I to RFI7I bits identify the source of remote failure indication interrupts. RFI1I to RFI7I bits report and acknowledge RFI interrupt of TU #1 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the received RFI state changes. An RFI*x*I bit is set high when a change of RFI state on the associated tributary (TU #1 in TUG2 #*x*) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. RFI*x*I remains valid when interrupts are not enabled (RFIE set low) and may be polled to detect change of remote failure indication events.

Register 133DH: RTOP, TU #1 in TUG2 #1 to TUG2 #7, Inband Error Reporting Configuration

Bit	Type	Function	Default
Bit 7		Unused	x
Bit 6	R/W	IBER7	0
Bit 5	R/W	IBER6	0
Bit 4	R/W	IBER5	0
Bit 3	R/W	IBER4	0
Bit 2	R/W	IBER3	0
Bit 1	R/W	IBER2	0
Bit 0	R/W	IBER1	0

This register enables the inband error reporting mode of the tributaries TU #1 in TUG2 #1 to TUG2 #7.

IBER1-IBER7:

The IBER1 to IBER7 bits control in band error reporting for tributary TU #1 in TUG2 #2 to TUG2 #7, respectively. Setting an IBER*x* bit high causes in band error reporting information to be inserted in the V5 byte of tributary TU #1 of the corresponding TUG2. When an IBER*x* bit is low, in band error reporting is disabled and the V5 byte of tributary TU #1 of the corresponding TUG2 is not modified.

Register 1340H, 1348H, 1350H, 1358H, 1360H, 1368H, 1370H: RTOP, TU #2 in TUG2 #1 to TUG2 #7, Configuration

Bit	Type	Function	Default
Bit 7	R	Reserved	1
Bit 6	R	TU11	1
Bit 5	R/W	BLKBIP	0
Bit 4	R/W	PSLUE	0
Bit 3	R/W	PSLME	0
Bit 2	R/W	COPSLE	0
Bit 1	R/W	RFIE	0
Bit 0	R/W	RDIE	0

This set of registers configures the operational modes of TU #2 in TUG2 #1 to TUG2 #7.

RDIE:

The RDIE bit enables the remote defect indication interrupt for tributary TU #1 in the corresponding TUG2. When RDIE is set high, an interrupt is generated upon changes of RDI status. Interrupts due to RDI status change are masked when RDIE is set low. The RDI status is derived from bit 8 of the V5 byte when RDIZ7EN is set low and from bits 5 to 7 of the Z7 byte when RDIZ7EN is set high.

RFIE:

The RFIE bit enables the remote failure indication interrupt for tributary TU #1 in the corresponding TUG2. When RDIZ7EN is set low, an interrupt is generated upon assertion and negation events of the RFIV bit when RFIE is set high. Interrupts due to RFIV status change are masked when RFIE is set low. When RDIZ7EN is set high, RFIE is ignored.

COPSLE:

The COPSLE bit enables the change of tributary path signal label interrupt for tributary TU #2 in the corresponding TUG2. When COPSLE is set high, an interrupt is generated when the accepted path signal label changes. Interrupts due to change of PSL are masked when COPSLE is set low.

PSLME:

The PSLME bit enables the tributary path signal label mismatch interrupt for tributary TU #2 in the corresponding TUG2. When PSLME is set high, an interrupt is generated when the accepted path signal label changes from mismatching the provisioned PSL to matching the provisioned value, or vice versa. Interrupts due to PSL mismatch status change are masked when PSLME is set low.

PSLUE:

The PSLUE bit enables the tributary path signal label unstable interrupt for tributary TU #2 in the corresponding TUG2. When PSLUE is set high, an interrupt is generated when the received path signal label becomes unstable or returns to stable. Interrupts due to PSL unstable status change are masked when PSLUE is set low.

BLKBIP:

The BLKBIP bit controls the accumulation of tributary BIP-2 errors for the tributary TU #2 in the corresponding TUG2. When BLKBIP is set high, BIP-2 errors are counted on a block basis; the BIP error count is incremented by one when one or both of the BIP-2 bits are in error. When BLKBIP is set low, the BIP error count is incremented once for each BIP-2 bit that is in error.

TU11:

The TU11 bit reports the tributary configuration of the corresponding TUG2. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMAP.

Register 1341H, 1349H, 1351H, 1359H, 1361H, 1369H, 1371H: RTOP, TU #2 in TUG2 #1 to TUG2 #7, Configuration and Alarm Status

Bit	Type	Function	Default
Bit 7	R/W	RDIZ7EN	0
Bit 6	R/W	TUPTE	0
Bit 5	R/W	Reserved	0
Bit 4	R	PSLUV	X
Bit 3	R	PSLMV	X
Bit 2	R	ERDIV[2]	X
Bit 1	R	ERDIV[1]/RFIV	X
Bit 0	R	ERDIV[0]/RDIV	X

This set of registers reports alarm status and configures TU #2 in TUG2 #1 to TUG2 #7.

RDIV:

The RDIV bit indicates the remote defect indication status of tributary TU #2 in the corresponding TUG2 when RDIZ7EN is low. RDIV is set high when the RDI bit in the V5 byte is set high for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP Configuration register (address 1205H). RDIV is set low when the RDI bit is set low for five or ten consecutive multiframes as determined by the RDI10 bit

RFIV:

The RFIV bit indicates the remote failure indication status of tributary TU #2 in the corresponding TUG2 when RDIZ7EN is set low. RFIV is set high when the RFI bit in the V5 byte is set high for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP Configuration register (address 1205H). RFIV is set low when the RFI bit is set low for five or ten consecutive multiframes as determined by the RDI10 bit.

ERDIV[2:0]:

The ERDIV[2:0] bits indicates the extended remote defect indication status of tributary TU #2 in the corresponding TUG2 when RDIZ7EN is set high. The ERDIV[2:0] bits are set to a new code when the same code in the extended RDI bits of the Z7 byte is seen for five or ten consecutive multiframes as

determined by the RDI10 bit in the RTOP Configuration registers (address 1205H).

PSLMV:

The PSLMV bit indicates the path signal mismatch status of tributary TU #1 in the corresponding TUG2. PSLMV is set high when the accepted PSL differs from the provisioned value. PSLMV is set low when the accepted PSL has the same value as the provisioned one.

PSLUV:

The PSLUV bit indicates the path signal unstable status of tributary TU #2 in the corresponding TUG2. The PSL unstable counter is incremented if the PSL of the current multiframe differs form that in the previous multiframe. The counter is cleared to zero when the same PSL is received for five consecutive multiframes. The tributary PSL unstable alarm is asserted and PSLUV set high when the unstable counter reaches five. The PSL unstable alarm is negated and PSLUV set low when the unstable counter is cleared.

Reserved:

The Reserved bit must be programmed to logic 0 for normal operation.

TUPTE:

The TUPTE bit determines the alarm conditions under which AIS is inserted for tributary TU #2 in the corresponding TUG2. TUPTE is set high if tributary TU #2 is to be terminated in the network element containing this TEMAP device. In this case, tributary AIS is automatically inserted based on the contents of the global Tributary Alarm AIS Control register (address 1206H). TUPTE is set low if tributary TU #2 is part of the through traffic in the network element containing this TEMAP device. In this case, tributary AIS is only inserted when a loss of pointer (LOP) or a loss of multiframe (LOM) alarm is detected (as determined by the global Tributary Alarm AIS Control register).

RDIZ7EN:

The RDIZ7EN indicates which tributary path overhead byte is used for controlling the ERDI[2:0] or RDI/RFI bits of tributary TU #2 in the corresponding TUG2 . When RDIZ7EN is set low, the RDI and RFI bits in the V5 byte are used to control the RDIV and RFIV register bits. When RDIZ7EN is set high, the three bit extended RDI code in the Z7 byte is used to control the ERDIV[2:0] register bits.

Register 1342H, 134AH, 1352H, 135AH, 1362H, 136AH, 1372H: RTOP, TU #2 in TUG2 #1 to TUG2 #7, Expected Path Signal Label

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	EPSL[2]	0
Bit 1	R/W	EPSL[1]	0
Bit 0	R/W	EPSL[0]	0

This set of registers configures the expected path signal label of TU #2 in TUG2 #1 to TUG2 #7.

EPSL[2:0]:

The EPSL[2:0] bits specifies the expected path signal label of tributary TU #2 in the corresponding TUG2. The expected PSL is compared with the accepted PSL to determine the PSLM state.

Register 1343H, 134BH, 1353H, 135BH, 1363H, 136BH, 1373H: RTOP, TU #2 in TUG2 #1 to TUG2 #7, Accepted Path Signal Label

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	APSL[2]	0
Bit 1	R	APSL[1]	0
Bit 0	R	APSL[0]	0

This set of registers reports the accepted path signal label of TU #2 in TUG2 #1 to TUG2 #7.

APSL[2:0]:

The APSL[2:0] bits reports the accepted path signal label of tributary TU #2 in TUG2 #1 to TUG2 #7. An incoming PSL is accepted when the same value is received for five consecutive multiframes.

Register 1344H, 134CH, 1354H, 135CH, 1364H, 136CH, 1374H: RTOP, TU #2 in TUG2 #1 to TUG2 #7, BIP-2 Error Count LSB

Bit	Type	Function	Default
Bit 7	R	BIP[7]	X
Bit 6	R	BIP[6]	X
Bit 5	R	BIP[5]	X
Bit 4	R	BIP[4]	X
Bit 3	R	BIP[3]	X
Bit 2	R	BIP[2]	X
Bit 1	R	BIP[1]	X
Bit 0	R	BIP[0]	X

Register 1345H, 134DH, 1355H, 135DH, 1365H, 136DH, 1375H: RTOP, TU #2 in TUG2 #1 to TUG2 #7, BIP-2 Error Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	BIP[10]	X
Bit 1	R	BIP[9]	X
Bit 0	R	BIP[8]	X

These registers reports the number of block interleave parity (BIP-2) errors detected in TU #2 in TUG2 #1 to TUG2 #7 in the previous accumulation interval.

BIP[10:0]:

The BIP[10:0] bits reports the number of tributary path bit-interleaved parity errors that have been detected since the last time the BIP-2 registers were polled. The BIP-2 registers are polled by writing to the Master SONET/SDH Accumulate Trigger register. The write access transfers the internally

accumulated error count to the BIP-2 registers within 10 µs and resets the internal counter simultaneously to begin a new cycle of error accumulation.

Register 1346H, 134EH, 1356H, 135EH, 1366H, 136EH, 1376H: RTOP, TU #2 in TUG2 #1 to TUG2 #7, FEBE Error Count LSB

Bit	Type	Function	Default
Bit 7	R	FEBE[7]	X
Bit 6	R	FEBE[6]	X
Bit 5	R	FEBE[5]	X
Bit 4	R	FEBE[4]	X
Bit 3	R	FEBE[3]	X
Bit 2	R	FEBE[2]	X
Bit 1	R	FEBE[1]	X
Bit 0	R	FEBE[0]	X

Register 1347H, 134FH, 1357H, 135FH, 1367H, 136FH, 1377H: RTOP, TU #2 in TUG2 #1 to TUG2 #7, FEBE Error Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	FEBE[10]	X
Bit 1	R	FEBE[9]	X
Bit 0	R	FEBE[8]	X

These registers reports the number of far end block errors (FEBE) detected in TU #2 in TUG2 #1 to TUG2 #7 in the previous accumulation interval.

FEBE[10:0]:

The FEBE[10:0] bits reports the number of tributary path far end block errors that have been detected since the last time the FEBE registers were polled. The FEBE registers are polled by writing to the Master SONET/SDH Accumulate Trigger registers. The write access transfers the internally

accumulated error count to the FEBE registers within 10 µs and resets the internal counter simultaneously to begin a new cycle of error accumulation.

Register 1378H: RTOP, TU #2 in TUG2 #1 to TUG2 #7, COPSL Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	COPSL7I	0
Bit 5	R	COPSL6I	0
Bit 4	R	COPSL5I	0
Bit 3	R	COPSL4I	0
Bit 2	R	COPSL3I	0
Bit 1	R	COPSL2I	0
Bit 0	R	COPSL1I	0

This register is used to identify and acknowledge change of path signal label interrupts for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

COPSL1I-COPSL7I:

The COPSL1I to COPSL7I bits identify the source of change of path signal label interrupts. The COPSL1I to COPSL7I bits report and acknowledge COPSL interrupt of TU #2 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the accepted PSL changes. An COPSL*x*I bit is set high when a change of PSL event on the associated tributary (TU #2 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. COPSL*x*I remains valid when interrupts are not enabled (COPSLE set low) and may be polled to detect change of path signal label events.

Register 1379H: RTOP, TU #2 in TUG2 #1 to TUG2 #7, PSLM Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	PSLM7I	0
Bit 5	R	PSLM6I	0
Bit 4	R	PSLM5I	0
Bit 3	R	PSLM4I	0
Bit 2	R	PSLM3I	0
Bit 1	R	PSLM2I	0
Bit 0	R	PSLM1I	0

This register is used to identify and acknowledge path signal label mismatch interrupts for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

PSLM1I-PSLM7I:

The PSLM1I to PSLM7I bits identify the source of path signal label mismatch interrupts. The PSLM1I to PSLM7I bits report and acknowledge PSLM interrupt of TU #2 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the accepted PSL becomes matched to the expected PSL or becomes mismatched to the expected PSL. An PSLM*x*I bit is set high when a change of PSL matched state on the associated tributary (TU #2 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PSLM*x*I remains valid when interrupts are not enabled (PSLME set low) and may be polled to detect path signal label match/mismatch events.

Register 137AH: RTOP, TU #2 in TUG2 #1 to TUG2 #7, PSLU Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	PSLU7I	0
Bit 5	R	PSLU6I	0
Bit 4	R	PSLU5I	0
Bit 3	R	PSLU4I	0
Bit 2	R	PSLU3I	0
Bit 1	R	PSLU2I	0
Bit 0	R	PSLU1I	0

This register is used to identify and acknowledge path signal label unstable interrupts for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

PSLU1I-PSLU7I:

The PSLU1I to PSLU7I bits identify the source of path signal label mismatch interrupts. The PSLU1I to PSLU7I bits report and acknowledge PSLU interrupt of TU #2 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the received PSL becomes unstable or returns to stable. An PSLU*x*I bit is set high when a change of PSL unstable state on the associated tributary (TU #2 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PSLU*x*I remains valid when interrupts are not enabled (PSLUE set low) and may be polled to detect path signal label stable/unstable events.

Register 137BH: RTOP, TU #2 in TUG2 #1 to TUG2 #7, RDI Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	RDI7I	0
Bit 5	R	RDI6I	0
Bit 4	R	RDI5I	0
Bit 3	R	RDI4I	0
Bit 2	R	RDI3I	0
Bit 1	R	RDI2I	0
Bit 0	R	RDI1I	0

This register is used to identify and acknowledge remote defect indication interrupts for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

RDI1I-RDI7I:

The RDI1I to RDI7I bits identify the source of remote defect indication interrupts. The RDI1I to RDI7I bits report and acknowledge RDI interrupt of TU #2 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the received RDI state changes. An RDI*x*I bit is set high when a change of RDI state on the associated tributary (TU #2 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. RDI*x*I remains valid when interrupts are not enabled (RDIE set low) and may be polled to detect change of remote defect indication events.

Register 137CH: RTOP, TU #2 in TUG2 #1 to TUG2 #7, RFI Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	RFI7I	0
Bit 5	R	RFI6I	0
Bit 4	R	RFI5I	0
Bit 3	R	RFI4I	0
Bit 2	R	RFI3I	0
Bit 1	R	RFI2I	0
Bit 0	R	RFI1I	0

This register is used to identify and acknowledge remote failure indication interrupts for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

RFI1I-RFI7I:

The RFI1I to RFI7I bits identify the source of remote failure indication interrupts. The RFI1I to RFI7I bits report and acknowledge RFI interrupt of TU #2 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the received RFI state changes. An RFI*x*I bit is set high when a change of RFI state on the associated tributary (TU #2 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. RFI*x*I remains valid when interrupts are not enabled (RFIE set low) and may be polled to detect change of remote failure indication events.

Register 137DH: RTOP, TU #2 in TUG2 #1 to TUG2 #7, Inband Error Reporting Configuration

Bit	Type	Function	Default
Bit 7		Unused	x
Bit 6	R/W	IBER7	0
Bit 5	R/W	IBER6	0
Bit 4	R/W	IBER5	0
Bit 3	R/W	IBER4	0
Bit 2	R/W	IBER3	0
Bit 1	R/W	IBER2	0
Bit 0	R/W	IBER1	0

This register enables the inband error reporting mode for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

IBER1-IBER7:

The IBER1 to IBER7 bits control in band error reporting for tributary TU #2 in TUG2 #1 to TUG2 #7, respectively. Setting an IBER*x* bit high causes in band error reporting information to be inserted in the V5 byte of tributary TU #2 of the corresponding TUG2. When an IBER*x* bit is low, in band error reporting is disabled and the V5 byte of tributary TU #2 of the corresponding TUG2 is not modified.

Register 1380H, 1388H, 1390H, 1398H, 13A0H, 13A8H, 13B0H: RTOP, TU #3 in TUG2 #1 to TUG2 #7, Configuration

Bit	Type	Function	Default
Bit 7	R	Reserved	1
Bit 6	R	TU11	1
Bit 5	R/W	BLKBIP	0
Bit 4	R/W	PSLUE	0
Bit 3	R/W	PSLME	0
Bit 2	R/W	COPSLE	0
Bit 1	R/W	RFIE	0
Bit 0	R/W	RDIE	0

This set of registers configures the operational modes of TU #3 in TUG2 #1 to TUG2 #7.

RDIE:

The RDIE bit enables the remote defect indication interrupt for tributary TU #1 in the corresponding TUG2. When RDIE is set high, an interrupt is generated upon changes of RDI status. Interrupts due to RDI status change are masked when RDIE is set low. The RDI status is derived from bit 8 of the V5 byte when RDIZ7EN is set low and from bits 5 to 7 of the Z7 byte when RDIZ7EN is set high.

RFIE:

The RFIE bit enables the remote failure indication interrupt for tributary TU #1 in the corresponding TUG2. When RDIZ7EN is set low, an interrupt is generated upon assertion and negation events of the RFIV bit when RFIE is set high. Interrupts due to RFIV status change are masked when RFIE is set low. When RDIZ7EN is set high, RFIE is ignored.

COPSLE:

The COPSLE bit enables the change of tributary path signal label interrupt for tributary TU #3 in the corresponding TUG2. When COPSLE is set high, an interrupt is generated when the accepted path signal label changes. Interrupts due to change of PSL are masked when COPSLE is set low.

PSLME:

The PSLME bit enables the tributary path signal label mismatch interrupt for tributary TU #3 in the corresponding TUG2. When PSLME is set high, an interrupt is generated when the accepted path signal label changes from mismatching the provisioned PSL to matching the provisioned value, or vice versa. Interrupts due to PSL mismatch status change are masked when PSLME is set low.

PSLUE:

The PSLUE bit enables the tributary path signal label unstable interrupt for tributary TU #3 in the corresponding TUG2. When PSLUE is set high, an interrupt is generated when the received path signal label becomes unstable or returns to stable. Interrupts due to PSL unstable status change are masked when PSLUE is set low.

BLKBIP:

The BLKBIP bit controls the accumulation of tributary BIP-2 errors for the tributary TU #3 in the corresponding TUG2. When BLKBIP is set high, BIP-2 errors are counted on a block basis; the BIP error count is incremented by one when one or both of the BIP-2 bits are in error. When BLKBIP is set low, the BIP error count is incremented once for each BIP-2 bit that is in error.

TU11:

The TU11 bit reports the tributary configuration of the corresponding TUG2. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMAP.

Register 1381H, 1389H, 1391H, 1399H, 13A1H, 13A9H, 13B1H: RTOP, TU #3 in TUG2 #1 to TUG2 #7, Configuration and Alarm Status

Bit	Type	Function	Default
Bit 7	R/W	RDIZ7EN	0
Bit 6	R/W	TUPTE	0
Bit 5	R/W	Reserved	0
Bit 4	R	PSLUV	X
Bit 3	R	PSLMV	X
Bit 2	R	ERDIV[2]	X
Bit 1	R	ERDIV[1]/RFIV	X
Bit 0	R	ERDIV[0]/RDIV	X

This set of registers reports alarm status and configures TU #3 in TUG2 #1 to TUG2 #7.

RDIV:

The RDIV bit indicates the remote defect indication status of tributary TU #3 in the corresponding TUG2 when RDIZ7EN is low. RDIV is set high when the RDI bit in the V5 byte is set high for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP Configuration register (address 1205H). RDIV is set low when the RDI bit is set low for five or ten consecutive multiframes as determined by the RDI10 bit

RFIV:

The RFIV bit indicates the remote failure indication status of tributary TU #3 in the corresponding TUG2 when RDIZ7EN is set low. RFIV is set high when the RFI bit in the V5 byte is set high for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP Configuration register (address 1205H). RFIV is set low when the RFI bit is set low for five or ten consecutive multiframes as determined by the RDI10 bit.

ERDIV[2:0]:

The ERDIV[2:0] bits indicates the extended remote defect indication status of tributary TU #3 in the corresponding TUG2 when RDIZ7EN is set high. The ERDIV[2:0] bits are set to a new code when the same code in the extended RDI bits of the Z7 byte is seen for five or ten consecutive multiframes as

determined by the RDI10 bit in the RTOP Configuration register (address 1205H).

PSLMV:

The PSLMV bit indicates the path signal mismatch status of tributary TU #1 in the corresponding TUG2. PSLMV is set high when the accepted PSL differs from the provisioned value. PSLMV is set low when the accepted PSL has the same value as the provisioned one.

PSLUV:

The PSLUV bit indicates the path signal unstable status of tributary TU #3 in the corresponding TUG2. The PSL unstable counter is incremented if the PSL of the current multiframe differs form that in the previous multiframe. The counter is cleared to zero when the same PSL is received for five consecutive multiframes. The tributary PSL unstable alarm is asserted and PSLUV set high when the unstable counter reaches five. The PSL unstable alarm is negated and PSLUV set low when the unstable counter is cleared.

Reserved:

The Reserved bit must be programmed to logic 0 for normal operation.

TUPTE:

The TUPTE bit determines the alarm conditions under which AIS is inserted for tributary TU #3 in the corresponding TUG2. TUPTE is set high if tributary TU #3 is to be terminated in the network element containing this TEMAP device. In this case, tributary AIS is automatically inserted based on the contents of the global Tributary Alarm AIS Control register (address 1206H). TUPTE is set low if tributary TU #3 is part of the through traffic in the network element containing this TEMAP device. In this case, tributary AIS is only inserted when a loss of pointer (LOP) or a loss of multiframe (LOM) alarm is detected (as determined by the global Tributary Alarm AIS Control register).

RDIZ7EN:

The RDIZ7EN indicates which tributary path overhead byte is used for controlling the ERDI[2:0] or RDI/RFI bits of tributary TU #3 in the corresponding TUG2 . When RDIZ7EN is set low, the RDI and RFI bits in the V5 byte are used to control the RDIV and RFIV register bits. When RDIZ7EN is set high, the three bit extended RDI code in the Z7 byte is used to control the ERDIV[2:0] register bits.

Register 1382H, 138AH, 1392H, 139AH, 13A2H, 13AAH, 13B2H: RTOP, TU #3 in TUG2 #1 to TUG2 #7, Expected Path Signal Label

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	EPSL[2]	0
Bit 1	R/W	EPSL[1]	0
Bit 0	R/W	EPSL[0]	0

This set of registers configures the expected the path signal label of TU #3 in TUG2 #1 to TUG2 #7.

EPSL[2:0]:

The EPSL[2:0] bits specifies the expected path signal label of tributary TU #3 in the corresponding TUG2. The expected PSL is compared with the accepted PSL to determine the PSLM state.

Register 1383H, 138BH, 1393H, 139BH, 13A3H, 13ABH, 13B3H: RTOP, TU #3 in TUG2 #1 to TUG2 #7, Accepted Path Signal Label

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	APSL[2]	0
Bit 1	R	APSL[1]	0
Bit 0	R	APSL[0]	0

This set of registers reports the accepted the path signal label of TU #3 in TUG2 #1 to TUG2 #7.

APSL[2:0]:

The APSL[2:0] bits reports the accepted path signal label of tributary TU #3 in the corresponding TUG2. An incoming PSL is accepted when the same value is received for five consecutive multiframes.

Register 1384H, 138CH, 1394H, 139CH, 13A4H, 13ACH, 13B4H: RTOP, TU #3 in TUG2 #1 to TUG2 #7, BIP-2 Error Count LSB

Bit	Type	Function	Default
Bit 7	R	BIP[7]	X
Bit 6	R	BIP[6]	X
Bit 5	R	BIP[5]	X
Bit 4	R	BIP[4]	X
Bit 3	R	BIP[3]	X
Bit 2	R	BIP[2]	X
Bit 1	R	BIP[1]	X
Bit 0	R	BIP[0]	X

Register 1385H, 138DH, 1395H, 139DH, 13A5H, 13ADH, 13B5H: RTOP, TU #3 in TUG2 #1 to TUG2 #7, BIP-2 Error Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	BIP[10]	X
Bit 1	R	BIP[9]	X
Bit 0	R	BIP[8]	X

These registers reports the number of block interleave parity (BIP-2) errors detected in TU #3 in TUG2 #1 to TUG2 #7 in the previous accumulation interval.

BIP[10:0]:

The BIP[10:0] bits reports the number of tributary path bit-interleaved parity errors that have been detected since the last time the BIP-2 registers were polled. The BIP-2 registers are polled by writing to the Master SONET/SDH Accumulate Trigger register. The write access transfers the internally

accumulated error count to the BIP-2 registers within 10 µs and resets the internal counter simultaneously to begin a new cycle of error accumulation.

Register 1386H, 138EH, 1396H, 139EH, 13A6H, 13AEH, 13B6H: TU #3 in TUG2 #1 to TUG2 #7, FEBE Error Count LSB

Bit	Type	Function	Default
Bit 7	R	FEBE[7]	X
Bit 6	R	FEBE[6]	X
Bit 5	R	FEBE[5]	X
Bit 4	R	FEBE[4]	X
Bit 3	R	FEBE[3]	X
Bit 2	R	FEBE[2]	X
Bit 1	R	FEBE[1]	X
Bit 0	R	FEBE[0]	X

Register 1387H, 138FH, 1397H, 139FH, 13A7H, 13AFH, 13B7H: RTOP, TU #3 in TUG2 #1 to TUG2 #7, FEBE Error Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	FEBE[10]	X
Bit 1	R	FEBE[9]	X
Bit 0	R	FEBE[8]	X

These registers reports the number of far end block errors (FEBE) detected in TU #3 in TUG2 #1 to TUG2 #7 in the previous accumulation interval.

FEBE[10:0]:

The FEBE[10:0] bits reports the number of tributary path far end block errors that have been detected since the last time the FEBE registers were polled. The FEBE registers are polled by writing to the Master SONET/SDH Accumulate Trigger register. The write access transfers the internally

accumulated error count to the FEBE registers within 10 µs and resets the internal counter simultaneously to begin a new cycle of error accumulation.

Register 13B8H: RTOP, TU #3 in TUG2 #1 to TUG2 #7, COPSL Interrupt

Bit	Type	Function	Default
Bit 7		Reserved	X
Bit 6	R	COPSL7I	0
Bit 5	R	COPSL6I	0
Bit 4	R	COPSL5I	0
Bit 3	R	COPSL4I	0
Bit 2	R	COPSL3I	0
Bit 1	R	COPSL2I	0
Bit 0	R	COPSL1I	0

This register is used to identify and acknowledge change of path signal label interrupts for the tributaries TU #3 in TUG2 #1 TO TUG2 #7.

COPSL1I-COPSL7I:

The COPSL1I to COPSL7I bits identify the source of change of path signal label interrupts. The COPSL1I to COPSL7I bits report and acknowledge COPSL interrupt of TU #3 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the accepted PSL changes. An COPSL*x*I bit is set high when a change of PSL event on the associated tributary (TU #3 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. COPSL*x*I remains valid when interrupts are not enabled (COPSLE set low) and may be polled to detect change of path signal label events.

Reserved:

The Reserved bits must be written with a logic 0 for proper operation of the TUPP-PLUS.

Register 13B9H: RTOP, TU #3 in TUG2 #1 to TUG2 #7, PSLM Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	PSLM7I	0
Bit 5	R	PSLM6I	0
Bit 4	R	PSLM5I	0
Bit 3	R	PSLM4I	0
Bit 2	R	PSLM3I	0
Bit 1	R	PSLM2I	0
Bit 0	R	PSLM1I	0

This register is used to identify and acknowledge path signal label mismatch interrupts for the tributaries TU #3 in TUG2 #1 TO TUG2 #7.

PSLM1I-PSLM7I:

The PSLM1I to PSLM7I bits identify the source of path signal label mismatch interrupts. The PSLM1I to PSLM7I bits report and acknowledge PSLM interrupt of TU #3 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the accepted PSL becomes matched to the expected PSL or becomes mismatched to the expected PSL. An PSLM*x*I bit is set high when a change of PSL matched state on the associated tributary (TU #3 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PSLM*x*I remains valid when interrupts are not enabled (PSLME set low) and may be polled to detect path signal label match/mismatch events.

Register 13BAH: RTOP, TU #3 in TUG2 #1 to TUG2 #7, PSLU Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	PSLU7I	0
Bit 5	R	PSLU6I	0
Bit 4	R	PSLU5I	0
Bit 3	R	PSLU4I	0
Bit 2	R	PSLU3I	0
Bit 1	R	PSLU2I	0
Bit 0	R	PSLU1I	0

This register is used to identify and acknowledge path signal label unstable interrupts for the tributaries TU #3 in TUG2 #1 TO TUG2 #7.

PSLU1I-PSLU7I:

The PSLU1I to PSLU7I bits identify the source of path signal label mismatch interrupts. The PSLU1I to PSLU7I bits report and acknowledge PSLU interrupt of TU #3 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the received PSL becomes unstable or returns to stable. An PSLU*x*I bit is set high when a change of PSL unstable state on the associated tributary (TU #3 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PSLU*x*I remains valid when interrupts are not enabled (PSLUE set low) and may be polled to detect path signal label stable/unstable events.

Register 13BBH: RTOP, TU #3 in TUG2 #1 to TUG2 #7, RDI Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	RDI7I	0
Bit 5	R	RDI6I	0
Bit 4	R	RDI5I	0
Bit 3	R	RDI4I	0
Bit 2	R	RDI3I	0
Bit 1	R	RDI2I	0
Bit 0	R	RDI1I	0

This register is used to identify and acknowledge remote defect indication interrupts for the tributaries TU #3 in TUG2 #1 TO TUG2 #7.

RDI1I-RDI7I:

The RDI1I to RDI7I bits identify the source of remote defect indication interrupts. The RDI1I to RDI7I bits report and acknowledge RDI interrupt of TU #3 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the received RDI state changes. An RDI*x*I bit is set high when a change of RDI state on the associated tributary (TU #3 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. RDI*x*I remains valid when interrupts are not enabled (RDIE set low) and may be polled to detect change of remote defect indication events.

Register 13BCH: RTOP, TU #3 in TUG2 #1 to TUG2 #7, RFI Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	RFI7I	0
Bit 5	R	RFI6I	0
Bit 4	R	RFI5I	0
Bit 3	R	RFI4I	0
Bit 2	R	RFI3I	0
Bit 1	R	RFI2I	0
Bit 0	R	RFI1I	0

This register is used to identify and acknowledge remote failure indication interrupts for the tributaries TU #3 in TUG2 #1 TO TUG2 #7.

RFI1I-RFI7I:

The RFI1I to RFI7I bits identify the source of remote failure indication interrupts. The RFI1I to RFI7I bits report and acknowledge RFI interrupt of TU #3 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the received RFI state changes. An RFI*x*I bit is set high when a change of RFI state on the associated tributary (TU #3 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. RFI*x*I remains valid when interrupts are not enabled (RFIE set low) and may be polled to detect change of remote failure indication events.

Register 13BDH: RTOP, TU #3 in TUG2 #1 to TUG2 #7, Inband Error Reporting Configuration

Bit	Type	Function	Default
Bit 7		Unused	x
Bit 6	R/W	IBER7	0
Bit 5	R/W	IBER6	0
Bit 4	R/W	IBER5	0
Bit 3	R/W	IBER4	0
Bit 2	R/W	IBER3	0
Bit 1	R/W	IBER2	0
Bit 0	R/W	IBER1	0

This register enables the inband error reporting mode for the tributaries TU #3 in TUG2 #1 to TUG2 #7.

IBER1-IBER7:

The IBER1 to IBER7 bits control in band error reporting for tributary TU #3 in TUG2 #1 to TUG2 #7, respectively. Setting an IBER*x* bit high causes in band error reporting information to be inserted in the V5 byte of tributary TU #3 of the corresponding TUG2. When an IBER*x* bit is low, in band error reporting is disabled and the V5 byte of tributary TU #3 of the corresponding TUG2 is not modified.

Register 13C0H, 13C8H, 13D0H, 13D8H, 13E0H, 13E8H, 13F0H: RTOP, TU #4 in TUG2 #1 to TUG2 #7, Configuration

Bit	Type	Function	Default
Bit 7	R	Reserved	1
Bit 6	R	TU11	1
Bit 5	R/W	BLKBIP	0
Bit 4	R/W	PSLUE	0
Bit 3	R/W	PSLME	0
Bit 2	R/W	COPSLE	0
Bit 1	R/W	RFIE	0
Bit 0	R/W	RDIE	0

This set of registers configures the operational modes of TU #4 in TUG2 #1 to TUG2 #7. When the corresponding TUG2 tributary group is configured to TU12 (VT2) mode, the associated register in this set has no effect.

RDIE:

The RDIE bit enables the remote defect indication interrupt for tributary TU #4 in the corresponding TUG2. When RDIZ7EN is set low, an interrupt is generated upon assertion and negation events of the RDIV bit when RDIE is set high. Interrupts due to RDIV status change are masked when RDIE is set low.

When RDIZ7EN is set high, an interrupt is generated upon assertion or negation events of the ERDIV[2:0] bits when RDIE is set high. Interrupts due to ERDIV[2:0] status change are masked when RDIE is set low.

COPSLE:

The COPSLE bit enables the change of tributary path signal label interrupt for tributary TU #4 in the corresponding TUG2. When COPSLE is set high, an interrupt is generated when the accepted path signal label changes. Interrupts due to change of PSL are masked when COPSLE is set low.

PSLME:

The PSLME bit enables the tributary path signal label mismatch interrupt for tributary TU #4 in the corresponding TUG2. When PSLME is set high, an interrupt is generated when the accepted path signal label changes from

mismatching the provisioned PSL to matching the provisioned value, or vice versa. Interrupts due to PSL mismatch status change are masked when PSLME is set low.

PSLUE:

The PSLUE bit enables the tributary path signal label unstable interrupt for tributary TU #4 in the corresponding TUG2. When PSLUE is set high, an interrupt is generated when the received path signal label becomes unstable or returns to stable. Interrupts due to PSL unstable status change are masked when PSLUE is set low.

BLKBIP:

The BLKBIP bit controls the accumulation of tributary BIP-2 errors for the tributary TU #4 in the corresponding TUG2. When BLKBIP is set high, BIP-2 errors are counted on a block basis; the BIP error count is incremented by one when one or both of the BIP-2 bits are in error. When BLKBIP is set low, the BIP error count is incremented once for each BIP-2 bit that is in error.

TU11:

The TU11 bit reports the tributary configuration of the corresponding TUG2. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMAP.

Register 13C1H, 13C9H, 13D1H, 13D9H, 13E1H, 13E9H, 13F1H: RTOP, TU #4 in TUG2 #1 to TUG2 #7, Configuration and Alarm Status

Bit	Type	Function	Default
Bit 7	R/W	RDIZ7EN	0
Bit 6	R/W	TUPTE	0
Bit 5	R/W	Reserved	0
Bit 4	R	PSLUV	X
Bit 3	R	PSLMV	X
Bit 2	R	ERDIV[2]	X
Bit 1	R	ERDIV[1]/RFIV	X
Bit 0	R	ERDIV[0]/RDIV	X

This set of registers configures and reports the alarm status of TU #4 in TUG2 #1 to TUG2 #7. When the corresponding TUG2 tributary group is configured to TU12 (VT2) mode, the associated register in this set has no effect.

RDIV:

The RDIV bit indicates the remote defect indication status of tributary TU #4 in the corresponding TUG2 when RDIZ7EN is low. RDIV is set high when the RDI bit in the V5 byte is set high for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP Configuration register (address 1205H). RDIV is set low when the RDI bit is set low for five or ten consecutive multiframes as determined by the RDI10 bit

RFIV:

The RFIV bit indicates the remote failure indication status of tributary TU #4 in the corresponding TUG2 when RDIZ7EN is set low. RFIV is set high when the RFI bit in the V5 byte is set high for five or ten consecutive multiframes as determined by the RDI10 bit in the RTOP Configuration register (address 1205H). RFIV is set low when the RFI bit is set low for five or ten consecutive multiframes as determined by the RDI10 bit.

ERDIV[2:0]:

The ERDIV[2:0] bits indicates the extended remote defect indication status of tributary TU #4 in the corresponding TUG2 when RDIZ7EN is set high. The ERDIV[2:0] bits are set to a new code when the same code in the extended RDI bits of the Z7 byte is seen for five or ten consecutive multiframes as

determined by the RDI10 bit in the RTOP Configuration register (address 1205H).

PSLMV:

The PSLMV bit indicates the path signal mismatch status of tributary TU #1 in the corresponding TUG2. PSLMV is set high when the accepted PSL differs from the provisioned value. PSLMV is set low when the accepted PSL has the same value as the provisioned one.

PSLUV:

The PSLUV bit indicates the path signal unstable status of tributary TU #4 in the corresponding TUG2. The PSL unstable counter is incremented if the PSL of the current multiframe differs form that in the previous multiframe. The counter is cleared to zero when the same PSL is received for five consecutive multiframes. The tributary PSL unstable alarm is asserted and PSLUV set high when the unstable counter reaches five. The PSL unstable alarm is negated and PSLUV set low when the unstable counter is cleared.

Reserved:

The Reserved bit must be programmed to logic 0 for normal operation.

TUPTE:

The TUPTE bit determines the alarm conditions under which AIS is inserted for tributary TU #4 in the corresponding TUG2. TUPTE is set high if tributary TU #4 is to be terminated in the network element containing this TEMAP device. In this case, tributary AIS is automatically inserted based on the contents of the global Tributary Alarm AIS Control register (address 1206H). TUPTE is set low if tributary TU #4 is part of the through traffic in the network element containing this TEMAP device. In this case, tributary AIS is only inserted when a loss of pointer (LOP) or a loss of multiframe (LOM) alarm is detected (as determined by the global Tributary Alarm AIS Control register).

RDIZ7EN:

The RDIZ7EN indicates which tributary path overhead byte is used for controlling the ERDI[2:0] or RDI/RFI bits of tributary TU #4 in the corresponding TUG2 . When RDIZ7EN is set low, the RDI and RFI bits in the V5 byte are used to control the RDIV and RFIV register bits. When RDIZ7EN is set high, the three bit extended RDI code in the Z7 byte is used to control the ERDIV[2:0] register bits.

Register 13C2H, 13CAH, 13D2H, 13DAH, 13E2H, 13EAH, 13F2H: RTOP, TU #4 in TUG2 #1 to TUG2 #7, Expected Path Signal Label

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	EPSL[2]	0
Bit 1	R/W	EPSL[1]	0
Bit 0	R/W	EPSL[0]	0

This set of registers configures the expected path signal label of TU #4 in TUG2 #1 to TUG2 #7. When the corresponding TUG2 tributary group is configured to TU12 (VT2) mode, the associated register in this set has no effect.

EPSL[2:0]:

The EPSL[2:0] bits specifies the expected path signal label of tributary TU #4 in the corresponding TUG2. The expected PSL is compared with the accepted PSL to determine the PSLM state.

Register 13C3H, 13CBH, 13D3H, 13DBH, 13E3H, 13EBH, 13F3H: RTOP, TU #4 in TUG2 #1 to TUG2 #7, Path Signal Label

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	APSL[2]	0
Bit 1	R	APSL[1]	0
Bit 0	R	APSL[0]	0

This set of register reports the accepted path signal label of TU #4 in TUG2 #1 to TUG2 #7. When the corresponding TUG2 tributary group is configured to TU12 (VT2) mode, the associated register in this set has no effect.

APSL[2:0]:

The APSL[2:0] bits reports the accepted path signal label of tributary TU #4 in the corresponding TUG2. An incoming PSL is accepted when the same value is received for five consecutive multiframes.

Register 13C4H, 13CCH, 13D4H, 13DCH, 13E4H, 13ECH, 13F4H: RTOP, TU #4 in TUG2 #1 to TUG2 #7, BIP-2 Error Count LSB

Bit	Type	Function	Default
Bit 7	R	BIP[7]	X
Bit 6	R	BIP[6]	X
Bit 5	R	BIP[5]	X
Bit 4	R	BIP[4]	X
Bit 3	R	BIP[3]	X
Bit 2	R	BIP[2]	X
Bit 1	R	BIP[1]	X
Bit 0	R	BIP[0]	X

Register 13C5H, 13CDH, 13D5H, 13DDH, 13E5H, 13EDH, 13F5H: RTOP, TU #4 in TUG2 #1 to TUG2 #7, BIP-2 Error Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	BIP[10]	X
Bit 1	R	BIP[9]	X
Bit 0	R	BIP[8]	X

These registers reports the number of block interleave parity (BIP-2) errors detected in TU #4 in TUG2 #1 to TUG2 #7 in the previous accumulation interval. When the corresponding TUG2 tributary group is configured to TU12 (VT2) mode, the associated registers in this set contain invalid data. These registers do not saturate.

BIP[10:0]:

The BIP[10:0] bits reports the number of tributary path bit-interleaved parity errors that have been detected since the last time the BIP-2 registers were

polled. The BIP-2 registers are polled by writing to the Input Signal Activity Monitor, Accumulate Trigger register. The write access transfers the internally accumulated error count to the BIP-2 registers within 10 µs and resets the internal counter simultaneously to begin a new cycle of error accumulation.

Register 13C6H, 13CEH, 13D6H, 13DEH, 13E6H, 13EEH, 13F6H: RTOP, TU #4 in TUG2 #1 to TUG2 #7, FEBE Error Count LSB

Bit	Type	Function	Default
Bit 7	R	FEBE[7]	X
Bit 6	R	FEBE[6]	X
Bit 5	R	FEBE[5]	X
Bit 4	R	FEBE[4]	X
Bit 3	R	FEBE[3]	X
Bit 2	R	FEBE[2]	X
Bit 1	R	FEBE[1]	X
Bit 0	R	FEBE[0]	X

Register 13C7H, 13CFH, 13D7H, 13DFH, 13E7H, 13EFH, 13F7H: RTOP, TU #4 in TUG2 #1 to TUG2 #7, FEBE Error Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	FEBE[10]	X
Bit 1	R	FEBE[9]	X
Bit 0	R	FEBE[8]	X

These registers reports the number of far end block errors (FEBE) detected in TU #4 in TUG2 #1 to TUG2 #7 in the previous accumulation interval. When the corresponding TUG2 tributary group is configured to TU12 (VT2) mode, the associated registers in this set contain invalid data.

FEBE[10:0]:

The FEBE[10:0] bits reports the number of tributary path far end block errors that have been detected since the last time the FEBE registers were polled. The FEBE registers are polled by writing to the Input Signal Activity Monitor,

Accumulate Trigger register. The write access transfers the internally accumulated error count to the FEBE registers within 10 µs and resets the internal counter simultaneously to begin a new cycle of error accumulation.

Register 13F8H: RTOP, TU #4 in TUG2 #1 to TUG2 #7, COPSL Interrupt

Bit	Type	Function	Default
Bit 7		Unused	0
Bit 6	R	COPSL7I	0
Bit 5	R	COPSL6I	0
Bit 4	R	COPSL5I	0
Bit 3	R	COPSL4I	0
Bit 2	R	COPSL3I	0
Bit 1	R	COPSL2I	0
Bit 0	R	COPSL1I	0

This register is used to identify and acknowledge change of path signal label interrupts for the tributaries TU #4 in TUG2 #1 TO TUG2 #7.

COPSL1I-COPSL7I:

The COPSL1I to COPSL7I bits identify the source of change of path signal label interrupts. When the corresponding TUG2 tributary group is configured for TU12 (VT2) mode, the associated COPSL*x*I bit is unused and will return a logic 0 when read. When operational, the COPSL1I to COPSL7I bits report and acknowledge COPSL interrupt of TU #4 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the accepted PSL changes. An COPSL*x*I bit is set high when a change of PSL event on the associated tributary (TU #4 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. COPSL*x*I remains valid when interrupts are not enabled (COPSLE set low) and may be polled to detect change of path signal label events.

Register 13F9H: RTOP, TU #4 in TUG2 #1 to TUG2 #7, PSLM Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	PSLM7I	0
Bit 5	R	PSLM6I	0
Bit 4	R	PSLM5I	0
Bit 3	R	PSLM4I	0
Bit 2	R	PSLM3I	0
Bit 1	R	PSLM2I	0
Bit 0	R	PSLM1I	0

This register is used to identify and acknowledge path signal label mismatch interrupts for the tributaries TU #4 in TUG2 #1 TO TUG2 #7.

PSLM1I-PSLM7I:

The PSLM1I to PSLM7I bits identify the source of path signal label mismatch interrupts. When the corresponding TUG2 tributary group is configured for TU12 (VT2) mode, the associated PSLM*x*I bit is unused and will return a logic 0 when read. When operational, the PSLM1I to PSLM7I bits report and acknowledge PSLM interrupt of TU #4 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the accepted PSL becomes matched to the expected PSL or becomes mismatched to the expected PSL. An PSLM*x*I bit is set high when a change of PSL matched state on the associated tributary (TU #4 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PSLM*x*I remains valid when interrupts are not enabled (PSLME set low) and may be polled to detect path signal label match/mismatch events.

Register 13FAH: RTOP, TU #4 in TUG2 #1 to TUG2 #7, PSLU Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	PSLU7I	0
Bit 5	R	PSLU6I	0
Bit 4	R	PSLU5I	0
Bit 3	R	PSLU4I	0
Bit 2	R	PSLU3I	0
Bit 1	R	PSLU2I	0
Bit 0	R	PSLU1I	0

This register is used to identify and acknowledge path signal label unstable interrupts for the tributaries TU #4 in TUG2 #1 TO TUG2 #7.

PSLU1I-PSLU7I:

The PSLU1I to PSLU7I bits identify the source of path signal label mismatch interrupts. When the corresponding TUG2 tributary group is configured for TU12 (VT2) mode, the associated PSLU*x*I bit is unused and will return a logic 0 when read. When operational, the PSLU1I to PSLU7I bits report and acknowledge PSLU interrupt of TU #4 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the received PSL becomes unstable or returns to stable. An PSLU*x*I bit is set high when a change of PSL unstable state on the associated tributary (TU #4 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PSLU*x*I remains valid when interrupts are not enabled (PSLUE set low) and may be polled to detect path signal label stable/unstable events.

Register 13FBH: RTOP, TU #4 in TUG2 #1 to TUG2 #7, RDI Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	RDI7I	0
Bit 5	R	RDI6I	0
Bit 4	R	RDI5I	0
Bit 3	R	RDI4I	0
Bit 2	R	RDI3I	0
Bit 1	R	RDI2I	0
Bit 0	R	RDI1I	0

This register is used to identify and acknowledge remote defect indication interrupts for the tributaries TU #4 in TUG2 #1 TO TUG2 #7.

RDI1I-RDI7I:

The RDI1I to RDI7I bits identify the source of remote defect indication interrupts. When the corresponding TUG2 tributary group is configured for TU12 (VT2) mode, the associated RDI*x*I bit is unused and will return a logic 0 when read. When operational, the RDI1I to RDI7I bits report and acknowledge RDI interrupt of TU #4 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the received RDI state changes. An RDI*x*I bit is set high when a change of RDI state on the associated tributary (TU #4 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. RDI*x*I remains valid when interrupts are not enabled (RDIE set low) and may be polled to detect change of remote defect indication events.

Register 13FCH: RTOP, TU #4 in TUG2 #1 to TUG2 #7, RFI Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	RFI7I	0
Bit 5	R	RFI6I	0
Bit 4	R	RFI5I	0
Bit 3	R	RFI4I	0
Bit 2	R	RFI3I	0
Bit 1	R	RFI2I	0
Bit 0	R	RFI1I	0

This register is used to identify and acknowledge remote failure indication interrupts for the tributaries TU #4 in TUG2 #1 TO TUG2 #7.

RFI1I-RFI7I:

The RFI1I to RFI7I bits identify the source of remote failure indication interrupts. When the corresponding TUG2 tributary group is configured for TU12 (VT2) mode, the associated RFI*x*I bit is unused and will return a logic 0 when read. When operational, the RFI1I to RFI7I bits report and acknowledge RFI interrupt of TU #4 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated when the received RFI state changes. An RFI*x*I bit is set high when a change of RFI state on the associated tributary (TU #4 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. RFI*x*I remains valid when interrupts are not enabled (RFIE set low) and may be polled to detect change of remote failure indication events.

Register 13FDH: RTOP, TU #4 in TUG2 #1 to TUG2 #7, InBand Error Reporting Configuration

Bit	Type	Function	Default
Bit 7		Unused	x
Bit 6	R/W	IBER7	0
Bit 5	R/W	IBER6	0
Bit 4	R/W	IBER5	0
Bit 3	R/W	IBER4	0
Bit 2	R/W	IBER3	0
Bit 1	R/W	IBER2	0
Bit 0	R/W	IBER1	0

This register enables the inband error reporting mode for the tributaries TU #4 in TUG2 #1 to TUG2 #7.

IBER1-IBER7:

The IBER1 to IBER7 bits control in band error reporting for tributary TU #4 in TUG2 #1 to TUG2 #7, respectively. Setting an IBER*x* bit high causes in band error reporting information to be inserted in the V5 byte of tributary TU #4 of the corresponding TUG2. When an IBER*x* bit is low, in band error reporting is disabled and the V5 byte of tributary TU #4 of the corresponding TUG2 is not modified.

1.26 VTPP Egress Tributary Payload Processor Registers

Register 1400H: VTPP Egress, TU #1 in TUG2 #1, Configuration and Status

Bit	Type	Function	Default
Bit 7	R/W	Reserved	1
Bit 6	R/W	TU11	1
Bit 5	R/W	PF	0
Bit 4	R	LOPV	X
Bit 3	R/W	ALARME	0
Bit 2	R/W	DLOP	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	IPAIS	0

This register reports the status and configures the operational modes of TU #1 in TUG2 #1.

IPAIS:

The IPAIS bit enables the insertion of path AIS for tributary TU #1 in TUG2 #1. Tributary path AIS is inserted by forcing all ones into all tributary bytes.

DLOP:

The DLOP bit allows downstream pointer processing elements to be diagnosed. When DLOP is set high, the new data flag (NDF) field of the outgoing payload pointer in tributary TU #1 in TUG2 #1 is inverted to cause downstream pointer processing elements to enter a loss of pointer state. Insertion of an inverted new data flag can occur in concert with the insertion of a normal idle (unequipped) indication. The DLOP bit has no effect when the IPAIS bit is set high.

ALARME:

The ALARME bit enables loss of pointer and path AIS interrupts for tributary TU #1 in TUG2 #1. When ALARME is set high, an interrupt is generated upon entry to and exit from the LOP and AIS state of the pointer interpreter state diagram. Interrupts due to AIS and LOP status change are masked when ALARME is set low.

LOPV:

The LOPV bit indicates the loss of pointer status of tributary TU #1 in TUG2 #1.

PF:

The PF bit enables pointer follower mode for tributary TU #1 in TUG2 #1. In pointer follower mode, the tributary FIFO dead-zone is collapsed so that any variation in FIFO depth will result in an outgoing pointer justification event. Any TU pointer justification event on the corresponding incoming tributary, or an AU pointer justification event affecting this tributary will cause an outgoing pointer justification event.

TU11:

The TU11 bit specifies the tributary configuration of tributary group TUG2 #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

Bit 7 must be kept at a logic 1 for proper operation of the TEMAP while bit 1 must be kept to logic 0.

Register 1401H: VTPP Egress, TU #1 in TUG2 #1, Alarm Status

Bit	Type	Function	Default
Bit 7	R	SS[1]	X
Bit 6	R	SS[0]	X
Bit 5	R	NJEI	X
Bit 4	R	PJEI	X
Bit 3	R	ESEI	X
Bit 2	R/W	PEE	0
Bit 1	R	AISV	X
Bit 0	R/W	RELAYAIS	0

This register reports the alarm status of TU #1 in TUG2 #1.

RELAYAIS:

The RELAYAIS bit controls the number of consecutive AIS_ind indications required to enter the AIS state for tributary TU #1 in TUG2 #1. When RELAYAIS is set high, AIS is declared upon receipt of a single AIS_ind indication. When RELAYAIS is set low, AIS is declared after 3 consecutive AIS_ind indications.

AISV:

The AISV bit indicates the tributary path AIS status of tributary TU #1 in TUG2 #1.

PEE:

The PEE bit enables pointer event interrupts for tributary TU #1 in TUG2 #1. When PEE is set high, an interrupt is generated upon detection of FIFO underflows and overflows, upon detection of incoming pointer justification events when the MONIS bit is set high and upon detection of outgoing pointer justification events when the MONIS bit is set low. Interrupts due to elastic store errors and pointer justification events are masked when PEE is set low.

ESEI:

The ESEI bit reports and acknowledges the status of elastic store error interrupts for tributary TU #1 in TUG2 #1. Interrupts are generated upon FIFO underflows and overflows. ESEI is set high when an elastic store error occurs and is cleared immediately following a read of this register, which also

acknowledges and clears the interrupt. ESEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect elastic store error events.

PJEI:

The PJEI bit reports and acknowledges the status of the positive pointer justification event interrupts for tributary TU #1 in TUG2 #1. When the MONIS bit is set high, interrupts are generated upon reception of a positive pointer justification event in the incoming stream. When the MONIS bit is set low, interrupts are generated upon generation of a positive pointer justification event in the outgoing stream. PJEI is set high when a positive pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PJEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect positive pointer justification events.

NJEI:

The NJEI bit reports and acknowledges the status of the negative pointer justification event interrupts for tributary TU #1 in TUG2 #1. When the MONIS bit is set high, interrupts are generated upon reception of a negative pointer justification event in the incoming stream. When the MONIS bit is set low, interrupts are generated upon generation of a negative pointer justification event in the outgoing stream. NJEI is set high when a negative pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. NJEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect negative pointer justification events.

SS[1:0]:

The SS[1:0] bits reports the value of the size bits in the V1 byte of tributary TU #1 in TUG2 #1. The SS[1:0] bits are not filtered and must be software de-bounced.

Register 1402H, 1404H, 1406H, 1408H, 140AH, 140CH: VTPP Egress, TU #1 in TUG2 #2 to TUG2 #7, Configuration and Status

Bit	Type	Function	Default
Bit 7	R/W	Reserved	1
Bit 6	R/W	TU11	1
Bit 5	R/W	PF	0
Bit 4	R	LOPV	X
Bit 3	R/W	ALARME	0
Bit 2	R/W	DLOP	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	IPAIS	0

This set of registers reports the status and configures the operational modes of TU #1 in TUG2 #2 to TUG2 #7.

IPAIS:

The IPAIS bit enables the insertion of path AIS for tributary TU #1 in the corresponding TUG2. Tributary path AIS is inserted by forcing all ones into all tributary bytes.

DLOP:

The DLOP bit allows downstream pointer processing elements to be diagnosed. When DLOP is set high, the new data flag (NDF) field of the outgoing payload pointer in tributary TU #1 in the corresponding TUG2 is inverted to cause downstream pointer processing elements to enter a loss of pointer state. Insertion of an inverted new data flag can occur in concert with the insertion of a normal idle (unequipped) indication. The DLOP bit has no effect when the IPAIS bit is set high.

ALARME:

The ALARME bit enables loss of pointer and path AIS interrupts for tributary TU #1 in the corresponding TUG2. When ALARME is set high, an interrupt is generated upon entry to and exit from the LOP and AIS state of the pointer interpreter state diagram. Interrupts due to AIS and LOP status change are masked when ALARME is set low.

LOPV:

The LOPV bit indicates the loss of pointer status of tributary TU #1 in the corresponding TUG2.

PF:

The PF bit enables pointer follower mode for tributary TU #1 in the corresponding TUG2. In pointer follower mode, the tributary FIFO dead-zone is collapsed so that any variation in FIFO depth will result in an outgoing pointer justification event. Any TU pointer justification event on the corresponding incoming tributary, or an AU pointer justification event affecting this tributary will cause an outgoing pointer justification event.

TU11:

The TU11 bit specifies the tributary configuration of tributary group TUG2 #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

Bit 7 must be kept at a logic 1 for proper operation of the TEMAP while bit 1 must be kept to logic 0.

Register 1403H, 1405H, 1407H, 1409H, 140BH, 140DH: VTPP Egress, TU #1 in TUG2 #2 to TUG2 #7, Alarm Status

Bit	Type	Function	Default
Bit 7	R	SS[1]	X
Bit 6	R	SS[0]	X
Bit 5	R	NJEI	X
Bit 4	R	PJEI	X
Bit 3	R	ESEI	X
Bit 2	R/W	PEE	0
Bit 1	R	AISV	X
Bit 0	R/W	RELAYAIS	0

This set of registers reports the alarm status of TU #1 in TUG2 #2 to TUG2 #7.

RELAYAIS:

The RELAYAIS bit controls the number of consecutive AIS_ind indications required to enter the AIS state for tributary TU #1 in the corresponding TUG2. When RELAYAIS is set high, AIS is declared upon receipt of a single AIS_ind indication. When RELAYAIS is set low, AIS is declared after 3 consecutive AIS_ind indications.

AISV:

The AISV bit indicates the tributary path AIS status of tributary TU #1 in the corresponding TUG2.

PEE:

The PEE bit enables pointer event interrupts for tributary TU #1 in the corresponding TUG2. When PEE is set high, an interrupt is generated upon detection of FIFO underflows and overflows, upon detection of incoming pointer justification events when the MONIS bit is set high and upon detection of outgoing pointer justification events when the MONIS bit is set low. Interrupts due to elastic store errors and pointer justification events are masked when PEE is set low.

ESEI:

The ESEI bit reports and acknowledges the status of elastic store error interrupts for tributary TU #1 in the corresponding TUG2. Interrupts are

generated upon FIFO underflows and overflows. ESEI is set high when an elastic store error occurs and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. ESEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect elastic store error events.

PJEI:

The PJEI bit reports and acknowledges the status of the positive pointer justification event interrupts for tributary TU #1 in the corresponding TUG2. When the MONIS bit is set high, interrupts are generated upon reception of a positive pointer justification event in the incoming stream. When the MONIS bit is set low, interrupts are generated upon generation of a positive pointer justification event in the outgoing stream. PJEI is set high when a positive pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PJEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect positive pointer justification events.

NJEI:

The NJEI bit reports and acknowledges the status of the negative pointer justification event interrupts for tributary TU #1 in the corresponding TUG2. When the MONIS bit is set high, interrupts are generated upon reception of a negative pointer justification event in the incoming stream. When the MONIS bit is set low, interrupts are generated upon generation of a negative pointer justification event in the outgoing stream. NJEI is set high when a negative pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. NJEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect negative pointer justification events.

SS[1:0]:

The SS[1:0] bits reports the value of the size bits in the V1 byte of tributary TU #1 in the corresponding TUG2. The SS[1:0] bits are not filtered and must be software de-bounced.

Register 140EH: VTPP Egress, TU #1 in TUG2 #1 to TUG2 #7, LOP Interrupt

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R	LOP7I	0
Bit 5	R	LOP6I	0
Bit 4	R	LOP5I	0
Bit 3	R	LOP4I	0
Bit 2	R	LOP3I	0
Bit 1	R	LOP2I	0
Bit 0	R	LOP1I	0

This register is used to identify and acknowledge loss of pointer interrupts for the tributaries TU #1 in TUG2 #1 to TUG2 #7.

LOP1I:

The LOP1I bit identifies the source of loss of pointer interrupts. The LOP1I bit reports and acknowledges LOP interrupt of TU #1 in TUG2 #1. Interrupts are generated upon loss of pointer and upon re-acquisition. LOP1I is set high when the corresponding loss of pointer event occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. LOP1I remains valid when interrupts are not enabled (ALARME set low) and may be polled to detect loss of pointer events.

LOP2I-LOP7I:

The LOP2I to LOP7I bits identify the source of loss of pointer interrupts. The LOP2I to LOP7I bits report and acknowledge LOP interrupt of TU #1 in TUG2 #2 to TUG2 #7, respectively. Interrupts are generated upon loss of pointer and upon re-acquisition. An LOP*x*I bit is set high when a loss of pointer event on the associated tributary (TU #1 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. LOP*x*I remains valid when interrupts are not enabled (ALARME set low) and may be polled to detect loss of pointer events.

Reserved:

The Reserved bit must be written with a logic 0 for proper operation of the TEMAP.

Register 140FH: VTPP Egress, TU #1 in TUG2 #1 to TUG2 #7, AIS Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	AIS7I	0
Bit 5	R	AIS6I	0
Bit 4	R	AIS5I	0
Bit 3	R	AIS4I	0
Bit 2	R	AIS3I	0
Bit 1	R	AIS2I	0
Bit 0	R	AIS1I	0

This register is used to identify and acknowledge alarm indication signal interrupts for the tributaries TU #1 in TUG2 #1 to TUG2 #7.

AIS1I:

The AIS1I bit identifies the source of tributary path AIS interrupts. The AIS1I bit reports and acknowledges AIS interrupt of TU #1 in TUG2 #1. Interrupts are generated upon detection and removal of tributary path AIS alarm. AIS1I is set high when the corresponding tributary path AIS event occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. AIS1I remains valid when interrupts are not enabled (ALARME set low) and may be polled to detect tributary path AIS events.

AIS2I-AIS7I:

The AIS2I to AIS7I bits identify the source of tributary path AIS interrupts. The AIS2I to AIS7I bits report and acknowledge AIS interrupt of TU #1 in TUG2 #2 to TUG2 #7, respectively. Interrupts are generated upon detection and removal of tributary path AIS. An AIS*x*I bit is set high when a tributary path AIS event on the associated tributary (TU #1 in TUG2 #x) occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. AIS*x*I remains valid when interrupts are not enabled (ALARME set low) and may be polled to detect tributary path AIS events.

Register 1410H, 1412H, 1414H, 1416H, 1418H, 141AH, 141CH: VTPP Egress, TU #2 in TUG2 #1 to TUG2 #7, Configuration and Status

Bit	Type	Function	Default
Bit 7	R	Reserved	1
Bit 6	R	TU11	1
Bit 5	R/W	PF	0
Bit 4	R	LOPV	X
Bit 3	R/W	ALARME	0
Bit 2	R/W	DLOP	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	IPAIS	0

This set of registers reports the status and configures the operational modes of TU #2 in TUG2 #1 to TUG2 #7.

IPAIS:

The IPAIS bit enables the insertion of path AIS for tributary TU #2 in the corresponding TUG2. Tributary path AIS is inserted by forcing all ones into all tributary bytes.

DLOP:

The DLOP bit allows downstream pointer processing elements to be diagnosed. When DLOP is set high, the new data flag (NDF) field of the outgoing payload pointer in tributary TU #2 in the corresponding TUG2 is inverted, causing downstream pointer processing elements to enter a loss of pointer state. Insertion of an inverted new data flag can occur in concert with the insertion of a normal idle (unequipped) indication. The DLOP bit has no effect when the IPAIS bit is set high.

ALARME:

The ALARME bit enables loss of pointer and path AIS interrupts for tributary TU #2 in the corresponding TUG2. When ALARME is set high, an interrupt is generated upon entry to and exit from the LOP and AIS state of the pointer interpreter state diagram. Interrupts due to AIS and LOP status change are masked when ALARME is set low.

LOPV:

The LOPV bit indicates the loss of pointer status of tributary TU #2 in the corresponding TUG2.

PF:

The PF bit enables pointer follower mode for tributary TU #2 in the corresponding TUG2. In pointer follower mode, the tributary FIFO dead-zone is collapsed so that any variation in FIFO depth will result in an outgoing pointer justification event. Any TU pointer justification event on the corresponding incoming tributary, or an AU pointer justification event affecting this tributary will cause an outgoing pointer justification event.

TU11:

The TU11 bit is read-only and reflect the values written into the corresponding register of TU #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

Bit 7 must be kept at a logic 1 for proper operation of the TEMAP while bit 1 must be kept to logic 0.

Register 1411H, 1413H, 1415H, 1417H, 1419H, 141BH, 141DH: VTPP Egress, TU #2 in TUG2 #1 to TUG2 #7, Alarm Status

Bit	Type	Function	Default
Bit 7	R	SS[1]	X
Bit 6	R	SS[0]	X
Bit 5	R	NJEI	X
Bit 4	R	PJEI	X
Bit 3	R	ESEI	X
Bit 2	R/W	PEE	0
Bit 1	R	AISV	X
Bit 0	R/W	RELAYAIS	0

This set of registers reports the alarm status of TU #2 in TUG2 #1 to TUG2 #7.

RELAYAIS:

The RELAYAIS bit controls the number of consecutive AIS_ind indications required to enter the AIS state for tributary TU #2 in the corresponding TUG2. When RELAYAIS is set high, AIS is declared upon receipt of a single AIS_ind indication. When RELAYAIS is set low, AIS is declared after 3 consecutive AIS_ind indications.

AISV:

The AISV bit indicates the tributary path AIS status of tributary TU #2 in the corresponding TUG2.

PEE:

The PEE bit enables pointer event interrupts for tributary TU #2 in the corresponding TUG2. When PEE is set high, an interrupt is generated upon detection of FIFO underflows and overflows, upon detection of incoming pointer justification events when the MONIS bit is set high and upon detection of outgoing pointer justification events when the MONIS bit is set low. Interrupts due to elastic store errors and pointer justification events are masked when PEE is set low.

ESEI:

The ESEI bit reports and acknowledges the status of elastic store error interrupts for tributary TU #2 in the corresponding TUG2. Interrupts are

generated upon FIFO underflows and overflows. ESEI is set high when an elastic store error occurs and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. ESEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect elastic store error events.

PJEI:

The PJEI bit reports and acknowledges the status of the positive pointer justification event interrupts for tributary TU #2 in the corresponding TUG2. When the MONIS bit is set high, interrupts are generated upon reception of a positive pointer justification event in the incoming stream. When the MONIS bit is set low, interrupts are generated upon generation of a positive pointer justification event in the outgoing stream. PJEI is set high when a positive pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PJEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect positive pointer justification events.

NJEI:

The NJEI bit reports and acknowledges the status of the negative pointer justification event interrupts for tributary TU #2 in the corresponding TUG2. When the MONIS bit is set high, interrupts are generated upon reception of a negative pointer justification event in the incoming stream. When the MONIS bit is set low, interrupts are generated upon generation of a negative pointer justification event in the outgoing stream. NJEI is set high when a negative pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. NJEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect negative pointer justification events.

SS[1:0]:

The SS[1:0] bits reports the value of the size bits in the V1 byte of tributary TU #2 in the corresponding TUG2. The SS[1:0] bits are not filtered and must be software de-bounced.

Register 141EH: VTPP Egress, TU #2 in TUG2 #1 to TUG2 #7, LOP Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	LOP7I	0
Bit 5	R	LOP6I	0
Bit 4	R	LOP5I	0
Bit 3	R	LOP4I	0
Bit 2	R	LOP3I	0
Bit 1	R	LOP2I	0
Bit 0	R	LOP1I	0

This register is used to identify and acknowledge loss of pointer interrupts for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

LOP1I-LOP7I:

The LOP1I to LOP7I bits identify the source of loss of pointer interrupts. When operational, the LOP1I to LOP7I bits report and acknowledge LOP interrupts of TU #2 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon loss of pointer and upon re-acquisition. An LOP*x*I bit is set high when a loss of pointer event on the associated tributary occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. LOP*x*I remains valid when interrupts are not enabled (ALARME set low) and may be polled to detect loss of pointer events.

Register 141FH: VTPP Egress, TU #2 in TUG2 #1 to TUG2 #7 AIS Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	AIS7I	0
Bit 5	R	AIS6I	0
Bit 4	R	AIS5I	0
Bit 3	R	AIS4I	0
Bit 2	R	AIS3I	0
Bit 1	R	AIS2I	0
Bit 0	R	AIS1I	0

This register is used to identify and acknowledge tributary path AIS interrupts for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

AIS1I-AIS7I:

The AIS1I to AIS7I bits identify the source of tributary path AIS interrupts. When operational, the AIS1I to AIS7I bits report and acknowledge AIS interrupt of TU #2 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon detection and removal of tributary path AIS alarm. An AIS*x*I bit is set high when a tributary path AIS event on the associated tributary occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. AIS*x*I remains valid when interrupts are not enabled (ALARME set low) and may be polled to detect tributary path AIS events.

Register 1420H, 1422H, 1424H, 1426H, 1428H, 142AH, 142CH: VTPP Egress, TU #3 in TUG2 #1 to TUG2 #7, Configuration and Status

Bit	Type	Function	Default
Bit 7	R	Reserved	1
Bit 6	R	TU11	1
Bit 5	R/W	PF	0
Bit 4	R	LOPV	X
Bit 3	R/W	ALARME	0
Bit 2	R/W	DLOP	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	IPAIS	0

This set of registers reports the status and configures the operational modes of TU #3 in TUG2 #1 to TUG2 #7.

IPAIS:

The IPAIS bit enables the insertion of path AIS for tributary TU #3 in the corresponding TUG2. Tributary path AIS is inserted by forcing all ones into all tributary bytes.

DLOP:

The DLOP bit allows downstream pointer processing elements to be diagnosed. When DLOP is set high, the new data flag (NDF) field of the outgoing payload pointer in tributary TU #3 in the corresponding TUG2 is inverted, causing downstream pointer processing elements to enter a loss of pointer state. Insertion of an inverted new data flag can occur in concert with the insertion of a normal idle (unequipped) indication. The DLOP bit has no effect when the IPAIS bit is set high.

ALARME:

The ALARME bit enables loss of pointer and path AIS interrupts for tributary TU #3 in the corresponding TUG2. When ALARME is set high, an interrupt is generated upon entry to and exit from the LOP and AIS state of the pointer interpreter state diagram. Interrupts due to AIS and LOP status change are masked when ALARME is set low.

LOPV:

The LOPV bit indicates the loss of pointer status of tributary TU #3 in the corresponding TUG2.

PF:

The PF bit enables pointer follower mode for tributary TU #3 in the corresponding TUG2. In pointer follower mode, the tributary FIFO dead-zone is collapsed so that any variation in FIFO depth will result in an outgoing pointer justification event. Any TU pointer justification event on the corresponding incoming tributary, or an AU pointer justification event affecting this tributary will cause an outgoing pointer justification event.

TU11:

The TU11 bit is read-only and reflect the values written into the corresponding register of TU #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

Bit 7 must be kept at a logic 1 for proper operation of the TEMAP while bit 1 must be kept to logic 0.

Register 1421H, 1423H, 1425H, 1427H, 1429H, 142BH, 142DH: VTPP Egress, TU #3 in TUG2 #1 to TUG2 #7, Alarm Status

Bit	Type	Function	Default
Bit 7	R	SS[1]	X
Bit 6	R	SS[0]	X
Bit 5	R	NJEI	X
Bit 4	R	PJEI	X
Bit 3	R	ESEI	X
Bit 2	R/W	PEE	0
Bit 1	R	AISV	X
Bit 0	R/W	RELAYAIS	0

This set of registers reports the status and configures the operational modes of TU #3 in TUG2 #1 to TUG2 #7.

RELAYAIS:

The RELAYAIS bit controls the number of consecutive AIS_ind indications required to enter the AIS state for tributary TU #3 in the corresponding TUG2. When RELAYAIS is set high, AIS is declared upon receipt of a single AIS_ind indication. When RELAYAIS is set low, AIS is declared after 3 consecutive AIS_ind indications.

AISV:

The AISV bit indicates the tributary path AIS status of tributary TU #3 in the corresponding TUG2.

PEE:

The PEE bit enables pointer event interrupts for tributary TU #3 in the corresponding TUG2. When PEE is set high, an interrupt is generated upon detection of FIFO underflows and overflows, upon detection of incoming pointer justification events when the MONIS bit is set high and upon detection of outgoing pointer justification events when the MONIS bit is set low. Interrupts due to elastic store errors and pointer justification events are masked when PEE is set low.

ESEI:

The ESEI bit reports and acknowledges the status of elastic store error interrupts for tributary TU #3 in the corresponding TUG2. Interrupts are generated upon FIFO underflows and overflows. ESEI is set high when an elastic store error occurs and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. ESEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect elastic store error events.

PJEI:

The PJEI bit reports and acknowledges the status of the positive pointer justification event interrupts for tributary TU #3 in the corresponding TUG2. When the MONIS bit is set high, interrupts are generated upon reception of a positive pointer justification event in the incoming stream. When the MONIS bit is set low, interrupts are generated upon generation of a positive pointer justification event in the outgoing stream. PJEI is set high when a positive pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PJEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect positive pointer justification events.

NJEI:

The NJEI bit reports and acknowledges the status of the negative pointer justification event interrupts for tributary TU #3 in the corresponding TUG2. When the MONIS bit is set high, interrupts are generated upon reception of a negative pointer justification event in the incoming stream. When the MONIS bit is set low, interrupts are generated upon generation of a negative pointer justification event in the outgoing stream. NJEI is set high when a negative pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. NJEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect negative pointer justification events.

SS[1:0]:

The SS[1:0] bits reports the value of the size bits in the V1 byte of tributary TU #3 in the corresponding TUG2. The SS[1:0] bits are not filtered and must be software de-bounced.

Register 142EH: VTPP Egress, TU #3 in TUG2 #1 to TUG2 #7, LOP Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	LOP7I	0
Bit 5	R	LOP6I	0
Bit 4	R	LOP5I	0
Bit 3	R	LOP4I	0
Bit 2	R	LOP3I	0
Bit 1	R	LOP2I	0
Bit 0	R	LOP1I	0

This register is used to identify and acknowledge loss of pointer interrupts for the tributaries TU #2 in TUG2 #1 to TUG2 #7.

LOP1I-LOP7I:

The LOP1I to LOP7I bits identify the source of loss of pointer interrupts. When operational, the LOP1I to LOP7I bits report and acknowledge LOP interrupts of TU #3 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon loss of pointer and upon re-acquisition. An LOP*x*I bit is set high when a loss of pointer event on the associated tributary occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. LOP*x*I remains valid when interrupts are not enabled (ALARME set low) and may be polled to detect loss of pointer events.

Register 142FH: VTPP Egress, TU #3 in TUG2 #1 to TUG2 #7, AIS Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	AIS7I	0
Bit 5	R	AIS6I	0
Bit 4	R	AIS5I	0
Bit 3	R	AIS4I	0
Bit 2	R	AIS3I	0
Bit 1	R	AIS2I	0
Bit 0	R	AIS1I	0

This register is used to identify and acknowledge tributary path AIS interrupts for the tributaries TU #3 in TUG2 #1 to TUG2 #7.

AIS1I-AIS7I:

The AIS1I to AIS7I bits identify the source of tributary path AIS interrupts. When operational, the AIS1I to AIS7I bits report and acknowledge AIS interrupt of TU #3 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon detection and removal of tributary path AIS alarm. An AIS*x*I bit is set high when a tributary path AIS event on the associated tributary occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. AIS*x*I remains valid when interrupts are not enabled (ALARME set low) and may be polled to detect tributary path AIS events.

Register 1430H, 1432H, 1434H, 1436H, 1438H, 143AH, 143CH: VTPP Egress, TU #4 in TUG2 #1 to TUG2 #7, Configuration and Status

Bit	Type	Function	Default
Bit 7	R	Reserved	1
Bit 6	R	TU11	1
Bit 5	R/W	PF	0
Bit 4	R	LOPV	X
Bit 3	R/W	ALARME	0
Bit 2	R/W	DLOP	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	IPAIS	0

This set of registers reports the status and configures the operational modes of TU #4 in TUG2 #1 to TUG2 #7. When the corresponding TUG2 tributary group is configured to TU12 (VT2) mode, the associated register in this set has no effect.

IPAIS:

The IPAIS bit enables the insertion of path AIS for tributary TU #4 in the corresponding TUG2. Tributary path AIS is inserted by forcing all ones into all tributary bytes.

DLOP:

The DLOP bit allows downstream pointer processing elements to be diagnosed. When DLOP is set high, the new data flag (NDF) field of the outgoing payload pointer in tributary TU #4 in the corresponding TUG2 is inverted, causing downstream pointer processing elements to enter a loss of pointer state. Insertion of an inverted new data flag can occur in concert with the insertion of a normal idle (unequipped) indication. The DLOP bit has no effect when the IPAIS bit is set high.

ALARME:

The ALARME bit enables loss of pointer and path AIS interrupts for tributary TU #4 in the corresponding TUG2. When ALARME is set high, an interrupt is generated upon entry to and exit from the LOP and AIS state of the pointer interpreter state diagram. Interrupts due to AIS and LOP status change are masked when ALARME is set low.

LOPV:

The LOPV bit indicates the loss of pointer status of tributary TU #4 in the corresponding TUG2.

PF:

The PF bit enables pointer follower mode for tributary TU #4 in the corresponding TUG2. In pointer follower mode, the tributary FIFO dead-zone is collapsed so that any variation is FIFO depth will result in an outgoing pointer justification event. Any TU pointer justification event on the corresponding incoming tributary, or an AU pointer justification event affecting this tributary will cause an outgoing pointer justification event.

TU11:

The TU11 bit is read-only and reflect the values written into the corresponding register of TU #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

Bit 7 must be kept at a logic 1 for proper operation of the TEMAP while bit 1 must be kept to logic 0.

Register 1431H, 1433H, 1435H, 1437H, 1439H, 143BH, 143DH: VTPP Egress, TU #4 in TUG2 #1 to TUG2 #7, Alarm Status

Bit	Type	Function	Default
Bit 7	R	SS[1]	X
Bit 6	R	SS[0]	X
Bit 5	R	NJEI	X
Bit 4	R	PJEI	X
Bit 3	R	ESEI	X
Bit 2	R/W	PEE	0
Bit 1	R	AISV	X
Bit 0	R/W	RELAYAIS	0

This set of registers reports the alarm status of TU #4 in TUG2 #1 to TUG2 #7. When the corresponding TUG2 tributary group is configured to TU12 (VT2) mode, the associated register in this set has no effect.

RELAYAIS:

The RELAYAIS bit controls the number of consecutive AIS_ind indications required to enter the AIS state for tributary TU #4 in the corresponding TUG2. When RELAYAIS is set high, AIS is declared upon receipt of a single AIS_ind indication. When RELAYAIS is set low, AIS is declared after 3 consecutive AIS_ind indications.

AISV:

The AISV bit indicates the tributary path AIS status of tributary TU #4 in the corresponding TUG2.

PEE:

The PEE bit enables pointer event interrupts for tributary TU #4 in the corresponding TUG2. When PEE is set high, an interrupt is generated upon detection of FIFO underflows and overflows, upon detection of incoming pointer justification events when the MONIS bit is set high and upon detection of outgoing pointer justification events when the MONIS bit is set low. Interrupts due to elastic store errors and pointer justification events are masked when PEE is set low.

ESEI:

The ESEI bit reports and acknowledges the status of elastic store error interrupts for tributary TU #4 in the corresponding TUG2. Interrupts are generated upon FIFO underflows and overflows. ESEI is set high when an elastic store error occurs and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. ESEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect elastic store error events.

PJEI:

The PJEI bit reports and acknowledges the status of the positive pointer justification event interrupts for tributary TU #4 in the corresponding TUG2. When the MONIS bit is set high, interrupts are generated upon reception of a positive pointer justification event in the incoming stream. When the MONIS bit is set low, interrupts are generated upon generation of a positive pointer justification event in the outgoing stream. PJEI is set high when a positive pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. PJEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect positive pointer justification events.

NJEI:

The NJEI bit reports and acknowledges the status of the negative pointer justification event interrupts for tributary TU #4 in the corresponding TUG2. When the MONIS bit is set high, interrupts are generated upon reception of a negative pointer justification event in the incoming stream. When the MONIS bit is set low, interrupts are generated upon generation of a negative pointer justification event in the outgoing stream. NJEI is set high when a negative pointer justification event occurs in the monitored stream and is cleared immediately following a read of this register, which also acknowledges and clears the interrupt. NJEI remains valid when interrupts are not enabled (PEE set low) and may be polled to detect negative pointer justification events.

SS[1:0]:

The SS[1:0] bits reports the value of the size bits in the V1 byte of tributary TU #4 in the corresponding TUG2. The SS[1:0] bits are not filtered and must be software de-bounced.

Register 143EH: VTPP Egress, TU #4 in TUG2 #1 to TUG2 #7, LOP Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	LOP7I	0
Bit 5	R	LOP6I	0
Bit 4	R	LOP5I	0
Bit 3	R	LOP4I	0
Bit 2	R	LOP3I	0
Bit 1	R	LOP2I	0
Bit 0	R	LOP1I	0

This register is used to identify and acknowledge loss of pointer interrupts for the tributaries TU #4 in TUG2 #1 to TUG2 #7.

LOP1I-LOP7I:

The LOP1I to LOP7I bits identify the source of loss of pointer interrupts. When the corresponding TUG2 tributary group is configured TU12 (VT2) mode, the associated LOP*x*I bit is unused and will return a logic 0 when read. When operational, the LOP1I to LOP7I bits report and acknowledge LOP interrupt of TU #4 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon loss of pointer and upon re-acquisition. An LOP*x*I bit is set high when a loss of pointer event on the associated tributary occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. LOP*x*I remains valid when interrupts are not enabled (ALARME set low) and may be polled to detect loss of pointer events.

Register 143FH: VTPP Egress, TU #4 in TUG2 #1 to TUG2 #7, AIS Interrupt

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	AIS7I	0
Bit 5	R	AIS6I	0
Bit 4	R	AIS5I	0
Bit 3	R	AIS4I	0
Bit 2	R	AIS3I	0
Bit 1	R	AIS2I	0
Bit 0	R	AIS1I	0

This register is used to identify and acknowledge tributary path AIS interrupts for the tributaries TU #4 in TUG2 #1 to TUG2 #7.

AIS1I-AIS7I:

The AIS1I to AIS7I bits identify the source of tributary path AIS interrupts. When the corresponding TUG2 tributary group is configured for TU12 (VT2) mode, the associated AIS*x*I bit is unused and will return a logic 0 when read. When operational, the AIS1I to AIS7I bits report and acknowledge AIS interrupt of TU #4 in TUG2 #1 to TUG2 #7, respectively. Interrupts are generated upon detection and removal of tributary path AIS alarm. An AIS*x*I bit is set high when a tributary path AIS event on the associated tributary occurs and are cleared immediately following a read of this register, which also acknowledges and clears the interrupt. AIS*x*I remains valid when interrupts are not enabled (ALARME set low) and may be polled to detect tributary path AIS events.

1.27 TRAP Transmit Alarm Processor Registers

Register 1480H: TRAP TU #1 in TUG2 #1 of TUG3 #1, Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	1
Bit 6	R/W	TU11	1
Bit 5		Unused	X
Bit 4	R/W	FORCEEN	0
Bit 3	R/W	RFI	0
Bit 2	R/W	RDI	0
Bit 1	R/W	ERDI	0
Bit 0	R/W	POHDIS	0

This register configures the operational modes of TU #1 of TUG2 #1, TUG3 #1 in the incoming/outgoing egress data stream.

POHDIS:

The POHDIS bit controls the modification of the tributary path overhead bytes when tributary TU #1 of TUG2 #1, TUG3 #1 is on the egress data stream. When POHDIS is set high, the tributary path overhead bytes are not modified. This is primarily intended for use with transparent VTs from the SBI bus as configured by the ETVT bit the TTMP block. When POHDIS is set low, the tributary path overhead of TU #1 of TUG2 #1, TUG3 #1 is processed normally.

ERDI:

The ERDI bit selects between normal and extended RDI encoding on tributary TU #1 of TUG2 #1, TUG3 #1. When ERDI is set high, extended RDI is selected. The RDI and RFI indications to the TTOP are treated as a 2-bit codepoint. The TTOP block will insert the RDI indication into bit 5 of the Z7 byte and bit 8 of the V5 byte and the RFI indication into bit 6 of the Z7 byte and its complement into bit 7. When ERDI is set low, normal RDI is selected. The RDI and RFI indications are treated independently. TTOP will insert the RDI output into bit 8 of the V5 byte and the RFI output into bit 4 of the V5 byte. The ERDI bit in the TTOP must be configured the same as this bit.

RDI:

The RDI bit controls the value of the RDI indication to TTOP when tributary TU #1 of TUG2 #1, TUG3 #1 is on the egress data stream. When FORCEEN is set high, the RDI and RFI indications to TTOP are controlled directly by the RDI and RFI register bits. When FORCEEN is set low, the RDI and RFI Indications to TTOP reflect the remote alarm status from the remote alarm source selected via the TRAP Indirect Remote Alarm register.

RFI:

The RFI bit controls the value of the RFI indication to TTOP when tributary TU #1 of TUG2 #1, TUG3 #1 is on the outgoing data stream. When FORCEEN is set high, the RDI and RFI indications to TTOP are controlled directly by the RDI and RFI register bits. When FORCEEN is set low, the RDI and RFI Indications to TTOP reflect the remote alarm status from the remote alarm source selected via the TRAP Indirect Remote Alarm register.

FORCEEN:

The FORCEEN bit combined with the RFI and RDI register bits controls the RDI and RFI indications to TTOP. When FORCEEN is high the RDI and RFI indications to TTOP are controlled directly by the RDI and RFI register bits. When FORCEEN is set low the RDI and RFI indications reflect the remote alarm status from the remote alarm source selected via the TRAP Indirect Remote Alarm registers.

TU11:

The TU11 bit specifies the tributary configuration of the tributary group TUG2 #1, TUG3 #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMAP.

Register 1481H, 1482H, 1483H, 1484H, 1485H, 1486H: TRAP TU #1 in TUG2 #2 to TUG2 #7 of TUG3 #1, Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	1
Bit 6	R/W	TU11	1
Bit 5		Unused	X
Bit 4	R/W	FORCEEN	0
Bit 3	R/W	RFI	0
Bit 2	R/W	RDI	0
Bit 1	R/W	ERDI	0
Bit 0	R/W	POHDIS	0

This register configures the operational modes of TU #1 of TUG2 #2, TUG3 #1 to TU #1 of TUG2 #7, TUG3 #1 in the incoming/outgoing egress data stream.

POHDIS:

The POHDIS bit controls the modification of the tributary path overhead bytes when tributary TU #1 in the corresponding TUG2, TUG3 #1 is on the egress data stream. When POHDIS is set high, the tributary path overhead bytes are not modified. This is primarily intended for use with transparent VTs from the SBI bus as configured by the ETVT bit the TTMP block. When POHDIS is set low, the tributary path overhead of TU #1 in the corresponding TUG2, TUG3 #1 is processed normally.

ERDI:

The ERDI bit selects between normal and extended RDI encoding on tributary TU #1 in the corresponding TUG2, TUG3 #1. When ERDI is set high, extended RDI is selected. The RDI and RFI indications to the TTOP are treated as a 2-bit codepoint. The TTOP block will insert the RDI indication into bit 5 of the Z7 byte and bit 8 of the V5 byte and the RFI indication into bit 6 of the Z7 byte and its complement into bit 7. When ERDI is set low, normal RDI is selected. The RDI and RFI indications are treated independently. TTOP will insert the RDI output into bit 8 of the V5 byte and the RFI output into bit 4 of the V5 byte. The ERDI bit in the TTOP must be configured the same as this bit.

RDI:

The RDI bit controls the value of the RDI indication to TTOP when tributary TU #1 in the corresponding TUG2, TUG3 #1 is on the egress data stream. When FORCEEN is set high, the RDI and RFI indications to TTOP are controlled directly by the RDI and RFI register bits. When FORCEEN is set low, the RDI and RFI Indications to TTOP reflect the remote alarm status from the remote alarm source selected via the TRAP Indirect Remote Alarm register.

RFI:

The RFI bit controls the value of the RFI indication to TTOP when tributary TU #1 in the corresponding TUG2, TUG3 #1 is on the egress data stream. When FORCEEN is set high, the RDI and RFI indications to TTOP are controlled directly by the RDI and RFI register bits. When FORCEEN is set low, the RDI and RFI Indications to TTOP reflect the remote alarm status from the remote alarm source selected via the TRAP Indirect Remote Alarm register.

FORCEEN:

The FORCEEN bit combined with the RFI and RDI register bits controls the RDI and RFI indications to TTOP. When FORCEEN is high the RDI and RFI indications to TTOP are controlled directly by the RDI and RFI register bits. When FORCEEN is set low the RDI and RFI indications reflect the remote alarm status from the remote alarm source selected via the TRAP Indirect Remote Alarm registers.

TU11:

The TU11 bit specifies the tributary configuration of the corresponding TUG2 tributary group in TUG3 #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMAP.

Register 1487H: TRAP TU #1 in TUG2 #1 to TUG2 #7 of TUG3 #1, Egress AIS Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	EAIS7	0
Bit 5	R/W	EAIS6	0
Bit 4	R/W	EAIS5	0
Bit 3	R/W	EAIS4	0
Bit 2	R/W	EAIS3	0
Bit 1	R/W	EAIS2	0
Bit 0	R/W	EAIS1	0

This register controls the insertion of AIS when tributary TU #1 of TUG2 #1, TUG3 #1 to TU#1 of TUG2 #7, TUG3 #1 are on the egress data stream.

EAIS7 – EAIS1:

The EAIS1 to EAIS7 bits control the state of the AIS insertion when tributary TU #1 of TUG2 #1, TUG3 #1 to TUG2 #7, TUG3 #1, respectively, are on the egress data stream. When EAIS*x* is set high, tributary path AIS is inserted in the associated tributary of the egress data stream. When EAIS*x* is set low, tributary path AIS is not forced in the associated tributary of the egress data stream although tributary path AIS may still be inserted due to other alarm conditions.

Register 1488H, 1489H, 148AH, 148BH, 148CH, 148DH, 148EH: TRAP TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #1, Control

Bit	Type	Function	Default
Bit 7	R	Reserved	1
Bit 6	R	TU11	1
Bit 5		Unused	X
Bit 4	R/W	FORCEEN	0
Bit 3	R/W	RFI	0
Bit 2	R/W	RDI	0
Bit 1	R/W	ERDI	0
Bit 0	R/W	POHDIS	0

This register configures the operational modes of TU #2 of TUG2 #1, TUG3 #1 to TU #2 of TUG2 #7, TUG3 #1 in the incoming/outgoing egress data stream.

POHDIS:

The POHDIS bit controls the modification of the tributary path overhead bytes when tributary TU #2 in the corresponding TUG2, TUG3 #1 is on the egress data stream. When POHDIS is set high, the tributary path overhead bytes are not modified. This is primarily intended for use with transparent VTs from the SBI bus as configured by the ETVT bit the TTMP block. When POHDIS is set low, the tributary path overhead of TU #2 in the corresponding TUG2, TUG3 #1 is processed normally.

ERDI:

The ERDI bit selects between normal and extended RDI encoding on tributary TU #2 in the corresponding TUG2, TUG3 #1. When ERDI is set high, extended RDI is selected. The RDI and RFI indications to the TTOP are treated as a 2-bit codepoint. The TTOP block will insert the RDI indication into bit 5 of the Z7 byte and bit 8 of the V5 byte and the RFI indication into bit 6 of the Z7 byte and its complement into bit 7. When ERDI is set low, normal RDI is selected. The RDI and RFI indications are treated independently. TTOP will insert the RDI output into bit 8 of the V5 byte and the RFI output into bit 4 of the V5 byte. The ERDI bit in the TTOP must be configured the same as this bit.

RDI:

The RDI bit controls the value of the RDI indication to TTOP when tributary TU #2 in the corresponding TUG2, TUG3 #1 is on the egress data stream. When FORCEEN is set high, the RDI and RFI indications to TTOP are controlled directly by the RDI and RFI register bits. When FORCEEN is set low, the RDI and RFI Indications to TTOP reflect the remote alarm status from the remote alarm source selected via the TRAP Indirect Remote Alarm register.

RFI:

The RFI bit controls the value of the RFI indication to TTOP when tributary TU #2 in the corresponding TUG2, TUG3 #1 is on the egress data stream. When FORCEEN is set high, the RDI and RFI indications to TTOP are controlled directly by the RDI and RFI register bits. When FORCEEN is set low, the RDI and RFI Indications to TTOP reflect the remote alarm status from the remote alarm source selected via the TRAP Indirect Remote Alarm register.

FORCEEN:

The FORCEEN bit combined with the RFI and RDI register bits controls the RDI and RFI indications to TTOP. When FORCEEN is high the RDI and RFI indications to TTOP are controlled directly by the RDI and RFI register bits. When FORCEEN is set low the RDI and RFI indications reflect the remote alarm status from the remote alarm source selected via the TRAP Indirect Remote Alarm registers.

TU11:

The TU11 read only bit reports the tributary configuration written into the corresponding register of TU #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMAP.

Register 148FH: TRAP TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #1, Egress AIS Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	EAIS7	0
Bit 5	R/W	EAIS6	0
Bit 4	R/W	EAIS5	0
Bit 3	R/W	EAIS4	0
Bit 2	R/W	EAIS3	0
Bit 1	R/W	EAIS2	0
Bit 0	R/W	EAIS1	0

This register controls the insertion of AIS when tributary TU #2 of TUG2 #1, TUG3 #1 to TU#2 of TUG2 #7, TUG3 #1 are on the egress data stream.

EAIS7 – EAIS1:

The EAIS1 to EAIS7 bits control the state of the AIS insertion when tributary TU #2 of TUG2 #1, TUG3 #1 to TUG2 #7, TUG3 #1, respectively, are on the egress data stream. When EAIS*x* is set high, tributary path AIS is inserted in the associated tributary of the egress data stream. When EAIS*x* is set low, tributary path AIS is not forced in the associated tributary of the egress data stream although tributary path AIS may still be inserted due to other alarm conditions.

Register 1490H, 1491H, 1492H, 1493H, 1494H, 1495H, 1496H: TRAP TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #1 Control

Bit	Type	Function	Default
Bit 7	R	Reserved	1
Bit 6	R	TU11	1
Bit 5		Unused	X
Bit 4	R/W	FORCEEN	0
Bit 3	R/W	RFI	0
Bit 2	R/W	RDI	0
Bit 1	R/W	ERDI	0
Bit 0	R/W	POHDIS	0

This register configures the operational modes of TU #3 of TUG2 #1, TUG3 #1 to TU #3 of TUG2 #7, TUG3 #1 in the incoming/outgoing egress data stream.

POHDIS:

The POHDIS bit controls the modification of the tributary path overhead bytes when tributary TU #3 in the corresponding TUG2, TUG3 #1 is on the egress data stream. When POHDIS is set high, the tributary path overhead bytes are not modified. This is primarily intended for use with transparent VTs from the SBI bus as configured by the ETVT bit the TTMP block. When POHDIS is set low, the tributary path overhead of TU #3 in the corresponding TUG2, TUG3 #1 is processed normally.

ERDI:

The ERDI bit selects between normal and extended RDI encoding on tributary TU #3 in the corresponding TUG2, TUG3 #1. When ERDI is set high, extended RDI is selected. The RDI and RFI indications to the TTOP are treated as a 2-bit codepoint. The TTOP block will insert the RDI indication into bit 5 of the Z7 byte and bit 8 of the V5 byte and the RFI indication into bit 6 of the Z7 byte and its complement into bit 7. When ERDI is set low, normal RDI is selected. The RDI and RFI indications are treated independently. TTOP will insert the RDI output into bit 8 of the V5 byte and the RFI output into bit 4 of the V5 byte. The ERDI bit in the TTOP must be configured the same as this bit.

RDI:

The RDI bit controls the value of the RDI indication to TTOP when tributary TU #3 in the corresponding TUG2, TUG3 #1 is on the egress data stream. When FORCEEN is set high, the RDI and RFI indications to TTOP are controlled directly by the RDI and RFI register bits. When FORCEEN is set low, the RDI and RFI Indications to TTOP reflect the remote alarm status from the remote alarm source selected via the TRAP Indirect Remote Alarm register.

RFI:

The RFI bit controls the value of the RFI indication to TTOP when tributary TU #3 in the corresponding TUG2, TUG3 #1 is on the egress data stream. When FORCEEN is set high, the RDI and RFI indications to TTOP are controlled directly by the RDI and RFI register bits. When FORCEEN is set low, the RDI and RFI Indications to TTOP reflect the remote alarm status from the remote alarm source selected via the TRAP Indirect Remote Alarm register.

FORCEEN:

The FORCEEN bit combined with the RFI and RDI register bits controls the RDI and RFI indications to TTOP. When FORCEEN is high the RDI and RFI indications to TTOP are controlled directly by the RDI and RFI register bits. When FORCEEN is set low the RDI and RFI indications reflect the remote alarm status from the remote alarm source selected via the TRAP Indirect Remote Alarm registers.

TU11:

The TU11 read only bit reports the tributary configuration written into the corresponding register of TU #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMAP.

Register 1497H: TRAP TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #1, Egress AIS Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	EAIS7	0
Bit 5	R/W	EAIS6	0
Bit 4	R/W	EAIS5	0
Bit 3	R/W	EAIS4	0
Bit 2	R/W	EAIS3	0
Bit 1	R/W	EAIS2	0
Bit 0	R/W	EAIS1	0

This register controls the insertion of AIS when tributary TU #3 of TUG2 #1, TUG3 #1 to TU#3 of TUG2 #7, TUG3 #1 are on the egress data stream.

EAIS7 – EAIS1:

The EAIS1 to EAIS7 bits control the state of the AIS insertion when tributary TU #3 of TUG2 #1, TUG3 #1 to TUG2 #7, TUG3 #1, respectively, are on the egress data stream. When EAIS*x* is set high, tributary path AIS is inserted in the associated tributary of the egress data stream. When EAIS*x* is set low, tributary path AIS is not forced in the associated tributary of the egress data stream although tributary path AIS may still be inserted due to other alarm conditions.

Register 1498H, 1499H, 149AH, 149BH, 149CH, 149DH, 149EH: TRAP TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #1, Control

Bit	Type	Function	Default
Bit 7	R	Reserved	1
Bit 6	R	TU11	1
Bit 5		Unused	X
Bit 4	R/W	FORCEEN	0
Bit 3	R/W	RFI	0
Bit 2	R/W	RDI	0
Bit 1	R/W	ERDI	0
Bit 0	R/W	POHDIS	0

This register configures the operational modes of TU #4 of TUG2 #1, TUG3 #1 to TU #4 of TUG2 #7, TUG3 #1 in the incoming/outgoing egress data stream. When the corresponding TUG2 tributary group is configured to TU12 (VT2) mode, the associated register in this set has no effect.

POHDIS:

The POHDIS bit controls the modification of the tributary path overhead bytes when tributary TU #4 in the corresponding TUG2, TUG3 #1 is on the egress data stream. When POHDIS is set high, the tributary path overhead bytes are not modified. This is primarily intended for use with transparent VTs from the SBI bus as configured by the ETVT bit the TTMP block. When POHDIS is set low, the tributary path overhead of TU #4 in the corresponding TUG2, TUG3 #1 is processed normally.

ERDI:

The ERDI bit selects between normal and extended RDI encoding on tributary TU #4 in the corresponding TUG2, TUG3 #1. When ERDI is set high, extended RDI is selected. The RDI and RFI indications to the TTOP are treated as a 2-bit codepoint. The TTOP block will insert the RDI indication into bit 5 of the Z7 byte and bit 8 of the V5 byte and the RFI indication into bit 6 of the Z7 byte and its complement into bit 7. When ERDI is set low, normal RDI is selected. The RDI and RFI indications are treated independently. TTOP will insert the RDI output into bit 8 of the V5 byte and the RFI output into bit 4 of the V5 byte. The ERDI bit in the TTOP must be configured the same as this bit.

RDI:

The RDI bit controls the value of the RDI indication to TTOP when tributary TU #4 in the corresponding TUG2, TUG3 #1 is on the egress data stream. When FORCEEN is set high, the RDI and RFI indications to TTOP are controlled directly by the RDI and RFI register bits. When FORCEEN is set low, the RDI and RFI Indications to TTOP reflect the remote alarm status from the remote alarm source selected via the TRAP Indirect Remote Alarm register.

RFI:

The RFI bit controls the value of the RFI indication to TTOP when tributary TU #4 in the corresponding TUG2, TUG3 #1 is on the egress data stream. When FORCEEN is set high, the RDI and RFI indications to TTOP are controlled directly by the RDI and RFI register bits. When FORCEEN is set low, the RDI and RFI Indications to TTOP reflect the remote alarm status from the remote alarm source selected via the TRAP Indirect Remote Alarm register.

FORCEEN:

The FORCEEN bit combined with the RFI and RDI register bits controls the RDI and RFI indications to TTOP. When FORCEEN is high the RDI and RFI indications to TTOP are controlled directly by the RDI and RFI register bits. When FORCEEN is set low the RDI and RFI indications reflect the remote alarm status from the remote alarm source selected via the TRAP Indirect Remote Alarm registers.

TU11:

The TU11 read only bit reports the tributary configuration written into the corresponding register of TU #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMAP.

Register 149FH: TRAP TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #1, Egress AIS Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	EAIS7	0
Bit 5	R/W	EAIS6	0
Bit 4	R/W	EAIS5	0
Bit 3	R/W	EAIS4	0
Bit 2	R/W	EAIS3	0
Bit 1	R/W	EAIS2	0
Bit 0	R/W	EAIS1	0

This register controls the insertion of AIS when tributary TU #4 of TUG2 #1, TUG3 #1 to TU#3 of TUG2 #7, TUG3 #1 are on the egress data stream. When the corresponding TUG2 tributary group is configured to TU12 (VT2) mode, this register has no effect.

EAIS7 – EAIS1:

The EAIS1 to EAIS7 bits control the state of the AIS insertion when tributary TU #4 of TUG2 #1, TUG3 #1 to TUG2 #7, TUG3 #1, respectively, are on the egress data stream. When EAIS*x* is set high, tributary path AIS is inserted in the associated tributary of the egress data stream. When EAIS*x* is set low, tributary path AIS is not forced in the associated tributary of the egress data stream although tributary path AIS may still be inserted due to other alarm conditions.

Register 14A0H, 14A1H, 14A2H, 14A3H, 14A4H, 14A5H, 14A6H: TRAP TU #1 in TUG2 #1 to TUG2 #7 of TUG3 #2, Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	1
Bit 6	R/W	TU11	1
Bit 5		Unused	X
Bit 4	R/W	FORCEEN	0
Bit 3	R/W	RFI	0
Bit 2	R/W	RDI	0
Bit 1	R/W	ERDI	0
Bit 0	R/W	POHDIS	0

This register configures the operational modes of TU #1 of TUG2 #1, TUG3 #2 to TU #1 of TUG2 #7, TUG3 #2 in the incoming/outgoing egress data stream.

POHDIS:

The POHDIS bit controls the modification of the tributary path overhead bytes when tributary TU #1 in the corresponding TUG2, TUG3 #2 is on the egress data stream. When POHDIS is set high, the tributary path overhead bytes are not modified. This is primarily intended for use with transparent VTs from the SBI bus as configured by the ETVT bit the TTMP block. When POHDIS is set low, the tributary path overhead of TU #1 in the corresponding TUG2, TUG3 #2 is processed normally.

ERDI:

The ERDI bit selects between normal and extended RDI encoding on tributary TU #1 in the corresponding TUG2, TUG3 #2. When ERDI is set high, extended RDI is selected. The RDI and RFI indications to the TTOP are treated as a 2-bit codepoint. The TTOP block will insert the RDI indication into bit 5 of the Z7 byte and bit 8 of the V5 byte and the RFI indication into bit 6 of the Z7 byte and its complement into bit 7. When ERDI is set low, normal RDI is selected. The RDI and RFI indications are treated independently. TTOP will insert the RDI output into bit 8 of the V5 byte and the RFI output into bit 4 of the V5 byte. The ERDI bit in the TTOP must be configured the same as this bit.

RDI:

The RDI bit controls the value of the RDI indication to TTOP when tributary TU #1 in the corresponding TUG2, TUG3 #2 is on the egress data stream. When FORCEEN is set high, the RDI and RFI indications to TTOP are controlled directly by the RDI and RFI register bits. When FORCEEN is set low, the RDI and RFI Indications to TTOP reflect the remote alarm status from the remote alarm source selected via the TRAP Indirect Remote Alarm register.

RFI:

The RFI bit controls the value of the RFI indication to TTOP when tributary TU #1 in the corresponding TUG2, TUG3 #2 is on the egress data stream. When FORCEEN is set high, the RDI and RFI indications to TTOP are controlled directly by the RDI and RFI register bits. When FORCEEN is set low, the RDI and RFI Indications to TTOP reflect the remote alarm status from the remote alarm source selected via the TRAP Indirect Remote Alarm register.

FORCEEN:

The FORCEEN bit combined with the RFI and RDI register bits controls the RDI and RFI indications to TTOP. When FORCEEN is high the RDI and RFI indications to TTOP are controlled directly by the RDI and RFI register bits. When FORCEEN is set low the RDI and RFI indications reflect the remote alarm status from the remote alarm source selected via the TRAP Indirect Remote Alarm registers.

TU11:

The TU11 bit specifies the tributary configuration of the corresponding TUG2 tributary group in TUG3 #2. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMAP.

Register 14A7: TRAP TU #1 in TUG2 #1 to TUG2 #7 of TUG3 #2, Egress AIS Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	EAIS7	0
Bit 5	R/W	EAIS6	0
Bit 4	R/W	EAIS5	0
Bit 3	R/W	EAIS4	0
Bit 2	R/W	EAIS3	0
Bit 1	R/W	EAIS2	0
Bit 0	R/W	EAIS1	0

This register controls the insertion of AIS when tributary TU #1 of TUG2 #1, TUG3 #2 to TU#1 of TUG2 #7, TUG3 #2 are on the egress data stream.

EAIS7 – EAIS1:

The EAIS1 to EAIS7 bits control the state of the AIS insertion when tributary TU #1 of TUG2 #1, TUG3 #2 to TUG2 #7, TUG3 #2, respectively, are on the egress data stream. When EAIS*x* is set high, tributary path AIS is inserted in the associated tributary of the egress data stream. When EAIS*x* is set low, tributary path AIS is not forced in the associated tributary of the egress data stream although tributary path AIS may still be inserted due to other alarm conditions.

Register 14A8H, 14A9H, 14AAH, 14ABH, 14ACH, 14ADH, 14AEH: TRAP TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #2, Control

Bit	Type	Function	Default
Bit 7	R	Reserved	1
Bit 6	R	TU11	1
Bit 5		Unused	X
Bit 4	R/W	FORCEEN	0
Bit 3	R/W	RFI	0
Bit 2	R/W	RDI	0
Bit 1	R/W	ERDI	0
Bit 0	R/W	POHDIS	0

This register configures the operational modes of TU #2 of TUG2 #1, TUG3 #2 to TU #2 of TUG2 #7, TUG3 #2 in the incoming/outgoing egress data stream.

POHDIS:

The POHDIS bit controls the modification of the tributary path overhead bytes when tributary TU #2 in the corresponding TUG2, TUG3 #2 is on the egress data stream. When POHDIS is set high, the tributary path overhead bytes are not modified. This is primarily intended for use with transparent VTs from the SBI bus as configured by the ETVT bit the TTMP block. When POHDIS is set low, the tributary path overhead of TU #2 in the corresponding TUG2, TUG3 #2 is processed normally.

ERDI:

The ERDI bit selects between normal and extended RDI encoding on tributary TU #2 in the corresponding TUG2, TUG3 #2. When ERDI is set high, extended RDI is selected. The RDI and RFI indications to the TTOP are treated as a 2-bit codepoint. The TTOP block will insert the RDI indication into bit 5 of the Z7 byte and bit 8 of the V5 byte and the RFI indication into bit 6 of the Z7 byte and its complement into bit 7. When ERDI is set low, normal RDI is selected. The RDI and RFI indications are treated independently. TTOP will insert the RDI output into bit 8 of the V5 byte and the RFI output into bit 4 of the V5 byte. The ERDI bit in the TTOP must be configured the same as this bit.

RDI:

The RDI bit controls the value of the RDI indication to TTOP when tributary TU #2 in the corresponding TUG2, TUG3 #2 is on the egress data stream. When FORCEEN is set high, the RDI and RFI indications to TTOP are controlled directly by the RDI and RFI register bits. When FORCEEN is set low, the RDI and RFI Indications to TTOP reflect the remote alarm status from the remote alarm source selected via the TRAP Indirect Remote Alarm register.

RFI:

The RFI bit controls the value of the RFI indication to TTOP when tributary TU #2 in the corresponding TUG2, TUG3 #2 is on the egress data stream. When FORCEEN is set high, the RDI and RFI indications to TTOP are controlled directly by the RDI and RFI register bits. When FORCEEN is set low, the RDI and RFI Indications to TTOP reflect the remote alarm status from the remote alarm source selected via the TRAP Indirect Remote Alarm register.

FORCEEN:

The FORCEEN bit combined with the RFI and RDI register bits controls the RDI and RFI indications to TTOP. When FORCEEN is high the RDI and RFI indications to TTOP are controlled directly by the RDI and RFI register bits. When FORCEEN is set low the RDI and RFI indications reflect the remote alarm status from the remote alarm source selected via the TRAP Indirect Remote Alarm registers.

TU11:

The TU11 read only bit reports the tributary configuration written into the corresponding register of TU #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMAP.

Register 14AFH: TRAP TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #2, Egress AIS Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	EAIS7	0
Bit 5	R/W	EAIS6	0
Bit 4	R/W	EAIS5	0
Bit 3	R/W	EAIS4	0
Bit 2	R/W	EAIS3	0
Bit 1	R/W	EAIS2	0
Bit 0	R/W	EAIS1	0

This register controls the insertion of AIS when tributary TU #2 of TUG2 #1, TUG3 #2 to TU#2 of TUG2 #7, TUG3 #2 are on the egress data stream.

EAIS7 – EAIS1:

The EAIS1 to EAIS7 bits control the state of the AIS insertion when tributary TU #2 of TUG2 #1, TUG3 #2 to TUG2 #7, TUG3 #2, respectively, are on the egress data stream. When EAIS*x* is set high, tributary path AIS is inserted in the associated tributary of the egress data stream. When EAIS*x* is set low, tributary path AIS is not forced in the associated tributary of the egress data stream although tributary path AIS may still be inserted due to other alarm conditions.

Register 14B0H, 14B1H, 14B2H, 14B3H, 14B4H, 14B5H, 14B6H: TRAP TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #2, Control

Bit	Type	Function	Default
Bit 7	R	Reserved	1
Bit 6	R	TU11	1
Bit 5		Unused	X
Bit 4	R/W	FORCEEN	0
Bit 3	R/W	RFI	0
Bit 2	R/W	RDI	0
Bit 1	R/W	ERDI	0
Bit 0	R/W	POHDIS	0

This register configures the operational modes of TU #3 of TUG2 #1, TUG3 #2 to TU #3 of TUG2 #7, TUG3 #2 in the incoming/outgoing egress data stream.

POHDIS:

The POHDIS bit controls the modification of the tributary path overhead bytes when tributary TU #3 in the corresponding TUG2, TUG3 #2 is on the egress data stream. When POHDIS is set high, the tributary path overhead bytes are not modified. This is primarily intended for use with transparent VTs from the SBI bus as configured by the ETVT bit the TTMP block. When POHDIS is set low, the tributary path overhead of TU #3 in the corresponding TUG2, TUG3 #2 is processed normally.

ERDI:

The ERDI bit selects between normal and extended RDI encoding on tributary TU #3 in the corresponding TUG2, TUG3 #2. When ERDI is set high, extended RDI is selected. The RDI and RFI indications to the TTOP are treated as a 2-bit codepoint. The TTOP block will insert the RDI indication into bit 5 of the Z7 byte and bit 8 of the V5 byte and the RFI indication into bit 6 of the Z7 byte and its complement into bit 7. When ERDI is set low, normal RDI is selected. The RDI and RFI indications are treated independently. TTOP will insert the RDI output into bit 8 of the V5 byte and the RFI output into bit 4 of the V5 byte. The ERDI bit in the TTOP must be configured the same as this bit.

RDI:

The RDI bit controls the value of the RDI indication to TTOP when tributary TU #3 in the corresponding TUG2, TUG3 #2 is on the egress data stream. When FORCEEN is set high, the RDI and RFI indications to TTOP are controlled directly by the RDI and RFI register bits. When FORCEEN is set low, the RDI and RFI Indications to TTOP reflect the remote alarm status from the remote alarm source selected via the TRAP Indirect Remote Alarm register.

RFI:

The RFI bit controls the value of the RFI indication to TTOP when tributary TU #3 in the corresponding TUG2, TUG3 #2 is on the egress data stream. When FORCEEN is set high, the RDI and RFI indications to TTOP are controlled directly by the RDI and RFI register bits. When FORCEEN is set low, the RDI and RFI Indications to TTOP reflect the remote alarm status from the remote alarm source selected via the TRAP Indirect Remote Alarm register.

FORCEEN:

The FORCEEN bit combined with the RFI and RDI register bits controls the RDI and RFI indications to TTOP. When FORCEEN is high the RDI and RFI indications to TTOP are controlled directly by the RDI and RFI register bits. When FORCEEN is set low the RDI and RFI indications reflect the remote alarm status from the remote alarm source selected via the TRAP Indirect Remote Alarm registers.

TU11:

The TU11 read only bit reports the tributary configuration written into the corresponding register of TU #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMAP.

Register 14B7H: TRAP TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #2, Egress AIS Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	EAIS7	0
Bit 5	R/W	EAIS6	0
Bit 4	R/W	EAIS5	0
Bit 3	R/W	EAIS4	0
Bit 2	R/W	EAIS3	0
Bit 1	R/W	EAIS2	0
Bit 0	R/W	EAIS1	0

This register controls the insertion of AIS when tributary TU #3 of TUG2 #1, TUG3 #2 to TU#3 of TUG2 #7, TUG3 #2 are on the egress data stream.

EAIS7 – EAIS1:

The EAIS1 to EAIS7 bits control the state of the AIS insertion when tributary TU #3 of TUG2 #1, TUG3 #2 to TUG2 #7, TUG3 #2, respectively, are on the egress data stream. When EAIS*x* is set high, tributary path AIS is inserted in the associated tributary of the egress data stream. When EAIS*x* is set low, tributary path AIS is not forced in the associated tributary of the egress data stream although tributary path AIS may still be inserted due to other alarm conditions.

Register 14B8H, 14B9H, 14BAH, 14BBH, 14BCH, 14BDH, 14BEH: TRAP TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #2, Control

Bit	Type	Function	Default
Bit 7	R	Reserved	1
Bit 6	R	TU11	1
Bit 5		Unused	X
Bit 4	R/W	FORCEEN	0
Bit 3	R/W	RFI	0
Bit 2	R/W	RDI	0
Bit 1	R/W	ERDI	0
Bit 0	R/W	POHDIS	0

This register configures the operational modes of TU #4 of TUG2 #1, TUG3 #2 to TU #4 of TUG2 #7, TUG3 #2 in the incoming/outgoing egress data stream. When the corresponding TUG2 tributary group is configured to TU12 (VT2) mode, the associated register in this set has no effect.

POHDIS:

The POHDIS bit controls the modification of the tributary path overhead bytes when tributary TU #4 in the corresponding TUG2, TUG3 #2 is on the egress data stream. When POHDIS is set high, the tributary path overhead bytes are not modified. This is primarily intended for use with transparent VTs from the SBI bus as configured by the ETVT bit the TTMP block. When POHDIS is set low, the tributary path overhead of TU #4 in the corresponding TUG2, TUG3 #2 is processed normally.

ERDI:

The ERDI bit selects between normal and extended RDI encoding on tributary TU #4 in the corresponding TUG2, TUG3 #2. When ERDI is set high, extended RDI is selected. The RDI and RFI indications to the TTOP are treated as a 2-bit codepoint. The TTOP block will insert the RDI indication into bit 5 of the Z7 byte and bit 8 of the V5 byte and the RFI indication into bit 6 of the Z7 byte and its complement into bit 7. When ERDI is set low, normal RDI is selected. The RDI and RFI indications are treated independently. TTOP will insert the RDI output into bit 8 of the V5 byte and the RFI output into bit 4 of the V5 byte. The ERDI bit in the TTOP must be configured the same as this bit.

RDI:

The RDI bit controls the value of the RDI indication to TTOP when tributary TU #4 in the corresponding TUG2, TUG3 #2 is on the egress data stream. When FORCEEN is set high, the RDI and RFI indications to TTOP are controlled directly by the RDI and RFI register bits. When FORCEEN is set low, the RDI and RFI Indications to TTOP reflect the remote alarm status from the remote alarm source selected via the TRAP Indirect Remote Alarm register.

RFI:

The RFI bit controls the value of the RFI indication to TTOP when tributary TU #4 in the corresponding TUG2, TUG3 #2 is on the egress data stream. When FORCEEN is set high, the RDI and RFI indications to TTOP are controlled directly by the RDI and RFI register bits. When FORCEEN is set low, the RDI and RFI Indications to TTOP reflect the remote alarm status from the remote alarm source selected via the TRAP Indirect Remote Alarm register.

FORCEEN:

The FORCEEN bit combined with the RFI and RDI register bits controls the RDI and RFI indications to TTOP. When FORCEEN is high the RDI and RFI indications to TTOP are controlled directly by the RDI and RFI register bits. When FORCEEN is set low the RDI and RFI indications reflect the remote alarm status from the remote alarm source selected via the TRAP Indirect Remote Alarm registers.

TU11:

The TU11 read only bit reports the tributary configuration written into the corresponding register of TU #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMAP.

Register 14BFH: TRAP TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #2, Egress AIS Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	EAIS7	0
Bit 5	R/W	EAIS6	0
Bit 4	R/W	EAIS5	0
Bit 3	R/W	EAIS4	0
Bit 2	R/W	EAIS3	0
Bit 1	R/W	EAIS2	0
Bit 0	R/W	EAIS1	0

This register controls the insertion of AIS when tributary TU #4 of TUG2 #1, TUG3 #2 to TU#4 of TUG2 #7, TUG3 #2 are on the egress data stream. When the corresponding TUG2 tributary group is configured to TU12 (VT2) mode, this register has no effect.

EAIS7 – EAIS1:

The EAIS1 to EAIS7 bits control the state of the AIS insertion when tributary TU #4 of TUG2 #1, TUG3 #2 to TUG2 #7, TUG3 #2, respectively, are on the egress data stream. When EAIS*x* is set high, tributary path AIS is inserted in the associated tributary of the egress data stream. When EAIS*x* is set low, tributary path AIS is not forced in the associated tributary of the egress data stream although tributary path AIS may still be inserted due to other alarm conditions.

Register 14C0H, 14C1H, 14C2H, 14C3H, 14C4H, 14C5H, 14C6H: TRAP TU #1 in TUG2 #1 to TUG2 #7 of TUG3 #3, Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	1
Bit 6	R/W	TU11	1
Bit 5		Unused	X
Bit 4	R/W	FORCEEN	0
Bit 3	R/W	RFI	0
Bit 2	R/W	RDI	0
Bit 1	R/W	ERDI	0
Bit 0	R/W	POHDIS	0

This register configures the operational modes of TU #1 of TUG2 #1, TUG3 #3 to TU #1 of TUG2 #7, TUG3 #3 in the incoming/outgoing egress data stream.

POHDIS:

The POHDIS bit controls the modification of the tributary path overhead bytes when tributary TU #1 in the corresponding TUG2, TUG3 #3is on the egress data stream. When POHDIS is set high, the tributary path overhead bytes are not modified. This is primarily intended for use with transparent VTs from the SBI bus as configured by the ETVT bit the TTMP block. When POHDIS is set low, the tributary path overhead of TU #1 in the corresponding TUG2, TUG3 #3 is processed normally.

ERDI:

The ERDI bit selects between normal and extended RDI encoding on tributary TU #1 in the corresponding TUG2, TUG3 #3 When ERDI is set high, extended RDI is selected. The RDI and RFI indications to the TTOP are treated as a 2-bit codepoint. The TTOP block will insert the RDI indication into bit 5 of the Z7 byte and bit 8 of the V5 byte and the RFI indication into bit 6 of the Z7 byte and its complement into bit 7. When ERDI is set low, normal RDI is selected. The RDI and RFI indications are treated independently. TTOP will insert the RDI output into bit 8 of the V5 byte and the RFI output into bit 4 of the V5 byte. The ERDI bit in the TTOP must be configured the same as this bit.

RDI:

The RDI bit controls the value of the RDI indication to TTOP when tributary TU #1 in the corresponding TUG2, TUG3 #3is on the egress data stream. When FORCEEN is set high, the RDI and RFI indications to TTOP are controlled directly by the RDI and RFI register bits. When FORCEEN is set low, the RDI and RFI Indications to TTOP reflect the remote alarm status from the remote alarm source selected via the TRAP Indirect Remote Alarm register.

RFI:

The RFI bit controls the value of the RFI indication to TTOP when tributary TU #1 in the corresponding TUG2, TUG3 #3is on the egress data stream. When FORCEEN is set high, the RDI and RFI indications to TTOP are controlled directly by the RDI and RFI register bits. When FORCEEN is set low, the RDI and RFI Indications to TTOP reflect the remote alarm status from the remote alarm source selected via the TRAP Indirect Remote Alarm register.

FORCEEN:

The FORCEEN bit combined with the RFI and RDI register bits controls the RDI and RFI indications to TTOP. When FORCEEN is high the RDI and RFI indications to TTOP are controlled directly by the RDI and RFI register bits. When FORCEEN is set low the RDI and RFI indications reflect the remote alarm status from the remote alarm source selected via the TRAP Indirect Remote Alarm registers.

TU11:

The TU11 bit specifies the tributary configuration of the corresponding TUG2 tributary group in TUG3 #3. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMAP.

Register 14C7H: TRAP TU #1 in TUG2 #1 to TUG2 #7 of TUG3 #3, Egress AIS Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	EAIS7	0
Bit 5	R/W	EAIS6	0
Bit 4	R/W	EAIS5	0
Bit 3	R/W	EAIS4	0
Bit 2	R/W	EAIS3	0
Bit 1	R/W	EAIS2	0
Bit 0	R/W	EAIS1	0

This register controls the insertion of AIS when tributary TU #1of TUG2 #1, TUG3 #3 to TU#1 of TUG2 #7, TUG3 #3 are on the egress data stream.

EAIS7 – EAIS1:

The EAIS1 to EAIS7 bits control the state of the AIS insertion when tributary TU #1 of TUG2 #1, TUG3 #3 to TUG2 #7, TUG3 #3, respectively, are on the egress data stream. When EAIS*x* is set high, tributary path AIS is inserted in the associated tributary of the egress data stream. When EAIS*x* is set low, tributary path AIS is not forced in the associated tributary of the egress data stream although tributary path AIS may still be inserted due to other alarm conditions.

Register 14C8H, 14C9H, 14CAH, 14CBH, 14CCH, 14CDH, 14CEH: TRAP TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #3, Control

Bit	Type	Function	Default
Bit 7	R	Reserved	1
Bit 6	R	TU11	1
Bit 5		Unused	X
Bit 4	R/W	FORCEEN	0
Bit 3	R/W	RFI	0
Bit 2	R/W	RDI	0
Bit 1	R/W	ERDI	0
Bit 0	R/W	POHDIS	0

This register configures the operational modes of TU #2 of TUG2 #1, TUG3 #3 to TU #2 of TUG2 #7, TUG3 #3 in the incoming/outgoing egress data stream.

POHDIS:

The POHDIS bit controls the modification of the tributary path overhead bytes when tributary TU #2 in the corresponding TUG2, TUG3 #3 is on the egress data stream. When POHDIS is set high, the tributary path overhead bytes are not modified. This is primarily intended for use with transparent VTs from the SBI bus as configured by the ETVT bit the TTMP block. When POHDIS is set low, the tributary path overhead of TU #2 in the corresponding TUG2, TUG3 #3 is processed normally.

ERDI:

The ERDI bit selects between normal and extended RDI encoding on tributary TU #2 in the corresponding TUG2, TUG3 #3 When ERDI is set high, extended RDI is selected. The RDI and RFI indications to the TTOP are treated as a 2-bit codepoint. The TTOP block will insert the RDI indication into bit 5 of the Z7 byte and bit 8 of the V5 byte and the RFI indication into bit 6 of the Z7 byte and its complement into bit 7. When ERDI is set low, normal RDI is selected. The RDI and RFI indications are treated independently. TTOP will insert the RDI output into bit 8 of the V5 byte and the RFI output into bit 4 of the V5 byte. The ERDI bit in the TTOP must be configured the same as this bit.

RDI:

The RDI bit controls the value of the RDI indication to TTOP when tributary TU #2 in the corresponding TUG2, TUG3 #3 is on the egress data stream. When FORCEEN is set high, the RDI and RFI indications to TTOP are controlled directly by the RDI and RFI register bits. When FORCEEN is set low, the RDI and RFI Indications to TTOP reflect the remote alarm status from the remote alarm source selected via the TRAP Indirect Remote Alarm register.

RFI:

The RFI bit controls the value of the RFI indication to TTOP when tributary TU #2 in the corresponding TUG2, TUG3 #3 is on the egress data stream. When FORCEEN is set high, the RDI and RFI indications to TTOP are controlled directly by the RDI and RFI register bits. When FORCEEN is set low, the RDI and RFI Indications to TTOP reflect the remote alarm status from the remote alarm source selected via the TRAP Indirect Remote Alarm register.

FORCEEN:

The FORCEEN bit combined with the RFI and RDI register bits controls the RDI and RFI indications to TTOP. When FORCEEN is high the RDI and RFI indications to TTOP are controlled directly by the RDI and RFI register bits. When FORCEEN is set low the RDI and RFI indications reflect the remote alarm status from the remote alarm source selected via the TRAP Indirect Remote Alarm registers.

TU11:

The TU11 read only bit reports the tributary configuration written into the corresponding register of TU #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMAP.

Register 14CFH: TRAP TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #3, Egress AIS Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	EAIS7	0
Bit 5	R/W	EAIS6	0
Bit 4	R/W	EAIS5	0
Bit 3	R/W	EAIS4	0
Bit 2	R/W	EAIS3	0
Bit 1	R/W	EAIS2	0
Bit 0	R/W	EAIS1	0

This register controls the insertion of AIS when tributary TU #2of TUG2 #1, TUG3 #3 to TU#2 of TUG2 #7, TUG3 #3 are on the egress data stream.

EAIS7 – EAIS1:

The EAIS1 to EAIS7 bits control the state of the AIS insertion when tributary TU #2 of TUG2 #1, TUG3 #3 to TUG2 #7, TUG3 #3, respectively, are on the egress data stream. When EAIS*x* is set high, tributary path AIS is inserted in the associated tributary of the egress data stream. When EAIS*x* is set low, tributary path AIS is not forced in the associated tributary of the egress data stream although tributary path AIS may still be inserted due to other alarm conditions.

Register 14D0H, 14D1H, 14D2H, 14D3H, 14D4H, 14D5H, 14D6H: TRAP TU #3 in TUG2 #1 toTUG2 #7 of TUG3 #3, Control

Bit	Type	Function	Default
Bit 7	R	Reserved	1
Bit 6	R	TU11	1
Bit 5		Unused	X
Bit 4	R/W	FORCEEN	0
Bit 3	R/W	RFI	0
Bit 2	R/W	RDI	0
Bit 1	R/W	ERDI	0
Bit 0	R/W	POHDIS	0

This register configures the operational modes of TU #3 of TUG2 #1, TUG3 #3 to TU #3 of TUG2 #7, TUG3 #3 in the incoming/outgoing egress data stream.

POHDIS:

The POHDIS bit controls the modification of the tributary path overhead bytes when tributary TU #3 in the corresponding TUG2, TUG3 #3 is on the egress data stream. When POHDIS is set high, the tributary path overhead bytes are not modified. This is primarily intended for use with transparent VTs from the SBI bus as configured by the ETVT bit the TTMP block. When POHDIS is set low, the tributary path overhead of TU #3 in the corresponding TUG2, TUG3 #3 is processed normally.

ERDI:

The ERDI bit selects between normal and extended RDI encoding on tributary TU #3 in the corresponding TUG2, TUG3 #3 When ERDI is set high, extended RDI is selected. The RDI and RFI indications to the TTOP are treated as a 2-bit codepoint. The TTOP block will insert the RDI indication into bit 5 of the Z7 byte and bit 8 of the V5 byte and the RFI indication into bit 6 of the Z7 byte and its complement into bit 7. When ERDI is set low, normal RDI is selected. The RDI and RFI indications are treated independently. TTOP will insert the RDI output into bit 8 of the V5 byte and the RFI output into bit 4 of the V5 byte. The ERDI bit in the TTOP must be configured the same as this bit.

RDI:

The RDI bit controls the value of the RDI indication to TTOP when tributary TU #3 in the corresponding TUG2, TUG3 #3 is on the egress data stream. When FORCEEN is set high, the RDI and RFI indications to TTOP are controlled directly by the RDI and RFI register bits. When FORCEEN is set low, the RDI and RFI Indications to TTOP reflect the remote alarm status from the remote alarm source selected via the TRAP Indirect Remote Alarm register.

RFI:

The RFI bit controls the value of the RFI indication to TTOP when tributary TU #3 in the corresponding TUG2, TUG3 #3 is on the egress data stream. When FORCEEN is set high, the RDI and RFI indications to TTOP are controlled directly by the RDI and RFI register bits. When FORCEEN is set low, the RDI and RFI Indications to TTOP reflect the remote alarm status from the remote alarm source selected via the TRAP Indirect Remote Alarm register.

FORCEEN:

The FORCEEN bit combined with the RFI and RDI register bits controls the RDI and RFI indications to TTOP. When FORCEEN is high the RDI and RFI indications to TTOP are controlled directly by the RDI and RFI register bits. When FORCEEN is set low the RDI and RFI indications reflect the remote alarm status from the remote alarm source selected via the TRAP Indirect Remote Alarm registers.

TU11:

The TU11 read only bit reports the tributary configuration written into the corresponding register of TU #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMAP.

Register 14D7H: TRAP TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #3, Egress AIS Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	EAIS7	0
Bit 5	R/W	EAIS6	0
Bit 4	R/W	EAIS5	0
Bit 3	R/W	EAIS4	0
Bit 2	R/W	EAIS3	0
Bit 1	R/W	EAIS2	0
Bit 0	R/W	EAIS1	0

This register controls the insertion of AIS when tributary TU #3of TUG2 #1, TUG3 #3 to TU#3 of TUG2 #7, TUG3 #3 are on the egress data stream.

EAIS7 – EAIS1:

The EAIS1 to EAIS7 bits control the state of the AIS insertion when tributary TU #3 of TUG2 #1, TUG3 #3 to TUG2 #7, TUG3 #3, respectively, are on the egress data stream. When EAIS*x* is set high, tributary path AIS is inserted in the associated tributary of the egress data stream. When EAIS*x* is set low, tributary path AIS is not forced in the associated tributary of the egress data stream although tributary path AIS may still be inserted due to other alarm conditions.

Register 14D8H, 14D9H, 14DAH, 14DBH, 14DCH, 14DDH, 14DEH: TRAP TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #3, Control

Bit	Type	Function	Default
Bit 7	R	Reserved	1
Bit 6	R	TU11	1
Bit 5		Unused	X
Bit 4	R/W	FORCEEN	0
Bit 3	R/W	RFI	0
Bit 2	R/W	RDI	0
Bit 1	R/W	ERDI	0
Bit 0	R/W	POHDIS	0

This register configures the operational modes of TU #4 of TUG2 #1, TUG3 #3 to TU #4 of TUG2 #7, TUG3 #3 in the incoming/outgoing egress data stream. When the corresponding TUG2 tributary group is configured to TU12 (VT2) mode, the associated register in this set has no effect.

POHDIS:

The POHDIS bit controls the modification of the tributary path overhead bytes when tributary TU #4 in the corresponding TUG2, TUG3 #3 is on the egress data stream. When POHDIS is set high, the tributary path overhead bytes are not modified. This is primarily intended for use with transparent VTs from the SBI bus as configured by the ETVT bit the TTMP block. When POHDIS is set low, the tributary path overhead of TU #4 in the corresponding TUG2, TUG3 #3 is processed normally.

ERDI:

The ERDI bit selects between normal and extended RDI encoding on tributary TU #4 in the corresponding TUG2, TUG3 #3 When ERDI is set high, extended RDI is selected. The RDI and RFI indications to the TTOP are treated as a 2-bit codepoint. The TTOP block will insert the RDI indication into bit 5 of the Z7 byte and bit 8 of the V5 byte and the RFI indication into bit 6 of the Z7 byte and its complement into bit 7. When ERDI is set low, normal RDI is selected. The RDI and RFI indications are treated independently. TTOP will insert the RDI output into bit 8 of the V5 byte and the RFI output into bit 4 of the V5 byte. The ERDI bit in the TTOP must be configured the same as this bit.

RDI:

The RDI bit controls the value of the RDI indication to TTOP when tributary TU #4 in the corresponding TUG2, TUG3 #3 is on the egress data stream. When FORCEEN is set high, the RDI and RFI indications to TTOP are controlled directly by the RDI and RFI register bits. When FORCEEN is set low, the RDI and RFI Indications to TTOP reflect the remote alarm status from the remote alarm source selected via the TRAP Indirect Remote Alarm register.

RFI:

The RFI bit controls the value of the RFI indication to TTOP when tributary TU #4 in the corresponding TUG2, TUG3 #3 is on the egress data stream. When FORCEEN is set high, the RDI and RFI indications to TTOP are controlled directly by the RDI and RFI register bits. When FORCEEN is set low, the RDI and RFI Indications to TTOP reflect the remote alarm status from the remote alarm source selected via the TRAP Indirect Remote Alarm register.

FORCEEN:

The FORCEEN bit combined with the RFI and RDI register bits controls the RDI and RFI indications to TTOP. When FORCEEN is high the RDI and RFI indications to TTOP are controlled directly by the RDI and RFI register bits. When FORCEEN is set low the RDI and RFI indications reflect the remote alarm status from the remote alarm source selected via the TRAP Indirect Remote Alarm registers.

TU11:

The TU11 read only bit reports the tributary configuration written into the corresponding register of TU #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMAP.

Register 14DFH: TRAP TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #3, Egress AIS Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	EAIS7	0
Bit 5	R/W	EAIS6	0
Bit 4	R/W	EAIS5	0
Bit 3	R/W	EAIS4	0
Bit 2	R/W	EAIS3	0
Bit 1	R/W	EAIS2	0
Bit 0	R/W	EAIS1	0

This register controls the insertion of AIS when tributary TU #4 of TUG2 #1, TUG3 #3 to TU#4 of TUG2 #7, TUG3 #3 are on the egress data stream. When the corresponding TUG2 tributary group is configured to TU12 (VT2) mode, this register has no effect.

EAIS7 – EAIS1:

The EAIS1 to EAIS7 bits control the state of the AIS insertion when tributary TU #4 of TUG2 #1, TUG3 #3 to TUG2 #7, TUG3 #3, respectively, are on the egress data stream. When EAIS*x* is set high, tributary path AIS is inserted in the associated tributary of the egress data stream. When EAIS*x* is set low, tributary path AIS is not forced in the associated tributary of the egress data stream although tributary path AIS may still be inserted due to other alarm conditions.

Register 14E0H: TRAP Indirect Remote Alarm Page Address

Bit	Type	Function	Default
Bit 7	R	BUSY	X
Bit 6	R/W	RWB	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	RASEL[1]	0
Bit 0	R/W	RASEL[0]	0

This register selects the remote alarm port page used to access the ARBITER look-up table used to selects which incoming alarm source is used to generate an egress RDI, RFI or REI. Writing to this register triggers an indirect look-up table access.

RASEL[1:0]:

The RASEL[1:0] bits indexes into one of three pages in the ARBITER look-up table. The pages specified by the RASEL[1:0] bits are selected as follows:

RASEL[1]	RASEL[0]	Remote Alarm Source
0	0	Reserved
0	1	RADEAST Serial Alarm Port
1	0	RADWEST Serial Alarm Port
1	1	RTOP Ingress Data

The priority of the remote alarm source when mapping to an egress alarm indication is the RTOP Ingress data then RADEAST followed by RADWEST. In order for a lower priority alarm source to be selected over a higher priority alarm, the higher priority alarm port entry must be disabled by writing an invalid entry via the TRAP Indirect Datapath Tributary Data register.

RWB:

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the ARBITER look-up table. Writing a logic zero

to RWB triggers an indirect write operation. Data to be written is taken from the Indirect Datapath Tributary Data register. Writing a logic one to RWB triggers an indirect read operation. The read can be found in the Indirect Datapath Tributary Data register.

BUSY:

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set high when a write to the Indirect Remote Alarm Port Select register triggers an indirect access and will stay high until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the Indirect Datapath Tributary Select Data register or to determine when a new indirect write operation may commence. If LREFCLK disappears during an access, the BUSY bit can stay high.

Register 14E1H: TRAP Indirect Remote Alarm Tributary

Bit	Type	Function	Default
Bit 7	R/W	RTUG3[1]	0
Bit 6	R/W	RTUG3[0]	0
Bit 5	R/W	RTUG2[2]	0
Bit 4	R/W	RTUG2[1]	0
Bit 3	R/W	RTUG2[0]	0
Bit 2	R/W	RTU[2]	0
Bit 1	R/W	RTU[1]	0
Bit 0	R/W	RTU[0]	0

This register provides the remote alarm tributary number used to access the ARBITER look-up table.

RTU[2:0]:

The indirect remote alarm tributary unit bits (RTU[2:0]) indicate the tributary unit to be configured or interrogated in the indirect access. Legal RTU[2:0] ranges are ‘b001 to ‘b100.

RTUG2[2:0]:

The indirect remote alarm tributary unit group 2 bits (RTUG2[2:0]) indicate the tributary unit group 2 to be configured or interrogated in the indirect access. Legal RTUG2[2:0] ranges are ‘b001 to ‘b111.

RTUG3[1:0]:

The indirect remote alarm tributary unit group 3 bits (RTUG2[1:0]) indicate the tributary unit group 3 to be configured or interrogated in the indirect access. Legal RTUG3[1:0] ranges are ‘b01 to ‘b11.

Register 14E2H: TRAP Indirect Datapath Tributary

Bit	Type	Function	Default
Bit 7	R/W	DTUG3[1]	0
Bit 6	R/W	DTUG3[0]	0
Bit 5	R/W	DTUG2[2]	0
Bit 4	R/W	DTUG2[1]	0
Bit 3	R/W	DTUG2[0]	0
Bit 2	R/W	DTU[2]	0
Bit 1	R/W	DTU[1]	0
Bit 0	R/W	DTU[0]	0

This register contains data read from the ARBITER look-up tables after an indirect channel read operation or data to be inserted into the ARBITER look-up table in an indirect channel write operation.

Please note that if a particular datapath tributary is not mapped to a remote alarm tributary, as set by via Register 14E1H: TRAP Indirect Remote Alarm Tributary, it is recommended the desired alarm values be set manually. This can be accomplished using the FORCEEN bit in the following registers:

Register 1480H: TRAP TU #1 in TUG2 #1 of TUG3 #1, Control

Registers 1481H, 1482H, 1483H, 1484H, 1485H, 1486H: TRAP TU #1 in TUG2 #2 to TUG2 #7 of TUG3 #1, Control

Registers 1488H, 1489H, 148AH, 148BH, 148CH, 148DH, 148EH: TRAP TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #1, Control

Registers 1490H, 1491H, 1492H, 1493H, 1494H, 1495H, 1496H: TRAP TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #1 Control

Registers 1498H, 1499H, 149AH, 149BH, 149CH, 149DH, 149EH: TRAP TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #1, Control

Registers 14A0H, 14A1H, 14A2H, 14A3H, 14A4H, 14A5H, 14A6H: TRAP TU #1 in TUG2 #1 to TUG2 #7 of TUG3 #2, Control

Registers 14A8H, 14A9H, 14AAH, 14ABH, 14ACH, 14ADH, 14AEH: TRAP TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #2, Control

Registers 14B0H, 14B1H, 14B2H, 14B3H, 14B4H, 14B5H, 14B6H: TRAP TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #2, Control

Registers 14B8H, 14B9H, 14BAH, 14BBH, 14BCH, 14BDH, 14BEH: TRAP TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #2, Control

Registers 14C0H, 14C1H, 14C2H, 14C3H, 14C4H, 14C5H, 14C6H: TRAP TU #1 in TUG2 #1 to TUG2 #7 of TUG3 #3, Control

Registers 14C8H, 14C9H, 14CAH, 14CBH, 14CCH, 14CDH, 14CEH: TRAP TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #3, Control

Registers 14D0H, 14D1H, 14D2H, 14D3H, 14D4H, 14D5H, 14D6H: TRAP TU #3 in TUG2 #1 toTUG2 #7 of TUG3 #3, Control

Registers 14D8H, 14D9H, 14DAH, 14DBH, 14DCH, 14DDH, 14DEH: TRAP TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #3, Control

DTU[1:0]:

The indirect datapath tributary unit bits (DTU[2:0]) specifies the tributary number of the datapath tributary that is associated with the remote alarm tributary specified in the Indirect Remote Alarm Page Address register and the Indirect Remote Alarm Tributary Address register. In an indirect write operation, the datapath tributary number to be written to the ARBITER look-up table must be set up in this register before triggering the indirect write. When read back, DTU[2:0] reflects the value written until the completion of a subsequent indirect channel read operation. Normal DTU[2:0] ranges are ‘b001 to ‘b100. Values outside of this range disable the remote alarm tributary specified in the Indirect Remote Alarm Page Address register and the Indirect Remote Alarm Tributary Address register from being associated with a datapath tributary.

DTUG2[2:0]:

The indirect datapath tributary unit group 2 bits (DTUG2[2:0]) specifies the tributary unit group 2 number of the datapath tributary that is associated with the remote alarm tributary specified in the Indirect Remote Alarm Page Address register and the Indirect Remote Alarm Tributary Address register. In an indirect write operation, the datapath tributary unit 2 number to be written to the ARBITER look-up table must be set up in this register before triggering the indirect write. When read back, DTUG2[2:0] reflects the value written until the completion of a subsequent indirect channel read operation. Legal DTUG2[2:0] ranges are ‘b001 to ‘b111.

DTUG3[1:0]:

The indirect datapath tributary unit group 3 bits (DTUG3[2:0]) specifies the tributary unit group 3 number of the datapath tributary that is associated with the remote alarm tributary specified in the Indirect Remote Alarm Page Address register and the Indirect Remote Alarm Tributary Address register. In an indirect write operation, the datapath tributary unit 3 number to be written to the ARBITER look-up table must be set up in this register before triggering the indirect write. When read back, DTUG2[1:0] reflects the value written until the completion of a subsequent indirect channel read operation. Legal DTUG3[1:0] ranges are ‘b01 to ‘b11.

Register 14E3H: TRAP RDI Control

Bit	Type	Function	Default
Bit 7	R/W	RDIPRIA[1]	0
Bit 6	R/W	RDIPRIA[0]	0
Bit 5	R/W	RDIPRIB[1]	0
Bit 4	R/W	RDIPRIB[0]	0
Bit 3		Unused	X
Bit 2	R/W	RDI20MF[3]	0
Bit 1	R/W	RDI20MF[2]	0
Bit 0	R/W	RDI20MF[1]	0

This register allows configuration of two-bit alarm code point priority in ERDI for all tributaries. Also configures the maintenance of RDI for each TUG3.

RDI20MF[3:1]

The RDI20MF[3:1] bits specify the configuration of RDI maintenance duration for each of the three TUG3s. The standard required duration is 10 multiframes. The GR-253 objective duration is 20 multiframes. RDI20MF[X] controls the configuration of TUG3 #X. The two options for each TUG3 specified by the RDI20MF[3:1] bits are selected as follows:

RDI20MF[X]	Configuration
0	A particular RDI value for TUG3 #X will be maintained for the required 10 multiframes.
1	A particular RDI value for TUG3 #X will be maintained for the GR-253 objective 20 multiframes.

RDIPRIA[1:0]

The RDIPRIA[1:0] bits specify which two-bit alarm code point will be treated as the highest priority code. High priority codes will replace low priority codes at the next V5 byte, instead of allowing 10/20 copies to be sent. The highest priority alarm is sent 10/20 times before replacement is allowed.

RDIPRIB[1:0]

The RDIPRIB[1:0] bits specify which two-bit alarm code point will be treated as the second highest priority code. These bits combined with the RDIPRIA[1:0] bits allow almost any priority scheme to be specified. The bits are interpreted as follows:

RDIPRIA[1:0]	RDIPRIB[1:0]	Priority of Codes (3 = highest)	
		Code	Priority
00	00	11	1
		10	1
		01	1
		00	0
00	01	01	2
01	00	11	1
01	01	10	1
		00	0
00	10	10	2
10	00	11	1
10	10	01	1
		00	0
00	11	11	2
11	00	10	1
11	11	01	1
		00	0
11	01	11	3
		01	2
		10	1
		00	0
11	10	11	3
		10	2
		01	1

10	11	00	0
		10	3
		11	2
		01	1
		00	0
10	01	10	3
		01	2
		10	1
		00	0
01	11	01	3
		11	2
		10	1
		00	0
01	10	01	3
		10	2
		01	1
		00	0

Register 14E8H: TRAP Remote Parallel Alarm Port TUG2 #1 of TUG3 #1 Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	1
Bit 6	R/W	TU11	1
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register configures the operational modes of TUG2 #1, TUG3 #1 in the RTOP ingress data alarm port.

TU11:

The TU11 bit specifies the tributary configuration of tributary group TUG2 #1, TUG3 #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMAP.

Register14E9H, 14EAH, 14EBH, 14ECH, 14EDH, 14EEH: TRAP Remote Parallel Alarm Port TUG2 #2 to TUG2 #7 of TUG3 #1 Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	1
Bit 6	R/W	TU11	1
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register configures the operational modes of TUG2 #2, TUG3 #1 to TUG2 #7, TUG3 #1 in the RTOP ingress data alarm port.

TU11:

The TU11 bit specifies the tributary configuration of the corresponding TUG2 tributary group in TUG3 #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMAP.

Register 14F0H, 14F1H, 14F2H, 14F3H, 14F4H, 14F5H, 14F6H: TRAP Remote Parallel Alarm Port TUG2 #1 to TUG2 #7 of TUG3 #2 Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	1
Bit 6	R/W	TU11	1
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register configures the operational modes of TUG2 #1, TUG3 #2 to TUG2 #7, TUG3 #2 in the RTOP ingress data alarm port.

TU11:

The TU11 bit specifies the tributary configuration of the corresponding TUG2 tributary group in TUG3 #2. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMAP.

Register 14F8H, 14F9H, 14FAH, 14FBH, 14FCH, 14FDH, 14FEH: TRAP Remote Parallel Alarm Port TUG2 #1 to TUG2 #7 of TUG3 #3 Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	1
Bit 6	R/W	TU11	1
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register configures the operational modes of TUG2 #1, TUG3 #3 to TUG2 #7, TUG3 #3 in the RTOP ingress data alarm port.

TU11:

The TU11 bit specifies the tributary configuration of the corresponding TUG2 tributary group in TUG3 #3. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMAP.

1.28 TTOP Transmit Tributary Path Overhead Processor Registers

Register 1500H: TTOP TU #1 in TUG2 #1 of TUG3 #1, Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	1
Bit 6	R/W	TU11	1
Bit 5	R/W	PSL[2]	0
Bit 4	R/W	PSL[1]	1
Bit 3	R/W	PSL[0]	0
Bit 2	R/W	TTIEN	1
Bit 1	R/W	ERDI	0
Bit 0	R/W	IDLE	0

This register configures the operational modes of TU #1 of TUG2 #1, TUG3 #1.

IDLE:

The IDLE bit enables insertion of tributary idle on tributary TU #1 of TUG2 #1, TUG3 #1. When IDLE is set high, the egress tributary payload bytes are set to all-zeros or all-ones as selected by the ICODE register bit in the TTOP TUG3 #1 Control register at address 1560H. The outgoing active offset is forced to zero. When IDLE is set low, tributary TU #1 of TUG2 #1, TUG3 #1 is processed normally.

ERDI:

The ERDI bit selects between normal and extended RDI encoding on tributary TU #1 of TUG2 #1, TUG3 #1. When ERDI is set high, extended RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 5 of the Z7 byte and bit 8 of the V5 byte. The value of the RFI indication from TRAP is inserted into bit 6 of the Z7 byte and its complement into bit 7. Bit 4 of the V5 byte is set low. When ERDI is set low, normal RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 8 of the V5 byte. The value on the RFI indication from TRAP is inserted into bit 4 of the V5.

TTIEN:

The TTIEN bit enables insertion of trial trace identifier into tributary TU #1 of TUG2 #1, TUG3 #1. When TTIEN is set high, trail trace identifier insertion is

enabled. When TTIEN is set low, trail trace identifier insertion is disabled. The J2 byte is unused and will be set to all-zeros or all-ones as controlled by the UPOHV register bit.

PSL[2:0]:

The PSL[2:0] bits control the path signal label inserted into the PSL field of the V5 byte of tributary TU #1 of TUG2 #1, TUG3 #1. PSL[2] is inserted into bit 5, PSL[1] into bit 6 and PSL[0] into bit 7 of the V5 byte. The default value of ‘b010 denotes asynchronous mapping of payload into the tributary.

TU11:

The TU11 bit specifies the tributary configuration of tributary group TUG2 #1, TUG3 #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMAP.

Register 1501H, 1502H, 1503H, 1504H, 1505H, 1506H: TTOP TU #1 in TUG2 #2 to TUG2 #7 of TUG3 #1, Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	1
Bit 6	R/W	TU11	1
Bit 5	R/W	PSL[2]	0
Bit 4	R/W	PSL[1]	1
Bit 3	R/W	PSL[0]	0
Bit 2	R/W	TTIEN	1
Bit 1	R/W	ERDI	0
Bit 0	R/W	IDLE	0

This register configures the operational modes of TU #1 of TUG2 #2, TUG3 #1 to TU #1 of TUG2 #7, TUG3 #1.

IDLE:

The IDLE bit enables insertion of tributary idle on tributary TU #1 in the corresponding TUG2, TUG3 #1. When IDLE is set high, the egress tributary payload bytes are set to all-zeros or all-ones as selected by the ICODE register bit. The outgoing active offset is forced to zero. When IDLE is set low, tributary TU #1 in the corresponding TUG2, TUG3 #1 is processed normally.

ERDI:

The ERDI bit selects between normal and extended RDI encoding on tributary TU #1 in the corresponding TUG2, TUG3 #1. When ERDI is set high, extended RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 5 of the Z7 byte and bit 8 of the V5 byte. The value on the RFI indication from TRAP is inserted into bit 6 of the Z7 byte and its complement into bit 7. Bit 4 of the V5 byte is set low. When ERDI is set low, normal RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 8 of the V5 byte. The value on the RFI indication from TRAP is inserted into bit 4 of the V5.

TTIEN:

The TTIEN bit enables insertion of trial trace identifier into tributary TU #1 in the corresponding TUG2, TUG3 #1. When TTIEN is set high, trail trace

identifier insertion is enabled. When TTIEN is set low, trail trace identifier insertion is disabled. The J2 byte is unused and will be set to all-zeros or all-ones as controlled by the UPOHV register bit.

PSL[2:0]:

The PSL[2:0] bits control the path signal label inserted into the PSL field of the V5 byte of tributary TU #1 in the corresponding TUG2, TUG3 #1. PSL[2] is inserted into bit 5, PSL[1] into bit 6 and PSL[0] into bit 7 of the V5 byte. The default value of 'b010 denotes asynchronous mapping of payload into the tributary.

TU11:

The TU11 bit specifies the tributary configuration of the corresponding TUG2 tributary group in TUG3 #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMAP.

Register 1507H: TTOP TU #1 in TUG2 #1 to TUG2 #7 of TUG3 #1 BIP Diagnostic Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	DBIP7	0
Bit 5	R/W	DBIP6	0
Bit 4	R/W	DBIP5	0
Bit 3	R/W	DBIP4	0
Bit 2	R/W	DBIP3	0
Bit 1	R/W	DBIP2	0
Bit 0	R/W	DBIP1	0

This register controls the insertion of BIP-2 errors in tributaries TU #1 of TUG2 #1, TUG3 #1 to TU#1 of TUG2 #7, TUG3 #1.

DBIP7 – DBIP1:

The DBIP1 to DBIP7 bits allow diagnosis of downstream receive tributary path processors of tributary TU #1 of TUG2 #1, TUG3 #1 to TUG2 #7, TUG3 #1, respectively. When DBIP*x* is set high, the inverted BIP-2 code will be inserted into the V5 byte of TU #1 of the corresponding TUG2. When DBIP*x* is set low, the normal BIP-2 code will be inserted.

Register 1508H, 1509H, 150AH, 150BH, 150CH, 150DH, 150EH: TTOP TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #1, Control

Bit	Type	Function	Default
Bit 7	R	Reserved	1
Bit 6	R	TU11	1
Bit 5	R/W	PSL[2]	0
Bit 4	R/W	PSL[1]	1
Bit 3	R/W	PSL[0]	0
Bit 2	R/W	TTIEN	1
Bit 1	R/W	ERDI	0
Bit 0	R/W	IDLE	0

This register configures the operational modes of TU #2 of TUG2 #1, TUG3 #1 to TU #2 of TUG2 #7, TUG3 #1.

IDLE:

The IDLE bit enables insertion of tributary idle on tributary TU #2 in the corresponding TUG2, TUG3 #1. When IDLE is set high, the egress tributary payload bytes are set to all-zeros or all-ones as selected by the ICODE register bit. The outgoing active offset is forced to zero. When IDLE is set low, tributary TU #2 in the corresponding TUG2, TUG3 #1 is processed normally.

ERDI:

The ERDI bit selects between normal and extended RDI encoding on tributary TU #2 in the corresponding TUG2, TUG3 #1. When ERDI is set high, extended RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 5 of the Z7 byte and bit 8 of the V5 byte. The value on the RFI indication from TRAP is inserted into bit 6 of the Z7 byte and its complement into bit 7. Bit 4 of the V5 byte is set low. When ERDI is set low, normal RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 8 of the V5 byte. The value on the RFI indication from TRAP is inserted into bit 4 of the V5.

TTIEN:

The TTIEN bit enables insertion of trial trace identifier into tributary TU #2 in the corresponding TUG2, TUG3 #1. When TTIEN is set high, trail trace

identifier insertion is enabled. When TTIEN is set low, trail trace identifier insertion is disabled. The J2 byte is unused and will be set to all-zeros or all-ones as controlled by the UPOHV register bit.

PSL[2:0]:

The PSL[2:0] bits control the path signal label inserted into the PSL field of the V5 byte of tributary TU #2 in the corresponding TUG2, TUG3 #1. PSL[2] is inserted into bit 5, PSL[1] into bit 6 and PSL[0] into bit 7 of the V5 byte. The default value of 'b010 denotes asynchronous mapping of payload into the tributary.

TU11:

The TU11 read only bit reports the tributary configuration written into the corresponding register of TU #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMAP.

Register 150FH: TTOP TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #1 BIP Diagnostic Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	DBIP7	0
Bit 5	R/W	DBIP6	0
Bit 4	R/W	DBIP5	0
Bit 3	R/W	DBIP4	0
Bit 2	R/W	DBIP3	0
Bit 1	R/W	DBIP2	0
Bit 0	R/W	DBIP1	0

This register controls the insertion of BIP-2 errors in tributaries TU #2 of TUG2 #1, TUG3 #1 to TU#2 of TUG2 #7, TUG3 #1.

DBIP7 – DBIP1:

The DBIP1 to DBIP7 bits allow diagnosis of downstream receive tributary path processors of tributary TU #2 of TUG2 #1, TUG3 #1 to TUG2 #7, TUG3 #1, respectively. When DBIP*x* is set high, the inverted BIP-2 code will be inserted into the V5 byte of TU #2 of the corresponding TUG2. When DBIP*x* is set low, the normal BIP-2 code will be inserted.

Register 1510H, 1511H, 1512H, 1513H, 1514H, 1515H, 1516H: TTOP TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #1, Control

Bit	Type	Function	Default
Bit 7	R	Reserved	1
Bit 6	R	TU11	1
Bit 5	R/W	PSL[2]	0
Bit 4	R/W	PSL[1]	1
Bit 3	R/W	PSL[0]	0
Bit 2	R/W	TTIEN	1
Bit 1	R/W	ERDI	0
Bit 0	R/W	IDLE	0

This register configures the operational modes of TU #3 of TUG2 #1, TUG3 #1 to TU #3 of TUG2 #7, TUG3 #1.

IDLE:

The IDLE bit enables insertion of tributary idle on tributary TU #3 in the corresponding TUG2, TUG3 #1. When IDLE is set high, the egress tributary payload bytes are set to all-zeros or all-ones as selected by the ICODE register bit. The outgoing active offset is forced to zero. When IDLE is set low, tributary TU #3 in the corresponding TUG2, TUG3 #1 is processed normally.

ERDI:

The ERDI bit selects between normal and extended RDI encoding on tributary TU #3 in the corresponding TUG2, TUG3 #1. When ERDI is set high, extended RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 5 of the Z7 byte and bit 8 of the V5 byte. The value on the RFI indication from TRAP is inserted into bit 6 of the Z7 byte and its complement into bit 7. Bit 4 of the V5 byte is set low. When ERDI is set low, normal RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 8 of the V5 byte. The value on the RFI indication from TRAP is inserted into bit 4 of the V5.

TTIEN:

The TTIEN bit enables insertion of trial trace identifier into tributary TU #3 in the corresponding TUG2, TUG3 #1. When TTIEN is set high, trail trace

identifier insertion is enabled. When TTIEN is set low, trail trace identifier insertion is disabled. The J2 byte is unused and will be set to all-zeros or all-ones as controlled by the UPOHV register bit.

PSL[2:0]:

The PSL[2:0] bits control the path signal label inserted into the PSL field of the V5 byte of tributary TU #3 in the corresponding TUG2, TUG3 #1. PSL[2] is inserted into bit 5, PSL[1] into bit 6 and PSL[0] into bit 7 of the V5 byte. The default value of 'b010 denotes asynchronous mapping of payload into the tributary.

TU11:

The TU11 read only bit reports the tributary configuration written into the corresponding register of TU #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMAP.

Register 1517H: TTOP TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #1, BIP Diagnostic Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	DBIP7	0
Bit 5	R/W	DBIP6	0
Bit 4	R/W	DBIP5	0
Bit 3	R/W	DBIP4	0
Bit 2	R/W	DBIP3	0
Bit 1	R/W	DBIP2	0
Bit 0	R/W	DBIP1	0

This register controls the insertion of BIP-2 errors in tributaries TU #3 of TUG2 #1, TUG3 #1 to TU#3 of TUG2 #7, TUG3 #1.

DBIP7 – DBIP1:

The DBIP1 to DBIP7 bits allow diagnosis of downstream receive tributary path processors of tributary TU #3 of TUG2 #1, TUG3 #1 to TUG2 #7, TUG3 #1, respectively. When DBIP*x* is set high, the inverted BIP-2 code will be inserted into the V5 byte of TU #3 of the corresponding TUG2. When DBIP*x* is set low, the normal BIP-2 code will be inserted.

Register 1518H, 1519H, 151AH, 151BH, 151CH, 151DH, 151EH: TTOP TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #1, Control

Bit	Type	Function	Default
Bit 7	R	Reserved	1
Bit 6	R	TU11	1
Bit 5	R/W	PSL[2]	0
Bit 4	R/W	PSL[1]	1
Bit 3	R/W	PSL[0]	0
Bit 2	R/W	TTIEN	1
Bit 1	R/W	ERDI	0
Bit 0	R/W	IDLE	0

This register configures the operational modes of TU #4 of TUG2 #1, TUG3 #1 to TU #4 of TUG2 #7, TUG3 #1. When the corresponding TUG2 tributary group is configured to TU12 (VT2) mode, the associated register in this set has no effect.

IDLE:

The IDLE bit enables insertion of tributary idle on tributary TU #4 in the corresponding TUG2, TUG3 #1. When IDLE is set high, the egress tributary payload bytes are set to all-zeros or all-ones as selected by the ICODE register bit. The outgoing active offset is forced to zero. When IDLE is set low, tributary TU #4 in the corresponding TUG2, TUG3 #1 is processed normally.

ERDI:

The ERDI bit selects between normal and extended RDI encoding on tributary TU #4 in the corresponding TUG2, TUG3 #1. When ERDI is set high, extended RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 5 of the Z7 byte and bit 8 of the V5 byte. The value on the RFI indication from TRAP is inserted into bit 6 of the Z7 byte and its complement into bit 7. Bit 4 of the V5 byte is set low. When ERDI is set low, normal RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 8 of the V5 byte. The value on the RFI indication from TRAP is inserted into bit 4 of the V5.

TTIEN:

The TTIEN bit enables insertion of trial trace identifier into tributary TU #4 in the corresponding TUG2, TUG3 #1. When TTIEN is set high, trail trace identifier insertion is enabled. When TTIEN is set low, trail trace identifier insertion is disabled. The J2 byte is unused and will be set to all-zeros or all-ones as controlled by the UPOHV register bit.

PSL[2:0]:

The PSL[2:0] bits control the path signal label inserted into the PSL field of the V5 byte of tributary TU #4 in the corresponding TUG2, TUG3 #1. PSL[2] is inserted into bit 5, PSL[1] into bit 6 and PSL[0] into bit 7 of the V5 byte. The default value of ‘b010 denotes asynchronous mapping of payload into the tributary.

TU11:

The TU11 read only bit reports the tributary configuration written into the corresponding register of TU #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMAP.

Register 151FH: TTOP TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #1, BIP Diagnostic Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	DBIP7	0
Bit 5	R/W	DBIP6	0
Bit 4	R/W	DBIP5	0
Bit 3	R/W	DBIP4	0
Bit 2	R/W	DBIP3	0
Bit 1	R/W	DBIP2	0
Bit 0	R/W	DBIP1	0

This register controls the insertion of BIP-2 errors in tributaries TU #4 of TUG2 #1, TUG3 #1 to TU#4 of TUG2 #7, TUG3 #1. When the corresponding TUG2 tributary group is configured to TU12 (VT2) mode, this register has no effect.

DBIP7 – DBIP1:

The DBIP1 to DBIP7 bits allow diagnosis of downstream receive tributary path processors of tributary TU #4 of TUG2 #1, TUG3 #1 to TUG2 #7, TUG3 #1, respectively. When DBIP*x* is set high, the inverted BIP-2 code will be inserted into the V5 byte of TU #4 of the corresponding TUG2. When DBIP*x* is set low, the normal BIP-2 code will be inserted.

Register 1520H, 1521H, 1522H, 1523H, 1524H, 1525H, 1526H: TTOP TU #1 in TUG2 #1 to TUG2 #7 of TUG3 #2, Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	1
Bit 6	R/W	TU11	1
Bit 5	R/W	PSL[2]	0
Bit 4	R/W	PSL[1]	1
Bit 3	R/W	PSL[0]	0
Bit 2	R/W	TTIEN	1
Bit 1	R/W	ERDI	0
Bit 0	R/W	IDLE	0

This register configures the operational modes of TU #1 of TUG2 #2, TUG3 #2 to TU #1 of TUG2 #7, TUG3 #2.

IDLE:

The IDLE bit enables insertion of tributary idle on tributary TU #1 in the corresponding TUG2, TUG3 #2. When IDLE is set high, the egress tributary payload bytes are set to all-zeros or all-ones as selected by the ICODE register bit. The outgoing active offset is forced to zero. When IDLE is set low, tributary TU #1 in the corresponding TUG2, TUG3 #2 is processed normally.

ERDI:

The ERDI bit selects between normal and extended RDI encoding on tributary TU #1 in the corresponding TUG2, TUG3 #2. When ERDI is set high, extended RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 5 of the Z7 byte and bit 8 of the V5 byte. The value on the RFI indication from TRAP is inserted into bit 6 of the Z7 byte and its complement into bit 7. Bit 4 of the V5 byte is set low. When ERDI is set low, normal RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 8 of the V5 byte. The value on the RFI indication from TRAP is inserted into bit 4 of the V5.

TTIEN:

The TTIEN bit enables insertion of trial trace identifier into tributary TU #1 in the corresponding TUG2, TUG3 #2. When TTIEN is set high, trail trace

identifier insertion is enabled. When TTIEN is set low, trail trace identifier insertion is disabled. The J2 byte is unused and will be set to all-zeros or all-ones as controlled by the UPOHV register bit.

PSL[2:0]:

The PSL[2:0] bits control the path signal label inserted into the PSL field of the V5 byte of tributary TU #1 in the corresponding TUG2, TUG3 #2. PSL[2] is inserted into bit 5, PSL[1] into bit 6 and PSL[0] into bit 7 of the V5 byte. The default value of 'b010 denotes asynchronous mapping of payload into the tributary.

TU11:

The TU11 bit specifies the tributary configuration of the corresponding TUG2 tributary group in TUG3 #2. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMAP.

Register 1527H: TTOP TU #1 in TUG2 #1 to TUG2 #7 of TUG3 #2, BIP Diagnostic Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	DBIP7	0
Bit 5	R/W	DBIP6	0
Bit 4	R/W	DBIP5	0
Bit 3	R/W	DBIP4	0
Bit 2	R/W	DBIP3	0
Bit 1	R/W	DBIP2	0
Bit 0	R/W	DBIP1	0

This register controls the insertion of BIP-2 errors in tributaries TU #1 of TUG2 #1, TUG3 #2 to TU#1 of TUG2 #7, TUG3 #2.

DBIP7 – DBIP1:

The DBIP1 to DBIP7 bits allow diagnosis of downstream receive tributary path processors of tributary TU #1 of TUG2 #1, TUG3 #2 to TUG2 #7, TUG3 #2, respectively. When DBIP*x* is set high, the inverted BIP-2 code will be inserted into the V5 byte of TU #1 of the corresponding TUG2. When DBIP*x* is set low, the normal BIP-2 code will be inserted.

Register 1528H, 1529H, 152AH, 152BH, 152CH, 152DH, 152EH: TTOP TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #2, Control

Bit	Type	Function	Default
Bit 7	R	Reserved	1
Bit 6	R	TU11	1
Bit 5	R/W	PSL[2]	0
Bit 4	R/W	PSL[1]	1
Bit 3	R/W	PSL[0]	0
Bit 2	R/W	TTIEN	1
Bit 1	R/W	ERDI	0
Bit 0	R/W	IDLE	0

This register configures the operational modes of TU #2 of TUG2 #1, TUG3 #2 to TU #2 of TUG2 #7, TUG3 #2.

IDLE:

The IDLE bit enables insertion of tributary idle on tributary TU #2 in the corresponding TUG2, TUG3 #2. When IDLE is set high, the egress tributary payload bytes are set to all-zeros or all-ones as selected by the ICODE register bit. The outgoing active offset is forced to zero. When IDLE is set low, tributary TU #2 in the corresponding TUG2, TUG3 #2 is processed normally.

ERDI:

The ERDI bit selects between normal and extended RDI encoding on tributary TU #2 in the corresponding TUG2, TUG3 #2. When ERDI is set high, extended RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 5 of the Z7 byte and bit 8 of the V5 byte. The value on the RFI indication from TRAP is inserted into bit 6 of the Z7 byte and its complement into bit 7. Bit 4 of the V5 byte is set low. When ERDI is set low, normal RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 8 of the V5 byte. The value on the RFI indication from TRAP is inserted into bit 4 of the V5.

TTIEN:

The TTIEN bit enables insertion of trial trace identifier into tributary TU #2 in the corresponding TUG2, TUG3 #2. When TTIEN is set high, trail trace

identifier insertion is enabled. When TTIEN is set low, trail trace identifier insertion is disabled. The J2 byte is unused and will be set to all-zeros or all-ones as controlled by the UPOHV register bit.

PSL[2:0]:

The PSL[2:0] bits control the path signal label inserted into the PSL field of the V5 byte of tributary TU #2 in the corresponding TUG2, TUG3 #2. PSL[2] is inserted into bit 5, PSL[1] into bit 6 and PSL[0] into bit 7 of the V5 byte. The default value of 'b010 denotes asynchronous mapping of payload into the tributary.

TU11:

The TU11 read only bit reports the tributary configuration written into the corresponding register of TU #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMAP.

Register 152FH: TTOP TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #2, BIP Diagnostic Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	DBIP7	0
Bit 5	R/W	DBIP6	0
Bit 4	R/W	DBIP5	0
Bit 3	R/W	DBIP4	0
Bit 2	R/W	DBIP3	0
Bit 1	R/W	DBIP2	0
Bit 0	R/W	DBIP1	0

This register controls the insertion of BIP-2 errors in tributaries TU #2 of TUG2 #1, TUG3 #2 to TU#1 of TUG2 #7, TUG3 #2.

DBIP7 – DBIP1:

The DBIP1 to DBIP7 bits allow diagnosis of downstream receive tributary path processors of tributary TU #2 of TUG2 #1, TUG3 #2 to TUG2 #7, TUG3 #2, respectively. When DBIP*x* is set high, the inverted BIP-2 code will be inserted into the V5 byte of TU #2 of the corresponding TUG2. When DBIP*x* is set low, the normal BIP-2 code will be inserted.

Register 1530H, 1531H, 1532H, 1533H, 1534H, 1535H, 1536H: TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #2, Control

Bit	Type	Function	Default
Bit 7	R	Reserved	1
Bit 6	R	TU11	1
Bit 5	R/W	PSL[2]	0
Bit 4	R/W	PSL[1]	1
Bit 3	R/W	PSL[0]	0
Bit 2	R/W	TTIEN	1
Bit 1	R/W	ERDI	0
Bit 0	R/W	IDLE	0

This register configures the operational modes of TU #3 of TUG2 #1, TUG3 #2 to TU #3 of TUG2 #7, TUG3 #2.

IDLE:

The IDLE bit enables insertion of tributary idle on tributary TU #3 in the corresponding TUG2, TUG3 #2. When IDLE is set high, the egress tributary payload bytes are set to all-zeros or all-ones as selected by the ICODE register bit. The outgoing active offset is forced to zero. When IDLE is set low, tributary TU #3 in the corresponding TUG2, TUG3 #2 is processed normally.

ERDI:

The ERDI bit selects between normal and extended RDI encoding on tributary TU #3 in the corresponding TUG2, TUG3 #2. When ERDI is set high, extended RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 5 of the Z7 byte and bit 8 of the V5 byte. The value on the RFI indication from TRAP is inserted into bit 6 of the Z7 byte and its complement into bit 7. Bit 4 of the V5 byte is set low. When ERDI is set low, normal RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 8 of the V5 byte. The value on the RFI indication from TRAP is inserted into bit 4 of the V5.

TTIEN:

The TTIEN bit enables insertion of trial trace identifier into tributary TU #3 in the corresponding TUG2, TUG3 #2. When TTIEN is set high, trail trace

identifier insertion is enabled. When TTIEN is set low, trail trace identifier insertion is disabled. The J2 byte is unused and will be set to all-zeros or all-ones as controlled by the UPOHV register bit.

PSL[2:0]:

The PSL[2:0] bits control the path signal label inserted into the PSL field of the V5 byte of tributary TU #3 in the corresponding TUG2, TUG3 #2. PSL[2] is inserted into bit 5, PSL[1] into bit 6 and PSL[0] into bit 7 of the V5 byte. The default value of 'b010 denotes asynchronous mapping of payload into the tributary.

TU11:

The TU11 read only bit reports the tributary configuration written into the corresponding register of TU #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMAP.

Register 1537H: TTOP TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #2, BIP Diagnostic Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	DBIP7	0
Bit 5	R/W	DBIP6	0
Bit 4	R/W	DBIP5	0
Bit 3	R/W	DBIP4	0
Bit 2	R/W	DBIP3	0
Bit 1	R/W	DBIP2	0
Bit 0	R/W	DBIP1	0

This register controls the insertion of BIP-2 errors in tributaries TU #3 of TUG2 #1, TUG3 #2 to TU#1 of TUG2 #7, TUG3 #2.

DBIP7 – DBIP1:

The DBIP1 to DBIP7 bits allow diagnosis of downstream receive tributary path processors of tributary TU #3 of TUG2 #1, TUG3 #2 to TUG2 #7, TUG3 #2, respectively. When DBIP*x* is set high, the inverted BIP-2 code will be inserted into the V5 byte of TU #3 of the corresponding TUG2. When DBIP*x* is set low, the normal BIP-2 code will be inserted.

Register 1538H, 1539H, 153AH, 153BH, 153CH, 153DH, 153EH: TTOP TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #2, Control

Bit	Type	Function	Default
Bit 7	R	Reserved	1
Bit 6	R	TU11	1
Bit 5	R/W	PSL[2]	0
Bit 4	R/W	PSL[1]	1
Bit 3	R/W	PSL[0]	0
Bit 2	R/W	TTIEN	1
Bit 1	R/W	ERDI	0
Bit 0	R/W	IDLE	0

This register configures the operational modes of TU #4 of TUG2 #1, TUG3 #2 to TU #4 of TUG2 #7, TUG3 #2. When the corresponding TUG2 tributary group is configured to TU12 (VT2) mode, the associated register in this set has no effect.

IDLE:

The IDLE bit enables insertion of tributary idle on tributary TU #4 in the corresponding TUG2, TUG3 #2. When IDLE is set high, the egress tributary payload bytes are set to all-zeros or all-ones as selected by the ICODE register bit. The outgoing active offset is forced to zero. When IDLE is set low, tributary TU #4 in the corresponding TUG2, TUG3 #2 is processed normally.

ERDI:

The ERDI bit selects between normal and extended RDI encoding on tributary TU #4 in the corresponding TUG2, TUG3 #2. When ERDI is set high, extended RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 5 of the Z7 byte and bit 8 of the V5 byte. The value on the RFI indication from TRAP is inserted into bit 6 of the Z7 byte and its complement into bit 7. Bit 4 of the V5 byte is set low. When ERDI is set low, normal RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 8 of the V5 byte. The value on the RFI indication from TRAP is inserted into bit 4 of the V5.

TTIEN:

The TTIEN bit enables insertion of trial trace identifier into tributary TU #4 in the corresponding TUG2, TUG3 #2. When TTIEN is set high, trail trace identifier insertion is enabled. When TTIEN is set low, trail trace identifier insertion is disabled. The J2 byte is unused and will be set to all-zeros or all-ones as controlled by the UPOHV register bit.

PSL[2:0]:

The PSL[2:0] bits control the path signal label inserted into the PSL field of the V5 byte of tributary TU #4 in the corresponding TUG2, TUG3 #2. PSL[2] is inserted into bit 5, PSL[1] into bit 6 and PSL[0] into bit 7 of the V5 byte. The default value of ‘b010 denotes asynchronous mapping of payload into the tributary.

TU11:

The TU11 read only bit reports the tributary configuration written into the corresponding register of TU #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMAP.

Register 153FH: TTOP TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #2, BIP Diagnostic Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	DBIP7	0
Bit 5	R/W	DBIP6	0
Bit 4	R/W	DBIP5	0
Bit 3	R/W	DBIP4	0
Bit 2	R/W	DBIP3	0
Bit 1	R/W	DBIP2	0
Bit 0	R/W	DBIP1	0

This register controls the insertion of BIP-2 errors in tributaries TU #4 of TUG2 #1, TUG3 #2 to TU#1 of TUG2 #7, TUG3 #2. When the corresponding TUG2 tributary group is configured to TU12 (VT2) mode, this register has no effect.

DBIP7 – DBIP1:

The DBIP1 to DBIP7 bits allow diagnosis of downstream receive tributary path processors of tributary TU #4 of TUG2 #1, TUG3 #2 to TUG2 #7, TUG3 #2, respectively. When DBIP*x* is set high, the inverted BIP-2 code will be inserted into the V5 byte of TU #4 of the corresponding TUG2. When DBIP*x* is set low, the normal BIP-2 code will be inserted.

Register 1540H, 1541H, 1542H, 1543H, 1544H, 1545H, 1546H: TTOP TU #1 in TUG2 #1 to TUG2 #7 of TUG3 #3, Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	1
Bit 6	R/W	TU11	1
Bit 5	R/W	PSL[2]	0
Bit 4	R/W	PSL[1]	1
Bit 3	R/W	PSL[0]	0
Bit 2	R/W	TTIEN	1
Bit 1	R/W	ERDI	0
Bit 0	R/W	IDLE	0

This register configures the operational modes of TU #1 of TUG2 #2, TUG3 #3 to TU #1 of TUG2 #7, TUG3 #3.

IDLE:

The IDLE bit enables insertion of tributary idle on tributary TU #1 in the corresponding TUG2, TUG3 #3. When IDLE is set high, the egress tributary payload bytes are set to all-zeros or all-ones as selected by the ICODE register bit. The outgoing active offset is forced to zero. When IDLE is set low, tributary TU #1 in the corresponding TUG2, TUG3 #3 is processed normally.

ERDI:

The ERDI bit selects between normal and extended RDI encoding on tributary TU #1 in the corresponding TUG2, TUG3 #3. When ERDI is set high, extended RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 5 of the Z7 byte and bit 8 of the V5 byte. The value on the RFI indication from TRAP is inserted into bit 6 of the Z7 byte and its complement into bit 7. Bit 4 of the V5 byte is set low. When ERDI is set low, normal RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 8 of the V5 byte. The value on the RFI indication from TRAP is inserted into bit 4 of the V5.

TTIEN:

The TTIEN bit enables insertion of trial trace identifier into tributary TU #1 in the corresponding TUG2, TUG3 #3. When TTIEN is set high, trail trace

identifier insertion is enabled. When TTIEN is set low, trail trace identifier insertion is disabled. The J2 byte is unused and will be set to all-zeros or all-ones as controlled by the UPOHV register bit.

PSL[2:0]:

The PSL[2:0] bits control the path signal label inserted into the PSL field of the V5 byte of tributary TU #1 in the corresponding TUG2, TUG3 #3. PSL[2] is inserted into bit 5, PSL[1] into bit 6 and PSL[0] into bit 7 of the V5 byte. The default value of 'b010 denotes asynchronous mapping of payload into the tributary.

TU11:

The TU11 bit specifies the tributary configuration of the corresponding TUG2 tributary group in TUG3 #3. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMAP.

Register 1547H: TTOP TU #1 in TUG2 #1 to TUG2 #7 of TUG3 #3, BIP Diagnostic Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	DBIP7	0
Bit 5	R/W	DBIP6	0
Bit 4	R/W	DBIP5	0
Bit 3	R/W	DBIP4	0
Bit 2	R/W	DBIP3	0
Bit 1	R/W	DBIP2	0
Bit 0	R/W	DBIP1	0

This register controls the insertion of BIP-2 errors in tributaries TU #1 of TUG2 #1, TUG3 #3 to TU#1 of TUG2 #7, TUG3 #3.

DBIP7 – DBIP1:

The DBIP1 to DBIP7 bits allow diagnosis of downstream receive tributary path processors of tributary TU #1 of TUG2 #1, TUG3 #3 to TUG2 #7, TUG3 #3, respectively. When DBIP*x* is set high, the inverted BIP-2 code will be inserted into the V5 byte of TU #1 of the corresponding TUG2. When DBIP*x* is set low, the normal BIP-2 code will be inserted.

Register 1548H, 1549H, 154AH, 154BH, 154CH, 154DH, 154EH: TTOP TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #3, Control

Bit	Type	Function	Default
Bit 7	R	Reserved	1
Bit 6	R	TU11	1
Bit 5	R/W	PSL[2]	0
Bit 4	R/W	PSL[1]	1
Bit 3	R/W	PSL[0]	0
Bit 2	R/W	TTIEN	1
Bit 1	R/W	ERDI	0
Bit 0	R/W	IDLE	0

This register configures the operational modes of TU #2 of TUG2 #1, TUG3 #3 to TU #2 of TUG2 #7, TUG3 #3.

IDLE:

The IDLE bit enables insertion of tributary idle on tributary TU #2 in the corresponding TUG2, TUG3 #3. When IDLE is set high, the egress tributary payload bytes are set to all-zeros or all-ones as selected by the ICODE register bit. The outgoing active offset is forced to zero. When IDLE is set low, tributary TU #2 in the corresponding TUG2, TUG3 #3 is processed normally.

ERDI:

The ERDI bit selects between normal and extended RDI encoding on tributary TU #2 in the corresponding TUG2, TUG3 #3. When ERDI is set high, extended RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 5 of the Z7 byte and bit 8 of the V5 byte. The value on the RFI indication from TRAP is inserted into bit 6 of the Z7 byte and its complement into bit 7. Bit 4 of the V5 byte is set low. When ERDI is set low, normal RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 8 of the V5 byte. The value on the RFI indication from TRAP is inserted into bit 4 of the V5.

TTIEN:

The TTIEN bit enables insertion of trial trace identifier into tributary TU #2 in the corresponding TUG2, TUG3 #3. When TTIEN is set high, trail trace

identifier insertion is enabled. When TTIEN is set low, trail trace identifier insertion is disabled. The J2 byte is unused and will be set to all-zeros or all-ones as controlled by the UPOHV register bit.

PSL[2:0]:

The PSL[2:0] bits control the path signal label inserted into the PSL field of the V5 byte of tributary TU #2 in the corresponding TUG2, TUG3 #3. PSL[2] is inserted into bit 5, PSL[1] into bit 6 and PSL[0] into bit 7 of the V5 byte. The default value of 'b010 denotes asynchronous mapping of payload into the tributary.

TU11:

The TU11 read only bit reports the tributary configuration written into the corresponding register of TU #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMAP.

Register 154FH: TTOP TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #3, BIP Diagnostic Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	DBIP7	0
Bit 5	R/W	DBIP6	0
Bit 4	R/W	DBIP5	0
Bit 3	R/W	DBIP4	0
Bit 2	R/W	DBIP3	0
Bit 1	R/W	DBIP2	0
Bit 0	R/W	DBIP1	0

This register controls the insertion of BIP-2 errors in tributaries TU #2 of TUG2 #1, TUG3 #3 to TU#1 of TUG2 #7, TUG3 #3.

DBIP7 – DBIP1:

The DBIP1 to DBIP7 bits allow diagnosis of downstream receive tributary path processors of tributary TU #2 of TUG2 #1, TUG3 #3 to TUG2 #7, TUG3 #3, respectively. When DBIP*x* is set high, the inverted BIP-2 code will be inserted into the V5 byte of TU #2 of the corresponding TUG2. When DBIP*x* is set low, the normal BIP-2 code will be inserted.

Register 1550H, 1551H, 1552H, 1553H, 1554H, 1555H, 1556H: TTOP TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #3, Control

Bit	Type	Function	Default
Bit 7	R	Reserved	1
Bit 6	R	TU11	1
Bit 5	R/W	PSL[2]	0
Bit 4	R/W	PSL[1]	1
Bit 3	R/W	PSL[0]	0
Bit 2	R/W	TTIEN	1
Bit 1	R/W	ERDI	0
Bit 0	R/W	IDLE	0

This register configures the operational modes of TU #3 of TUG2 #1, TUG3 #3 to TU #3 of TUG2 #7, TUG3 #3.

IDLE:

The IDLE bit enables insertion of tributary idle on tributary TU #3 in the corresponding TUG2, TUG3 #3. When IDLE is set high, the egress tributary payload bytes are set to all-zeros or all-ones as selected by the ICODE register bit. The outgoing active offset is forced to zero. When IDLE is set low, tributary TU #3 in the corresponding TUG2, TUG3 #3 is processed normally.

ERDI:

The ERDI bit selects between normal and extended RDI encoding on tributary TU #3 in the corresponding TUG2, TUG3 #3. When ERDI is set high, extended RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 5 of the Z7 byte and bit 8 of the V5 byte. The value on the RFI indication from TRAP is inserted into bit 6 of the Z7 byte and its complement into bit 7. Bit 4 of the V5 byte is set low. When ERDI is set low, normal RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 8 of the V5 byte. The value on the RFI indication from TRAP is inserted into bit 4 of the V5.

TTIEN:

The TTIEN bit enables insertion of trial trace identifier into tributary TU #3 in the corresponding TUG2, TUG3 #3. When TTIEN is set high, trail trace

identifier insertion is enabled. When TTIEN is set low, trail trace identifier insertion is disabled. The J2 byte is unused and will be set to all-zeros or all-ones as controlled by the UPOHV register bit.

PSL[2:0]:

The PSL[2:0] bits control the path signal label inserted into the PSL field of the V5 byte of tributary TU #3 in the corresponding TUG2, TUG3 #3. PSL[2] is inserted into bit 5, PSL[1] into bit 6 and PSL[0] into bit 7 of the V5 byte. The default value of 'b010 denotes asynchronous mapping of payload into the tributary.

TU11:

The TU11 read only bit reports the tributary configuration written into the corresponding register of TU #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMAP.

Register 1557H: TTOP TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #3, BIP Diagnostic Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	DBIP7	0
Bit 5	R/W	DBIP6	0
Bit 4	R/W	DBIP5	0
Bit 3	R/W	DBIP4	0
Bit 2	R/W	DBIP3	0
Bit 1	R/W	DBIP2	0
Bit 0	R/W	DBIP1	0

This register controls the insertion of BIP-2 errors in tributaries TU #3 of TUG2 #1, TUG3 #3 to TU#1 of TUG2 #7, TUG3 #3

DBIP7 – DBIP1:

The DBIP1 to DBIP7 bits allow diagnosis of downstream receive tributary path processors of tributary TU #3 of TUG2 #1, TUG3 #3 to TUG2 #7, TUG3 #3, respectively. When DBIP*x* is set high, the inverted BIP-2 code will be inserted into the V5 byte of TU #3 of the corresponding TUG2. When DBIP*x* is set low, the normal BIP-2 code will be inserted.

Register 1558H, 1559H, 155AH, 155BH, 155CH, 155DH, 155EH: TTOP TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #3, Control

Bit	Type	Function	Default
Bit 7	R	Reserved	1
Bit 6	R	TU11	1
Bit 5	R/W	PSL[2]	0
Bit 4	R/W	PSL[1]	1
Bit 3	R/W	PSL[0]	0
Bit 2	R/W	TTIEN	1
Bit 1	R/W	ERDI	0
Bit 0	R/W	IDLE	0

This register configures the operational modes of TU #4 of TUG2 #1, TUG3 #3 to TU #4 of TUG2 #7, TUG3 #3. When the corresponding TUG2 tributary group is configured to TU12 (VT2) mode, the associated register in this set has no effect.

IDLE:

The IDLE bit enables insertion of tributary idle on tributary TU #4 in the corresponding TUG2, TUG3 #3. When IDLE is set high, the egress tributary payload bytes are set to all-zeros or all-ones as selected by the ICODE register bit. The outgoing active offset is forced to zero. When IDLE is set low, tributary TU #4 in the corresponding TUG2, TUG3 #3 is processed normally.

ERDI:

The ERDI bit selects between normal and extended RDI encoding on tributary TU #4 in the corresponding TUG2, TUG3 #3. When ERDI is set high, extended RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 5 of the Z7 byte and bit 8 of the V5 byte. The value on the RFI indication from TRAP is inserted into bit 6 of the Z7 byte and its complement into bit 7. Bit 4 of the V5 byte is set low. When ERDI is set low, normal RDI is selected. The value sampled on the RDI indication from TRAP is inserted into bit 8 of the V5 byte. The value on the RFI indication from TRAP is inserted into bit 4 of the V5.

TTIEN:

The TTIEN bit enables insertion of trial trace identifier into tributary TU #4 in the corresponding TUG2, TUG3 #3. When TTIEN is set high, trail trace identifier insertion is enabled. When TTIEN is set low, trail trace identifier insertion is disabled. The J2 byte is unused and will be set to all-zeros or all-ones as controlled by the UPOHV register bit.

PSL[2:0]:

The PSL[2:0] bits control the path signal label inserted into the PSL field of the V5 byte of tributary TU #4 in the corresponding TUG2, TUG3 #3. PSL[2] is inserted into bit 5, PSL[1] into bit 6 and PSL[0] into bit 7 of the V5 byte. The default value of ‘b010 denotes asynchronous mapping of payload into the tributary.

TU11:

The TU11 read only bit reports the tributary configuration written into the corresponding register of TU #1. The configuration specified by the TU11 bit is selected as follows:

TU11	Configuration	Active TU (VT)
0	TU12 (VT2)	#1, #2, #3
1	TU11 (VT1.5)	#1, #2, #3, #4

Reserved:

This bit must be kept at a logic 1 for proper operation of the TEMAP.

Register 155FH: TTOP TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #3, BIP Diagnostic Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	DBIP7	0
Bit 5	R/W	DBIP6	0
Bit 4	R/W	DBIP5	0
Bit 3	R/W	DBIP4	0
Bit 2	R/W	DBIP3	0
Bit 1	R/W	DBIP2	0
Bit 0	R/W	DBIP1	0

This register controls the insertion of BIP-2 errors in tributaries TU #4 of TUG2 #1, TUG3 #3 to TU#1 of TUG2 #7, TUG3 #3. When the corresponding TUG2 tributary group is configured to TU12 (VT2) mode, this register has no effect

DBIP7 – DBIP1:

The DBIP1 to DBIP7 bits allow diagnosis of downstream receive tributary path processors of tributary TU #4 of TUG2 #1, TUG3 #3 to TUG2 #7, TUG3 #3, respectively. When DBIP*x* is set high, the inverted BIP-2 code will be inserted into the V5 byte of TU #4 of the corresponding TUG2. When DBIP*x* is set low, the normal BIP-2 code will be inserted.

Register 1560H: TTOP TUG3 #1 Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	UPOHV	0
Bit 0	R/W	ICODE	0

This register contains control bits that are applicable to all tributaries in TUG3 #1.

ICODE:

The ICODE bit controls the value of the tributary payload bytes inserted into payload bytes of idle tributaries in TUG3 #1. When ICODE is set high, the tributary payload of an idle tributary (the corresponding IDLE bit set high) is set to all-ones. When ICODE is set low, the tributary payload is set to all-zeros.

UPOHV:

The UPOHV bit controls the value inserted into unused bits in tributary path overhead bytes of tributaries in TUG3 #1. When UPOHV is set high, unused tributary path overhead bits are set high. When UPOHV is set low, unused tributary path overhead bits are set low. Unused tributary POH bits include the J2 byte when trail trace identifier insertion is disabled (TTIEN set low), all bits in the Z6 byte, and bits 1, 2, 3, and 4 and 8 of the Z7 byte when extended RDI is enabled (ERDI set high) and all the bits of the Z7 byte when extended RDI is disabled (ERDI set low).

Register 1561H: TTOP TUG3 #2 Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	UPOHV	0
Bit 0	R/W	ICODE	0

This register contains control bits that are applicable to all tributaries in TUG3 #2.

ICODE:

The ICODE bit controls the value of the tributary payload bytes inserted into payload bytes of idle tributaries in TUG3 #1. When ICODE is set high, the tributary payload of an idle tributary (the corresponding IDLE bit set high) is set to all-ones. When ICODE is set low, the tributary payload is set to all-zeros.

UPOHV:

The UPOHV bit controls the value inserted into unused bits in tributary path overhead bytes of tributaries in TUG3 #2. When UPOHV is set high, unused tributary path overhead bits are set high. When UPOHV is set low, unused tributary path overhead bits are set low. Unused tributary POH bits include the J2 byte when trail trace identifier insertion is disabled (TTIEN set low), all bits in the Z6 byte, bits 1, 2, 3, and 4 of the Z7 byte when extended RDI is enabled (ERDI set high) and all the bits of the Z7 byte when extended RDI is disabled (ERDI set low).

Register 1562H: TTOP TUG3 #3 Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	UPOHV	0
Bit 0	R/W	ICODE	0

This register contains control bits that are applicable to all tributaries in TUG3 #3.

ICODE:

The ICODE bit controls the value of the tributary payload bytes inserted into payload bytes of idle tributaries in TUG3 #3. When ICODE is set high, the tributary payload of an idle tributary (the corresponding IDLE bit set high) is set to all-ones. When ICODE is set low, the tributary payload is set to all-zeros.

UPOHV:

The UPOHV bit controls the value inserted into unused bits in tributary path overhead bytes of tributaries in TUG3 #3. When UPOHV is set high, unused tributary path overhead bits are set high. When UPOHV is set low, unused tributary path overhead bits are set low. Unused tributary POH bits include the J2 byte when trail trace identifier insertion is disabled (TTIEN set low), all bits in the Z6 byte, bits 1, 2, 3, and 4 of the Z7 byte when extended RDI is enabled (ERDI set high) and all the bits of the Z7 byte when extended RDI is disabled (ERDI set low).

Register 1564H: TTOP Trail Trace Identifier Page Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	SBUFINUSE	0
Bit 0	R/W	USESB	0

This register allows the selection of one of either the primary RAM bank or the shadow buffer to be accessed in indirect operations. This register also triggers a shadow RAM use request for the tributary specified in the Indirect Trail Trace Identifier Buffer Address register. Active use of the shadow RAM by any tributary is also indicated within this register.

SBUFINUSE:

The shadow buffer RAM in use, SBUFINUSE, bit is a read only bit that identifies when the shadow buffer RAM is selected for use by one of the virtual tributaries. Use of the shadow buffer RAM is under explicit control of the USESBUF bit described below. When SBUFINUSE is high, the shadow RAM is in use for the tributary designated at the time the USESBUF bit was set high. The trail trace identifier for the designated tributary can at this point be modified through an indirect access to the tributary trail trace identifier buffer RAM. When SBUFINUSE is low the shadow buffer RAM is not being used by any of the tributaries.

USESB:

The request shadow buffer RAM use bit, USESB, directs the TTOP block to begin using the shadow RAM for retrieval of the tributary trail trace identifier for the tributary specified in the Indirect Trail Trace Identifier Buffer Address register at the time the USESB bit is set. When USESB is set high, the trail trace identifier stored in the shadow RAM is read sequentially and inserted into the J2 byte of the corresponding tributary. When USESB is set low, the trail trace identifiers stored in the tributary trail trace identifier buffer RAM are

read sequentially and inserted into the J2 byte of the corresponding tributary. When setting the USESB bit from low to high or high to low, the corresponding tributary must be identified in the Indirect Trail Trace Identifier Buffer Address register. Switches between the RAM to be accessed, as a result of write accesses to USESB, are synchronized to the start of the trail trace identifier of each tributary. In other words, the requested change will not occur until after the last byte of the trail trace identifier in the current RAM is written out.

Register 1565H: TTOP Indirect Trail Trace Identifier Tributary Select

Bit	Type	Function	Default
Bit 7	R/W	TUG3[1]	0
Bit 6	R/W	TUG3[0]	0
Bit 5	R/W	TUG2[2]	0
Bit 4	R/W	TUG2[1]	0
Bit 3	R/W	TUG2[0]	0
Bit 2	R/W	TU[2]	0
Bit 1	R/W	TU[1]	0
Bit 0	R/W	TU[0]	0

This register provides the tributary number used to access the Indirect Trail Trace Identifier configuration RAM. Writing to this register does not trigger an indirect Indirect Trail Trace Identifier configuration register access.

In order to access the buffered RAM of the TTOP Trail Trace Message, one must set all bits of this register to logic 0. Then The Trail Trace Message can be written into RAM via Register 1566H: Indirect Trail Trace Identifier Buffer Address and Register 1567H: TTOP Indirect Trail Trace Identifier Buffer Data.

Register 1566H: Indirect Trail Trace Identifier Buffer Address register must be written to in order to trigger an indirect Indirect Trail Trace Identifier configuration register access. In order to obtain predictable indirect access results, the Indirect Trail Trace Identifier Tributary Select register should be modified (if necessary) prior to writing to the Indirect Trail Trace Identifier Buffer Address register.

The buffered RAM can then be used by setting USESB in Register 1564H: TTOP Trail Trace Identifier Page Select to logic 1.

TU[2:0]:

The indirect tributary unit bits (TU[2:0]) indicate the tributary unit to be configured or interrogated in the indirect access. Legal TU[2:0] ranges are ‘b001 to ‘b100. Out of range values will result in undefined results during indirect access operations.

TUG2[2:0]:

The indirect tributary unit group 2 bits (TUG2[2:0]) indicate the tributary unit group 2 to be configured or interrogated in the indirect access. Legal

TUG2[2:0] ranges are ‘b001 to ‘b111. Out of range values will result in undefined results during indirect access operations.

TUG3[1:0]:

The indirect tributary unit group 3 bits (TUG2[1:0]) indicate the tributary unit group 3 to be configured or interrogated in the indirect access. Legal TUG3[1:0] ranges are ‘b01 to ‘b11. Out of range values will result in undefined results during indirect access operations.

Register 1566H: TTOP Indirect Trail Trace Identifier Buffer Address

Bit	Type	Function	Default
Bit 7	R	BUSY	X
Bit 6	R/W	RWB	0
Bit 5	R/W	A[5]	0
Bit 4	R/W	A[4]	0
Bit 3	R/W	A[3]	0
Bit 2	R/W	A[2]	0
Bit 1	R/W	A[1]	0
Bit 0	R/W	A[0]	0

This register provides the buffer location used to access the trail trace identifier buffer RAM. Writing to this register triggers an indirect time trail trace buffer access.

A[5:0]:

The A[5:0] indexes into the trail trace identifier buffer associated with the tributary specified by the Trail Trace Identifier Tributary Select register. Selection between the trail trace identifier buffer and the shadow buffer of the trail trace identifier buffer RAM is controlled by the USESB register bit.

RWB:

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the trial trace identifier buffer of the associated tributary. Writing a logic zero to RWB triggers an indirect write operation. Data to be written is taken from the Indirect Tributary Data register. Writing a logic one to RWB triggers an indirect read operation. The read can be found in the Indirect Tributary Data register.

BUSY:

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set high when a write to the Indirect Trail trace Identifier Buffer Address register triggers an indirect access and will stay high until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the Indirect Trail trace Identifier Buffer Data register or to determine when a new indirect write operation may

commence. If LREFCLK disappears during an access, the BUSY bit can stay high.

Register 1567H: TTOP Indirect Trail Trace Identifier Buffer Data

Bit	Type	Function	Default
Bit 7	R/W	D[7]	0
Bit 6	R/W	D[6]	0
Bit 5	R/W	D[5]	0
Bit 4	R/W	D[4]	0
Bit 3	R/W	D[3]	0
Bit 2	R/W	D[2]	0
Bit 1	R/W	D[1]	0
Bit 0	R/W	D[0]	0

This register contains data read from the TTOP Indirect Trail Trace Identifier configuration RAM after an indirect channel read operation or it contains data to be inserted into the Indirect Trail Trace Identifier configuration RAM in an indirect channel write operation.

D[7:0]:

The D[7:0] bits reports the data read from the trail trace identifier buffer associated with the tributary specified by the Trail Trace Identifier Tributary Select register after an indirect read operation has completed. Data to be written to the associated tributary buffer in an indirect write operation must be set up in this register before triggering the write operation. Data in this register reflects the value written until the completion of the subsequent indirect read operation.

1.29 TTMP Transmit Tributary Mapper Registers

Register 1580H, 1581H, 1582H, 1583H, 1584H, 1585H, 1586H: TTMP TU #1 in TUG2 #1 to TUG2 #7of TUG3 #1, Tributary Control

Bit	Type	Function	Default
Bit 7	R/W	TU11	1
Bit 6	R/W	T1	1
Bit 5	R/W	PROV	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	ETVTPTRDIS	0
Bit 1	R/W	ETVT	0
Bit 0	R/W	LAOE	0

LAOE:

The Line Add Bus Output Enable bit, LAOE, enables individual tributaries to be output on the line side telecom bus when the LADDSEL[1:0] bits in the Master SONET/SDH Configuration register are set to “00”. When LADDSEL[1:0] is not set to “00” this register bit has no affect. When LADDSEL[1:0] is set to “00” and LAOE is a logic 1 the tributary payload will be output on the Line Add bus. The line, section and path overhead bits will not be output on the Line Add bus. When LAOE is a logic 0 the tributary will not be output on the Line Add bus. This bit also controls the LAOE Line Add Bus Output Enable pin if the LADDOE bit is set to logic 1 in the Master SONET/SDH Configuration register. LAOE must be set to logic 0 when TVTs are enabled over the Telecom bus in AU3 mode.

ETVT:

The Egress Transparent Virtual Tributary control bit, ETVT, selects a Transparent VT from the SBI bus interface in place of a T1 or E1 mapped into a VT1.5 or VT2. When ETVT is a logic 0 the T1 or E1 will be asynchronous mapped into a virtual tributary in the egress direction. When ETVT is a logic 1 the transparent virtual tributary from the SBI bus will be output in the egress direction. The TU11 bit in this register controls whether the tributary is a TU-11/VT1.5 or a TU-12/VT2.

ETVTPTRDIS:

The Egress Transparent Virtual Tributary pointer disable bit, ETVTPTRDIS, selects whether the V1,V2 pointers with the egress transparent virtual tributary, enabled via the ETVT register bit, are valid. Transparent virtual tributaries from the SBI can be configured to have valid pointers or can use the SBI V5 signal to indicate transparent VT alignment. When the egress transparent VT has a valid pointer and the egress VTPP is in the egress data path, the ETVTPTRDIS bit must be set to 0 so that the egress VTPP will process the pointer and if required align the TVT to the telecom Add bus. When the egress transparent virtual tributary does not have valid pointer the ETVTPTRDIS bit must be set to 1 so that the egress VTPP does not attempt to interpret the V1 and V2 pointers and instead uses the V5 indicator to align the transparent VT.

PROV:

The Provisioned, PROV, bit enables processing of this tributary. When PROV is set high, this tributary is mapped normally into either a VT1.5 Payload or VT2 Payload as controlled by the TU11 and T1 bits. When PROV is set low, this tributary is not processed.

TU11 and T1 Bits:

The TU11 and T1 bits specify the configuration of this tributary.

TU11	T1	Configuration	Active TU (VT)
0	0	E1 in TU-12 (VT2)	#1, #2, #3
0	1	T1 in TU-12	#1, #2, #3
1	X	T1 in TU-11 (VT1.5)	#1, #2, #3, #4

All tributaries in each VT Group must be configured to the same tributary type (i.e. VT1.5 or VT2). In fact, for each VT Group, all tributaries reference the TU11 bit of the first tributary in the group (TU #1). The TU11 bit of all other tributaries in the VT Group are read-only. The T1 bit must be configured the same for each individual tributary.

Register 1588H, 1589H, 158AH, 158BH, 158CH, 158DH, 158EH: TTMP TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #1, Tributary Control

Bit	Type	Function	Default
Bit 7	R/W	TU11	1
Bit 6	R/W	T1	1
Bit 5	R/W	PROV	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	ETVTPTRDIS	0
Bit 1	R/W	ETVT	0
Bit 0	R/W	LAOE	0

LAOE:

The Line Add Bus Output Enable bit, LAOE, enables individual tributaries to be output on the line side telecom bus when the LADDSEL[1:0] bits in the Master SONET/SDH Configuration register are set to “00”. When LADDSEL[1:0] is not set to “00” this register bit has no affect. When LADDSEL[1:0] is set to “00” and LAOE is a logic 1 the tributary payload will be output on the Line Add bus. The line, section and path overhead bits will not be output on the Line Add bus. When LAOE is a logic 0 the tributary will not be output on the Line Add bus. This bit also controls the LAOE Line Add Bus Output Enable pin if the LADDOE bit is set to logic 1 in the Master SONET/SDH Configuration register. LAOE must be set to logic 0 when TVTs are enabled over the Telecom bus in AU3 mode.

ETVT:

The Egress Transparent Virtual Tributary control bit, ETVT, selects a Transparent VT from the SBI bus interface in place of a T1 or E1 mapped into a VT1.5 or VT2. When ETVT is a logic 0 the T1 or E1 will be asynchronous mapped into a virtual tributary in the egress direction. When ETVT is a logic 1 the transparent virtual tributary from the SBI bus will be output in the egress direction. The TU11 bit in this register controls whether the tributary is a TU-11/VT1.5 or a TU-12/VT2.

ETVTPTRDIS:

The Egress Transparent Virtual Tributary pointer disable bit, ETVTPTRDIS, selects whether the V1,V2 pointers with the egress transparent virtual

tributary, enabled via the ETVT register bit, are valid. Transparent virtual tributaries from the SBI can be configured to have valid pointers or can use the SBI V5 signal to indicate transparent VT alignment. When the egress transparent VT has a valid pointer and the egress VTPP is in the egress data path, the ETVTPTRDIS bit must be set to 0 so that the egress VTPP will process the pointer and if required align the TVT to the telecom Add bus. When the egress transparent virtual tributary does not have valid pointer the ETVTPTRDIS bit must be set to 1 so that the egress VTPP does not attempt to interpret the V1 and V2 pointers and instead uses the V5 indicator to align the transparent VT.

PROV:

The Provisioned, PROV, bit enables processing of this tributary. When PROV is set high, this tributary is mapped normally into either a VT1.5 Payload or VT2 Payload as controlled by the TU11 and T1 bits. When PROV is set low, this tributary is not processed.

TU11 and T1 Bits:

The TU11 and T1 bits specify the configuration of this tributary.

TU11	T1	Configuration	Active TU (VT)
0	0	E1 in TU-12 (VT2)	#1, #2, #3
0	1	T1 in TU-12	#1, #2, #3
1	X	T1 in TU-11 (VT1.5)	#1, #2, #3, #4

All tributaries in each VT Group must be configured to the same tributary type (i.e. VT1.5 or VT2). In fact, for each VT Group, all tributaries reference the TU11 bit of the first tributary in the group (TU #1). The TU11 bit of all other tributaries in the VT Group are read-only. The T1 bit must be configured the same for each individual tributary.

Register 1590H, 1591H, 1592H, 1593H, 1594H, 1595H, 1596H: TTMP TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #1, Tributary Control

Bit	Type	Function	Default
Bit 7	R/W	TU11	1
Bit 6	R/W	T1	1
Bit 5	R/W	PROV	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	ETVTPTRDIS	0
Bit 1	R/W	ETVT	0
Bit 0	R/W	LAOE	0

LAOE:

The Line Add Bus Output Enable bit, LAOE, enables individual tributaries to be output on the line side telecom bus when the LADDSEL[1:0] bits in the Master SONET/SDH Configuration register are set to “00”. When LADDSEL[1:0] is not set to “00” this register bit has no affect. When LADDSEL[1:0] is set to “00” and LAOE is a logic 1 the tributary payload will be output on the Line Add bus. The line, section and path overhead bits will not be output on the Line Add bus. When LAOE is a logic 0 the tributary will not be output on the Line Add bus. This bit also controls the LAOE Line Add Bus Output Enable pin if the LADDOE bit is set to logic 1 in the Master SONET/SDH Configuration register. LAOE must be set to logic 0 when TVTs are enabled over the Telecom bus in AU3 mode.

ETVT:

The Egress Transparent Virtual Tributary control bit, ETVT, selects a Transparent VT from the SBI bus interface in place of a T1 or E1 mapped into a VT1.5 or VT2. When ETVT is a logic 0 the T1 or E1 will be asynchronous mapped into a virtual tributary in the egress direction. When ETVT is a logic 1 the transparent virtual tributary from the SBI bus will be output in the egress direction. The TU11 bit in this register controls whether the tributary is a TU-11/VT1.5 or a TU-12/VT2.

ETVTPTRDIS:

The Egress Transparent Virtual Tributary pointer disable bit, ETVTPTRDIS, selects whether the V1,V2 pointers with the egress transparent virtual

tributary, enabled via the ETVT register bit, are valid. Transparent virtual tributaries from the SBI can be configured to have valid pointers or can use the SBI V5 signal to indicate transparent VT alignment. When the egress transparent VT has a valid pointer and the egress VTPP is in the egress data path, the ETVTPTRDIS bit must be set to 0 so that the egress VTPP will process the pointer and if required align the TVT to the telecom Add bus. When the egress transparent virtual tributary does not have valid pointer the ETVTPTRDIS bit must be set to 1 so that the egress VTPP does not attempt to interpret the V1 and V2 pointers and instead uses the V5 indicator to align the transparent VT.

PROV:

The Provisioned, PROV, bit enables processing of this tributary. When PROV is set high, this tributary is mapped normally into either a VT1.5 Payload or VT2 Payload as controlled by the TU11 and T1 bits. When PROV is set low, this tributary is not processed.

TU11 and T1 Bits:

The TU11 and T1 bits specify the configuration of this tributary.

TU11	T1	Configuration	Active TU (VT)
0	0	E1 in TU-12 (VT2)	#1, #2, #3
0	1	T1 in TU-12	#1, #2, #3
1	X	T1 in TU-11 (VT1.5)	#1, #2, #3, #4

All tributaries in each VT Group must be configured to the same tributary type (i.e. VT1.5 or VT2). In fact, for each VT Group, all tributaries reference the TU11 bit of the first tributary in the group (TU #1). The TU11 bit of all other tributaries in the VT Group are read-only. The T1 bit must be configured the same for each individual tributary.

Register 1598H, 1599H, 159AH, 159BH, 159CH, 159DH, 159EH: TTMP TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #1, Tributary Control

Bit	Type	Function	Default
Bit 7	R/W	TU11	1
Bit 6	R/W	T1	1
Bit 5	R/W	PROV	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	ETVTPTRDIS	0
Bit 1	R/W	ETVT	0
Bit 0	R/W	LAOE	0

LAOE:

The Line Add Bus Output Enable bit, LAOE, enables individual tributaries to be output on the line side telecom bus when the LADDSEL[1:0] bits in the Master SONET/SDH Configuration register are set to “00”. When LADDSEL[1:0] is not set to “00” this register bit has no affect. When LADDSEL[1:0] is set to “00” and LAOE is a logic 1 the tributary payload will be output on the Line Add bus. The line, section and path overhead bits will not be output on the Line Add bus. When LAOE is a logic 0 the tributary will not be output on the Line Add bus. This bit also controls the LAOE Line Add Bus Output Enable pin if the LADDOE bit is set to logic 1 in the Master SONET/SDH Configuration register. LAOE must be set to logic 0 when TVTs are enabled over the Telecom bus in AU3 mode.

ETVT:

The Egress Transparent Virtual Tributary control bit, ETVT, selects a Transparent VT from the SBI bus interface in place of a T1 or E1 mapped into a VT1.5 or VT2. When ETVT is a logic 0 the T1 or E1 will be asynchronous mapped into a virtual tributary in the egress direction. When ETVT is a logic 1 the transparent virtual tributary from the SBI bus will be output in the egress direction. The TU11 bit in this register controls whether the tributary is a TU-11/VT1.5 or a TU-12/VT2.

ETVTPTRDIS:

The Egress Transparent Virtual Tributary pointer disable bit, ETVTPTRDIS, selects whether the V1,V2 pointers with the egress transparent virtual

tributary, enabled via the ETVT register bit, are valid. Transparent virtual tributaries from the SBI can be configured to have valid pointers or can use the SBI V5 signal to indicate transparent VT alignment. When the egress transparent VT has a valid pointer and the egress VTPP is in the egress data path, the ETVTPTRDIS bit must be set to 0 so that the egress VTPP will process the pointer and if required align the TVT to the telecom Add bus. When the egress transparent virtual tributary does not have valid pointer the ETVTPTRDIS bit must be set to 1 so that the egress VTPP does not attempt to interpret the V1 and V2 pointers and instead uses the V5 indicator to align the transparent VT.

PROV:

The Provisioned, PROV, bit enables processing of this tributary. When PROV is set high, this tributary is mapped normally into either a VT1.5 Payload or VT2 Payload as controlled by the TU11 and T1 bits. When PROV is set low, this tributary is not processed.

TU11 and T1 Bits:

The TU11 and T1 bits specify the configuration of this tributary.

TU11	T1	Configuration	Active TU (VT)
0	0	E1 in TU-12 (VT2)	#1, #2, #3
0	1	T1 in TU-12	#1, #2, #3
1	X	T1 in TU-11 (VT1.5)	#1, #2, #3, #4

All tributaries in each VT Group must be configured to the same tributary type (i.e. VT1.5 or VT2). In fact, for each VT Group, all tributaries reference the TU11 bit of the first tributary in the group (TU #1). The TU11 bit of all other tributaries in the VT Group are read-only. The T1 bit must be configured the same for each individual tributary.

Register 15A0H, 15A1H, 15A2H, 15A3H, 15A4H, 15A5H, 15A6H: TTMP TU #1 in TUG2 #1 to TUG2 #7 of TUG3 #2, Tributary Control

Bit	Type	Function	Default
Bit 7	R/W	TU11	1
Bit 6	R/W	T1	1
Bit 5	R/W	PROV	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	ETVTPTRDIS	0
Bit 1	R/W	ETVT	0
Bit 0	R/W	LAOE	0

LAOE:

The Line Add Bus Output Enable bit, LAOE, enables individual tributaries to be output on the line side telecom bus when the LADDSEL[1:0] bits in the Master SONET/SDH Configuration register are set to “00”. When LADDSEL[1:0] is not set to “00” this register bit has no affect. When LADDSEL[1:0] is set to “00” and LAOE is a logic 1 the tributary payload will be output on the Line Add bus. The line, section and path overhead bits will not be output on the Line Add bus. When LAOE is a logic 0 the tributary will not be output on the Line Add bus.This bit also controls the LAOE Line Add Bus Output Enable pin if the LADDOE bit is set to logic 1 in the Master SONET/SDH Configuration register. LAOE must be set to logic 0 when TVTs are enabled over the Telecom bus in AU3 mode.

ETVT:

The Egress Transparent Virtual Tributary control bit, ETVT, selects a Transparent VT from the SBI bus interface in place of a T1 or E1 mapped into a VT1.5 or VT2. When ETVT is a logic 0 the T1 or E1 will be asynchronous mapped into a virtual tributary in the egress direction. When ETVT is a logic 1 the transparent virtual tributary from the SBI bus will be output in the egress direction. The TU11 bit in this register controls whether the tributary is a TU-11/VT1.5 or a TU-12/VT2.

ETVTPTRDIS:

The Egress Transparent Virtual Tributary pointer disable bit, ETVTPTRDIS, selects whether the V1,V2 pointers with the egress transparent virtual

tributary, enabled via the ETVT register bit, are valid. Transparent virtual tributaries from the SBI can be configured to have valid pointers or can use the SBI V5 signal to indicate transparent VT alignment. When the egress transparent VT has a valid pointer and the egress VTPP is in the egress data path, the ETVTPTRDIS bit must be set to 0 so that the egress VTPP will process the pointer and if required align the TVT to the telecom Add bus. When the egress transparent virtual tributary does not have valid pointer the ETVTPTRDIS bit must be set to 1 so that the egress VTPP does not attempt to interpret the V1 and V2 pointers and instead uses the V5 indicator to align the transparent VT.

PROV:

The Provisioned, PROV, bit enables processing of this tributary. When PROV is set high, this tributary is mapped normally into either a VT1.5 Payload or VT2 Payload as controlled by the TU11 and T1 bits. When PROV is set low, this tributary is not processed.

TU11 and T1 Bits:

The TU11 and T1 bits specify the configuration of this tributary.

TU11	T1	Configuration	Active TU (VT)
0	0	E1 in TU-12 (VT2)	#1, #2, #3
0	1	T1 in TU-12	#1, #2, #3
1	X	T1 in TU-11 (VT1.5)	#1, #2, #3, #4

All tributaries in each VT Group must be configured to the same tributary type (i.e. VT1.5 or VT2). In fact, for each VT Group, all tributaries reference the TU11 bit of the first tributary in the group (TU #1). The TU11 bit of all other tributaries in the VT Group are read-only. The T1 bit must be configured the same for each individual tributary.

Register 15A8H, 15A9H, 15AAH, 15ABH, 15ACH, 15ADH, 15AEH: TTMP TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #2, Tributary Control

Bit	Type	Function	Default
Bit 7	R/W	TU11	1
Bit 6	R/W	T1	1
Bit 5	R/W	PROV	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	ETVTPTRDIS	0
Bit 1	R/W	ETVT	0
Bit 0	R/W	LAOE	0

LAOE:

The Line Add Bus Output Enable bit, LAOE, enables individual tributaries to be output on the line side telecom bus when the LADDSEL[1:0] bits in the Master SONET/SDH Configuration register are set to “00”. When LADDSEL[1:0] is not set to “00” this register bit has no affect. When LADDSEL[1:0] is set to “00” and LAOE is a logic 1 the tributary payload will be output on the Line Add bus. The line, section and path overhead bits will not be output on the Line Add bus. When LAOE is a logic 0 the tributary will not be output on the Line Add bus.This bit also controls the LAOE Line Add Bus Output Enable pin if the LADDOE bit is set to logic 1 in the Master SONET/SDH Configuration register. LAOE must be set to logic 0 when TVTs are enabled over the Telecom bus in AU3 mode.

ETVT:

The Egress Transparent Virtual Tributary control bit, ETVT, selects a Transparent VT from the SBI bus interface in place of a T1 or E1 mapped into a VT1.5 or VT2. When ETVT is a logic 0 the T1 or E1 will be asynchronous mapped into a virtual tributary in the egress direction. When ETVT is a logic 1 the transparent virtual tributary from the SBI bus will be output in the egress direction. The TU11 bit in this register controls whether the tributary is a TU-11/VT1.5 or a TU-12/VT2.

ETVTPTRDIS:

The Egress Transparent Virtual Tributary pointer disable bit, ETVTPTRDIS, selects whether the V1,V2 pointers with the egress transparent virtual

tributary, enabled via the ETVT register bit, are valid. Transparent virtual tributaries from the SBI can be configured to have valid pointers or can use the SBI V5 signal to indicate transparent VT alignment. When the egress transparent VT has a valid pointer and the egress VTPP is in the egress data path, the ETVTPTRDIS bit must be set to 0 so that the egress VTPP will process the pointer and if required align the TVT to the telecom Add bus. When the egress transparent virtual tributary does not have valid pointer the ETVTPTRDIS bit must be set to 1 so that the egress VTPP does not attempt to interpret the V1 and V2 pointers and instead uses the V5 indicator to align the transparent VT.

PROV:

The Provisioned, PROV, bit enables processing of this tributary. When PROV is set high, this tributary is mapped normally into either a VT1.5 Payload or VT2 Payload as controlled by the TU11 and T1 bits. When PROV is set low, this tributary is not processed.

TU11 and T1 Bits:

The TU11 and T1 bits specify the configuration of this tributary.

TU11	T1	Configuration	Active TU (VT)
0	0	E1 in TU-12 (VT2)	#1, #2, #3
0	1	T1 in TU-12	#1, #2, #3
1	X	T1 in TU-11 (VT1.5)	#1, #2, #3, #4

All tributaries in each VT Group must be configured to the same tributary type (i.e. VT1.5 or VT2). In fact, for each VT Group, all tributaries reference the TU11 bit of the first tributary in the group (TU #1). The TU11 bit of all other tributaries in the VT Group are read-only. The T1 bit must be configured the same for each individual tributary.

Register 15B0H, 15B1H, 15B2H, 15B3H, 15B4H, 15B5H, 15B6H: TTMP TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #2, Tributary Control

Bit	Type	Function	Default
Bit 7	R/W	TU11	1
Bit 6	R/W	T1	1
Bit 5	R/W	PROV	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	ETVTPTRDIS	0
Bit 1	R/W	ETVT	0
Bit 0	R/W	LAOE	0

LAOE:

The Line Add Bus Output Enable bit, LAOE, enables individual tributaries to be output on the line side telecom bus when the LADDSEL[1:0] bits in the Master SONET/SDH Configuration register are set to “00”. When LADDSEL[1:0] is not set to “00” this register bit has no affect. When LADDSEL[1:0] is set to “00” and LAOE is a logic 1 the tributary payload will be output on the Line Add bus. The line, section and path overhead bits will not be output on the Line Add bus. When LAOE is a logic 0 the tributary will not be output on the Line Add bus. This bit also controls the LAOE Line Add Bus Output Enable pin if the LADDOE bit is set to logic 1 in the Master SONET/SDH Configuration register. LAOE must be set to logic 0 when TVTs are enabled over the Telecom bus in AU3 mode.

ETVT:

The Egress Transparent Virtual Tributary control bit, ETVT, selects a Transparent VT from the SBI bus interface in place of a T1 or E1 mapped into a VT1.5 or VT2. When ETVT is a logic 0 the T1 or E1 will be asynchronous mapped into a virtual tributary in the egress direction. When ETVT is a logic 1 the transparent virtual tributary from the SBI bus will be output in the egress direction. The TU11 bit in this register controls whether the tributary is a TU-11/VT1.5 or a TU-12/VT2.

ETVTPTRDIS:

The Egress Transparent Virtual Tributary pointer disable bit, ETVTPTRDIS, selects whether the V1,V2 pointers with the egress transparent virtual

tributary, enabled via the ETVT register bit, are valid. Transparent virtual tributaries from the SBI can be configured to have valid pointers or can use the SBI V5 signal to indicate transparent VT alignment. When the egress transparent VT has a valid pointer and the egress VTPP is in the egress data path, the ETVTPTRDIS bit must be set to 0 so that the egress VTPP will process the pointer and if required align the TVT to the telecom Add bus. When the egress transparent virtual tributary does not have valid pointer the ETVTPTRDIS bit must be set to 1 so that the egress VTPP does not attempt to interpret the V1 and V2 pointers and instead uses the V5 indicator to align the transparent VT.

PROV:

The Provisioned, PROV, bit enables processing of this tributary. When PROV is set high, this tributary is mapped normally into either a VT1.5 Payload or VT2 Payload as controlled by the TU11 and T1 bits. When PROV is set low, this tributary is not processed.

TU11 and T1 Bits:

The TU11 and T1 bits specify the configuration of this tributary.

TU11	T1	Configuration	Active TU (VT)
0	0	E1 in TU-12 (VT2)	#1, #2, #3
0	1	T1 in TU-12	#1, #2, #3
1	X	T1 in TU-11 (VT1.5)	#1, #2, #3, #4

All tributaries in each VT Group must be configured to the same tributary type (i.e. VT1.5 or VT2). In fact, for each VT Group, all tributaries reference the TU11 bit of the first tributary in the group (TU #1). The TU11 bit of all other tributaries in the VT Group are read-only. The T1 bit must be configured the same for each individual tributary.

Register 15B8H, 15B9H, 15BAH, 15BBH, 15BCH, 15BDH, 15BEH: TTMP TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #2, Tributary Control

Bit	Type	Function	Default
Bit 7	R/W	TU11	1
Bit 6	R/W	T1	1
Bit 5	R/W	PROV	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	ETVTPTRDIS	0
Bit 1	R/W	ETVT	0
Bit 0	R/W	LAOE	0

LAOE:

The Line Add Bus Output Enable bit, LAOE, enables individual tributaries to be output on the line side telecom bus when the LADDSEL[1:0] bits in the Master SONET/SDH Configuration register are set to “00”. When LADDSEL[1:0] is not set to “00” this register bit has no affect. When LADDSEL[1:0] is set to “00” and LAOE is a logic 1 the tributary payload will be output on the Line Add bus. The line, section and path overhead bits will not be output on the Line Add bus. When LAOE is a logic 0 the tributary will not be output on the Line Add bus.This bit also controls the LAOE Line Add Bus Output Enable pin if the LADDOE bit is set to logic 1 in the Master SONET/SDH Configuration register. LAOE must be set to logic 0 when TVTs are enabled over the Telecom bus in AU3 mode.

ETVT:

The Egress Transparent Virtual Tributary control bit, ETVT, selects a Transparent VT from the SBI bus interface in place of a T1 or E1 mapped into a VT1.5 or VT2. When ETVT is a logic 0 the T1 or E1 will be asynchronous mapped into a virtual tributary in the egress direction. When ETVT is a logic 1 the transparent virtual tributary from the SBI bus will be output in the egress direction. The TU11 bit in this register controls whether the tributary is a TU-11/VT1.5 or a TU-12/VT2.

ETVTPTRDIS:

The Egress Transparent Virtual Tributary pointer disable bit, ETVTPTRDIS, selects whether the V1,V2 pointers with the egress transparent virtual

tributary, enabled via the ETVT register bit, are valid. Transparent virtual tributaries from the SBI can be configured to have valid pointers or can use the SBI V5 signal to indicate transparent VT alignment. When the egress transparent VT has a valid pointer and the egress VTPP is in the egress data path, the ETVTPTRDIS bit must be set to 0 so that the egress VTPP will process the pointer and if required align the TVT to the telecom Add bus. When the egress transparent virtual tributary does not have valid pointer the ETVTPTRDIS bit must be set to 1 so that the egress VTPP does not attempt to interpret the V1 and V2 pointers and instead uses the V5 indicator to align the transparent VT.

PROV:

The Provisioned, PROV, bit enables processing of this tributary. When PROV is set high, this tributary is mapped normally into either a VT1.5 Payload or VT2 Payload as controlled by the TU11 and T1 bits. When PROV is set low, this tributary is not processed.

TU11 and T1 Bits:

The TU11 and T1 bits specify the configuration of this tributary.

TU11	T1	Configuration	Active TU (VT)
0	0	E1 in TU-12 (VT2)	#1, #2, #3
0	1	T1 in TU-12	#1, #2, #3
1	X	T1 in TU-11 (VT1.5)	#1, #2, #3, #4

All tributaries in each VT Group must be configured to the same tributary type (i.e. VT1.5 or VT2). In fact, for each VT Group, all tributaries reference the TU11 bit of the first tributary in the group (TU #1). The TU11 bit of all other tributaries in the VT Group are read-only. The T1 bit must be configured the same for each individual tributary.

Register 15C0H, 15C1H, 15C2H, 15C3H, 15C4H, 15C5H, 15C6H: TTMP TU #1 in TUG2 #1 to TUG2 #7 of TUG3 #3, Tributary Control

Bit	Type	Function	Default
Bit 7	R/W	TU11	1
Bit 6	R/W	T1	1
Bit 5	R/W	PROV	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	ETVTPTRDIS	0
Bit 1	R/W	ETVT	0
Bit 0	R/W	LAOE	0

LAOE:

The Line Add Bus Output Enable bit, LAOE, enables individual tributaries to be output on the line side telecom bus when the LADDSEL[1:0] bits in the Master SONET/SDH Configuration register are set to “00”. When LADDSEL[1:0] is not set to “00” this register bit has no affect. When LADDSEL[1:0] is set to “00” and LAOE is a logic 1 the tributary payload will be output on the Line Add bus. The line, section and path overhead bits will not be output on the Line Add bus. When LAOE is a logic 0 the tributary will not be output on the Line Add bus.This bit also controls the LAOE Line Add Bus Output Enable pin if the LADDOE bit is set to logic 1 in the Master SONET/SDH Configuration register. LAOE must be set to logic 0 when TVTs are enabled over the Telecom bus in AU3 mode.

ETVT:

The Egress Transparent Virtual Tributary control bit, ETVT, selects a Transparent VT from the SBI bus interface in place of a T1 or E1 mapped into a VT1.5 or VT2. When ETVT is a logic 0 the T1 or E1 will be asynchronous mapped into a virtual tributary in the egress direction. When ETVT is a logic 1 the transparent virtual tributary from the SBI bus will be output in the egress direction. The TU11 bit in this register controls whether the tributary is a TU-11/VT1.5 or a TU-12/VT2.

ETVTPTRDIS:

The Egress Transparent Virtual Tributary pointer disable bit, ETVTPTRDIS, selects whether the V1,V2 pointers with the egress transparent virtual

tributary, enabled via the ETVT register bit, are valid. Transparent virtual tributaries from the SBI can be configured to have valid pointers or can use the SBI V5 signal to indicate transparent VT alignment. When the egress transparent VT has a valid pointer and the egress VTPP is in the egress data path, the ETVTPTRDIS bit must be set to 0 so that the egress VTPP will process the pointer and if required align the TVT to the telecom Add bus. When the egress transparent virtual tributary does not have valid pointer the ETVTPTRDIS bit must be set to 1 so that the egress VTPP does not attempt to interpret the V1 and V2 pointers and instead uses the V5 indicator to align the transparent VT.

PROV:

The Provisioned, PROV, bit enables processing of this tributary. When PROV is set high, this tributary is mapped normally into either a VT1.5 Payload or VT2 Payload as controlled by the TU11 and T1 bits. When PROV is set low, this tributary is not processed.

TU11 and T1 Bits:

The TU11 and T1 bits specify the configuration of this tributary.

TU11	T1	Configuration	Active TU (VT)
0	0	E1 in TU-12 (VT2)	#1, #2, #3
0	1	T1 in TU-12	#1, #2, #3
1	X	T1 in TU-11 (VT1.5)	#1, #2, #3, #4

All tributaries in each VT Group must be configured to the same tributary type (i.e. VT1.5 or VT2). In fact, for each VT Group, all tributaries reference the TU11 bit of the first tributary in the group (TU #1). The TU11 bit of all other tributaries in the VT Group are read-only. The T1 bit must be configured the same for each individual tributary.

Register 15C8H, 15C9H, 15CAH, 15CBH, 15CCH, 15CDH, 15CEH: TTMP TU #2 in TUG2 #1 to TUG2 #7 of TUG3 #3, Tributary Control

Bit	Type	Function	Default
Bit 7	R/W	TU11	1
Bit 6	R/W	T1	1
Bit 5	R/W	PROV	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	ETVTPTRDIS	0
Bit 1	R/W	ETVT	0
Bit 0	R/W	LAOE	0

LAOE:

The Line Add Bus Output Enable bit, LAOE, enables individual tributaries to be output on the line side telecom bus when the LADDSEL[1:0] bits in the Master SONET/SDH Configuration register are set to “00”. When LADDSEL[1:0] is not set to “00” this register bit has no affect. When LADDSEL[1:0] is set to “00” and LAOE is a logic 1 the tributary payload will be output on the Line Add bus. The line, section and path overhead bits will not be output on the Line Add bus. When LAOE is a logic 0 the tributary will not be output on the Line Add bus. This bit also controls the LAOE Line Add Bus Output Enable pin if the LADDOE bit is set to logic 1 in the Master SONET/SDH Configuration register. LAOE must be set to logic 0 when TVTs are enabled over the Telecom bus in AU3 mode.

ETVT:

The Egress Transparent Virtual Tributary control bit, ETVT, selects a Transparent VT from the SBI bus interface in place of a T1 or E1 mapped into a VT1.5 or VT2. When ETVT is a logic 0 the T1 or E1 will be asynchronous mapped into a virtual tributary in the egress direction. When ETVT is a logic 1 the transparent virtual tributary from the SBI bus will be output in the egress direction. The TU11 bit in this register controls whether the tributary is a TU-11/VT1.5 or a TU-12/VT2.

ETVTPTRDIS:

The Egress Transparent Virtual Tributary pointer disable bit, ETVTPTRDIS, selects whether the V1,V2 pointers with the egress transparent virtual

tributary, enabled via the ETVT register bit, are valid. Transparent virtual tributaries from the SBI can be configured to have valid pointers or can use the SBI V5 signal to indicate transparent VT alignment. When the egress transparent VT has a valid pointer and the egress VTPP is in the egress data path, the ETVTPTRDIS bit must be set to 0 so that the egress VTPP will process the pointer and if required align the TVT to the telecom Add bus. When the egress transparent virtual tributary does not have valid pointer the ETVTPTRDIS bit must be set to 1 so that the egress VTPP does not attempt to interpret the V1 and V2 pointers and instead uses the V5 indicator to align the transparent VT.

PROV:

The Provisioned, PROV, bit enables processing of this tributary. When PROV is set high, this tributary is mapped normally into either a VT1.5 Payload or VT2 Payload as controlled by the TU11 and T1 bits. When PROV is set low, this tributary is not processed.

TU11 and T1 Bits:

The TU11 and T1 bits specify the configuration of this tributary.

TU11	T1	Configuration	Active TU (VT)
0	0	E1 in TU-12 (VT2)	#1, #2, #3
0	1	T1 in TU-12	#1, #2, #3
1	X	T1 in TU-11 (VT1.5)	#1, #2, #3, #4

All tributaries in each VT Group must be configured to the same tributary type (i.e. VT1.5 or VT2). In fact, for each VT Group, all tributaries reference the TU11 bit of the first tributary in the group (TU #1). The TU11 bit of all other tributaries in the VT Group are read-only. The T1 bit must be configured the same for each individual tributary.

Register 15D0H, 15D1H, 15D2H, 15D3H, 15D4H, 15D5H, 15D6H: TTMP TU #3 in TUG2 #1 to TUG2 #7 of TUG3 #3, Tributary Control

Bit	Type	Function	Default
Bit 7	R/W	TU11	1
Bit 6	R/W	T1	1
Bit 5	R/W	PROV	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	ETVTPTRDIS	0
Bit 1	R/W	ETVT	0
Bit 0	R/W	LAOE	0

LAOE:

The Line Add Bus Output Enable bit, LAOE, enables individual tributaries to be output on the line side telecom bus when the LADDSEL[1:0] bits in the Master SONET/SDH Configuration register are set to “00”. When LADDSEL[1:0] is not set to “00” this register bit has no affect. When LADDSEL[1:0] is set to “00” and LAOE is a logic 1 the tributary payload will be output on the Line Add bus. The line, section and path overhead bits will not be output on the Line Add bus. When LAOE is a logic 0 the tributary will not be output on the Line Add bus. This bit also controls the LAOE Line Add Bus Output Enable pin if the LADDOE bit is set to logic 1 in the Master SONET/SDH Configuration register. LAOE must be set to logic 0 when TVTs are enabled over the Telecom bus in AU3 mode.

ETVT:

The Egress Transparent Virtual Tributary control bit, ETVT, selects a Transparent VT from the SBI bus interface in place of a T1 or E1 mapped into a VT1.5 or VT2. When ETVT is a logic 0 the T1 or E1 will be asynchronous mapped into a virtual tributary in the egress direction. When ETVT is a logic 1 the transparent virtual tributary from the SBI bus will be output in the egress direction. The TU11 bit in this register controls whether the tributary is a TU-11/VT1.5 or a TU-12/VT2.

ETVTPTRDIS:

The Egress Transparent Virtual Tributary pointer disable bit, ETVTPTRDIS, selects whether the V1,V2 pointers with the egress transparent virtual

tributary, enabled via the ETVT register bit, are valid. Transparent virtual tributaries from the SBI can be configured to have valid pointers or can use the SBI V5 signal to indicate transparent VT alignment. When the egress transparent VT has a valid pointer and the egress VTPP is in the egress data path, the ETVTPTRDIS bit must be set to 0 so that the egress VTPP will process the pointer and if required align the TVT to the telecom Add bus. When the egress transparent virtual tributary does not have valid pointer the ETVTPTRDIS bit must be set to 1 so that the egress VTPP does not attempt to interpret the V1 and V2 pointers and instead uses the V5 indicator to align the transparent VT.

PROV:

The Provisioned, PROV, bit enables processing of this tributary. When PROV is set high, this tributary is mapped normally into either a VT1.5 Payload or VT2 Payload as controlled by the TU11 and T1 bits. When PROV is set low, this tributary is not processed.

TU11 and T1 Bits:

The TU11 and T1 bits specify the configuration of this tributary.

TU11	T1	Configuration	Active TU (VT)
0	0	E1 in TU-12 (VT2)	#1, #2, #3
0	1	T1 in TU-12	#1, #2, #3
1	X	T1 in TU-11 (VT1.5)	#1, #2, #3, #4

All tributaries in each VT Group must be configured to the same tributary type (i.e. VT1.5 or VT2). In fact, for each VT Group, all tributaries reference the TU11 bit of the first tributary in the group (TU #1). The TU11 bit of all other tributaries in the VT Group are read-only. The T1 bit must be configured the same for each individual tributary.

Register 15D8H, 15D9H, 15DAH, 15DBH, 15DCH, 15DDH, 15DEH: TTMP TU #4 in TUG2 #1 to TUG2 #7 of TUG3 #3, Tributary Control

Bit	Type	Function	Default
Bit 7	R/W	TU11	1
Bit 6	R/W	T1	1
Bit 5	R/W	PROV	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	ETVTPTRDIS	0
Bit 1	R/W	ETVT	0
Bit 0	R/W	LAOE	0

LAOE:

The Line Add Bus Output Enable bit, LAOE, enables individual tributaries to be output on the line side telecom bus when the LADDSEL[1:0] bits in the Master SONET/SDH Configuration register are set to “00”. When LADDSEL[1:0] is not set to “00” this register bit has no affect. When LADDSEL[1:0] is set to “00” and LAOE is a logic 1 the tributary payload will be output on the Line Add bus. The line, section and path overhead bits will not be output on the Line Add bus. When LAOE is a logic 0 the tributary will not be output on the Line Add bus. This bit also controls the LAOE Line Add Bus Output Enable pin if the LADDOE bit is set to logic 1 in the Master SONET/SDH Configuration register. LAOE must be set to logic 0 when TVTs are enabled over the Telecom bus in AU3 mode.

ETVT:

The Egress Transparent Virtual Tributary control bit, ETVT, selects a Transparent VT from the SBI bus interface in place of a T1 or E1 mapped into a VT1.5 or VT2. When ETVT is a logic 0 the T1 or E1 will be asynchronous mapped into a virtual tributary in the egress direction. When ETVT is a logic 1 the transparent virtual tributary from the SBI bus will be output in the egress direction. The TU11 bit in this register controls whether the tributary is a TU-11/VT1.5 or a TU-12/VT2.

ETVTPTRDIS:

The Egress Transparent Virtual Tributary pointer disable bit, ETVTPTRDIS, selects whether the V1,V2 pointers with the egress transparent virtual

tributary, enabled via the ETVT register bit, are valid. Transparent virtual tributaries from the SBI can be configured to have valid pointers or can use the SBI V5 signal to indicate transparent VT alignment. When the egress transparent VT has a valid pointer and the egress VTPP is in the egress data path, the ETVTPTRDIS bit must be set to 0 so that the egress VTPP will process the pointer and if required align the TVT to the telecom Add bus. When the egress transparent virtual tributary does not have valid pointer the ETVTPTRDIS bit must be set to 1 so that the egress VTPP does not attempt to interpret the V1 and V2 pointers and instead uses the V5 indicator to align the transparent VT.

PROV:

The Provisioned, PROV, bit enables processing of this tributary. When PROV is set high, this tributary is mapped normally into either a VT1.5 Payload or VT2 Payload as controlled by the TU11 and T1 bits. When PROV is set low, this tributary is not processed.

TU11 and T1 Bits:

The TU11 and T1 bits specify the configuration of this tributary.

TU11	T1	Configuration	Active TU (VT)
0	0	E1 in TU-12 (VT2)	#1, #2, #3
0	1	T1 in TU-12	#1, #2, #3
1	X	T1 in TU-11 (VT1.5)	#1, #2, #3, #4

All tributaries in each VT Group must be configured to the same tributary type (i.e. VT1.5 or VT2). In fact, for each VT Group, all tributaries reference the TU11 bit of the first tributary in the group (TU #1). The TU11 bit of all other tributaries in the VT Group are read-only. The T1 bit must be configured the same for each individual tributary.

Register 15E1H: TTMP Time Switch Page Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	APAGE	0

This register allows selection of one of two pages in the time switch configuration RAM to be the active page.

APAGE:

The time switch configuration RAM active page select bit, APAGE, controls the selection of one of two pages in the time switch configuration RAM to be the active page. When APAGE is set high, the configuration in page 1 of the time switch configuration RAM is used to associate outgoing VT Payloads to logical FIFOs in the payload buffer. When APAGE is set low, the configuration in page 0 of the time switch configuration RAM is used to associate outgoing VT Payloads to logical FIFOs in the payload buffer. Changes of the active page as a result of write accesses to APAGE are synchronized to SCLK and effective immediately.

Register 15E2H: TTMP Indirect Time Switch RAM Control and Status

Bit	Type	Function	Default
Bit 7	R	BUSY	X
Bit 6	R/W	RWB	1
Bit 5	R/W	PAGE	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register provides control and status for the indirect RAM containing time switch tributary information. Writing to this register triggers an indirect time switch configuration register access. Note that when an indirect write access is to be performed, the Indirect Time Switch Internal Link Data register and the Indirect Egress Tributary Address register must first be setup before writing to this register.

PAGE:

The indirect page select bit, PAGE, selects between accesses to the two pages in the time switch configuration RAM. When PAGE is set high, page 1 of the time switch configuration RAM is accessed. When PAGE is set low, page 0 of the RAM is accessed. The PAGE bit should be different than the APAGE bit (register 061H) when writing to the RAM as writing to the active page is not recommended.

RWB:

The indirect access control bit, RWB, selects between a configure (write) or interrogate (read) access to the time switch configuration RAM. Writing a logic zero to RWB triggers an indirect write operation. Data to be written is taken from the Indirect Time Switch Tributary register. Writing a logic one to RWB triggers an indirect read operation. The read can be found in the Indirect Tributary Data register.

BUSY:

The BUSY bit reports the status of the prevailing indirect access operation. BUSY is set high when a write to the Indirect Time Switch Tributary Address

register triggers an indirect access and remains high until the access is complete. The BUSY bit should be polled until it is low to determine when data from an indirect read operation is available in the Indirect Tributary Data register or when a new indirect write operation may commence. If LREFCLK disappears during an access, the BUSY bit can stay high.

Register 15E3H: TTMP Indirect Egress Tributary Address

Bit	Type	Function	Default
Bit 7	R/W	EGR_TUG3[1]	0
Bit 6	R/W	EGR_TUG3[0]	1
Bit 5	R/W	EGR_TUG2[2]	0
Bit 4	R/W	EGR_TUG2[1]	0
Bit 3	R/W	EGR_TUG2[0]	1
Bit 2	R/W	EGR_TU[2]	0
Bit 1	R/W	EGR_TU[1]	0
Bit 0	R/W	EGR_TU[0]	1

The address specified by this register is the tributary identifier for egress tributaries out of the TEMAP that are switched from internal links when the Egress Time Switch Enable register bit, ETSEN, in the Master SONET/SDH Master Egress Configuration register is a logic 1. The internal link that will be switched to the egress tributary is the internal link specified in the TTMP Indirect Time Switch Internal Link Data register and is indirectly accessed in the time switch RAM at the address specified by this register.

When switching tributaries via the egress time switch, the LADDSEL[1:0] bits in the SONET/SDH Mapper Master Configuration register must be set to “00” for switched access to all tributaries within the STS-3/STM-1.

EGR_TU[2:0]:

The indirect egress tributary unit bits, EGR_TU[2:0], indicate the tributary unit that internal links identified in the TTMP Indirect Time Switch Internal Link Data register will be switched to. Legal EGR_TU[2:0] ranges are ‘b001 to ‘b100.

EGR_TUG2[2:0]:

The indirect egress tributary unit group 2 bits, EGR_TUG2[2:0], indicate the tributary unit group 2 that internal links identified in the TTMP Indirect Time Switch Internal Link Data register will be switched to. Legal EGR_TUG2[2:0] ranges are ‘b001 to ‘b111.

EGR_TUG3[1:0]:

The indirect egress tributary unit group 3 bits, EGR_TUG2[1:0], indicate the tributary unit group 3 that internal links identified in the TTMP Indirect Time Switch Internal Link Data register will be switched to. Legal EGR_TUG3[1:0] ranges are ‘b01 to ‘b11.

Register 15E4H: TTMP Indirect Time Switch Internal Link Data

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	INT_SPE[1]	X
Bit 5	R/W	INT_SPE[0]	X
Bit 4	R/W	INT_LINK[4]	X
Bit 3	R/W	INT_LINK[3]	X
Bit 2	R/W	INT_LINK[2]	X
Bit 1	R/W	INT_LINK[1]	X
Bit 0	R/W	INT_LINK[0]	X

This register identifies an internal link that will be switched to an egress tributary through the egress time switch RAM. An indirect access to the TTMP egress time switch RAM associates the internal link specified in this register with the egress link specified as the time switch address in the TTMP Indirect Egress Tributary Address register. The time switch configuration via this indirect register are inactive when the Egress Time Switch Enable register bit, ETSEN, in the Master SONET/SDH Egress Configuration register is a logic 0.

INT_LINK [4:0]:

The indirect internal link number bits, INT_LINK[4:0], associate the specified T1 or E1 internal link with the egress tributary specified in the TTMP Indirect Egress Tributary Address register. In an indirect write operation, the internal link number to be written to the time switch configuration RAM at the egress tributary address must be set up in this register before triggering the indirect write. When read back, INT_LINK[4:0] reflects the value written until the completion of a subsequent indirect channel read operation. INT_LINK[4:0] ranges from 00001b to 10101b (1 to 21) for E1 streams and from 00001b to 11100b (1 to 28) for T1 streams.

INT_SPE[1:0]:

The indirect internal synchronous payload envelope bits, INT_ SPE[1:0], associate the specified T1 or E1 internal link with the tributary specified in the TTMP Indirect Egress Tributary Address register. In an indirect write operation, the internal SPE number to be written to the time switch configuration RAM at the egress tributary address must be set up in this register before triggering the indirect write. INT_SPE[1:0] reflects the value written until the completion of a subsequent indirect channel read operation.

Register 15E5H: TTMP Telecom Interface Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	LOCK0	0

LOCK0:

LOCK0 configures the position of the SPE in the egress direction. When LOCK0 is logic 1 the H1,H2 pointer is set to zero and the first byte of the SPE (J1) will occur immediately after H3. When LOCK0 is a logic 0 the H1,H2 pointer is set to 522 and the first byte of the SPE will occur immediately after C1.

When using the TEMAP with Transparent VTs between the SBI bus and the line side telecom bus LOCK0 must be set to 0 such that J1 immediately follows C1. When the egress VTPP is bypassed the setting of this bit determines the SPE position on the line side Telecom Add bus.

Register 15E6H: TTMP FIFO Depth

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	FIFO_DEPTH[3]	0
Bit 2	R/W	FIFO_DEPTH[2]	0
Bit 1	R/W	FIFO_DEPTH[1]	0
Bit 0	R/W	FIFO_DEPTH[0]	0

This register configures the Depth of the SBIIP Interface FIFOs.

FIFO_DEPTH:

FIFO_DEPTH increases the depth of the input FIFOs. The value in the register is coded as an unsigned integer and is valid from 0 through 8. Other values are illegal. The effective depth is 8 + the value in the register:

Reg 15E6h Value	FIFO Depth	Default
8	16	
7	15	
6	14	
5	13	
4	12	
3	11	
2	10	
1	9	
0	8	←

Please note that increasing this value will increase low frequency jitter tolerance at the expense of overall system latency.

Register 15E7H: TTMP MAP SVRam Capture Address

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	map capture address[6]	0
Bit 5	R/W	map capture address [5]	0
Bit 4	R/W	map capture address [4]	0
Bit 3	R/W	map capture address [3]	0
Bit 2	R/W	map capture address [2]	0
Bit 1	R/W	map capture address [1]	0
Bit 0	R/W	map capture address [0]	0

This is the detection facility used in conjunction with Reg 15E8H to capture specified locations in the TTMP state vector ram (SVRAM) during operation. This register sets the desired SVRAM address.

Register 15E8H: TTMP MAP SVRam Control Signals and Bistinit Abort

Bit	Type	Function	Default
Bit 7	R/W	map capture enable	0
Bit 6	R/W	map read new	1
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	Bistinit_abort	0

When map capture enable is set high data from the SVram address set by 15E7H is available in the registers 15E9-15F6H. When enabled, data is captured by these registers every time the tributary column is processed.

When map read new is high, the current data is available, when low the data from the last read is available (there are two sets of registers - shift register style)

Bisinit abort is placed here for convenience. This bit, when set high, will cause the ram initialisation on startup to be aborted.

Registers 15E9H to 15F5H: TTMP MAP SVRam Data

Bit	Type	Function	Default
Bit 7	R	Map capture data[7..103]	0
Bit 6	R	Map capture data[6..102]	0
Bit 5	R	Map capture data[5..101]	0
Bit 4	R	map capture data[4..100]	0
Bit 3	R	map capture data[3..99]	0
Bit 2	R	map capture data[2..98]	0
Bit 1	R	map capture data[1..97]	0
Bit 0	R	map capture data[0..96]	0

1.30 D3MD DS3 Drop Side Mapper Registers

Register 1640H: D3MD Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	AISGEN	0

AISGEN:

The active high DS3 Alarm Indication Signal enable bit, AISGEN, configures the TEMAP to generate a DS3 AIS signal in the ingress data stream. Any data on the STS-1 SPE is lost due to the assertion of AISGEN.

Register 1641H: D3MD Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	OFLI	0
Bit 0	R	UFLI	0

The OFLI and UFLI bits and the interrupt are cleared when this register is read.

OFLI:

When a logic 1, this bit indicates that an overflow condition has occurred in the elastic store. This error resets the elastic store's read and write addresses to 180° apart.

UFLI:

When a logic 1, this bit indicates that an underflow condition has occurred in the elastic store. This error resets the elastic store's read and write addresses to 180° apart.

Register 1642H: D3MD Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	OFLIEN	0
Bit 0	R/W	UFLIEN	0

OFLIEN:

When set High, this bit enables generation of an interrupt if an elastic store overflow condition, OFLI, occurs.

UFLIEN:

When set High, this bit enables generation of an interrupt if an elastic store underflow condition, UFLI, occurs.

1.31 D3MA DS3 Add Side Mapper Registers

Register 1644H: D3MA Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	RBSO	0
Bit 0	R/W	AISGEN	0

AISGEN:

The active high DS3 Alarm Indication Signal enable bit, AISGEN, configures the TEMAP to generate a DS3 AIS signal in the egress data stream. Any data on the STS-1 SPE is lost due to the assertion of AISGEN.

RBSO:

When RBSO is a logic 1, R bits are set to ‘1’s. If RBSO bit is a logic 0, R bits are set to ‘0’s.

Register 1645H: D3MA Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	OFLI	0
Bit 0	R	UFLI	0

The OFLI and UFLI bits and the interrupt are cleared when this register is read.

OFLI:

When set High, this bit indicates that an overflow condition has occurred in the elastic store. This error resets the elastic store's read and write addresses to 180° apart.

UFLI:

When set High, this bit indicates that an underflow condition has occurred in the elastic store. This error resets the elastic store's read and write addresses to 180° apart.

Register 1646H: D3MA Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	OFLIEN	0
Bit 0	R/W	UFLIEN	0

OFLIEN:

When set to a logic 1, this bit enables generation of an interrupt if an elastic store overflow condition, OFLI, occurs.

UFLIEN:

When set High, this bit enables generation of an interrupt if an elastic store underflow condition, UFLI, occurs.

1.32 Scaleable Bandwidth Interconnect Master Configuration Register

Register 1700H: SBI Master Reset / Bus Signal Monitor

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	SC1FPA	X
Bit 5	R	SADA	X
Bit 4	R	SAV5A	X
Bit 3	R	SAPLA	X
Bit 2	R	SBIDET1A	X
Bit 1	R	SBIDET0A	X
Bit 0	R/W	RESET	0

When a monitored SBI Bus signal makes a low to high transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point all the bits in this register are cleared. A lack of transitions is indicated by the corresponding register bit reading low. This register should be read at periodic intervals to detect clock failures.

RESET:

The RESET bit forces a software reset of all the SBI blocks. This will force all direct and indirect registers to their default values. When the RESET bit is set to a logic 1 the SBI blocks are held reset which is also the low power state. When RESET is set low the SBI is operational. The SBI blocks are operational by default.

SC1FPA:

The SC1FP active, SC1FPA, bit monitors for low to high transitions on the SC1FP input. SC1FPA is set high on a rising edge of SC1FP, and is set low when this register is read.

SBIDET0A:

The SBIDET0 active, SBIDET0A, bit monitors for low to high transitions on the SBIDET0 input. SBIDET0A is set high on a rising edge of SBIDET0, and is set low when this register is read.

SBIDET1A:

The SBIDET1 active, SBIDET1A, bit monitors for low to high transitions on the SBIDET1 input. SBIDET1A is set high on a rising edge of SBIDET1, and is set low when this register is read.

SAPLA:

The SAPL active, SAPLA, bit monitors for low to high transitions on the SAPL input. SAPLA is set high on a rising edge of SAPL, and is set low when this register is read.

SAV5A:

The SAV5 active, SAV5A, bit monitors for low to high transitions on the SAV5 input. SAV5A is set high on a rising edge of SAV5, and is set low when this register is read.

SADA:

The SADATA bus active, SADA, bit monitors for low to high transitions on the least significant data bit of the SBI Add bus, SADATA[0], as an indication of bus activity on the SBI Add bus data and parity signals. SADA is set high when a rising edge has been observed on SADATA[0], and is set low when this register is read.

Register 1701H: SBI Master Configuration

Bit	Type	Function	Default
Bit 7	R/W	FASTCLKFREQ	0
Bit 6	R/W	SC1FPMSTR	0
Bit 5	R/W	MFSC1FP	0
Bit 4		Unused	X
Bit 3	R/W	SADDSEL1	0
Bit 2	R/W	SADDSEL0	0
Bit 1	R/W	SDROPSEL1	0
Bit 0	R/W	SDROPSEL0	0

Please note that these bits must be set before any tributary is enabled and should only be changed when tributaries are disabled

SDROPSEL[1:0]:

The System DROP Bus select bits, SDROPSEL[1:0], determine which SPE the SBI DROP interface will insert its tributaries according to the following table:

SDROPSEL[1:0]	SBI DROP Bus Interface SPE Selection
00	Disabled
01	SPE #1
10	SPE #2
11	SPE #3

SADDSEL[1:0]:

The System ADD Bus select bits, SADDSEL[1:0], determine which SPE the SBI ADD interface will extract its tributaries according to the following table:

SADDSEL[1:0]	SBI ADD Bus Interface SPE Selection
00	Disabled
01	SPE #1
10	SPE #2
11	SPE #3

MFSC1FP:

The multiframe SC1FP alignment bit, MFSC1FP, enables the TEMAP for generating signaling multiframe alignment on the SBI bus. When MFSC1FP is high the SC1FP pulse is generated once per 48 SBI frames, or once per every 12 SBI multiframes of 2KHz. This period allows signaling multiframe alignment for both 16 frame multiframes for E1 and 24 frame multiframes for T1. In Sync mode SC1FP can occur less often than every 48 SBI frames but must be a multiple of 48 SBI frames. When MFSC1FP is low the SC1FP pulse is generated once every 4 SBI frames or once per SBI multiframe at 2KHz. SC1FP can occur less often than every 4 SBI frames but must be a multiple of 4 SBI frames. This bit is only effective when SC1FPMSTR is high.

SC1FPMSTR:

The SC1FP master mode bit, SC1FPMSTR, enables the TEMAP to be the SC1FP master in an SBI system. Only one device per SBI bus can be SC1FP master. When SC1FPMSTR is high the TEMAP will generate the SC1FP pulse at a period set by the MFSC1FP register bit. When SC1FPMSTR is low the TEMAP will listen to the SC1FP pulse which is generated elsewhere.

FASTCLKFREQ:

The Fast Clock Frequency select bit indicates the frequency of the CLK52M reference clock connected to the TEMAP. When FASTCLKFREQ is set high the CLK52M reference clock is selected to be 51.84MHz. When FASTCLKFREQ is set low the CLK52M reference clock is selected to be 44.928MHz. This setting must match the FASTCLKFREQ bit in the SONET/SDH Master DS3 Clock Generation Control register.

Register 1702H: SBI Bus Master Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	BUSMASTER	0

BUSMASTER:

This SBI Bus Master bit, BUSMASTER, enables the TEMAP to drive the SBI Drop bus whenever no other SBI device is driving the bus. When BUSMASTER is set to 0 the TEMAP drives the SBI Drop bus only during links that enabled for this device. During all other links or SBI overhead bytes the TEMAP will tri-state the SBI Drop bus signals. When BUSMASTER is set to 1 the TEMAP will drive the SBI Drop bus during all links and SBI overhead bytes except when it detects other SBI devices are driving the bus when the SBIDET[1:0] signals are set to 1. It is recommended that one (1) TEMAP be selected as bus master for the SBI drop bus, to ensure that the SBI is driven during all locations not driven by other devices.

1.33 EXSBI Extract Scaleable Bandwidth Interconnect Registers

Register 1710H: EXSBI Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	DC_RSTEN	1
Bit 5	R/W	DC_RESYNCE	0
Bit 4	R/W	FIFO_OVRE	0
Bit 3	R/W	FIFO_UDRE	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	SBI_PERR_EN	0
Bit 0	R/W	SBI_PAR_CTL	1

SBI_PAR_CTL:

The SBI_PAR_CTL bit is used to configure the Parity mode for checking of the SBI parity signal, SADP and SDDP. When SBI_PAR_CTL is a logic 0 parity will be even. When SBI_PAR_CTL is logic 1 parity will be odd

SBI_PERR_EN:

The SBI_PERR_EN bit is used to enable the SBI Parity Error interrupt generation. When SBI_PERR_EN is a logic 0 SBI Parity Error Interrupts will be disabled. When SBI_PERR_EN is a logic 1 SBI Parity Error Interrupts will be enabled. In both cases the SBI Parity checker logic will update the SBI Parity Error Interrupt Reason Register. With parity enabled, checking is done every clock cycle, independent of whether the tributaries are enabled via the ENBL bit in register 1716H. Overhead bits are also included in the parity check. When sourcing overhead bytes, ensure parity is generated.

FIFO_UDRE:

This bit is set to enable the generation of an interrupt when a FIFO under-run is detected.

FIFO_OVRE:

This bit is set to enable the generation of an interrupt when a FIFO over-run is detected.

DC_RESYNCE:

This depth check and bus resynchronization interrupt enable bit, DC_RESYNCE, enables the generation of an interrupt when either a Depth Check error or an external resynchronization event occurs on either the SC1FP or internal synchronization signals. When DC_RESYNCE is a 1 interrupts will be generated when one of the depth check or resynchronization errors occur. When DC_RESYNCE is a logic 0 interrupts will not be set, nor will the DC_INTI register bit be set due to these events.
Depth check events should only happen when the SBI bus is misconfigured and will reset the link. SC1FP resynchroniztion events will reset the entire SBI bus interface and are reported by the SC1FP_SYNCI. Internal synchronization errors should only occur during configuration and are reported by the SBIIP_SYNCI.

DC_RSTEN:

The Depth check automatic reset enable bit, DC_RSTEN, allows the EXSBI to automatically reset a link if it underruns or overruns. When DC_RSTEN is a 1 the link will automatically reset when a depth check error is detected. When DC_RSTEN is a 0 the link must be reset manually when a depth check error is detected and reported via the depth check error interrupt, DC_ERRI bit in the EXSBI Depth Check Interrupt Status register.
When DC_RSTEN is a logic 0 interrupts must be enabled via the DC_RESYNCE interrupt enable bit. When DC_RSTEN is a 1 and depth check interrupts are enabled via DC_RESYNCE, multiple interrupts can be expected until the link fifo is at the correct operating level.

Reserved:

These bits must be left as a logic 0 for proper operation.

Register 1711H: EXSBI FIFO Underrun Interrupt Status

Bit	Type	Function	Default
Bit 7	R	SPE[1]	X
Bit 6	R	SPE[0]	X
Bit 5	R	LINK[4]	X
Bit 4	R	LINK[3]	X
Bit 3	R	LINK[2]	X
Bit 2	R	LINK[1]	X
Bit 1	R	LINK[0]	X
Bit 0	R	FIFO_UDRI	0

This register is cleared when read.

FIFO_UDRI:

This bit is set when a FIFO under-run is detected.

LINK[4:0] and SPE[1:0]:

The LINK[4:0] and SPE[1:0] fields are used to specify the SBI link associated with the FIFO buffer in which the over-run was detected.
Legal values for LINK[4:0] are b’00001’ through b‘11100’. Legal values for SPE[1:0] are b’01’ through b‘11’.

Register 1712H: EXSBI FIFO Overrun Interrupt Status

Bit	Type	Function	Default
Bit 7	R	SPE1	X
Bit 6	R	SPE0	X
Bit 5	R	LINK4	X
Bit 4	R	LINK3	X
Bit 3	R	LINK2	X
Bit 2	R	LINK1	X
Bit 1	R	LINK0	X
Bit 0	R	FIFO_OVRI	0

This register is cleared when read.

FIFO_OVRI:

This bit is set when a FIFO over-run is detected.

LINK[4:0] and SPE[1:0]:

The LINK[4:0] and SPE[1:0] fields are used to specify the SBI link associated with the FIFO buffer in which the over-run was detected.
Legal values for LINK[4:0] are b’00001’ through b‘11100’. Legal values for SPE[1:0] are b’01’ through b‘11’.

Register 1713H: EXSBI Tributary RAM Indirect Access Address

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	SPE[1]	0
Bit 5	R/W	SPE[0]	0
Bit 4	R/W	TRIB[4]	0
Bit 3	R/W	TRIB[3]	0
Bit 2	R/W	TRIB[2]	0
Bit 1	R/W	TRIB[1]	0
Bit 0	R/W	TRIB[0]	0

TRIB[4:0] and SPE[1:0]:

The TRIB[4:0] and SPE[1:0] fields are used to fully specify which SBI tributary the Control register write or read operation will apply.
TRIB[4:0] specifies the SBI tributary number within the SBI SPE as specified by the SPE[1:0] field. Legal values for TRIB[4:0] are b’00001’ through b‘11100’ in T1 mode, b’00001’ through b‘10101 in E1 mode and b’00001 in DS3 mode. Legal values for SPE[1:0] are b’01’ through b‘11’.

Reserved:

This register must always be written as a logic 0 for correct operation.

Register 1714H: EXSBI Tributary RAM Indirect Access Control

Bit	Type	Function	Default
Bit 7	R	BUSY	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	RWB	0
Bit 0	R/W	Reserved	0

Reserved:

A logic 0 must be written to this bit for proper operation.

RWB:

The indirect access control bit, RWB selects between a configure (write) or interrogate (read) access to the tributary control configuration RAM. Writing a logic 0 to RWB triggers an indirect write operation. Data to be written is taken from the Extract Tributary Control Indirect Access Data Register. Writing a logic 1 to RWB triggers an indirect read operation. The data read can be found in the Extract Tributary Control Indirect Access Data Register.

BUSY:

The indirect access status bit, BUSY reports the progress of an indirect access. BUSY is set high when a write to the Extract Tributary Control Indirect Access Data Register triggers an indirect access and will stay high until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the Indirect Tributary Data register or to determine when a new indirect write operation may commence. If SREFCLK disappears during an access, the BUSY bit can stay high.

Register 1716H: EXSBI Tributary Control Indirect Access Data

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	CLK_MODE[1]	0
Bit 5	R/W	CLK_MODE[0]	0
Bit 4	R/W	CLK_MSTR	0
Bit 3	R/W	TRIB_TYP[1]	0
Bit 2	R/W	TRIB_TYP[0]	0
Bit 1		Unused	X
Bit 0	R/W	ENBL	0

ENBL:

The ENBL bit is used to enable the Tributary. Writing to an Extract Tributary Control and Status Register with the ENBL bit set enables the EXSBI to take tributary data from an SBI tributary and transmit that data to the PISO block for serialization.

TRIB_TYP[1:0]

The TRIB_TYP[1:0] bits must be programmed to “10” for proper operation of the TEMAP. This selected the Unframed SBI tributary type.

CLK_MSTR:

The CLK_MSTR bit is used to specify whether the Extract block tributary functions as a clock master or a clock slave. When this bit is a logic 1 the TEMAP is the clock master for the selected tributary and will use the SAJUST_REQ SBI signal to speed-up or slow-down SBI slaves connected to that tributary. When this bit is a logic 0 the TEMAP is a clock slave for the selected tributary and will adapt to the incoming tributary rate.

CLK_MODE[1:0]:

The CLK_MODE[1:0] field controls how the Extracted Link Rate octet is used. In applications where the Link Rate octet is not used CLK_MODE[1:0] must be 00. When Link Rate is available CLK_MODE[1:0] can be configured to use the Link Rate information to produce a smoother egress T1/E1 clock. When using the phase field of the Link Rate octet, the SYNC bit in the RJAT configuration register needs to be set.

CLK_MODE[1:0]	Description
00	Link Rate octet not used
01	Use only ClkRate field of Link Rate octet
10	Use only Phase field of Link Rate octet – not available in DS3 mode
11	Reserved – must not be used for normal operation

Register 1717H: SBI Parity Error Interrupt Status

Bit	Type	Function	Default
Bit 7	R	SPE[1]	X
Bit 6	R	SPE[0]	X
Bit 5	R	TRIB[4]	X
Bit 4	R	TRIB[3]	X
Bit 3	R	TRIB[2]	X
Bit 2	R	TRIB[1]	X
Bit 1	R	TRIB[0]	X
Bit 0	R	PERRI	0

PERRI:

When set PERRI indicates that an SBI parity error has been detected. This bit is cleared when read.

TRIB[4:0] and SPE[1:0]:

The TRIB[4:0] and SPE[1:0] field are used to specify the SBI tributary for which a parity error was detected. These fields are only valid only when PERRI is set.

Register 171EH: EXSBI Depth Check Interrupt Status

Bit	Type	Function	Default
Bit 7	R	SPE[1]	0
Bit 6	R	SPE[0]	1
Bit 5	R	LINK[4]	0
Bit 4	R	LINK[3]	0
Bit 3	R	LINK[2]	0
Bit 2	R	LINK[1]	0
Bit 1	R	LINK[0]	0
Bit 0	R	DC_ERRI	0

DC_ERRI:

This bit is set when a Depth Check error is detected. Reading this register clears this bit unless another Depth Check Interrupt is pending. Pending interrupts can occur when many links are reset simultaneously due to a reconfiguration or SBI bus resynchronization. Multiple pending interrupts can also occur on a single link when the DC_RSTEN bit is set, persisting until the link fifo is stable.

LINK[4:0] and SPE[1:0]:

The LINK[4:0] and SPE[1:0] fields are used to specify the SBI tributary associated with the FIFO buffer in which the depth check error was detected. Legal values for LINK[4:0] are b'00001' through b'11100'. Legal values for SPE[1:0] are b'01' through b'11'. When an over run has not been detected the LINK field may contain an out of range link value. Values in these fields are only valid when DCR_INTI is a '1'.

Register 171FH: Extract External ReSynch Interrupt Status

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	SBIIP_SYNCI	0
Bit 0	R	SC1FP_SYNCI	0

SC1FP_SYNCI:

This bit is set when a SC1FP realignment has been detected and the DC_RESYNCE register bit is set to 1. Reading this register clears this interrupt source.

SBIIP_SYNCI:

This bit is set when an internal SBI bus realignment has been detected and the DC_RESYNCE register bit is set to 1. Reading this register clears this interrupt source.

Reserved

This bit must be set to logic 0 for correct operation.

1.34 INSBI Insert Scaleable Bandwidth Interconnect Registers

Register 1720H: INSBI Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	DC_RSTEN	1
Bit 5	R/W	DC_RESYNCE	0
Bit 4	R/W	FIFO_OVRE	0
Bit 3	R/W	FIFO_UDRE	0
Bit 2	R/W	Reserved	0
Bit 1		Unused	X
Bit 0	R/W	SBI_PAR_CTL	1

SBI_PAR_CTL:

The SBI_PAR_CTL bit is used to configure the Parity mode for generation of the SBI data parity signal, DP. When SBI_PAR_CTL is a logic 0 parity will be even. When SBI_PAR_CTL is a logic 1 parity will be odd.

FIFO_UDRE:

The FIFO_UDRE bit is used to enable/disable the generation of an interrupt when a FIFO underrun is detected. When FIFO_UDRE is a logic 0 underrun interrupt generation is disabled. When FIFO_UDRE is a logic 1 underrun interrupt generation is enabled.

FIFO_OVRE:

The FIFO_OVRE bit is used to enable/disable the generation of an interrupt when a FIFO overrun is detected. When FIFO_OVRE is a logic 0 overrun interrupt generation is disabled. When FIFO_OVRE is a logic 1 overrun interrupt generation is enabled.

DC_RESYNCE:

This DC_RESYNCE bit enables the generation of an interrupt when either a Depth Check error or an external resynchronization event occurs on either the SC1FP or internal synchronization signals. When DC_RESYNCE is a 1 interrupts will be generated when one of the depth check or resynchronization

errors occur. When DC_RESYNCE is a logic 0 interrupts will not be set, nor will the DC_ERRI register bit be set due to these events.
Depth check events should only happen when the SBI bus is misconfigured and will reset the link. SC1FP resynchroniztion events will reset the entire SBI bus interface and are reported by the SC1FP_SYNCI. Internal synchronization errors should only occur during configuration and are reported by the SBIIP_SYNCI.

DC_RSTEN:

The Depth check automatic reset enable bit, DC_RSTEN, allows the INSBI to automatically reset a link if it underruns or overruns. When DC_RSTEN is a 1 the link will automatically reset when a depth check error is detected. When DC_RSTEN is a 0 the link must be reset manually when a depth check error is detected and reported via the depth check error interrupt, DC_ERRI bit in the INSBI Depth Check Interrupt Status register.
When DC_RSTEN is a logic 0 interrupts must be enabled via the DC_RESYNCE interrupt enable bit. When DC_RSTEN is a 1 and depth check interrupts are enabled via DC_RESYNCE, multiple interrupts can be expected until the link fifo is at the correct operating level.

Reserved:

These bits must be left as a logic 0 for proper operation.

Register 1721H: INSBI FIFO Underrun Interrupt Status

Bit	Type	Function	Default
Bit 7	R	SPE[1]	X
Bit 6	R	SPE[0]	X
Bit 5	R	LINK[4]	X
Bit 4	R	LINK[3]	X
Bit 3	R	LINK[2]	X
Bit 2	R	LINK[1]	X
Bit 1	R	LINK[0]	X
Bit 0	R	FIFO_UDRI	0

This interrupt status register is cleared when read.

FIFO_UDRI:

This bit is set when a FIFO underrun is detected.

LINK[4:0] and SPE[1:0]:

The LINK[4:0] and SPE[1:0] fields are used to specify the SBI link associated with the FIFO buffer in which the underrun was detected.
Legal values for LINK[4:0] are b'00001' through b'11100'. Legal values for SPE[1:0] are b'01' through b'11'.
LINK[4:0] and SPE[1:0] are invalid unless FIFO_UDRI is set.

Register 1722H: INSBI FIFO Overrun Interrupt Status

Bit	Type	Function	Default
Bit 7	R	SPE[1]	X
Bit 6	R	SPE[0]	X
Bit 5	R	LINK[4]	X
Bit 4	R	LINK[3]	X
Bit 3	R	LINK[2]	X
Bit 2	R	LINK[1]	X
Bit 1	R	LINK[0]	X
Bit 0	R	FIFO_OVRI	0

This interrupt status register is cleared when read.

FIFO_OVRI:

This bit is set when a FIFO overrun is detected.

LINK[4:0] and SPE[1:0]:

The LINK[4:0] and SPE[1:0] fields are used to specify the SBI link associated with the FIFO buffer in which the overrun was detected.
Legal values for LINK[4:0] are b'00001' through b'11100'. Legal values for SPE[1:0] are b'01' through b'11'.
LINK[4:0] and SPE[1:0] are invalid unless FIFO_OVRI is set.

Register 1723H: INSBI Tributary Register Indirect Access Address

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	SPE[1]	0
Bit 5	R/W	SPE[0]	0
Bit 4	R/W	TRIB[4]	0
Bit 3	R/W	TRIB[3]	0
Bit 2	R/W	TRIB[2]	0
Bit 1	R/W	TRIB[1]	0
Bit 0	R/W	TRIB[0]	0

TRIB[4:0] and SPE[1:0]:

The TRIB[4:0] and SPE[1:0] fields are used to fully specify for which SBI tributary the Control register write or read operation will apply.
TRIB[4:0] specifies the SBI tributary number within the SBI SPE as specified by the SPE[1:0] field. Legal values for TRIB[4:0] are b’00001’ through b‘11100’. Legal values for SPE[1:0] are b’01’ through b‘11’.

Reserved:

A logic 0 must be written to this bit for proper operation.

Register 1724H: INSBI Tributary Register Indirect Access Control

Bit	Type	Function	Default
Bit 7	R	BUSY	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	RWB	0
Bit 0	R/W	Reserved	0

Reserved:

A logic 0 must be written to this bit for proper operation.

RWB:

The indirect access control bit (RWB) selects between a configure (write) or interrogate (read) access to the tributary control configuration RAM. Writing a '0' to RWB triggers an indirect write operation. Data to be written is taken from the Insert Tributary Control Indirect Access Data Register. Writing a '1' to RWB triggers an indirect read operation. The data read can be found in the Insert Tributary Control Indirect Access Data Register.

BUSY:

The indirect access status bit (BUSY) reports the progress of an indirect access. BUSY is set high when a write to the Insert Tributary Control Indirect Access Data Register triggers an indirect access and will stay high until the access is complete. This register should be polled to determine when data from an indirect read operation is available in the Indirect Tributary Data register or to determine when a new indirect write operation may commence. The BUSY bit is asserted for up to 4.32us after a page switch. If SREFCLK disappears during an access, the BUSY bit can stay high.

Register 1726H: INSBI Tributary Control Indirect Access Data

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4		Unused	X
Bit 3	R/W	TRIB_TYP[1]	0
Bit 2	R/W	TRIB_TYP[0]	0
Bit 1	R/W	ITVT	0
Bit 0	R/W	ENBL	0

ENBL:

The ENBL bit is used to enable the Tributary. Writing to an Insert Tributary Control and Status Register with the ENBL bit set to a logic 1 enables the INSBI to take tributary data from an SBIIP link and transmit that data to the SBI tributary mapped to that link. This bit must also be set to a logic 1 when ingress Transparanet VTs are enabled via the ITVT bit in this register.

ITVT:

The Ingress Transparent Virtual Tributary bit, ITVT, selects a Transparent VT in place of the tributary specified by SPE[1:0] and TRIB[4:0] in the INSBI Insert Tributary Mapping Indirect Access Data Register. This capability is only applicable for VTs coming from the SONET/SDH mapper and will result in incorrect data for the selected tributary when used with the DS3 multiplexer. The ENBL bit in this register must also be set to logic 1 when ITVT is set to logic 1.

TRIB_TYP[1:0]

The TRIB_TYP[1:0] bits must be programmed to “10” for proper operation of the TEMAP. This selected the Unframed SBI tributary type.

Reserved:

This bit must be set to logic 0 for proper operation of the TEMAP.

Register 1731H: INSBI Depth Check Interrupt Status

Bit	Type	Function	Default
Bit 7	R	SPE[1]	0
Bit 6	R	SPE[0]	1
Bit 5	R	LINK[4]	0
Bit 4	R	LINK[3]	0
Bit 3	R	LINK[2]	0
Bit 2	R	LINK[1]	0
Bit 1	R	LINK[0]	0
Bit 0	R	DC_ERRI	0

DC_ERRI:

This bit is set when a Depth Check error is detected. Reading this register clears this bit unless another Depth Check Interrupt is pending. Pending interrupts can occur when many links are reset simultaneously due to a reconfiguration or SBI bus resynchronization. Multiple pending interrupts can also occur on a single link when the DC_RSTEN bit is set, persisting until the link fifo is stable.

LINK[4:0] and SPE[1:0]:

The LINK[4:0] and SPE[1:0] fields are used to specify the SBI tributary associated with the FIFO buffer in which the depth check error was detected. Legal values for LINK[4:0] are b'00001' through b'11100'. Legal values for SPE[1:0] are b'01' through b'11'. When an over run has not been detected the LINK field may contain an out of range link value. Values in these fields are only valid when DCR_INTI is a '1'.

Register 1732H: Insert External ReSynch Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	SBIIP_SYNCI	0
Bit 0	R	C1FP_SYNCI	0

SC1FP_SYNCI:

This bit is set when a SC1FP realignment has been detected and the DC_RESYNCE register bit is set to 1. Reading this register clears this interrupt source.

SBIIP_SYNCI:

This bit is set when an internal SBI bus realignment has been detected and the DC_RESYNCE register bit is set to 1. Reading this register clears this interrupt source.

NOTES

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