

DATA SHEET

74LVC1G14

Single Schmitt-trigger inverter

Product specification
Supersedes data of 2001 Apr 06

2002 May 21

Single Schmitt-trigger inverter

74LVC1G14

FEATURES

- Wide supply voltage range from 1.65 to 5.5 V
- High noise immunity
- Complies with JEDEC standard:
 - JESD8-7 (1.65 to 1.95 V)
 - JESD8-5 (2.3 to 2.7 V)
 - JESD8B/JESD36 (2.7 to 3.6 V).
- ± 24 mA output drive ($V_{CC} = 3.0$ V)
- CMOS low power consumption
- Latch-up performance ≤ 250 mA
- Direct interface with TTL levels
- Inputs accepts voltages up to 5 V
- Multiple package options
- Specified from -40 to $+125$ °C.

DESCRIPTION

The 74LVC1G14 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The input can be driven from either 3.3 or 5 V devices. This feature allows the use of this device in a mixed 3.3 and 5 V environment.

Schmitt-trigger action at the input makes the circuit tolerant for slower input rise and fall time.

This device is fully specified for partial power-down applications using I_{off} . The I_{off} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

The 74LVC1G14 provides the inverting buffer function with Schmitt-trigger action.

QUICK REFERENCE DATA

Ground = 0 V; $T_{amb} = 25$ °C; $t_r = t_f \leq 2.5$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A to Y	$V_{CC} = 1.8$ V; $C_L = 30$ pF; $R_L = 1$ k Ω	4.1	ns
		$V_{CC} = 2.5$ V; $C_L = 30$ pF; $R_L = 500$ Ω	2.8	ns
		$V_{CC} = 3.3$ V; $C_L = 50$ pF; $R_L = 500$ Ω	3.0	ns
		$V_{CC} = 5.0$ V; $C_L = 50$ pF; $R_L = 500$ Ω	2.2	ns
C_I	input capacitance		5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	15.4	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts.

2. The condition is $V_i = \text{GND}$ to V_{CC} .

Single Schmitt-trigger inverter

74LVC1G14

FUNCTION TABLE

See note 1.

INPUT	OUTPUT
A	Y
L	H
H	L

Note

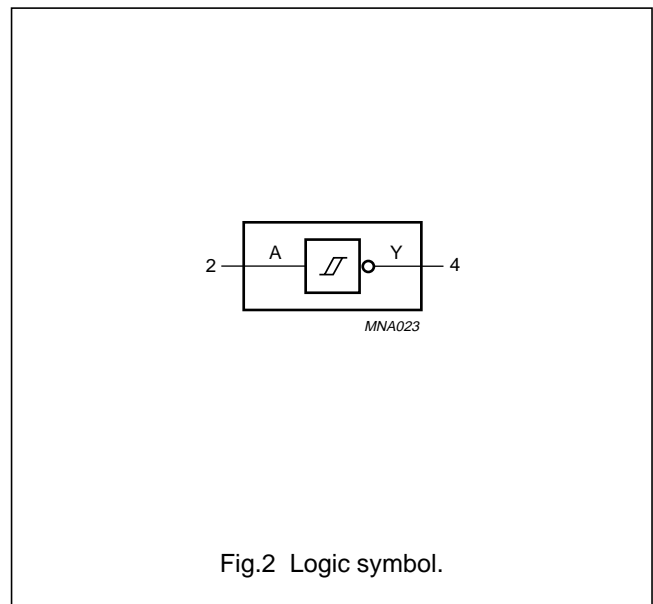
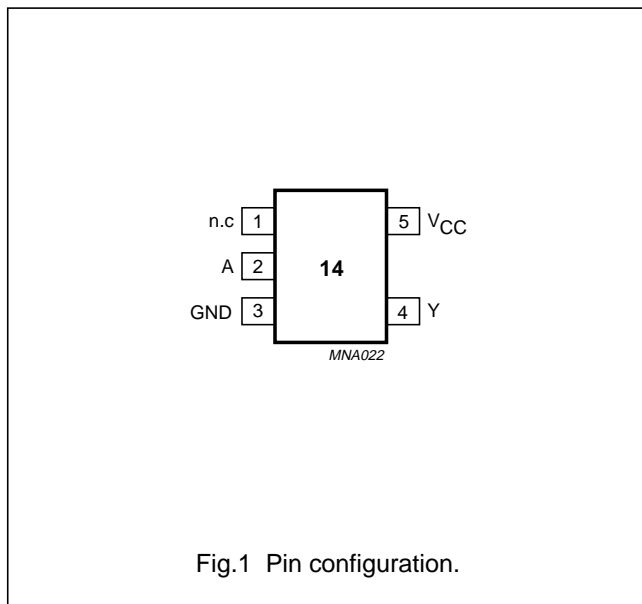
1. H = HIGH voltage level;
L = LOW voltage level.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE					
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE	MARKING
74LVC1G14GW	-40 to +125 °C	5	SC-88A	plastic	SOT353	VF
74LVC1G14GV	-40 to +125 °C	5	SC-74A	plastic	SOT753	V14

PINNING

PIN	SYMBOL	DESCRIPTION
1	n.c.	not connected
2	A	data input A
3	GND	ground (0 V)
4	Y	data output Y
5	V _{CC}	supply voltage



Single Schmitt-trigger inverter

74LVC1G14



Fig.3 IEE/IEC logic symbol.

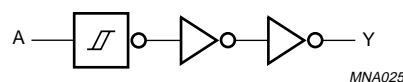


Fig.4 Logic diagram.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		1.65	5.5	V
V_I	input voltage		0	5.5	V
V_O	output voltage	active mode	0	V_{CC}	V
		Power-down mode; $V_{CC} = 0$ V	0	5.5	V
T_{amb}	operating ambient temperature		-40	+125	°C
t_r, t_f	input rise and fall times	$V_{CC} = 1.65$ to 2.7 V	0	20	ns/V
		$V_{CC} = 2.7$ to 5.5 V	0	10	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		-0.5	+6.5	V
I_{IK}	input diode current	$V_I < 0$	-	-50	mA
V_I	input voltage	note 1	-0.5	+6.5	V
I_{OK}	output diode current	$V_O > V_{CC}$ or $V_O < 0$	-	±50	mA
V_O	output voltage	active mode; notes 1 and 2	-0.5	$V_{CC} + 0.5$	V
		Power-down mode; notes 1 and 2	-0.5	+6.5	V
I_O	output source or sink current	$V_O = 0$ to V_{CC}	-	±50	mA
I_{CC}, I_{GND}	V_{CC} or GND current		-	±100	mA
T_{stg}	storage temperature		-65	+150	°C
P_D	power dissipation per package	for temperature range from -40 to +125 °C	-	250	mW

Notes

- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- When $V_{CC} = 0$ V (Power-down mode), the output voltage can be 5.5 V in normal operation.

Single Schmitt-trigger inverter

74LVC1G14

DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T _{amb} (°C)					UNIT
		OTHER	V _{CC} (V)	-40 to +85			-40 to +125		
				MIN.	TYP. ⁽¹⁾	MAX.	MIN.	MAX.	
V _{OL}	LOW-level output voltage	V _I = V _{CC} or GND; I _O = 100 μA	1.65 to 5.5	–	–	0.1	–	0.1	V
		V _I = V _{CC} or GND; I _O = 4 mA	1.65	–	–	0.45	–	0.7	V
		V _I = V _{CC} or GND; I _O = 8 mA	2.3	–	–	0.3	–	0.45	V
		V _I = V _{CC} or GND; I _O = 12 mA	2.7	–	–	0.4	–	0.6	V
		V _I = V _{CC} or GND; I _O = 24 mA	3.0	–	–	0.55	–	0.8	V
		V _I = V _{CC} or GND; I _O = 32 mA	4.5	–	–	0.55	–	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{CC} or GND; I _O = -100 μA	1.65 to 5.5	V _{CC} - 0.1	–	–	V _{CC} - 0.1	–	V
		V _I = V _{CC} or GND; I _O = -4 mA	1.65	1.2	–	–	0.95	–	V
		V _I = V _{CC} or GND; I _O = -8 mA	2.3	1.9	–	–	1.7	–	V
		V _I = V _{CC} or GND; I _O = -12 mA	2.7	2.2	–	–	1.9	–	V
		V _I = V _{CC} or GND; I _O = -24 mA	3.0	2.3	–	–	2.0	–	V
		V _I = V _{CC} or GND; I _O = -32 mA	4.5	3.8	–	–	3.4	–	V
I _{LI}	input leakage current	V _I = 5.5 V or GND	3.6	–	±0.1	±5	–	±100	μA
I _{off}	power OFF leakage current	V _I or V _O = 5.5 V	0	–	±0.1	±10	–	±200	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	5.5	–	0.1	10	–	200	μA
I _{CC}	additional quiescent supply current per pin	V _I = V _{CC} - 0.6 V; I _O = 0	2.3 to 5.5	–	5	500	–	5000	μA

Note

1. All typical values are measured at maximum V_{CC} and T_{amb} = 25 °C.

Single Schmitt-trigger inverter

74LVC1G14

TRANSFER CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T _{amb} (°C)					UNIT
		OTHER	V _{CC} (V)	-40 to +85			-40 to +125		
				MIN.	TYP. ⁽¹⁾	MAX.	MIN.	MAX.	
V _{T+}	positive-going threshold voltage	see Figs. 7 and 8	1.8	0.82	1.0	1.14	0.79	1.14	V
			2.3	1.03	1.2	1.40	1.00	1.40	V
			3.0	1.29	1.5	1.71	1.26	1.71	V
			4.5	1.84	2.1	2.36	1.81	2.36	V
			5.5	2.19	2.5	2.79	2.16	2.79	V
V _{T-}	negative-going threshold voltage	see Figs. 7 and 8	1.8	0.46	0.6	0.75	0.46	0.78	V
			2.3	0.65	0.8	0.96	0.65	0.99	V
			3.0	0.88	1.0	1.24	0.88	1.27	V
			4.5	1.32	1.5	1.84	1.32	1.87	V
			5.5	1.58	1.8	2.24	1.58	2.27	V
V _H	hysteresis voltage (V _{T+} - V _{T-})	see Figs. 7 and 8	1.8	0.26	0.4	0.51	0.19	0.51	V
			2.3	0.28	0.4	0.57	0.22	0.57	V
			3.0	0.31	0.5	0.64	0.25	0.64	V
			4.5	0.40	0.6	0.77	0.34	0.77	V
			5.5	0.47	0.6	0.88	0.41	0.88	V

Note1. All typical values are measured at T_{amb} = 25 °C.

Single Schmitt-trigger inverter

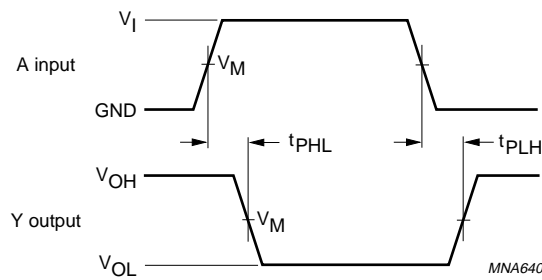
74LVC1G14

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.0$ ns.

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)					UNIT
		WAVEFORMS	V_{CC} (V)	-40 to +85			-40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	
t_{PHL}/t_{PLH}	propagation delay A to Y	see Figs 5 and 6	1.65 to 1.95	1.0	4.1	11.0	1.0	14.0	ns
			2.3 to 2.7	0.7	2.8	6.5	0.7	8.5	ns
			2.7	0.7	3.2	6.5	0.7	8.5	ns
			3.0 to 3.6	0.7	3.0	5.5	0.7	7.0	ns
			4.5 to 5.5	0.7	2.2	5.0	0.7	6.5	ns

AC WAVEFORMS



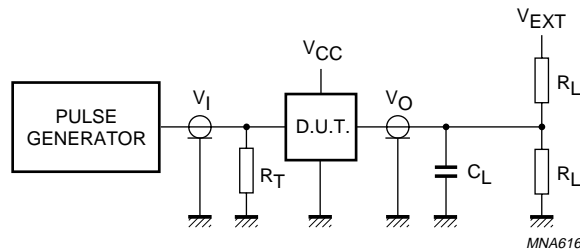
V_{CC}	V_M	INPUT	
		V_I	$t_r = t_f$
1.65 to 1.95 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.3 to 2.7 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns
4.5 to 5.5 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.5 ns

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.5 Input A to output Y propagation delay times.

Single Schmitt-trigger inverter

74LVC1G14



V _{CC}	V _I	C _L	R _L	V _{EXT}		
				t _{PLH} /t _{PHL}	t _{PZH} /t _{PHZ}	t _{PZL} /t _{PLZ}
1.65 to 1.95 V	V _{CC}	30 pF	1 kΩ	open	GND	2 × V _{CC}
2.3 to 2.7 V	V _{CC}	30 pF	500 Ω	open	GND	2 × V _{CC}
2.7 V	2.7 V	50 pF	500 Ω	open	GND	6 V
3.0 to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	6 V
4.5 to 5.5 V	V _{CC}	50 pF	500 Ω	open	GND	2 × V _{CC}

Definitions for test circuit:

R_L = Load resistor.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.6 Load circuitry for switching times.

Single Schmitt-trigger inverter

74LVC1G14

TRANSFER CHARACTERISTIC WAVEFORMS

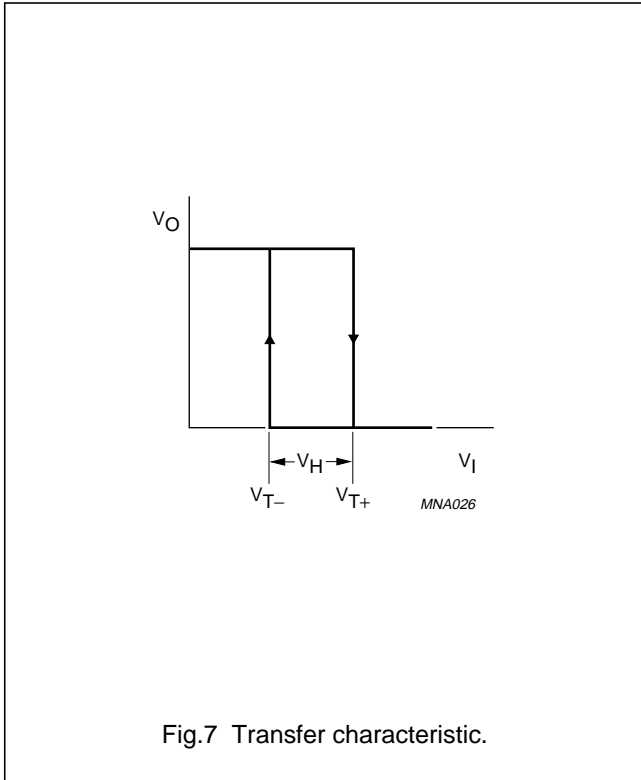


Fig.7 Transfer characteristic.

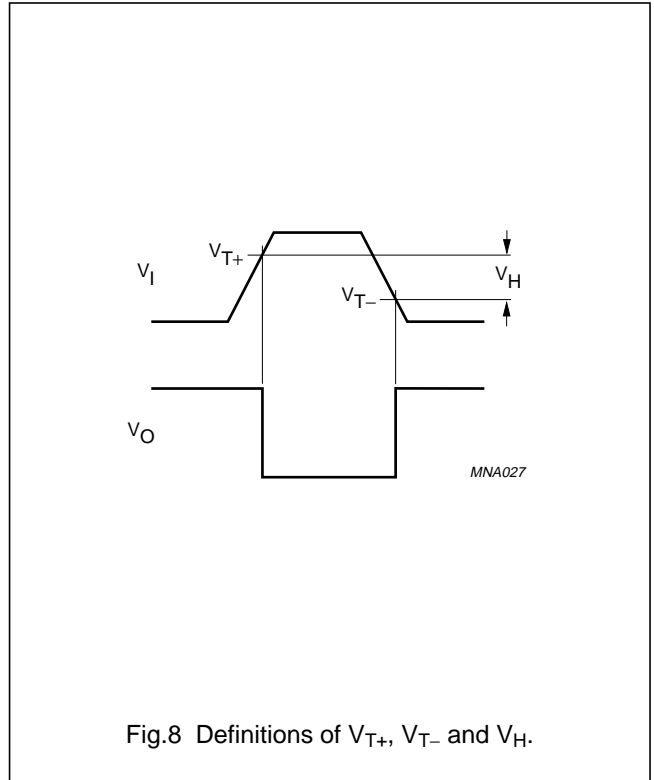


Fig.8 Definitions of V_{T+} , V_{T-} and V_H .

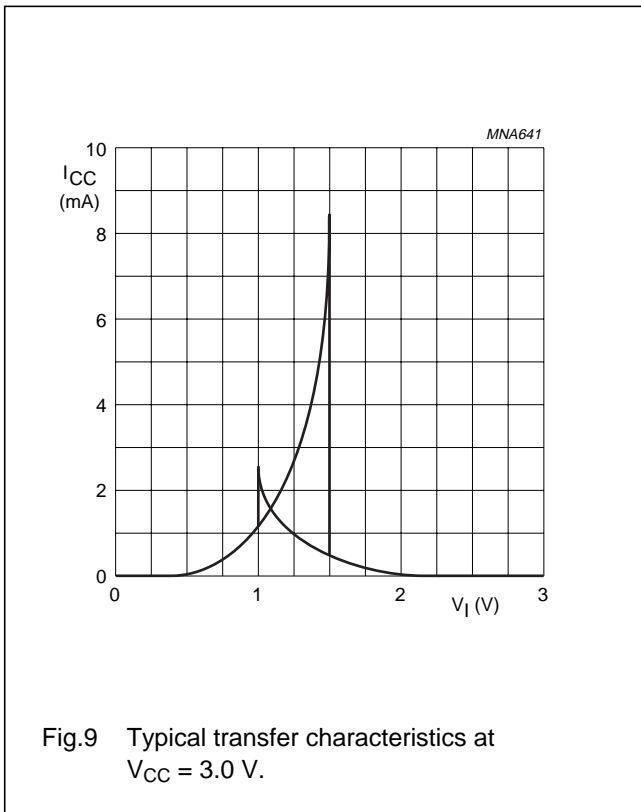


Fig.9 Typical transfer characteristics at $V_{CC} = 3.0$ V.

Single Schmitt-trigger inverter

74LVC1G14

APPLICATION INFORMATION

The slow input rise and fall times cause additional power dissipation, this can be calculated using the following formula:

$$P_{ad} = f_i \times (t_r \times I_{CC(AV)} + t_f \times I_{CC(AV)}) \times V_{CC}$$

where:

- P_{ad} = additional power dissipation (μW);
- f_i = input frequency (MHz);
- t_r = input rise time (ns); 10% to 90%;
- t_f = input fall time (ns); 90% to 10%;
- $I_{CC(AV)}$ = average additional supply current (μA).

Average I_{CC} differs with positive or negative input transitions, as shown in Fig.10.

An example of a relaxation circuit using the 74LVC1G14 is shown in Fig.11.

Remark to the application information

All values given are typical values unless otherwise specified.

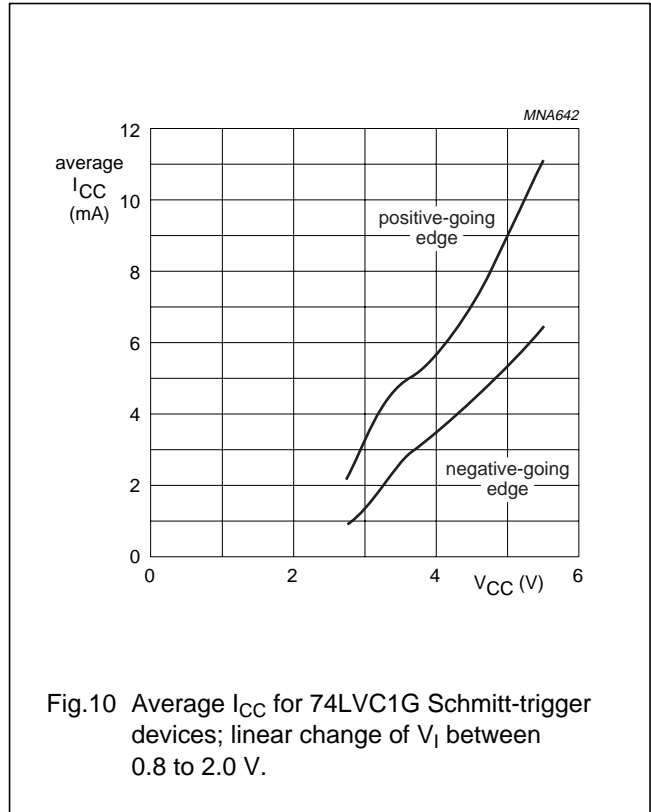
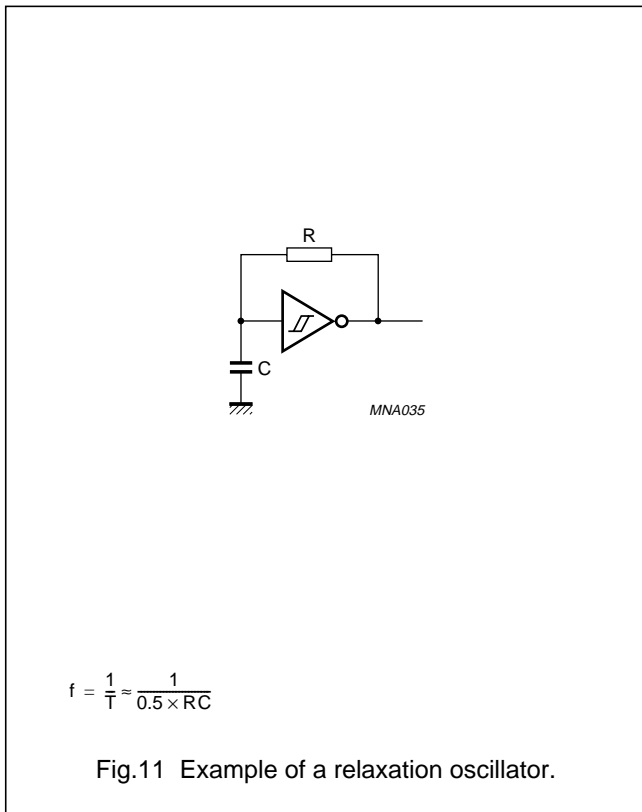


Fig.10 Average I_{CC} for 74LVC1G Schmitt-trigger devices; linear change of V_I between 0.8 to 2.0 V.



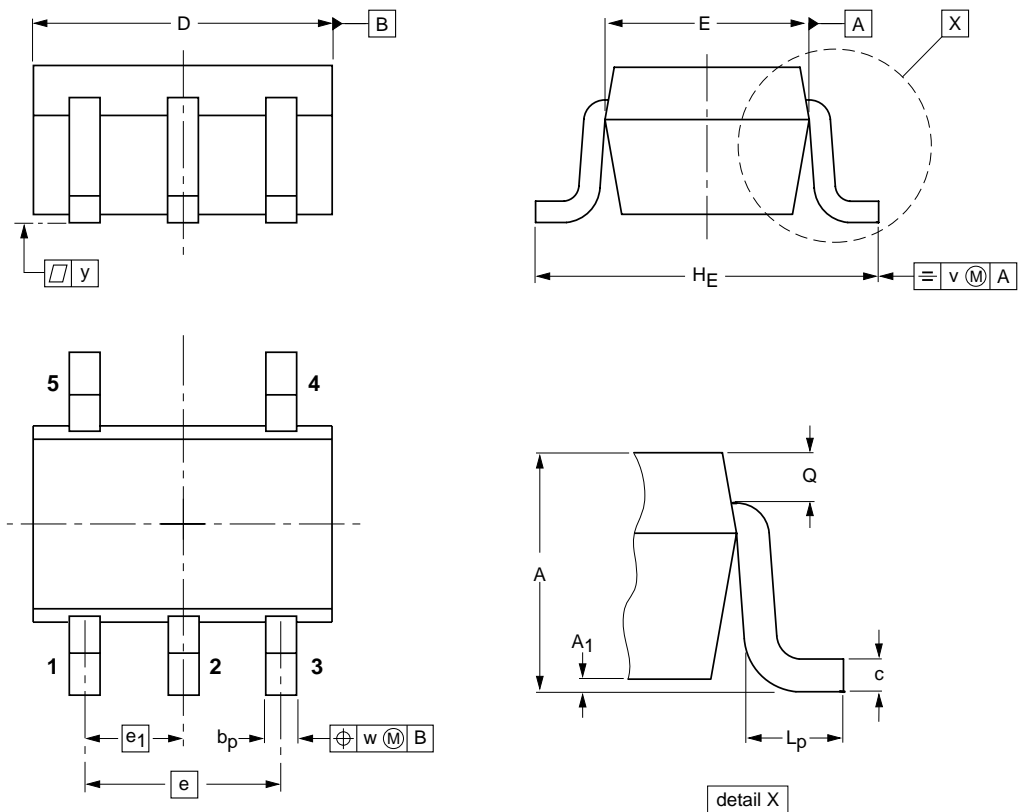
Single Schmitt-trigger inverter

74LVC1G14

PACKAGE OUTLINES

Plastic surface mounted package; 5 leads

SOT353



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	bp	c	D	E ⁽²⁾	e	e ₁	H _E	L _p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT353			SC-88A			97-02-28

Single Schmitt-trigger inverter

74LVC1G14

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Single Schmitt-trigger inverter

74LVC1G14

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE ⁽¹⁾	SOLDERING METHOD	
	WAVE	REFLOW ⁽²⁾
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable ⁽³⁾	suitable
PLCC ⁽⁴⁾ , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended ⁽⁴⁾⁽⁵⁾	suitable
SSOP, TSSOP, VSO	not recommended ⁽⁶⁾	suitable

Notes

1. For more detailed information on the BGA packages refer to the “(LF)BGA Application Note” (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the “Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

Single Schmitt-trigger inverter

74LVC1G14

DATA SHEET STATUS

DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITIONS
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Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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