T-46-13-47

Features

- Third Generation Programmable Logic Structure
  - Easily Achieves Gate Utilization Factors of 80%
- Increased Logic Flexibility
  - 86 Inputs and 72 Sum Terms
- Flexible Output Macrocell
  - 48 Flip-Flops - 2 per Macrocell
  - 3 Sum Terms - Can Be OR'ed and Shared
- High Speed
- Low Power - Less than 0.5mA Typical (ATV2500)
- Multiple Feedback Paths Provide For Buried State Machines and I/O Bus Compatibility
- Asynchronous Clocks and Resets
  - Multiple Synchronous Presets - 1 per 4 or 8 Flip-Flops
- Proven and Reliable High Speed CMOS EPROM Process
  - 2000V ESD Protection
  - 200 mA Latchup Immunity
- Reprogrammable - Tested 100% for Programmability
- 40 pin Dual-In-line and 44 Lead Surface Mount Packages

High Density UV Erasable Programmable Logic Device

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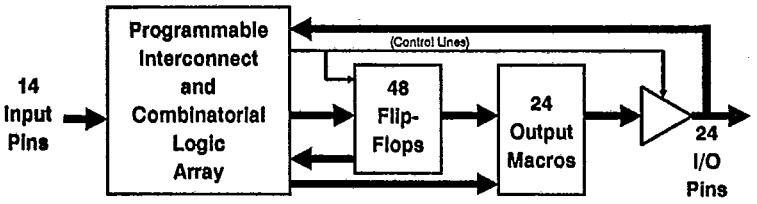
Block Diagram



Description

The ATV2500/H is the most powerful programmable logic device available in a 40 pin package. Increased Product terms, Sum Terms, and Flip-Flops translate into many more usable gates. High gate utilization is easily obtainable.

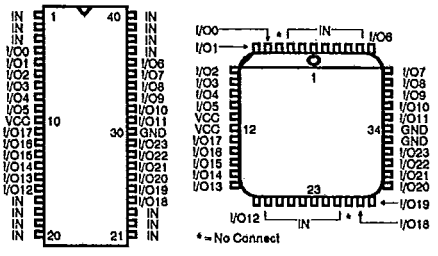
The ATV2500/H is organized around a global bus. All pin and feedback terms are always available to every Logic Cell. Each of the 38 logic pins and their complements are array inputs, as well as the true and false outputs of each of the 48 Flip-Flops.

There are 416 Product Terms available. Four Product Terms are input to each Sum Term. The 3 Sum terms per Logic Cell can be combined to provide up to 12 Product Terms, Combinatorial and Registered. Independent of output configuration, the 2 Flip-Flops are always usable, and always have at least 4 Product Term inputs.

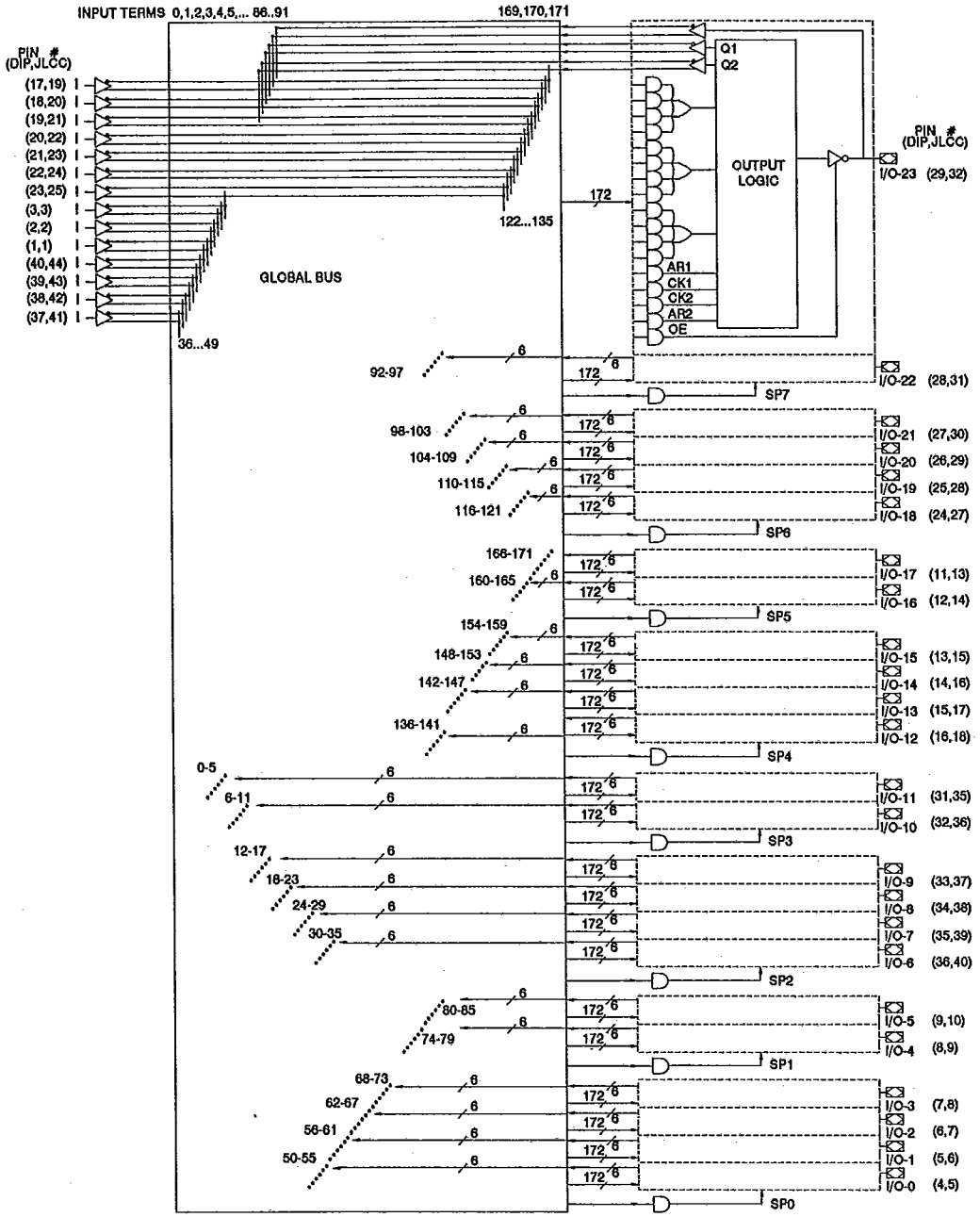
Product terms are available providing Asynchronous Resets, Flip-Flop clocks, and Output Enables. One reset and one clock term are provided per Flip-Flop, with one Enable term per output. Eight product terms provide local Synchronous Presets, divided up into banks of 4 and 8 Flip-Flops. Register Preload and buried register observability simplify testing. The device has an internal power up clear function.

Pin Configurations

Pin Name	Function
IN	Logic Inputs
I/O	Bidirectional Buffers
I/O,0,2,4..	"Even" I/O Buffers
I/O,1,3,5..	"Odd" I/O Buffers
*	No Internal Connection
VCC	+5V Supply



Functional Logic Diagram ATV2500/H



Functional Logic Diagram Description

The ATV2500/H Functional Logic Diagram describes the interconnections between the input, feedback pins and Logic Cells. All interconnections are routed through the Global Bus.

The ATV2500/H is a straightforward and uniform EPLD. The 24 Macrocells are numbered 0 through 23. Each Macrocell contains 17 AND gates. All AND gates have 172 inputs. The five lower product terms provide AR1, CK1, CK2, AR2, and OE. These are: one asynchronous reset and clock per Flip-Flop, and an Output Enable. The top 12 product terms are grouped into 3 sum terms, which are used as shown in the Macrocell diagrams.

Eight Synchronous Preset terms are distributed in a 2/4 pattern. The first four Macrocells share Preset 0, the next two share Preset 1, and so on, ending with the last two Macrocells sharing Preset 7.

The 14 dedicated inputs and their complements use the numbered positions in the global bus as shown. Each Macrocell provides 6 inputs to the global bus: (left to right) Flip-Flop Q2 true and false, Flip-Flop Q1 true and false, and the pin true and false. The positions occupied by these signals in the Global Bus are the six numbers in the bus diagram next to each Macrocell.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0V to +14.0V(1)
Programming Voltage with Respect to Ground	-2.0V to +14.0V(1)
Integrated UV Erase Dose	7258 W•sec/cm²

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:
1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is V_{CC}+0.75V dc which may overshoot to +7.0V for pulses of less than 20ns.

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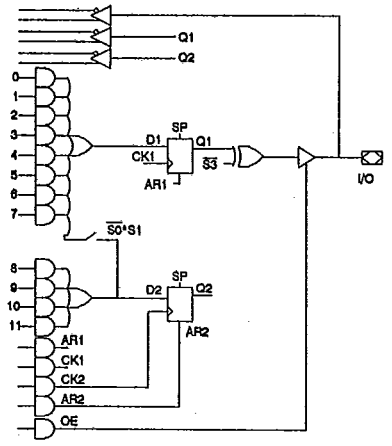
Operating Modes

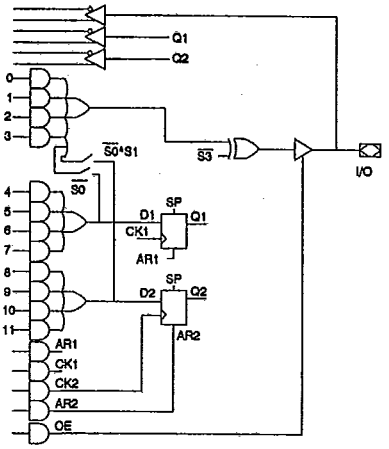
	40 DIP PIN	21	2	38	23	20	V_{CC}(10)	Odd	Even
Mode	44 JLCC PIN	23	2	42	25	22	V_{CC}(11,12)	I/O's	I/O's
"EPLD"		X[1]	X	X	X	X	5V	I/O	I/O
Program		V_{PP}	X	X	X	V_H (2)	6V	D_{IN}	N.C.
PGM Verify		V_{PP}	X	X	X	V_{IL}	6V	D_{OUT}	V_{OH}
PGM Inhibit		V_{PP}	X	X	X	V_{IH}	6V	High Z	High Z
Preload Q1		⎍	X	V_H	V_{IL}/V_{IH}	V_{IL}	5V	D_{IN}(Even/Odd)	V_{IH}
Preload Q2		⎍	X	V_H	V_{IL}/V_{IH}	V_{IH}	5V	D_{IN}(Even/Odd)	V_{IH}
Observe Q2		X	V_H	X	X	X	5V	D_{OUT}	D_{OUT}

Notes: 1. X can be V_{IL} or V_{IH}.
2. V_H = 11.0V to 14.0V

Output Logic, Registered (1)



Output Logic, Combinatorial (1)



Note: 1. These diagrams shows equivalent logic functions, not necessarily the actual circuit implementation.

ATMEL CORP

29E D

			Terms In		
S2	S1	S0	D1	D2	Output Configuration
0	0	0	8	4	Registered (Q1)
0	1	0	12	4(1)	Registered (Q1)

Note: 1. These 4 terms are shared with D1.

S3	Output Configuration
0	Active Low
1	Active High

			Terms In		
S2	S1	S0	D1	D2	Output Configuration
1	0	0	4(1)	4	Combinatorial (8 Terms)
1	0	1	4	4	Combinatorial (4 Terms)
1	1	0	4(1)	4(1)	Combinatorial (12 Terms)

Note: 1. These 4 terms are shared with D1.

S3	Output Configuration
0	Active Low
1	Active High

D.C. and A.C. Operating Conditions

		ATV2500H-25(1)	ATV2500/H-30(1)	ATV2500/H-35	ATV2500-40	ATV2500-45
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C(2)	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C(2)	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

Notes: 1. Preliminary data for all ATV2500H-25's and all ATV2500-30's.
2. Preliminary data for both Industrial and Military ATV2500-35 .

D.C. Characteristics

Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1V to V_{CC} + 1V					10	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1V to V_{CC} + 0.1V					10	µA
I_{CC}	Power Supply Current	V_{CC} = MAX, V_{IN} = GND or V_{CC} Outputs Open	ATV2500	Com.		0.5	5	mA
				Ind.,Mil.		0.5	10	mA
			ATV2500H	Com.		65	120	mA
				Ind.,Mil.		65	140	mA
I_{CC2}	Clocked Power Supply Current (ATV2500)	f = 1MHz, V_{CC} = MAX Outputs Open		Com.		10	15	mA
				Ind.,Mil.		10	20	mA
I_{OS} (1)	Output Short Circuit Current	V_{OUT} = 0.5V					-90	mA
V_{IL}	Input Low Voltage				-0.6		0.8	V
V_{IH}	Input High Voltage				2.0		V_{CC} + 0.75	V
V_{OL}	Output Low Voltage	V_{IN} = V_{IH} or V_{IL}, I_{OL} = 8mACom,Ind;6mA Mil.					0.5	V
V_{OH}	Output High Voltage	I_{OH} = -100µA			V_{CC}-0.3			V
		I_{OH} = -4.0mA			2.4			V

Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.This parameter is only sampled and is not 100% tested. See Absolute Maximum Ratings.

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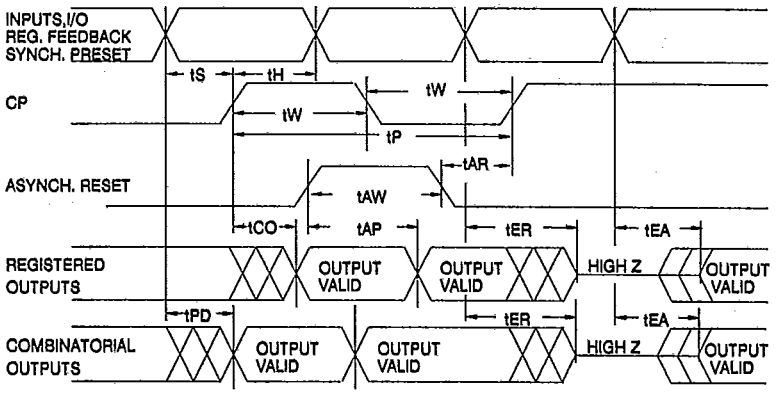
Pin Capacitance (f = 1MHz T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

A.C. Waveforms[1]



Note: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

A.C. Characteristics for the ATV2500

Symbol	Parameter	ATV2500-30[1] Min	ATV2500-30[1] Max	ATV2500-35 Min	ATV2500-35 Max	ATV2500-40 Min	ATV2500-40 Max	ATV2500-45 Min	ATV2500-45 Max	Units
t_{PD}	Input or Feedback to Non-Registered Output		30		35		40		45	ns
t_{EA}	Input to Output Enable		30		35		40		45	ns
t_{ER}	Input to Output Disable		30		35		40		45	ns
t_{CO}	Clock to Output	5	30	5	35	5	40	5	45	ns
t_{CF}	Clock to Feedback	10	20	15	20	15	22	15	25	ns
t_{SI1}	Input Setup Time, Output Register	20		22		25		30		ns
t_{SI2}	Input Setup Time, Buried Register[2]	5		5		5		5		ns
t_{SF}	Feedback Setup Time	10		15		18		20		ns
t_{H1}	Hold Time, Output Register	10		15		15		15		ns
t_{H2}	Hold Time, Buried Register[2]	5		5		5		5		ns
t_W	Clock Width	12		15		17		20		ns
t_P	Clock Period	30		35		40		45		ns
F_{MAX}	Maximum Frequency (1/t_P)		33		28		25		22	MHz
t_{AW}	Asynchronous Reset Width	18		20		22		25		ns
t_{AR}	Asynchronous Reset Recovery Time	18		20		22		25		ns
t_{AP}	Asynchronous Reset to Registered Output Reset		30		35		40		45	ns

Note: 1. Preliminary data.
2. Buried registers include all 24 Q2 registers and any of the 24 Q1 registers in macrocells configured as combinatorial.

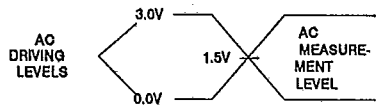
A.C. Characteristics for the ATV2500H

Symbol	Parameter	ATV2500H-25[1] Min	ATV2500H-25[1] Max	ATV2500H-30 Min	ATV2500H-30 Max	ATV2500H-35 Min	ATV2500H-35 Max	Units
t_{PD}	Input or Feedback to Non-Registered Output		25		30		35	ns
t_{EA}	Input to Output Enable		25		30		35	ns
t_{ER}	Input to Output Disable		25		30		35	ns
t_{CO}	Clock to Output	10	25	12	30	15	35	ns
t_{CF}	Clock to Feedback	10	18	12	20	15	20	ns
t_{SI1}	Input Setup Time, Output Register	10		12		15		ns
t_{SI2}	Input Setup Time, Buried Register[2]	5		5		5		ns
t_{SF}	Feedback Setup Time	7		10		15		ns
t_{H1}	Hold Time	5		5		5		ns
t_W	Clock Width	10		12		15		ns
t_P	Clock Period	25		30		35		ns
F_{MAX}	Maximum Frequency (1/t_P)		40		33		28	MHz
t_{AW}	Asynchronous Reset Width	15		18		20		ns
t_{AR}	Asynchronous Reset Recovery Time	15		18		20		ns
t_{AP}	Asynchronous Reset to Registered Output Reset		25		30		35	ns

Note: 1. Preliminary Data.
2. Buried registers include all 24 Q2 registers and any of the 24 Q1 registers in macrocells configured as combinatorial.

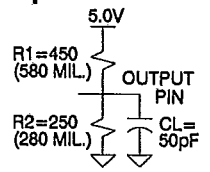
7

Input Test Waveforms and Measurement Levels



tR, tF < 5ns (10% to 90%)

Output Test Load

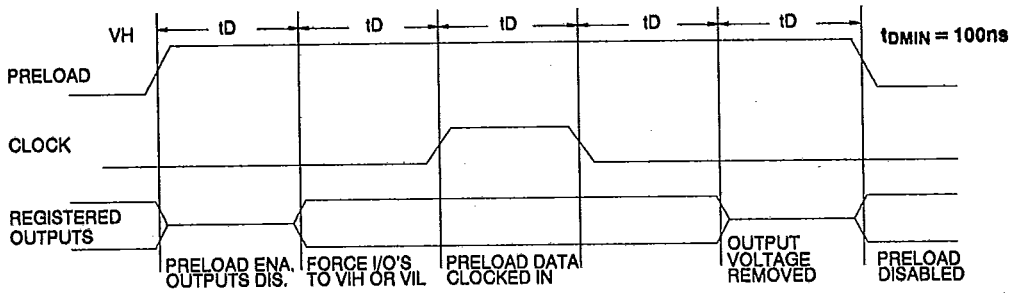


Preload and Observability of Registered Outputs

The ATV2500/H's registers are provided with circuitry to allow loading of each register asynchronously with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A V_{IH} level on the Odd I/O pins will force the appropriate register high; a V_{IL} will force it low, independent of the polarity or other configuration bit settings.

The PRELOAD state is entered by placing an 11V to 14V signal on pin 38 on the DIP and pin 42 on the SMP. When the clock term is pulsed high, (pin 21 on the DIP, pin 23 on the SMP) the data on the I/O pins is placed into the 12 registers chosen by the Q Select and Even/Odd Select Pins.

Register 2 Observability Mode is entered by placing an 11V to 14V signal on pin 2 (DIP or SMP). In this mode, the contents of the Buried Register bank will appear on the associated outputs when the OE control signals are active.



Level forced on Odd I/O pin during PRELOAD cycle.	Q Select Pin State	Even/ Odd Select	Even Q1 state after cycle	Even Q2 state after cycle	Odd Q1 state after cycle	Odd Q2 state after cycle
V_{IH}	Low	Low	High	X	X	X
V_{IL}	Low	Low	Low	X	X	X
V_{IH}	High	Low	X	High	X	X
V_{IL}	High	Low	X	Low	X	X
V_{IH}	Low	High	X	X	High	X
V_{IL}	Low	High	X	X	Low	X
V_{IH}	High	High	X	X	X	High
V_{IL}	High	High	X	X	X	Low

Power Up Reset

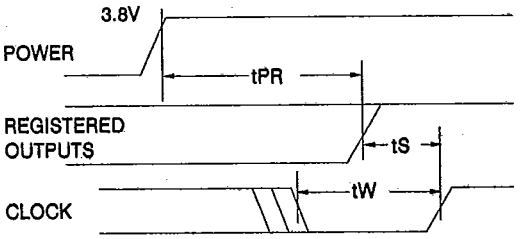
The registers in the ATV2500/H are designed to reset during power up. At a point delayed slightly from V_{CC} crossing 3.8V, all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1) The V_{CC} rise must be monotonic,

2) After reset occurs, all input and feedback setup times must be met before driving the clock term high, and

3) The signals from which the clock is derived must remain stable during t_{PR}.



Parameter	Description	Min	Typ	Max	Units
t_{PR}	Power-Up Reset Time		600	1000	ns

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATV2500/H fuse patterns. Once programmed, the outputs will read programmed during verify. The security fuse should be programmed last, as its effect is immediate.

The security fuse also inhibits Preload and Q2 observability.

Atmel CMOS EPLDs

Atmel's Erasable Programmable Logic Devices utilize an advanced 1.25 micron CMOS EPROM technology. This technology's state of the art features are the optimum combination for EPLDs:

- CMOS technology provides high speed, low power, and high noise immunity.
- EPROM technology is the most cost effective method for producing EPLDs - surpassing bipolar fusible link technology in low cost, while providing the necessary reprogrammability.
- EPROM reprogrammability, which is 100% tested before shipment, provides inherently better programmability and reliability than one-time fusible PLDs.
- Atmel's EPROM process has proven extremely reliable in the volume production of a full line of advanced EPROM memory products, from 64k to 1024k bit devices.

Using The ATV2500's Many Advanced Features

The ATV2500's flexibility puts more usable gates in 40 pins than other EPLDs. Some of the ATV2500's key features are:

- Asynchronous Clocks -

Each of the Flip-Flops in the ATV2500/H has a dedicated product term driving the clock. The user is no longer constrained to using one clock for all the registers. Buried state machines, counters, and registers can all coexist in one device, while running on separate clocks. The ATV2500/H clock period matches that of similar synchronous devices.

- A Total of 48 Registers -

The ATV2500/H provides two Flip-Flops for each Output Macrocell - a total of 48. Each register has its own clock and reset product terms, as well as its own SUM term.

- Independent I/O Pin and Feedback Paths -

Each I/O pin on the ATV2500/H has a dedicated input path. Each of the 48 registers has individual feedback terms into the array. This feature, combined with individual product terms for each I/O's Output Enable, facilitates designs using bi-directional I/O buses.

- 3 Sum Terms per Macrocell -

The ATV2500/H Macrocell can be configured with one Sum term feeding the output, and still have 2 Sum terms feeding the Flip-Flops. This is the simplest method for interfacing with an I/O bus, and no Flip-Flops need be sacrificed.

- Combinable Sum Terms -

Each Output Macrocell's 3 SUM terms can be combined in an OR gate before the Output or the Register. This provides up to 12 product terms per Output or Flip-Flop. When the Registered Output configuration is chosen, 8 terms are automatically available to D1. The 4 terms feeding D2 can also be shared with D1, giving it a total of 12. In the combinatorial mode, 4, 8, or 12 terms can feed the output, with the middle 4 still driving D1 and the bottom 4 still driving D2.

7

Programming Software Support

Software which is capable of transforming Boolean equations, state machine descriptions and truth tables into JEDEC files for the ATV2500/H is available from the following sources:

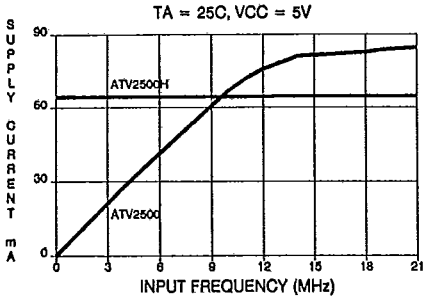
Data I/O / Futurenet Corp.	- ABEL 3.0, 3.1, and above
Logical Devices	- CUPL 3.0 and above
Atmel Corp.	-Atmel-ABEL™ 1.01

Erasure Characteristics

The entire memory array of an ATV2500/H is erased after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of $15 W \cdot sec/cm^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPLD which will be subjected to continuous fluorescent indoor lighting or sunlight.

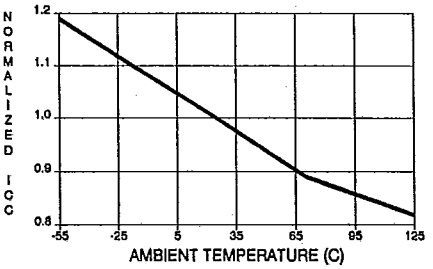
SUPPLY CURRENT vs. INPUT FREQUENCY

TA = 25C, VCC = 5V



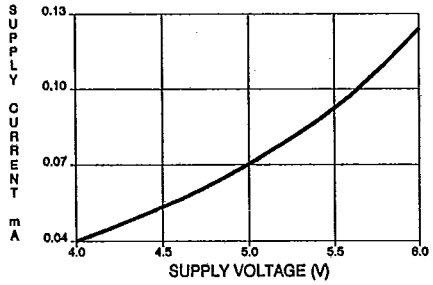
NORMALIZED ICC vs. AMBIENT TEMP.

f = 20 MHz, VCC = 5V



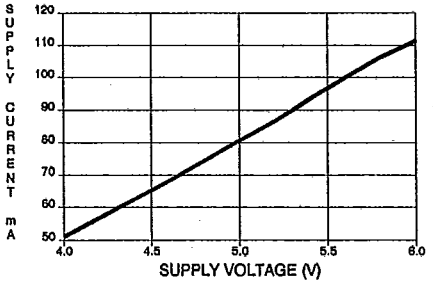
SUPPLY CURRENT vs. SUPPLY VOLTAGE

f = 0 HZ, TA = 25C



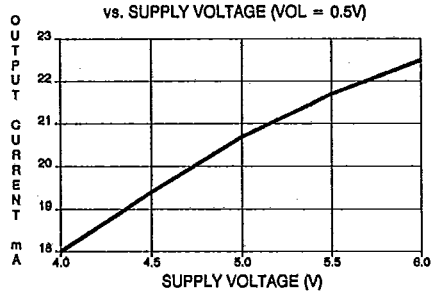
SUPPLY CURRENT vs. SUPPLY VOLTAGE

f = 20 MHz , TA = 25C



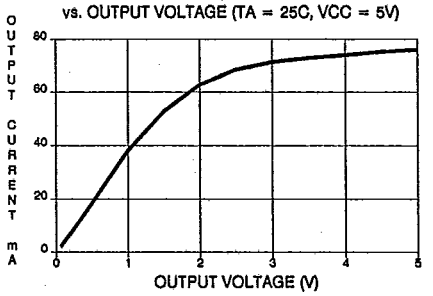
OUTPUT SINK CURRENT

vs. SUPPLY VOLTAGE (VOL = 0.5V)



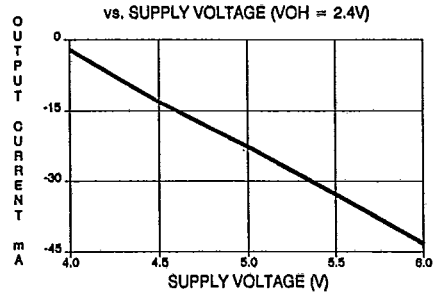
OUTPUT SINK CURRENT

vs. OUTPUT VOLTAGE (TA = 25C, VCC = 5V)



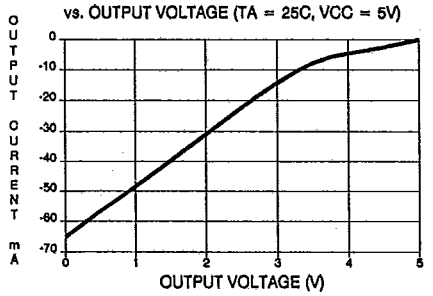
OUTPUT SOURCE CURRENT

vs. SUPPLY VOLTAGE (VOH = 2.4V)

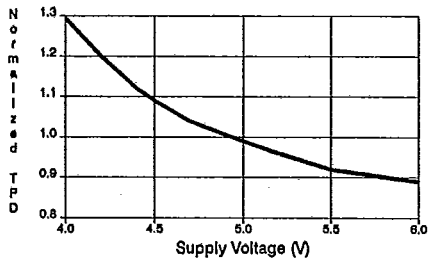


OUTPUT SOURCE CURRENT

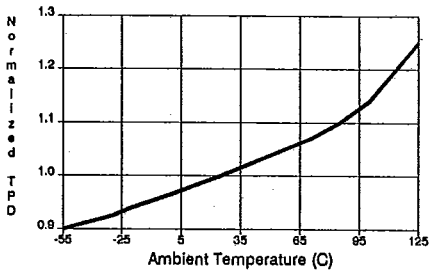
vs. OUTPUT VOLTAGE (TA = 25C, VCC = 5V)



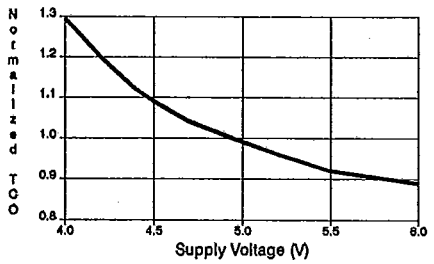
NORMALIZED TPD
vs. SUPPLY VOLTAGE



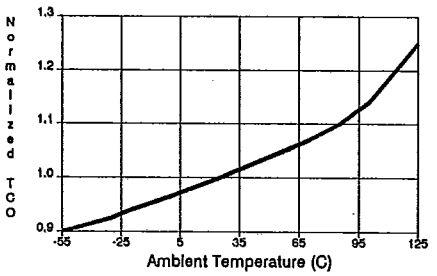
NORMALIZED TPD
vs. TEMPERATURE



NORMALIZED TCO
vs. SUPPLY VOLTAGE

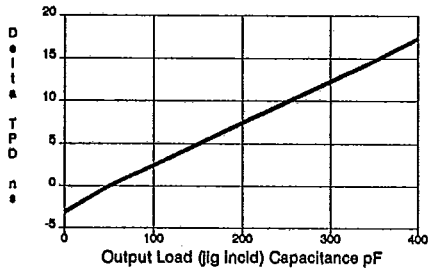


NORMALIZED TCO
vs. TEMPERATURE



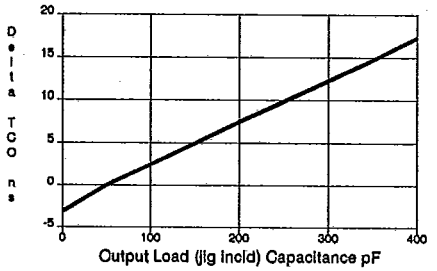
DELTA TPD vs. OUTPUT LOADING

TA = 25C, VCC = 5V



DELTA TCO vs. OUTPUT LOADING

TA = 25C, VCC = 5V



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Ordering Information

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
30	30	33	ATV2500-30DC ATV2500-30JC ATV2500-30KC ATV2500-30LC ATV2500-30PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
35	35	28	ATV2500-35DC ATV2500-35JC ATV2500-35KC ATV2500-35LC ATV2500-35PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
			ATV2500-35DI ATV2500-35JI ATV2500-35KI ATV2500-35LI ATV2500-35PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
			ATV2500-35DM ATV2500-35KM ATV2500-35LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			ATV2500-35DM/883 ATV2500-35KM/883 ATV2500-35LM/883	40DW6 44KW 44LW	Military (-55°C to 125°C) Class B, Fully Compliant
40	40	25	ATV2500-40DC ATV2500-40JC ATV2500-40KC ATV2500-40LC ATV2500-40PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
			ATV2500-40DI ATV2500-40JI ATV2500-40KI ATV2500-40LI ATV2500-40PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
			ATV2500-40DM ATV2500-40KM ATV2500-40LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			ATV2500-40DM/883 ATV2500-40KM/883 ATV2500-40LM/883	40DW6 44KW 44LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
45	45	22	ATV2500-45DI ATV2500-45JI ATV2500-45KI ATV2500-45LI ATV2500-45PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)

Ordering Information

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
45	45	22	ATV2500-45DM ATV2500-45KM ATV2500-45LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			ATV2500-45DM/883 ATV2500-45KM/883 ATV2500-45LM/883	40DW6 44KW 44LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant

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Package Type	
40DW6	40 Lead, 0.600" Wide Windowed, Ceramic Dual Inline Package (Cerdip)
44J	44 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
44KW	44 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
44LW	44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
40P6	40 Lead, 0.600" Wide Plastic Dual Inline Package OTP (PDIP)

Ordering Information

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
25	25	40	ATV2500H-25DC ATV2500H-25JC ATV2500H-25KC ATV2500H-25LC ATV2500H-25PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
			ATV2500H-25DI ATV2500H-25JI ATV2500H-25KI ATV2500H-25LI ATV2500H-25PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
			ATV2500H-25DM ATV2500H-25KM ATV2500H-25LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			ATV2500H-25DM/883 ATV2500H-25KM/883 ATV2500H-25LM/883	40DW6 44KW 44LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
30	30	33	ATV2500H-30DC ATV2500H-30JC ATV2500H-30KC ATV2500H-30LC ATV2500H-30PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
			ATV2500H-30DI ATV2500H-30JI ATV2500H-30KI ATV2500H-30LI ATV2500H-30PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
			ATV2500H-30DM ATV2500H-30KM ATV2500H-30LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			ATV2500H-30DM/883 ATV2500H-30KM/883 ATV2500H-30LM/883	40DW6 44KW 44LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
35	35	28	ATV2500H-35DC ATV2500H-35JC ATV2500H-35KC ATV2500H-35LC ATV2500H-35PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
			ATV2500H-35DI ATV2500H-35JI ATV2500H-35KI ATV2500H-35LI ATV2500H-35PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
			ATV2500H-35DM ATV2500H-35KM ATV2500H-35LM	40DW6 44KW 44LW	Military (-55°C to 125°C)

Ordering Information

t_{PD} (ns)	t_{CO} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
35	35	28	ATV2500H-35DM/883 ATV2500H-35KM/883 ATV2500H-35LM/883	40DW6 44KW 44LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant

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Package Type	
40DW6	40 Lead, 0.600" Wide Windowed, Ceramic Dual Inline Package (Cerdip)
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44KW	44 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
44LW	44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
40P6	40 Lead, 0.600" Wide Plastic Dual Inline Package OTP (PDIP)