

## 32K x 16 Static RAM

### Features

- **3.3V operation (3.0V - 3.6V)**
- **High speed**  
—  $t_{AA} = 10 \text{ ns}$
- **Low active power**  
— **540 mW (max., 12 ns)**
- **Very Low standby power**  
— **330  $\mu\text{W}$  (max., "L" version)**
- **Automatic power-down when deselected**
- **Independent Control of Upper and Lower bytes**
- **Available in 44-pin TSOP II and 400-mil SOJ**

### Functional Description

The CY7C1020V is a high-performance CMOS static RAM organized as 32,768 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

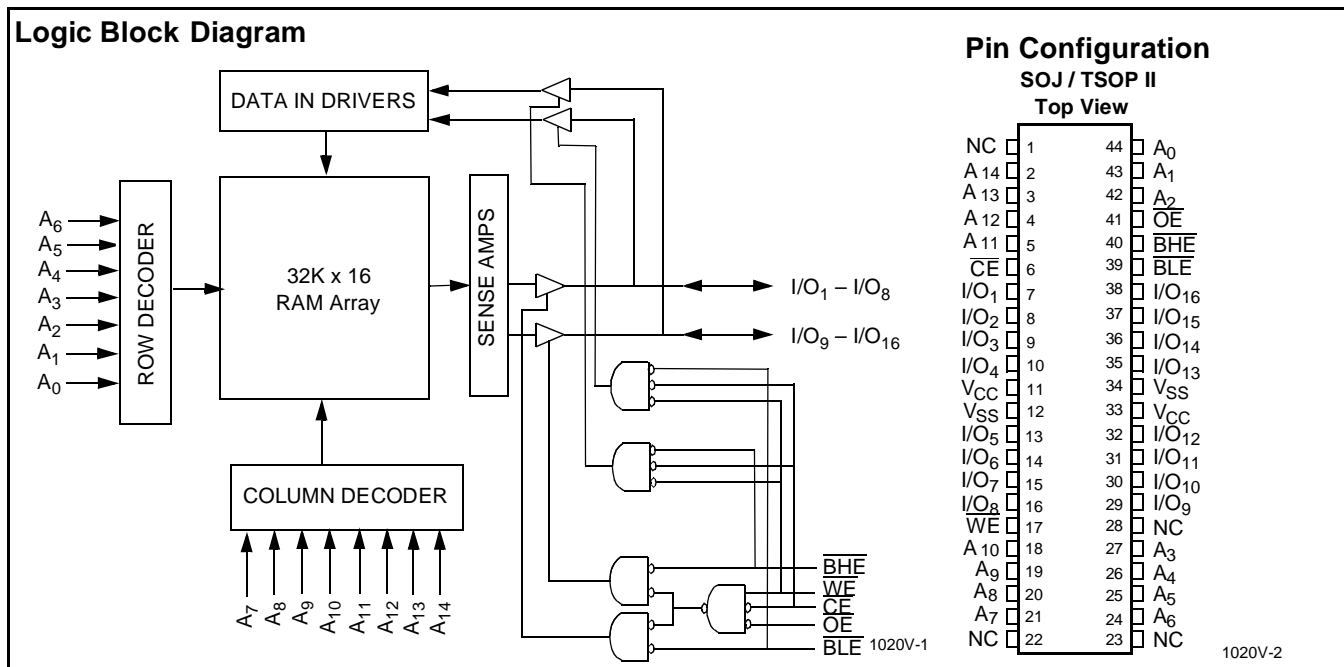
Writing to the device is accomplished by taking chip enable ( $\overline{\text{CE}}$ ) and write enable ( $\overline{\text{WE}}$ ) inputs LOW. If byte low enable

( $\overline{\text{BLE}}$ ) is LOW, then data from I/O pins ( $\text{I/O}_1$  through  $\text{I/O}_8$ ), is written into the location specified on the address pins ( $\text{A}_0$  through  $\text{A}_{14}$ ). If byte high enable ( $\overline{\text{BHE}}$ ) is LOW, then data from I/O pins ( $\text{I/O}_9$  through  $\text{I/O}_{16}$ ) is written into the location specified on the address pins ( $\text{A}_0$  through  $\text{A}_{14}$ ).

Reading from the device is accomplished by taking chip enable ( $\overline{\text{CE}}$ ) and output enable ( $\overline{\text{OE}}$ ) LOW while forcing the write enable ( $\overline{\text{WE}}$ ) HIGH. If byte low enable ( $\overline{\text{BLE}}$ ) is LOW, then data from the memory location specified by the address pins will appear on  $\text{I/O}_1$  to  $\text{I/O}_8$ . If byte high enable ( $\overline{\text{BHE}}$ ) is LOW, then data from memory will appear on  $\text{I/O}_9$  to  $\text{I/O}_{16}$ . See the truth table at the back of this datasheet for a complete description of read and write modes.

The input/output pins ( $\text{I/O}_1$  through  $\text{I/O}_{16}$ ) are placed in a high-impedance state when the device is deselected ( $\overline{\text{CE}}$  HIGH), the outputs are disabled ( $\overline{\text{OE}}$  HIGH), the  $\overline{\text{BHE}}$  and  $\overline{\text{BLE}}$  are disabled ( $\overline{\text{BHE}}$ ,  $\overline{\text{BLE}}$  HIGH), or during a write operation ( $\overline{\text{CE}}$  LOW, and  $\overline{\text{WE}}$  LOW).

The CY7C1020V is available in standard 44-pin TSOP type II and 400-mil-wide SOJ packages.



### Selection Guide

	7C1020V-10	7C1020V-12	7C1020V-15	7C1020V-20
Maximum Access Time (ns)	10	12	15	20
Maximum Operating Current (mA)		130	120	110
	L	100	90	80
Maximum CMOS Standby Current (mA)		1	1	1
	L	0.1	0.1	0.1

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with  
 Power Applied ..... -55°C to +125°C  
 Supply Voltage on  $V_{CC}$  to Relative GND<sup>[1]</sup> ..... -0.5V to +4.6V  
 DC Voltage Applied to Outputs  
 in High Z State<sup>[1]</sup> ..... -0.5V to  $V_{CC} + 0.5V$   
 DC Input Voltage<sup>[1]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

Current into Outputs (LOW) ..... 20 mA  
 Static Discharge Voltage ..... >2001V  
 (per MIL-STD-883, Method 3015)  
 Latch-Up Current ..... >200 mA

**Operating Range**

Range	Ambient Temperature <sup>[2]</sup>	$V_{CC}$
Commercial	0°C to +70°C	3.0V - 3.6V
Industrial	-40°C to +85°C	3.0V - 3.6V

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	7C1020V-10		7C1020V-12		Unit
			Min.	Max.	Min.	Max.	
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		2.4		V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4		0.4	V
$V_{IH}$	Input HIGH Voltage		2.0	$V_{CC} + 0.3V$	2.0	$V_{CC} + 0.3V$	V
$V_{IL}$	Input LOW Voltage <sup>[1]</sup>		-0.5	0.8	-0.5	0.8	V
$I_{IX}$	Input Load Current	$GND \leq V_I \leq V_{CC}$	-1	+1	-1	+1	$\mu\text{A}$
$I_{OZ}$	Output Leakage Current	$GND \leq V_I \leq V_{CC}$ , Output Disabled	-2	+2	-2	+2	$\mu\text{A}$
$I_{CC}$	$V_{CC}$ Operating Supply Current	$V_{CC} = \text{Max.}, I_{OUT} = 0 \text{ mA}, f = f_{MAX} = 1/t_{RC}$		130		120	mA
			L	100		90	mA
$I_{SB1}$	Automatic CE Power-Down Current — TTL Inputs	Max. $V_{CC}$ , $\overline{CE} \geq V_{IH}$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}, f = f_{MAX}$		15		15	mA
			L	7		7	mA
$I_{SB2}$	Automatic CE Power-Down Current — CMOS Inputs	Max. $V_{CC}$ , $\overline{CE} \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ , or $V_{IN} \leq 0.3V, f=0$		1		1	mA
			L	100		100	$\mu\text{A}$

**Notes:**

- $V_{IL}$  (min.) = -2.0V for pulse durations of less than 20 ns.
- $T_A$  is the "instant on" case temperature.



**Electrical Characteristics** Over the Operating Range (continued)

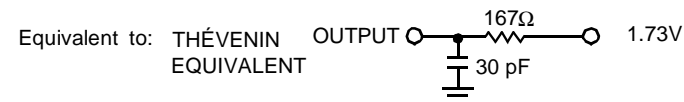
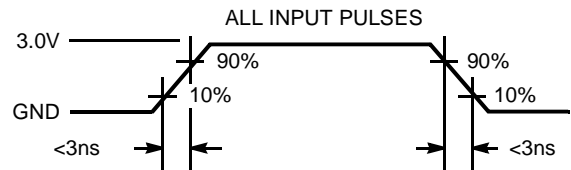
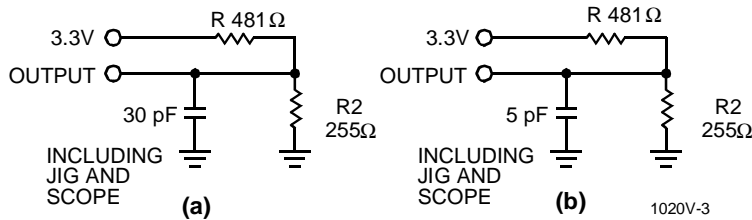
Parameter	Description	Test Conditions	7C1020V-15		7C1020V-20		Unit
			Min.	Max.	Min.	Max.	
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		2.4		V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4		0.4	V
$V_{IH}$	Input HIGH Voltage		2.0	$V_{CC} + 0.3\text{V}$	2.0	$V_{CC} + 0.3\text{V}$	V
$V_{IL}$	Input LOW Voltage <sup>[1]</sup>		-0.5	0.8	-0.5	0.8	V
$I_{IX}$	Input Load Current	$GND \leq V_I \leq V_{CC}$	-1	+1	-1	+1	$\mu\text{A}$
$I_{OZ}$	Output Leakage Current	$GND \leq V_I \leq V_{CC}$ , Output Disabled	-2	+2	-2	+2	$\mu\text{A}$
$I_{CC}$	$V_{CC}$ Operating Supply Current	$V_{CC} = \text{Max.}, I_{OUT} = 0 \text{ mA}, f = f_{MAX} = 1/t_{RC}$		110		100	mA
			L	80		70	mA
$I_{SB1}$	Automatic CE Power-Down Current — TTL Inputs	Max. $V_{CC}$ , $\overline{CE} \geq V_{IH}$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{MAX}$		15		15	mA
			L	7		7	mA
$I_{SB2}$	Automatic CE Power-Down Current — CMOS Inputs	Max. $V_{CC}$ , $CE \geq V_{CC} - 0.3\text{V}$ , $V_{IN} \geq V_{CC} - 0.3\text{V}$ , or $V_{IN} \leq 0.3\text{V}$ , $f=0$		1		1	mA
			L	100		100	$\mu\text{A}$

**Capacitance<sup>[3]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ\text{C}, f = 1 \text{ MHz}, V_{CC} = 3.3\text{V}$	8	pF
$C_{OUT}$	Output Capacitance		8	pF

**Notes:**

3. Tested initially and after any design or process changes that may affect these parameters.

**AC Test Loads and Waveforms**


1020V-4



**Switching Characteristics<sup>[4]</sup> Over the Operating Range**

Parameter	Description	7C1020V-10		7C1020V-12		7C1020V-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>								
t <sub>RC</sub>	Read Cycle Time	10		12		15		ns
t <sub>AA</sub>	Address to Data Valid		10		12		15	ns
t <sub>OHA</sub>	Data Hold from Address Change	3		3		3		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		10		12		15	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		5		6		7	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[5, 6]</sup>		5		6		7	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low Z <sup>[6]</sup>	3		3		3		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High Z <sup>[5, 6]</sup>		5		6		7	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power-Down		12		12		15	ns
t <sub>DBE</sub>	Byte enable to Data Valid		5		6		7	ns
t <sub>LZBE</sub>	Byte enable to Low Z	0		0		0		ns
t <sub>HZBE</sub>	Byte disable to High Z		5		6		7	ns
<b>WRITE CYCLE<sup>[7]</sup></b>								
t <sub>WC</sub>	Write Cycle Time	10		12		15		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	8		9		10		ns
t <sub>AW</sub>	Address Set-Up to Write End	7		8		10		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	7		8		10		ns
t <sub>SD</sub>	Data Set-Up to Write End	5		6		10		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		0		ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[6]</sup>	3		3		3		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[5, 6]</sup>		5		6		7	ns
t <sub>BW</sub>	Byte enable to end of write	7		8		9		ns

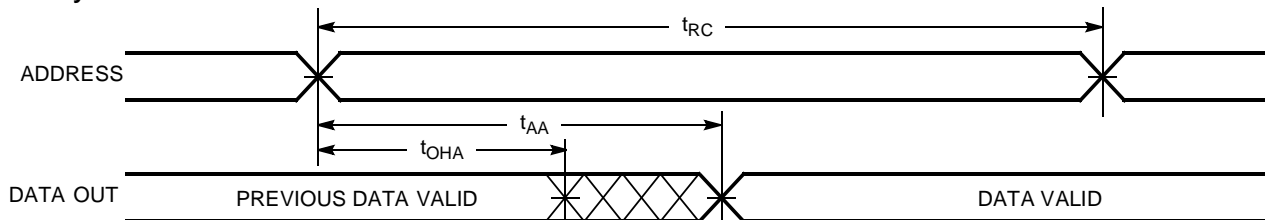
**Notes:**

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30-pF load capacitance.
- t<sub>HZOE</sub>, t<sub>HZBE</sub>, t<sub>HZCE</sub>, and t<sub>HZWE</sub> are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
- At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW,  $\overline{WE}$  LOW and BHE / BLE LOW.  $\overline{CE}$ ,  $\overline{WE}$  and BHE / BLE must be LOW to initiate a write, and the transition of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.



**Switching Characteristics<sup>[4]</sup> Over the Operating Range (continued)**

Parameter	Description	7C1020V-20		Unit
		Min.	Max.	
<b>READ CYCLE</b>				
$t_{RC}$	Read Cycle Time	20		ns
$t_{AA}$	Address to Data Valid		20	ns
$t_{OHA}$	Data Hold from Address Change	3		ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid		20	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		9	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z	0		ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low Z <sup>[6]</sup>	3		ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High Z <sup>[5, 6]</sup>		9	ns
$t_{PU}$	$\overline{CE}$ LOW to Power-Up	0		ns
$t_{PD}$	$\overline{CE}$ HIGH to Power-Down		20	ns
$t_{DBE}$	Byte enable to Data Valid		9	ns
$t_{LZBE}$	Byte enable to Low Z	0		ns
$t_{HZBE}$	Byte disable to High Z		9	ns
<b>WRITE CYCLE<sup>[7]</sup></b>				
$t_{WC}$	Write Cycle Time	20		ns
$t_{SCE}$	$\overline{CE}$ LOW to Write End	12		ns
$t_{AW}$	Address Set-Up to Write End	12		ns
$t_{HA}$	Address Hold from Write End	0		ns
$t_{SA}$	Address Set-Up to Write Start	0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	12		ns
$t_{SD}$	Data Set-Up to Write End	10		ns
$t_{HD}$	Data Hold from Write End	0		ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[6]</sup>	3		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[5, 6]</sup>		9	ns
$t_{BW}$	Byte enable to end of write	12		ns

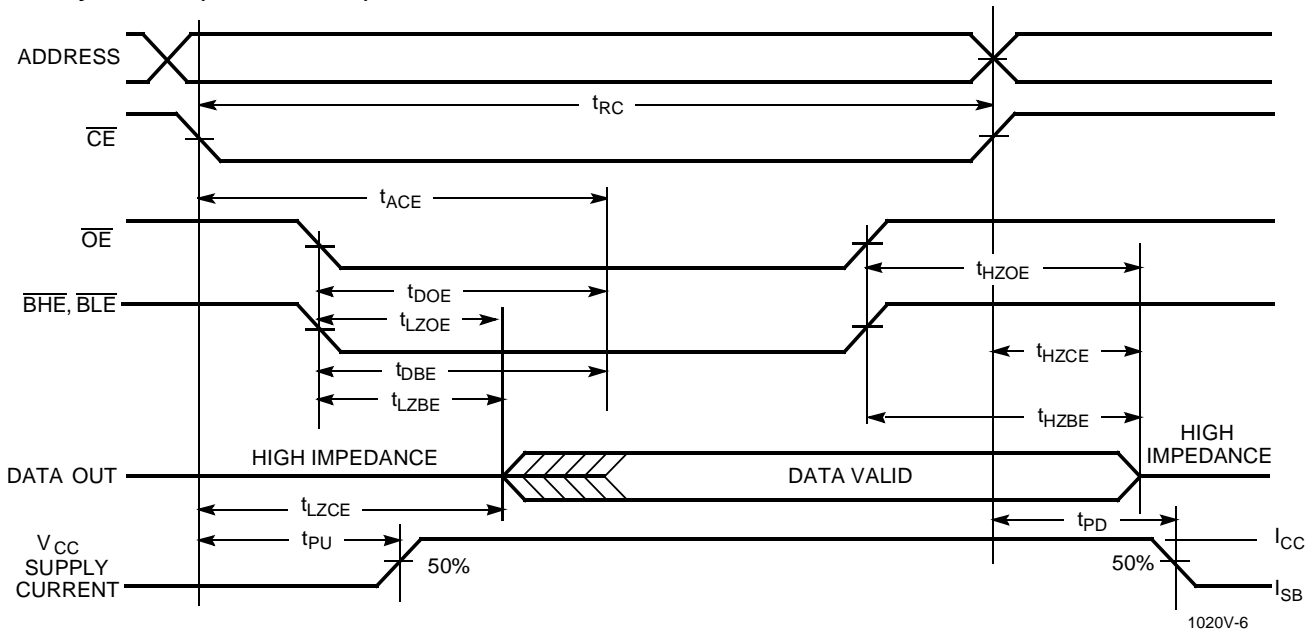
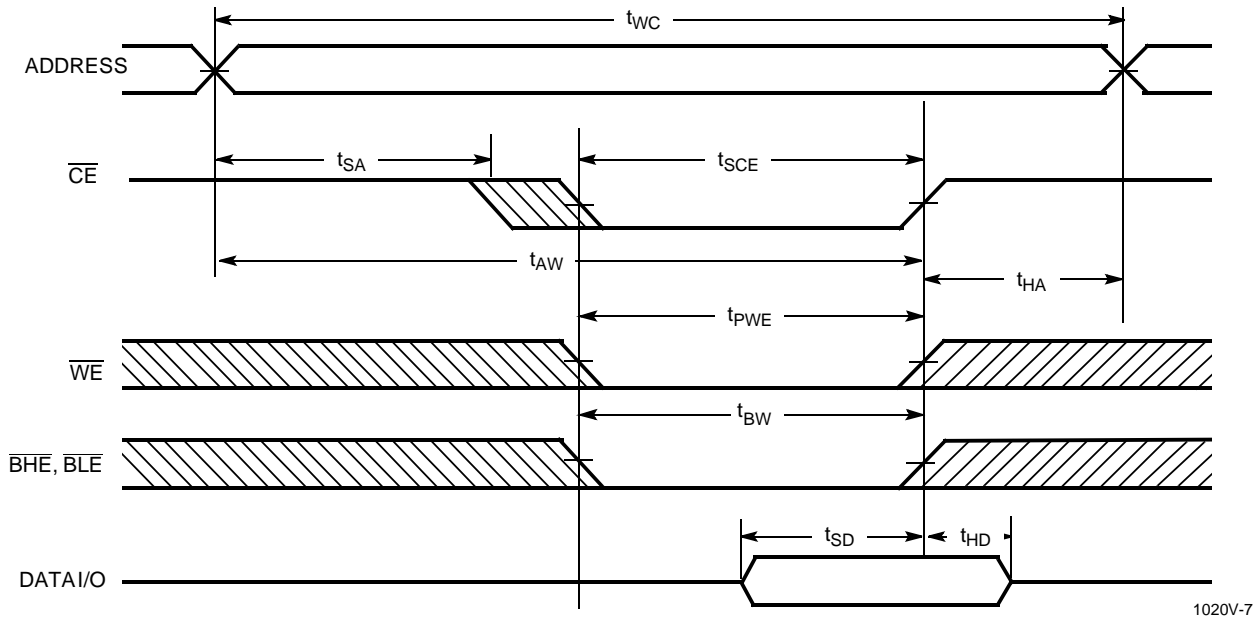
**Switching Waveforms**
**Read Cycle No.1<sup>[8, 9]</sup>**


1020V-5

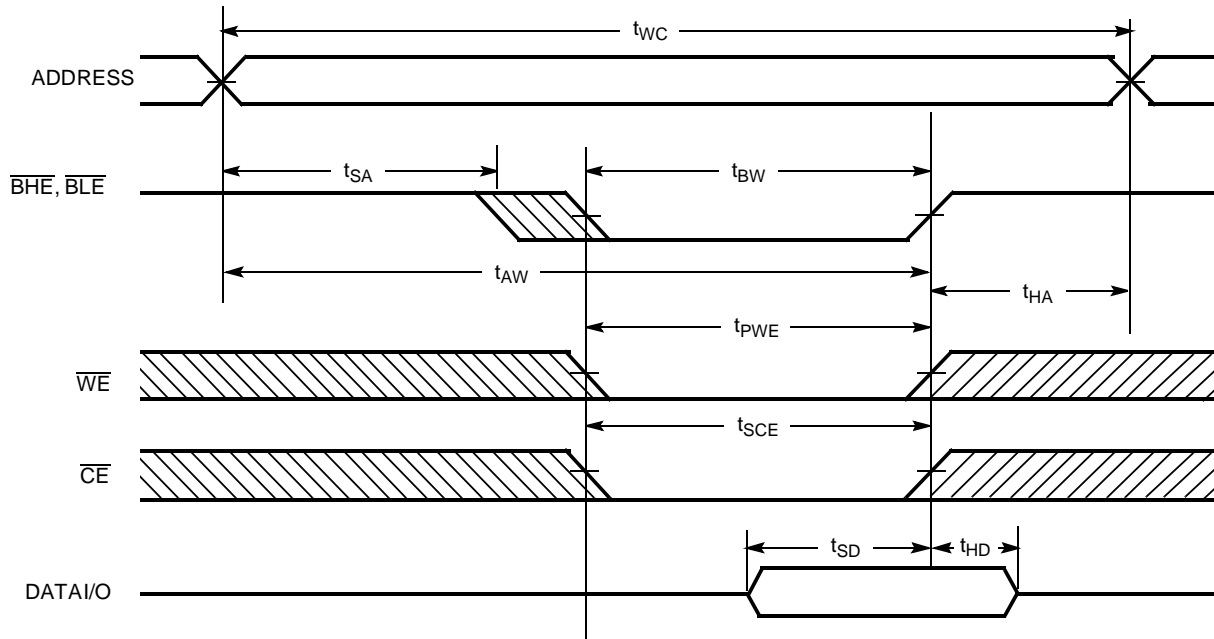
**Notes:**

8. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$ ,  $\overline{BHE}$ , and/or  $\overline{BHE} = V_{IL}$
9.  $\overline{WE}$  is HIGH for read cycle.

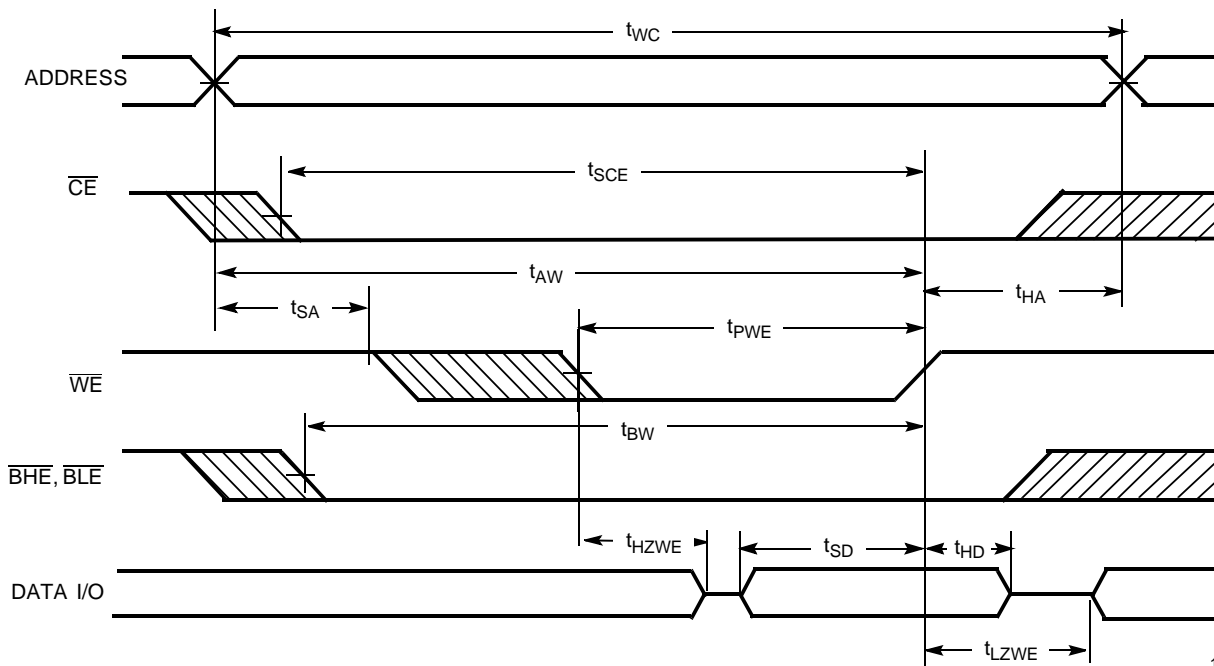


**Switching Waveforms (continued)**
**Read Cycle No.2 ( $\overline{OE}$  Controlled)** <sup>[9, 10]</sup>

**Write Cycle No. 1 ( $\overline{CE}$  Controlled)** <sup>[11, 12]</sup>

**Notes:**

10. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
11. Data I/O is high impedance if  $\overline{OE}$  or BHE and/or BLE =  $V_{IH}$ .
12. If  $\overline{CE}$  goes HIGH simultaneously with WE going HIGH, the output remains in a high-impedance state.

**Switching Waveforms (continued)**
**Write Cycle No. 2 ( $\overline{\text{BLE}}$  or  $\overline{\text{BHE}}$  Controlled)**


1020V-8

**Write Cycle No.3 ( $\overline{\text{WE}}$  Controlled, LOW)**


1020V-10

**Truth Table**

<b>CE</b>	<b>OE</b>	<b>WE</b>	<b>BLE</b>	<b>BHE</b>	<b>I/O<sub>1</sub> - I/O<sub>8</sub></b>	<b>I/O<sub>9</sub> - I/O<sub>16</sub></b>	<b>Mode</b>	<b>Power</b>
H	X	X	X	X	High Z	High Z	Power-Down	Standby (I <sub>SB</sub> )
L	L	H	L	L	Data Out	Data Out	Read - All bits	Active (I <sub>CC</sub> )
			L	H	Data Out	High Z	Read - Lower bits only	Active (I <sub>CC</sub> )
			H	L	High Z	Data Out	Read - Upper bits only	Active (I <sub>CC</sub> )
L	X	L	L	L	Data In	Data In	Write - All bits	Active (I <sub>CC</sub> )
			L	H	Data In	High Z	Write - Lower bits only	Active (I <sub>CC</sub> )
			H	L	High Z	Data In	Write - Upper bits only	Active (I <sub>CC</sub> )
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active (I <sub>CC</sub> )
L	X	X	H	H	High Z	High Z	Selected, Outputs Disabled	Active (I <sub>CC</sub> )

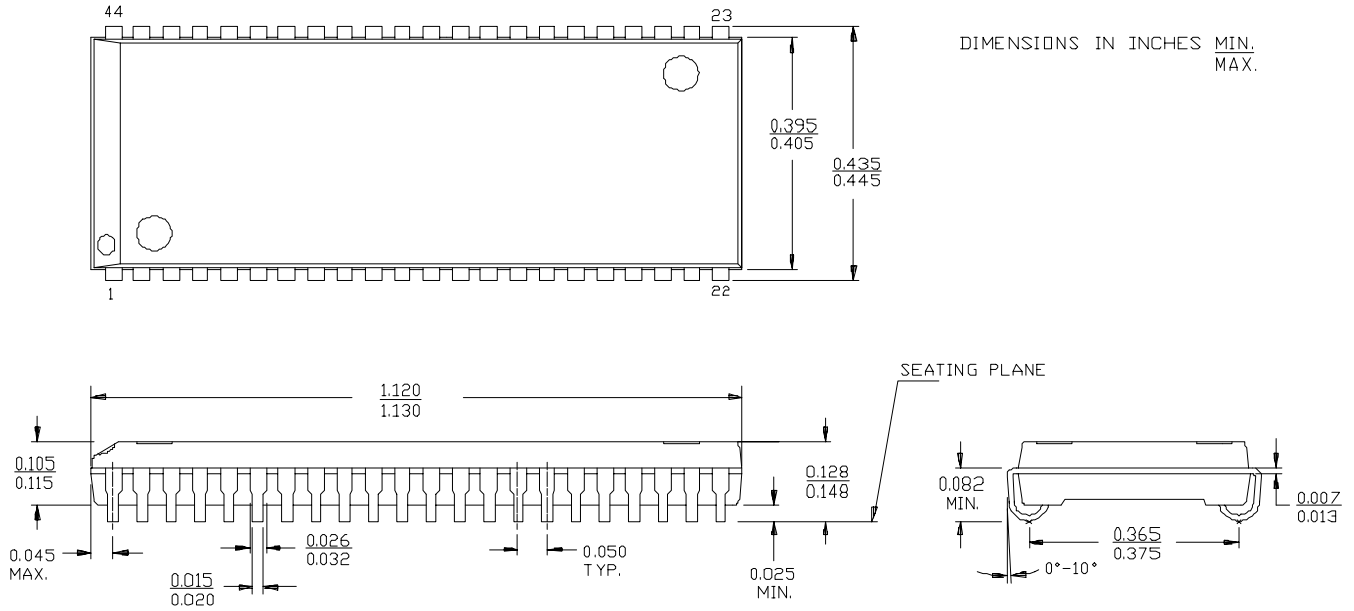
**Ordering Information**

<b>Speed (ns)</b>	<b>Ordering Code</b>	<b>Package Name</b>	<b>Package Type</b>	<b>Operating Range</b>
10	CY7C1020V33-10VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1020V33L-10VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1020V33-10ZC	Z44	44-Lead TSOP Type II	Commercial
	CY7C1020V33L-10ZC	Z44	44-Lead TSOP Type II	Commercial
12	CY7C1020V33-12VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1020V33L-12VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1020V33-12ZC	Z44	44-Lead TSOP Type II	Commercial
	CY7C1020V33L-12ZC	Z44	44-Lead TSOP Type II	Commercial
15	CY7C1020V33-15VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1020V33L-15VC	V34	44-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1020V33-15ZC	Z44	44-Lead TSOP Type II	Commercial
	CY7C1020V33L-15ZC	Z44	44-Lead TSOP Type II	Commercial
	CY7C1020V33-15ZI	Z44	44-Lead TSOP Type II	Industrial
20	CY7C1020V33L-20ZC	Z44	44-Lead TSOP Type II	Commercial

Document #: 38-00543-B

**Package Diagrams**

**44-Lead (400-Mil) Molded SOJ V34**



**44-Pin TSOP II Z44**

DIMENSION IN MM (INCH)  
MAX  
MIN  
LEAD COPLANARITY 0.004 INCHES.

