

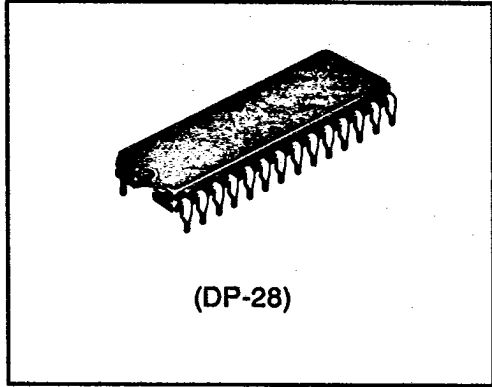
HD44007A

T-77-17

Sync Signal Generator for TV Cameras (NTSC, PAL/SECAM)

Functions

- Four times chroma sub-carrier oscillator frequency
- (B-Y) and (R-Y) chroma sub-carrier output circuit
- Active filter genlock phase detector
- Horizontal programmable logic array
- Vertical programmable logic array
- Horizontal/vertical programmable logic array



(DP-28)

Ordering Information

Type No.	Package
HD44007A	DP-28



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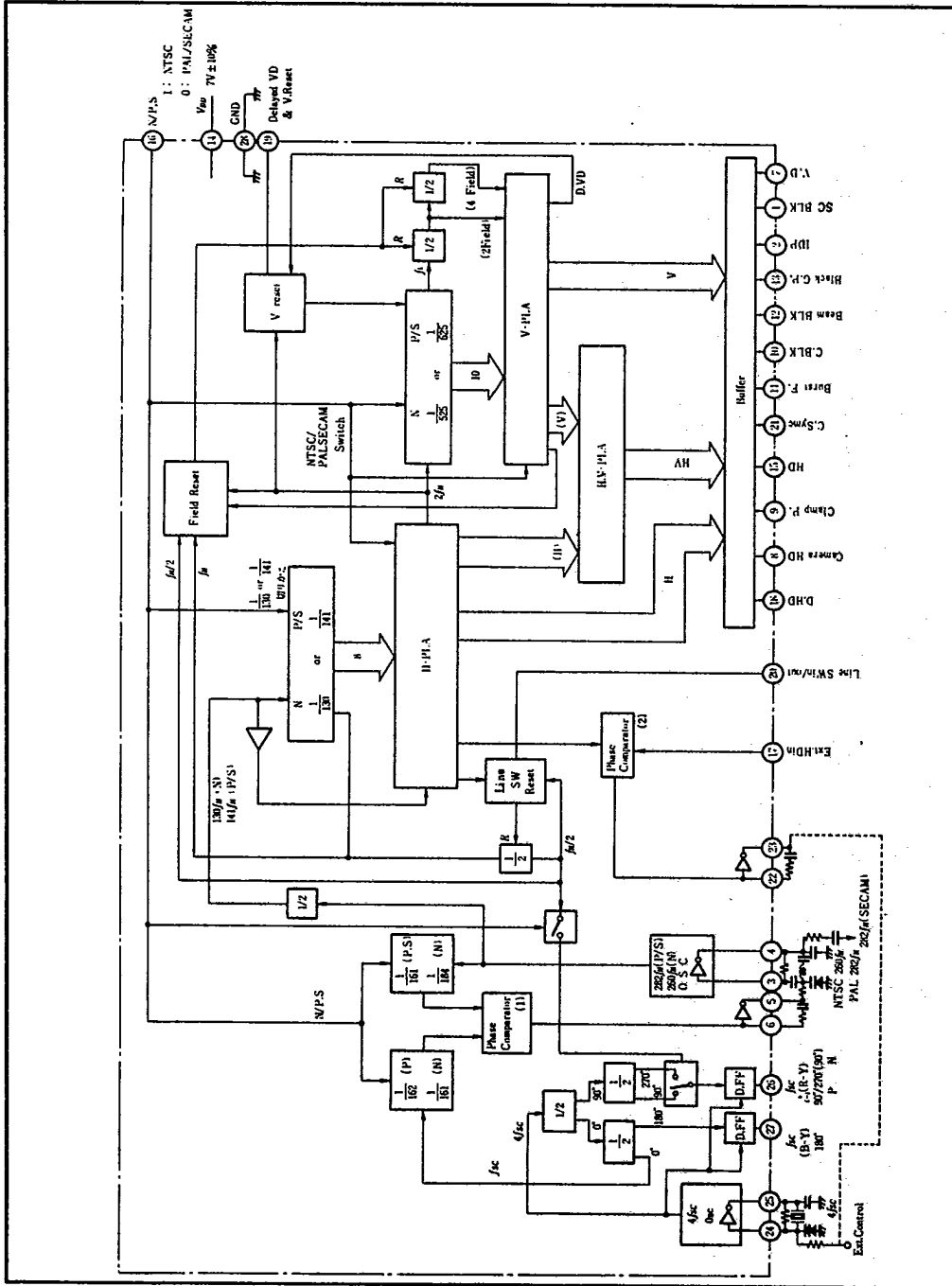
Pin Description

Pin No.	Function	Note	Max Output Current
1	SC. BLK	Identification pulse for SECAM	+250 μ A
2	ID. P	Identification pulse for SECAM	+250 μ A
3	260 f _H /282 f _H osc	In	
4	260 f _H /282 f _H osc	Out	
5	Filter	Out	
6	Filter	In	
7	VD		\pm 250 μ A
8	Camera HD		\pm 500 μ A
9	Clamp P		\pm 500 μ A
10	Composite BLK		\pm 500 μ A
11	Burst flag P		\pm 100 μ A
12	Beam BLK		\pm 500 μ A
13	Black gate P		\pm 500 μ A
14	V _{DD}	6.3 V to 7.0 V, typ 7.7 V	
15	HD		\pm 500 μ A
16	Selector input	High level for NTSC, low level for PAL and SECAM	
17	External HD in	H genlock input	
18	Delayed HD		\pm 500 μ A
19	Delayed VD in/out	In/out, output: V _{OH} \geq 0.8 V _{DD} , V _{OL} = 0.5 V _{DD} , input threshold 0.25 V _{DD}	-500 μ A
20	Line SW in/out	In/out, pull-up resistor built-in	+250 μ A
21	Composite Sync		
22	Filter	In	
23	Filter	Out	
24	4 f _{SC} osc	In	
25	4 f _{SC} osc	Out	
26	SC (90°/270°)	For NTSC, 90° only (high level at pin 16)	\pm 100 μ A
27	SC (180°)		\pm 100 μ A
28	GND		



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Block Diagram



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Operations

Interleave (external HS input, pin 17 and phase comparator 2 are not used.) See figures 1 and 2.

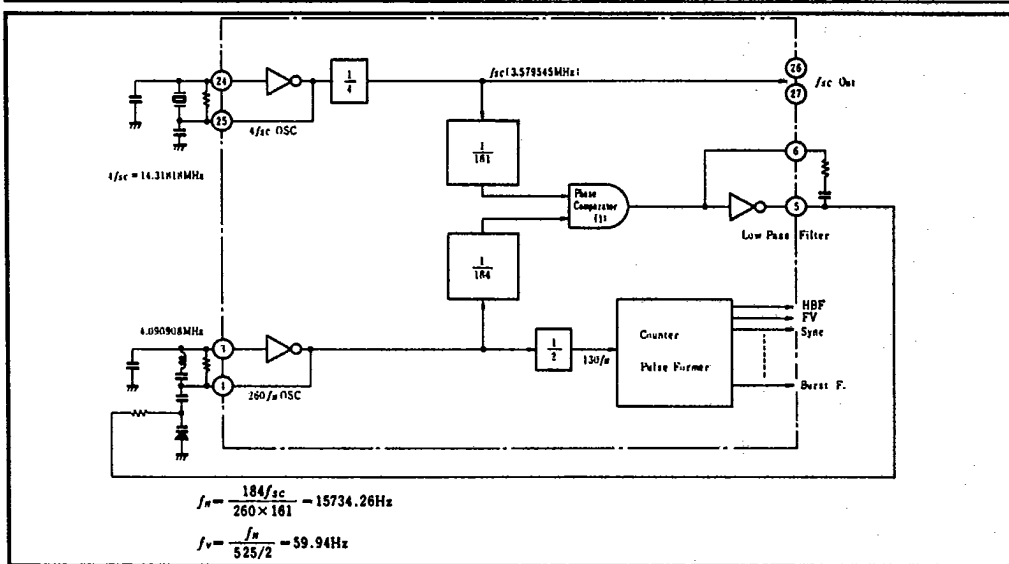


Figure 1 NTSC

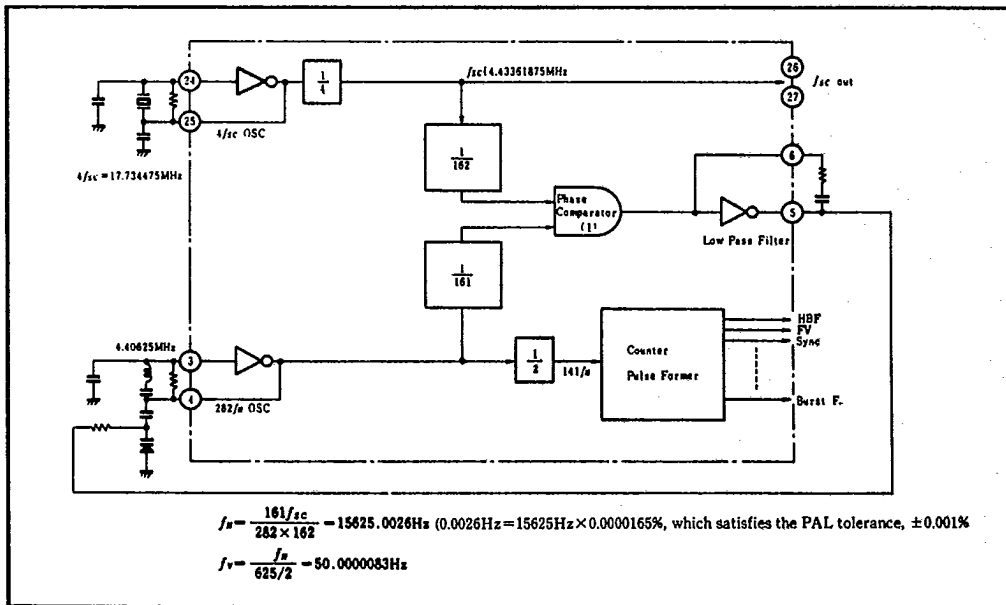


Figure 2 PAL, SECAM



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Genlock

In genlock mode, the operating principles of NTSC and PAL/SECAM are the same, so only NTSC is described below. See figure 3.

Phase comparator 1 is not used. See figure 4.

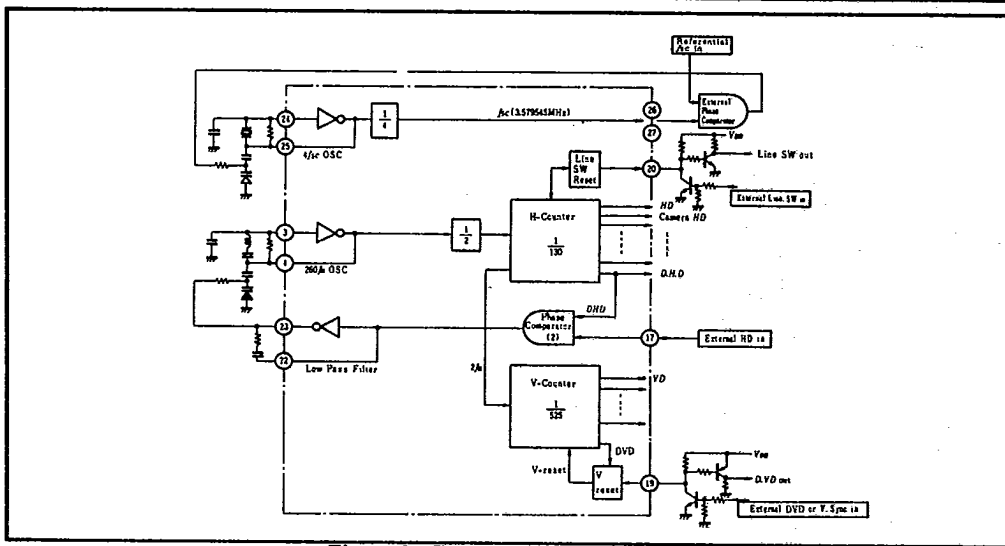
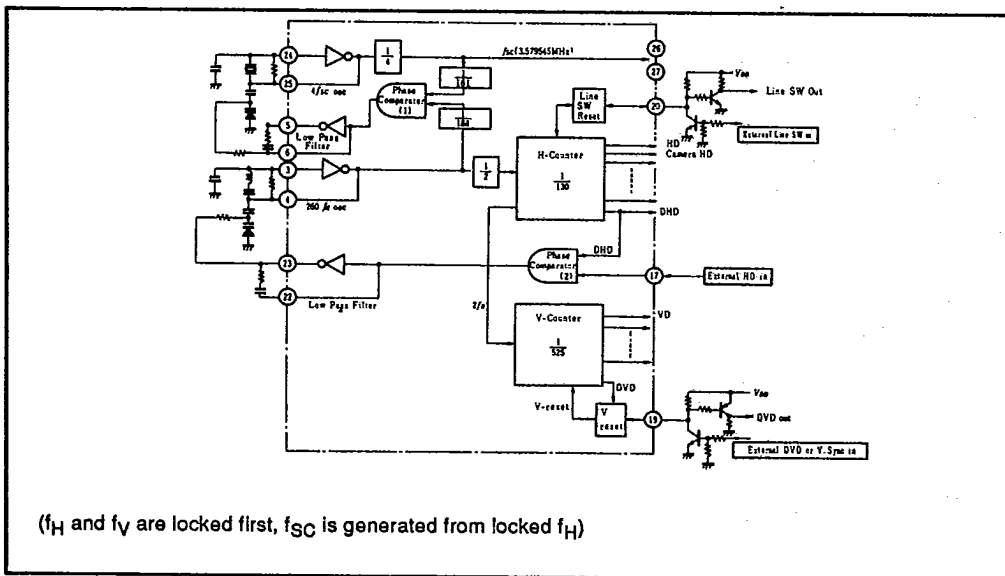


Figure 3 Genlock in Color Cameras



(f_H and f_V are locked first, f_{SC} is generated from locked f_H)

Figure 4 Genlock in B/W Cameras



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Special Input/Output Terminals

Pin 20 is for line SW input and output (figure 5). Figure 6 shows the internal circuit and IC operation. The LC oscillator uses a CMOS inverter and crystal oscillator. There is no internal DC

feedback resistor, so an external resistor for feedback should be connected, as in figure 7.

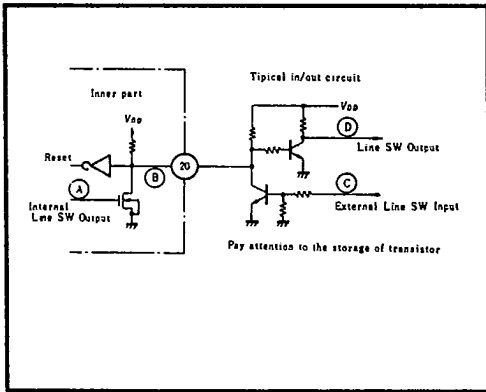


Figure 5 Pin 20 (Line SW In/Out)

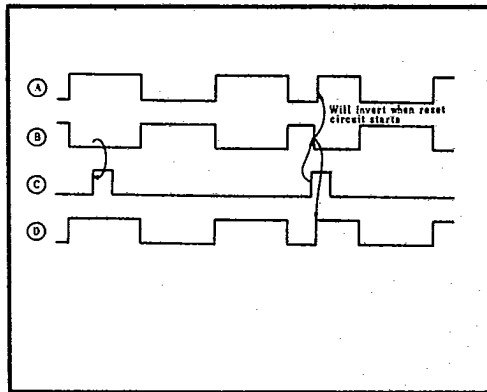


Figure 6 Internal Circuit and IC Operation

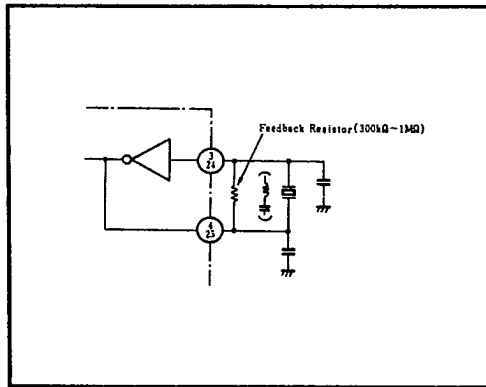


Figure 7 Pins 3, 4 and 24, 25 (260 f_H/282 f_H osc, 4 f_{SC} osc)



Pin 19 is for VD output and V reset input. Figure 8 shows the internal circuit and IC operation. Output impedance is 500 Ω to 2 kΩ when pin 19 output is $V_{DD}/2$.

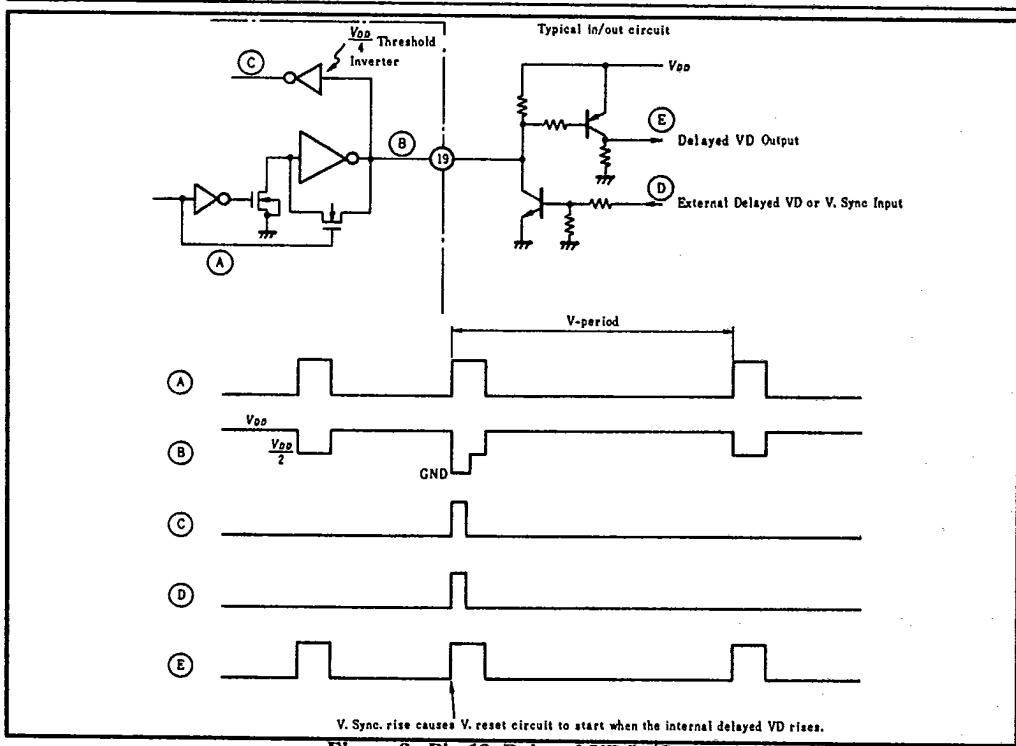


Figure 8 Pin 19, Delayed VD In/Out



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Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V _{DD}	10	V
Input Voltage	V _{IN}	-0.3 to V _{DD} + 0.3	V
Power Dissipation (Ta = 85°C)	P _T	450	mW
Operating Temperature	T _{opr}	-30 to +85	°C
Storage Temperature	T _{stg}	-55 to +125	°C

Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Operating Supply Voltage	V _{DD}	6.3	7.0	7.7	V	
Supply Current	I _{DD}	—	—	40	mA	Output pins open, under oscillation
Input Voltage	V _{IH}	0.8 V _{p-p}	—	V _{DD} + 0.3	V	Pins 16, 17, and 20
	V _{IL}	-0.3	—	0.2 V _{DD}	V	
Input Threshold Voltage	V _{IH}	0.2 V _{DD}	0.25 V _{DD}	0.3 V _{DD}	V	Pin 19
Output Voltage	V _{OH}	0.8 V _{DD}	—	—	V	Pins 11, 26, and 27, I _{OH} = -100 μA
		0.8 V _{DD}	—	—	V	Pins 1, 2, and 7, I _{OH} = -250 μA
		0.8 V _{DD}	—	—	V	Pins 8, 9, 10, 12, 13, 15, 18, 19 and 21, I _{OH} = -500 μA
	V _{OL}	—	—	0.2 V _{DD}	V	Pins 11, 26, and 27, I _{OL} = 100 μA
		—	—	0.2 V _{DD}	V	Pins 1, 2, 7, and 20, I _{OL} = 250 μA
				0.2 V _{DD}	V	Pins 8, 9, 10, 12, 13, 15, 18, and 21, I _{OL} = 500 μA
				0.4 V _{DD}	0.5 V _{DD}	0.6 V _{DD}
Output Impedance	Z _{out}	500	1000	2000	Ω	Low output level at pin 19
Pull-Up Resistance	I _R	-200	-100	-50	μA	High output level at pin 20, pin 20 grounded



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Electrical Characteristics (cont)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Maximum Clock Pulse Frequency	f_C max	20	—	—	MHz	$V_{DD} = 6.3$ V, 20 MHz crystal resonator between pins 24 and 25, output at pins 26 and 27 (20/4 = 5 MHz output)
Maximum Divider Operating Frequency	f_D max	5.0	—	—	MHz	$V_{DD} = 6.3$ V, LC between pins 3 and 4, normal oscillation frequency at output terminal
Pin 26 Output Phase Angle (NTSC)	ϕ_N	88	90	92	deg	Pin 26 output phase referred to 180° (= pin 27 output phase), pin 16: V_{DD} , $V_{DD} = 6.3-7.7$ V
Pin 26 Output Phase Angle (PAL 1)	ϕ_{P1}	88	90	92	deg	Pin 26 output phase referred to 180° (= pin 27 output phase), pin 16: GND, high level line output
Pin 26 Output Phase Angle (PAL 2)	ϕ_{P2}	268	270	272	deg	Pin 26 output phase referred to 180° (= pin 27 output phase), pin 16: GND, low level line output



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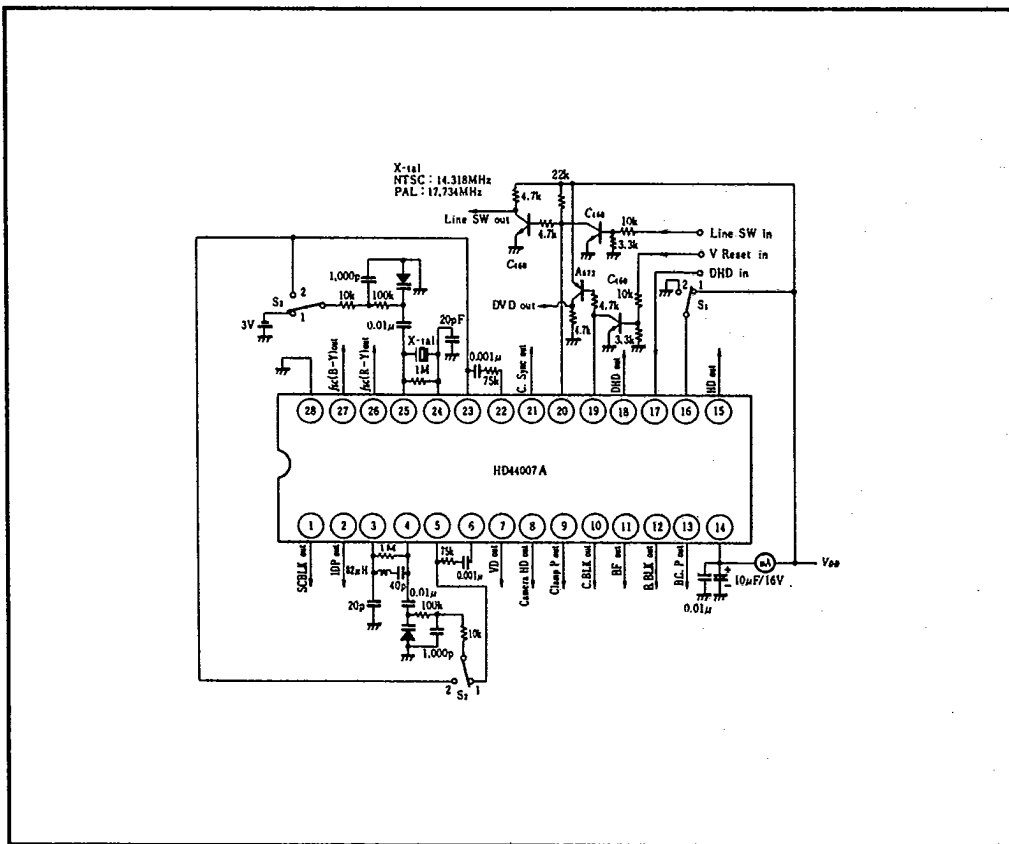


Figure 9 Test Circuit

Table 1 Test Circuit

	S ₂	S ₃
Interleave	1	1
Genlock	2	2

	S ₁	x-tal
NTSC	1	14.318 MHz
PAL/SECAM	2	17.734 MHz



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Timing Charts

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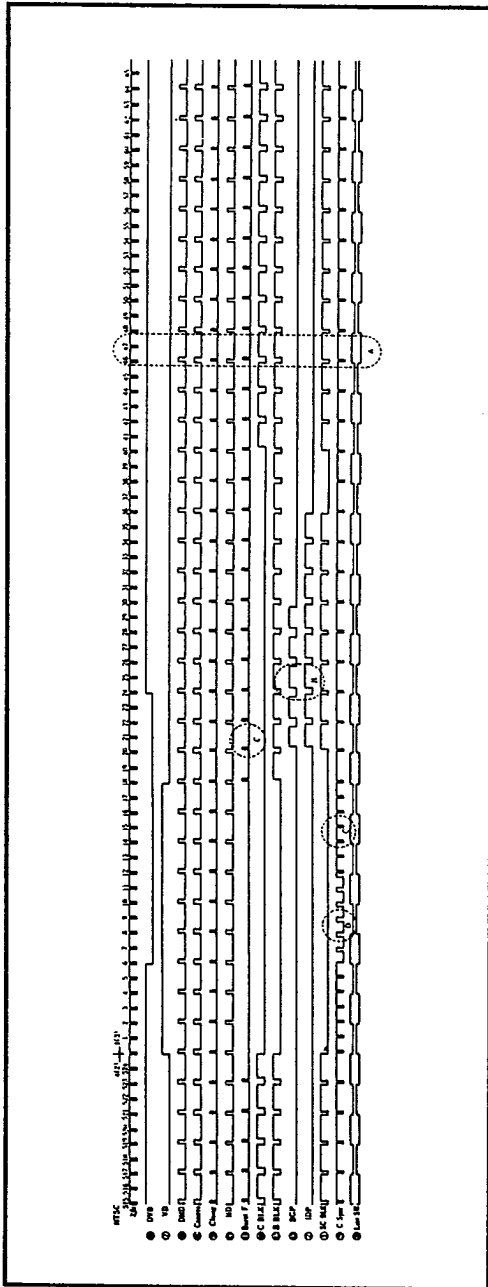


Figure 10 Timing Chart 1

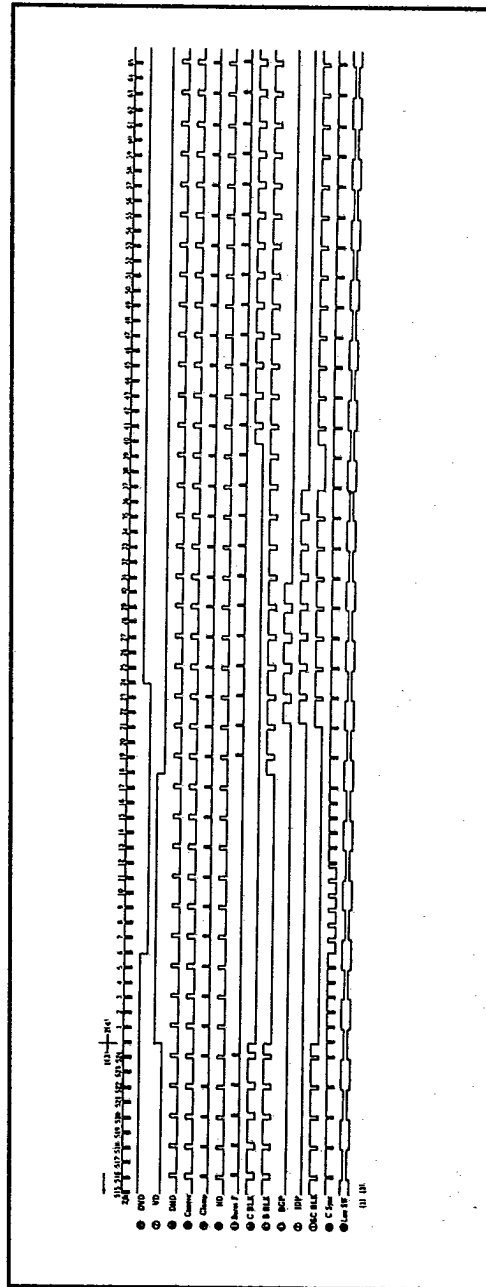


Figure 11 Timing Chart 2



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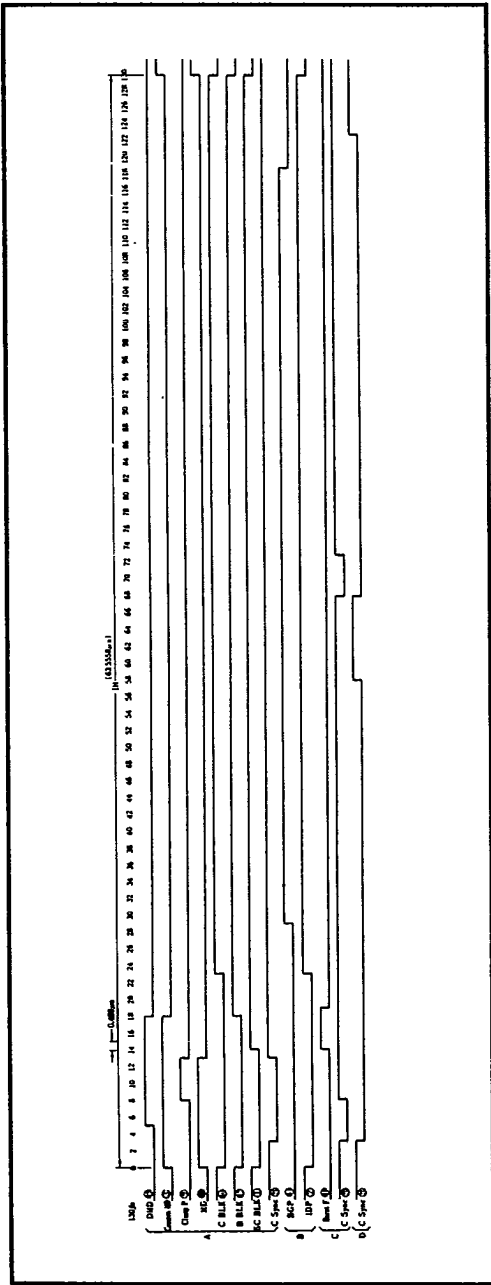


Figure 12 Timing Chart 3

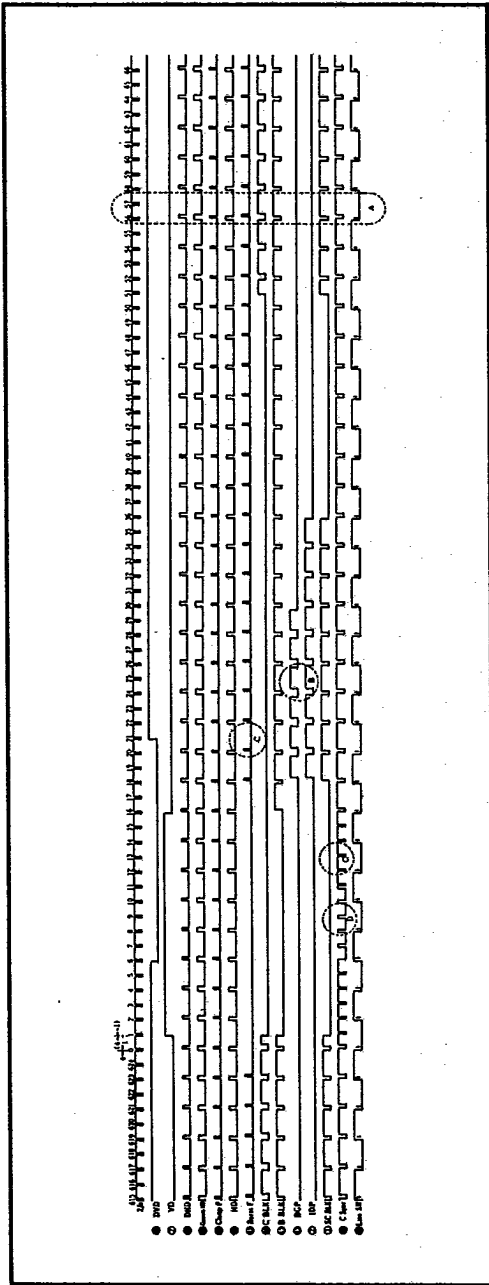


Figure 13 Timing Chart 4



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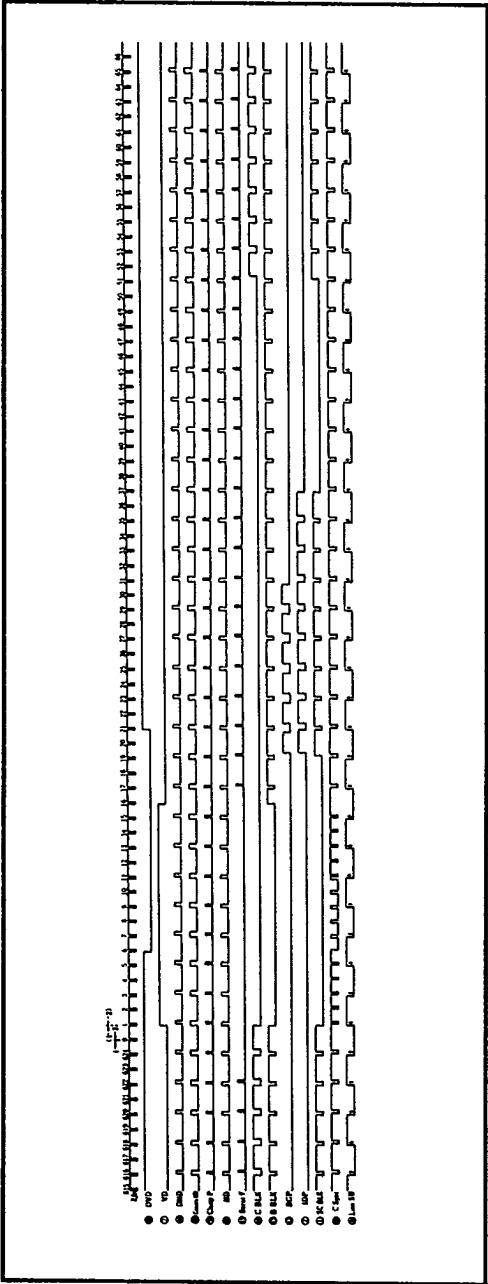


Figure 14 Timing Chart 5

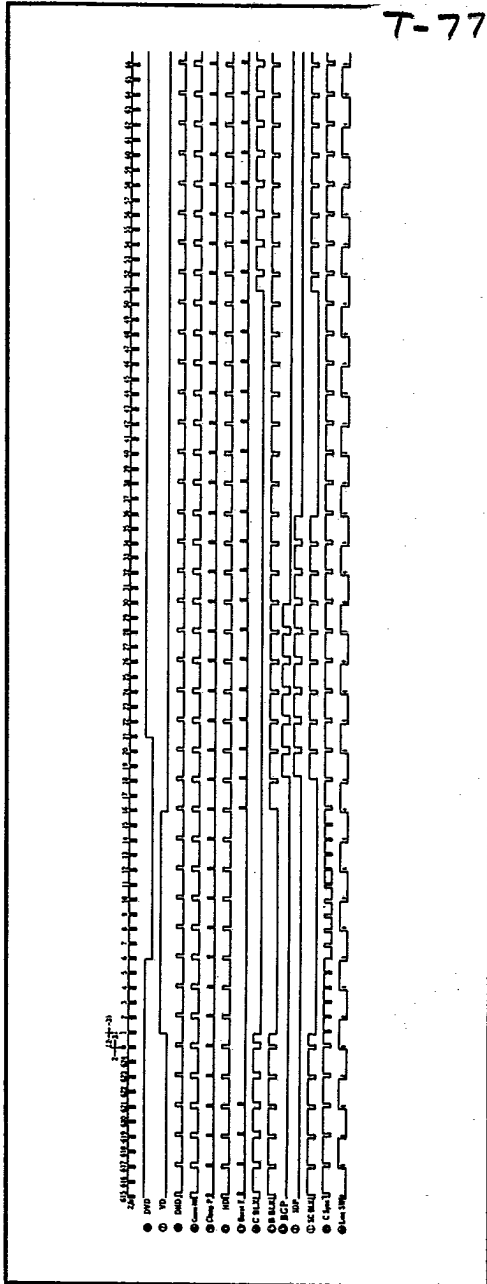


Figure 15 Timing Chart 6



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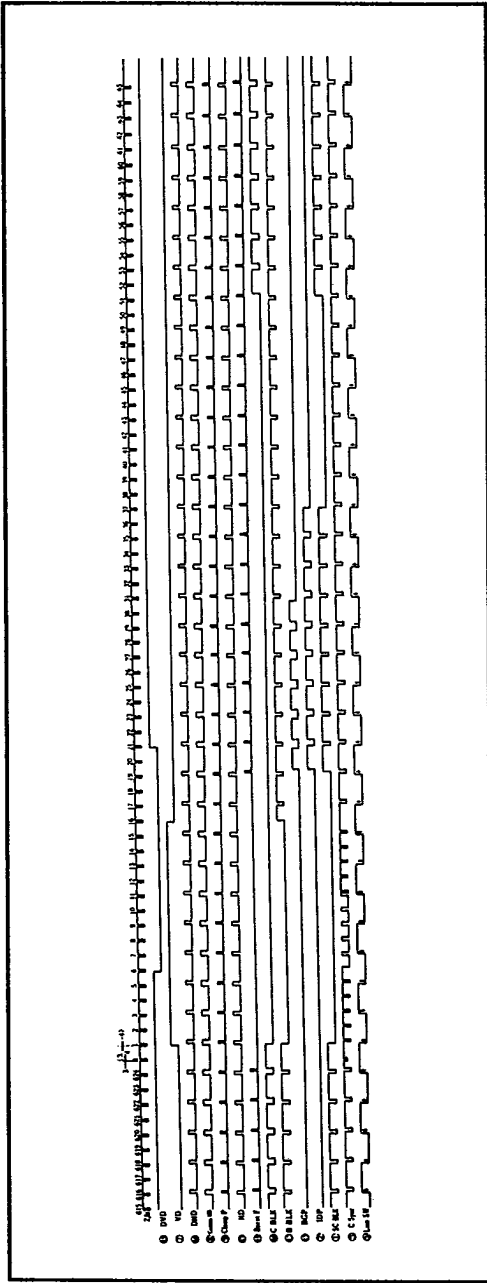


Figure 16 Timing Chart 7

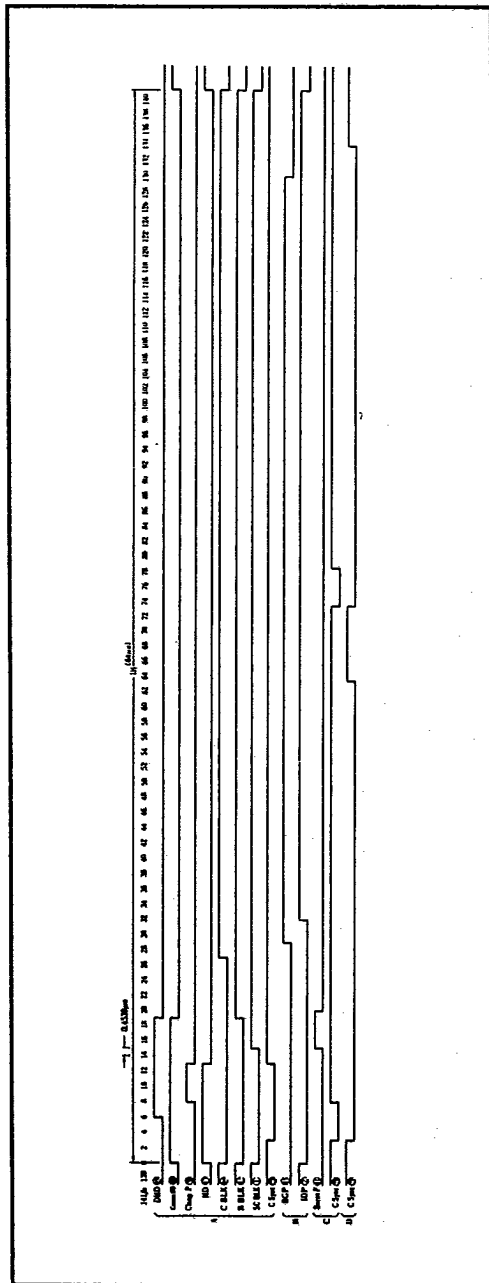


Figure 17 Timing Chart 8



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