HD66781

720-channel Source Driver for a-Si TFT/Low Temperature Poly-Si TFT Panels with 262,144-color display RAM

REJxxxxxxx-xxxxZ
Rev.0.5
July.31.2003

- **Index**

Description

The HD66781 is a 720-channel source driver with graphics acceleration function, incorporating RAM compliant to 262,144 TFT colors and 240RGB x 320 dot graphics. In combination with the HD66783, which incorporates a power-supply integrated circuit and a gate driver on a single chip, the HD66781 can drive an a-Si TFT panel of 240 RGB x 320 dots at maximum. Also in combination with the HD667P21, which is a power-supply IC chip, the HD66781 can drive a low-temperature poly-Si TFT panel of 240 RGB x 320 dots at maximum with an incorporated gate driver.

The HD66781's high-speed RAM-write function through a high-speed interface of 8/9/16/18-bit bus enables efficient data transfer with high-speed burst RAM write function. The HD66781 is compliant to DMA transfer single address mode to keep control on bus traffic occupation when a large volume of data is transferred from external memory. The HD66781 can also handle moving picture display through an RGB interface (VSYNC, HSYNC, DOTCLK, ENABLE, and PD 17 to 0).

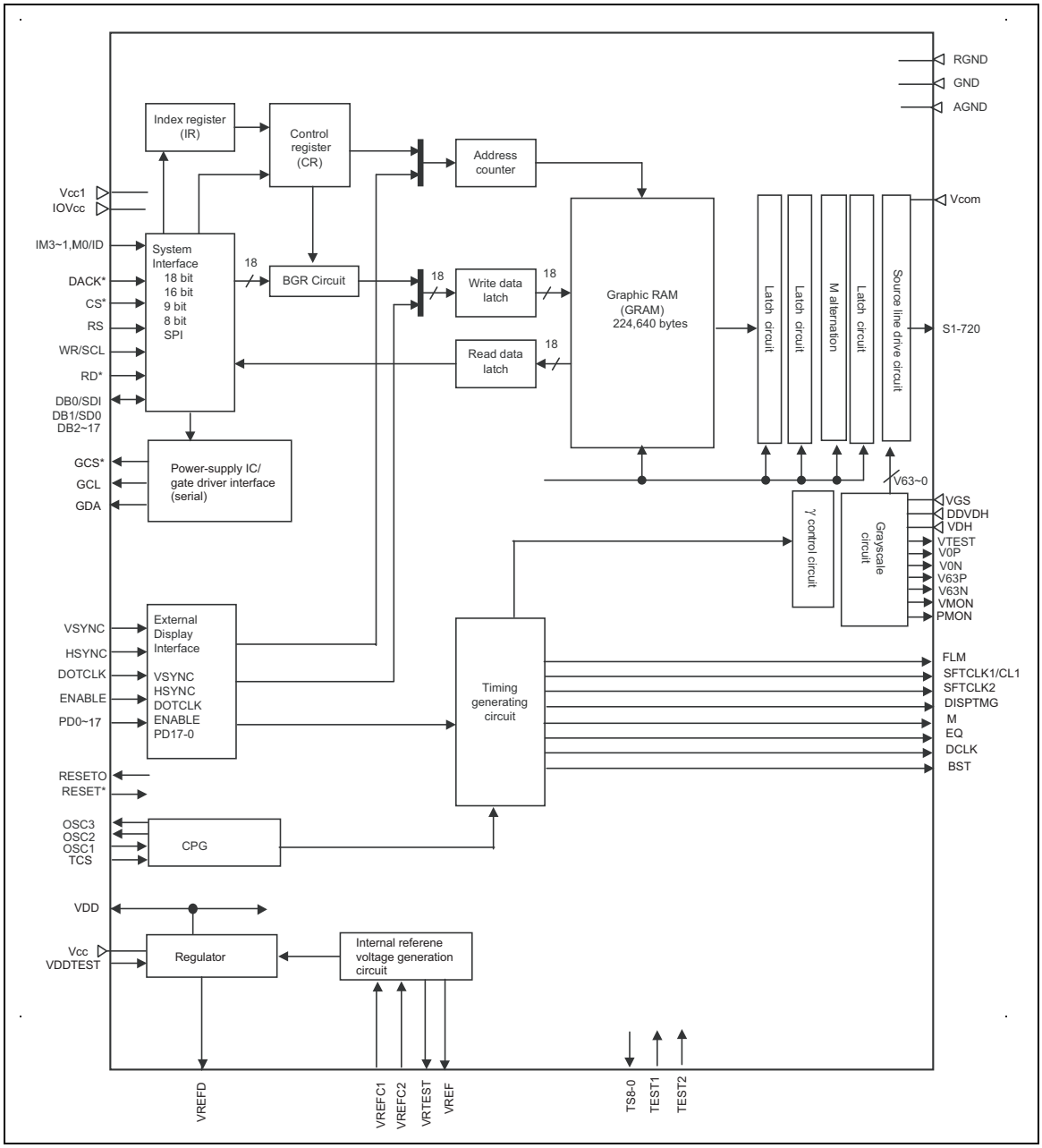
The HD66781 incorporates RAM with the capacity of one QVGA-sized whole screen of 240 RGB x 320 x 18bits plus 96 raster-rows. In addition to OSD and α blending functions, which use this RAM area, the HD66781 also handles resizing function, which is compliant to data transfer for a large screen display. These functions make the HD66781 the best solution for the efficient and various ways of display.

The combined use of HD66781 with HD66783 or HD667P21 supports the function to reduce power consumption by a liquid crystal display system. The HD66781's RAM can display 240 RGB x 320-dot color display (max.) with low voltage operation up to 1.7 V. The HD66781 incorporates a voltage follower circuit to generate liquid crystal driving voltages and an interfacing circuit that enables through HD66781 to make instruction settings to HD66783 and HD667P21. In addition, the HD66781 supports power-saving modes such as standby mode and 8-color display mode, which allow precise power management by software. These features make this LSI the ideal solution for medium or small-sized portable battery-driven products such as digital cellular phones or small PDA with color displays, where long battery life and board size are a major concern.

Features

- Drive 262,144 TFT-color 240RGB x 320 dot graphics display in combination with HD66783 (a-Si TFT panel) or HD667P21 (low-temperature poly-Si TFT panel)
- Output signals to control HD66783, which incorporates a power supply integrated circuit and a gate driver on a single chip.
- Output signals to control a low-temperature poly-Si TFT panel with an incorporated gate driver (combined use with HD667P21)
- System interface
  - High-speed bus interface with 8-/9-/16-/18-bit data bus
  - Serial Peripheral Interface (SPI)
- Interfaces for moving picture display
  - RGB interface with 6-/16-/18-bit data bus (VSYNC, HSYNC, DOTCLK, ENABLE, PD17-0)
  - VSYNC interface (System interface + VSYNC)
- High-speed burst RAM write function
- Compliant to single address mode for DMA transfer that controls data bus occupation ratio when transferring data from external SRAM
- Window address function to write data to a rectangular area of RAM specified by the window address
  - Interfaces for moving picture display, which write data to a rectangular RAM address area
  - Reduce data transfer by transferring only the data for the moving picture display area
  - Simultaneous display of moving picture area and still picture area that displays the contents of internal RAM
  - Resizing function (contraction rate: x1/2, x1/4 / magnification rate: x2, x4)
- Various functions to control color display
  - Simultaneous availability of 262,144 colors (settings are programmable)
  - Partial OSD function
  - α-blending function (transmission rate: 0%, 25%, 50%, 75%, 100%)
- Features for low-power architecture
  - Interface I/O power supply IOVcc = 1.7 ~ 3.3 V
    Vcc1 = 1.7 ~ 3.3 V
  - Logic regulator power supply Vcc = 2.5 ~ 3.3 V
  - Source driver liquid crystal driving voltage DDVDH-GND = 4.0 ~ 5.9 V
  - Power saving functions: standby mode, deep standby mode etc.
  - Step-up circuits to generate liquid crystal drive voltage up to 12 times (HD66783 and HD667P21)
  - Voltage followers for a liquid crystal drive power-supply, which fends off the direct current from bleeder-resistors
- Cst structure only (Common Vcom formula)
- 224,640-byte (240 x (320+96) x 18bits) internal RAM
- Incorporated LCD driver with 720 source outputs
- Compliant to COG

Block Diagram



Pin Functions

<table>
<tr><th>Signals</th><th>Number of Pins</th><th>I/O</th><th>Connected to</th><th>Functions</th><th>Unused pins</th></tr>
<tr><td>IM3~1, IM0/ID</td><td>4</td><td>I</td><td>GND or Vcc1</td><td>Pins to select an interfacing mode with MPU.
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>MPU-Interface Mode</th><th>DB Pins</th><th>Colors</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>80-system 16-bit interface</td><td>DB17-10, DB8-1</td><td>65,536 Note 1)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>80-system 8-bit interface (Big-endian)</td><td>DB17-10</td><td>65,536 Note 2)</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>*</td><td>Serial peripheral interface (SPI)</td><td>DB1-0</td><td>65,536</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>80-system 8-bit interface (Little-endian)</td><td>DB17-10</td><td>65,536 Note 2)</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>80-system 18-bit interface</td><td>DB17-10</td><td>262,144</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>80-system 9-bit interface</td><td>DB17-9</td><td>262,144</td></tr>
<tr><td>1</td><td>1</td><td>*</td><td>*</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
</table>
Note 1) 262,144 colors available (max.) in 2-transfer mode.
Note 2) 262,144 colors available (max.) in 3-transfer mode.</td><td>-</td></tr>
<tr><td>CS*</td><td>1</td><td>I</td><td>MPU</td><td>Select the HD66781.
Low: the HD66781 is selected and is accessible
High: the HD66781 is not selected and is inaccessible</td><td>IOVcc</td></tr>
<tr><td>RS</td><td>1</td><td>I</td><td>MPU</td><td>Select the register.
Low: Index/status registers
High: Control registers</td><td>IOVcc</td></tr>
<tr><td>WR*/SCL</td><td>1</td><td>I</td><td>MPU</td><td>Write strobe signal in the 80-system bus interface
Write data at the “Low” level.
In the Serial Peripheral Interface, a synchronizing clock signal.</td><td>-</td></tr>
<tr><td>RD*</td><td>1</td><td>I</td><td>MPU</td><td>Read-strobe signal in the 80-system bus interface
Read data at the “Low” level.</td><td>IOVcc</td></tr>
<tr><td>DACK*</td><td>1</td><td>I</td><td>MPU</td><td>Select the HD66781 in the DMA transfer single address mode.
Low: Select the HD66781 (Accessible)
High: Not Select the HD66781 (Inaccessible)</td><td>Vcc1</td></tr>
<tr><td>DB0/SDI</td><td>1</td><td>I/O</td><td>MPU</td><td>18-bit parallel bi-directional data bus.
8-bit bus: DB17-DB10
9-bit bus: DB17-DB9
16-bit bus: DB17-DB10 and DB8-DB1
18-bit bus: DB17-DB0
Serial data input pin (SDI) in the Serial Peripheral Interface mode to input data on the rising edge of SCL signal.</td><td>IOVcc</td></tr>
</table>

Signals	Number of Pins	I/O	Connected to	Functions	Unused pins
DB1/SDO	1	I/O	MPU	18-bit parallel bi-directional data bus. 8-bit bus: DB17-DB10 9-bit bus: DB17-DB9 16-bit bus: DB17-DB10 and DB8-DB1 18-bit bus: DB17-DB0 Serial data output pin (SDO) in the Serial Peripheral Interface mode to output data on the falling edge of SCL signal.	IOVcc
DB2~DB17	16	I/O	MPU	18-bit parallel bi-directional data bus. 8-bit bus: DB17-DB10 9-bit bus: DB17-DB9 16-bit bus: DB17-DB10 and DB8-DB1 18-bit bus: DB17-DB0	IOVcc
RESET*	1	I	MPU or external R-C circuit	Reset pin. Initialize the LSI at the “Low” level. A power-on reset required after turning on the power.	-
RESETO1 RESETO2	2	O	HD66783 or HD667P21	Output the same polarity level as RESET*. Control both HD66781 and HD66783 or HD66781 and HD667P21 by connecting to HD66783 or HD667P21.	Open
OSC1 OSC2	2	I or O	Oscillation resistor	Connect an external resistor for R-C oscillation.	-
ENABLE	1	I	MPU or LCDC	Data enable signal in the RGB interface mode. Low: Select (accessible) High: Not select (inaccessible) ENABLE signal inverts the polarity according to the setting of EPL resister. Set ENABLE inactive while it is not used and its level is fixed or the polarity is set with registers.	GND/ IOVcc
VSYNC	1	I	MPU or LCDC	Frame synchronizing signal. This signal is active low. The polarity of VSYNC is inverted by setting VSPL register. Set VSYNC inactive while it is not used and its level is fixed or the polarity is set with registers.	GND/ IOVcc
HSYNC	1	I	MPU or LCDC	Line synchronizing signal. This signal is active low. The polarity of HSYNC is inverted by setting HSPL register. Set HSYNC inactive while it is not used and its level is fixed or the polarity is set with registers.	GND/ IOVcc
DOTCLK	1	I	MPU or LCDC	Dot clock signal. The timing of data input is determined at the rising edge. This signal is active low. The polarity of DOTCLK is inverted by setting DPL register. Set DOTCLK inactive while it is not used and its level is fixed or the polarity is set with registers.	GND/ IOVcc
PD0~PD17	18	I	MPU or LCDC	18-bit bus for RGB data. 6-bit bus: PD17-PD12 16-bit bus: PD17-PD13 and PD11-PD1 18-bit bus: PD17-PD0	GND/ IOVcc

Signals	Number of Pins	I/O	Connected to	Functions	Unused pins
BST	1	O	MPU or LCDC	Output a pulse that indicates the start of blank (front porch). When writing data in synchronization with display scan, serve as a trigger signal. Amplitude: Vcc1 and GND.	Open
S1~S720	720	O	Liquid Crystal	Output a voltage applied to liquid crystal. The correspondence between the RAM write address and source output signal is changeable with SS bit. When SS=0, data in the RAM address “h00000” are output from S1-3. When SS=1, data in the RAM address “h00000” are output from S718-720. S1, S4, S7, ... display red (R), S2, S5, S8, ... display green (G), and S3, S6, S9, ... display blue (B) (SS = 0).	Open
FLM1 FLM2	2	O	HD66783 or HD667P21	Output a frame head pulse.	Open
CL11/ SFTCLK11 CL12/ SFTCLK12	2	O	HD66783 or HD667P21	Output a different signal according to the LTPS register setting. LTPS=0: Output a pulse of one line cycle. Connect to CL1 pin of HD66783. LTPS=1: Gate shift clock for LTPS. Output a pulse of 2-line cycles.	Open
SFTCLK21 SFTCLK22	2	O	HD667P21	Output a different signal according to the LTPS register setting. LTPS=0: Output is GND. No connection with HD66783 is required. LTPS=1: Gate shift clock for LTPS. Output a pulse of 2-line cycles.	Open
DISPTMG1 DISPTMG2	2	O	HD66783 or HD667P21	Gate off signal during partial display. Low: Voff output High: Normal output For an LTPS LCD panel, a control signal for the gate driver incorporated therein.	Open
M1 M2	2	O	HD66783 or HD667P21	Output alternating pulse.	Open
EQ1 EQ2	2	O	HD66783 or HD667P21	Make Vcom output Hi-z in Vcom transition timing during Vcom alternating drive. Low: Output VcomH or VcomL from Vcom High: Make Vcom output Hi-z	Open
DCCLK1 DCCLK2	2	O	HD66783 or HD667P21	Output step-up clocks.	Open
GCL1 GCL2	2	O	HD66783 or HD667P21	Clock signal for making a serial transfer of values set in registers to gate driver/power supply IC. Output data from the falling edge of the clock.	Open
GDA1 GDA2	2	O	HD66783 or HD667P21	Data signal for making a serial transfer of values set in registers to gate driver/power supply IC.	Open
GCS1* GCS2*	2	O	HD66783 or HD667P21	Select the HD66781. Low: Select the HD66781 (Serial transfer) High: Not select the HD66781 (Serial transfer not available)	Open

Signals	Number of Pins	I/O	Connected to	Functions	Unused pins
GND	1	-	Power supply	Ground for the logic side. GND = 0V When assembled on COG, connect to GND on the FPC to avoid effects from the noise.	-
AGND	1	-	Power supply	Ground for the I/O side and analogue circuits other than logic circuits and the internal GRAM, which operate with VDD voltage. AGND = 0V When assembled on COG, connect to GND on the FPC to avoid effects from the noise.	-
RGND	1	-	Power supply	Ground for the internal RAM. RGND = 0V. When assembled on COG, connect to GND on the FPC to avoid effects from the noise.	-
IOVcc	1	-	Power supply	Supply with the power supply voltage for interface pins. IOVcc = 1.7~3.3V. IOVcc ≤ Vcc1 ≤ Vcc	-
Vcc	1	I	Power supply	Power supply for internal logic regulator. Connect to an external power supply of Vcc = 2.5~3.3V. IOVcc ≤ Vcc1 ≤ Vcc	-
Vcc1	1	I	Power supply	Power supply voltage for a deep standby control circuit and the I/O side. IOVcc ≤ Vcc1 ≤ Vcc	-
VREF	1	O	Power supply	Reference voltage output for internal logic regulator. Leave open.	Open
VDD	1	I/O	Stabilizing Capacitor	Power supply output for an internal logic. Do not connect to other than stabilizing capacitors.	-
DDVDH	1	I	HD66783 or HD667P21	Supply with a liquid crystal drive voltage through HD66783 or HD667P21. DDVDH = +4.0V~+5.9V	-
VDH	1	I	HD66783 or HD667P21	A reference level for a grayscale voltage generation circuit. Can be supplied through HD66783 or HD667P21.	-
VGS	1	I	GND or External Resistor	A reference level for a grayscale voltage generation circuit. Connect to an external variable resistor to make a level adjustment for each panel.	-
Vcom	1	I	HD66783 or HD667P21	Signal for equalization. Short-circuit all liquid crystal output (S1~S720) to Vcom level (Hi-z) while EQ = High. Leave open when Vcom < 0V.	Open
TEST1 TEST2	2	I	GND	Test pins. Must be fixed to the GND level.	-
TSC	1	I	GND	Test pin. Must be fixed to the GND level.	-
OSC3	1	O	Open	Test pin. Leave open.	Open
TS8-0	9	O	Open	Test pins. Leave open.	Open
VTEST	1	O	Open	Test pin. Leave open.	Open
VRTEST	1	O	Open	Test pin. Leave open.	Open
VREFC1 VREFC2	2	I	GND	Test pins. Must be fixed to GND level.	-

Signals	Number of Pins	I/O	Connected to	Functions	Unused pins
VDDTEST	1	I	GND	Test pin. Must be fixed to GND level.	-
VREFD	1	O	Open	Test pin. Leave open.	Open
PMON	1	O	Open	Test pin. Leave open.	Open
VMON	1	O	Open	Test pin. Leave open.	Open
V0P V63P	2	I or O	Open	Test pins. Leave open.	-
V0N V63N	2	I or O	Open	Test pins. Leave open.	-
TIN1	1	I	GND	Test pin. Must be fixed to GND level.	-
TOUT1-3	3	O	Open	Test pins. Leave open.	Open
TVcc1 TVcc2	2	I	GND	Test pins. Must be fixed to GND level.	-
DUMMY14 DUMMY15	2	-	-	Dummy pads. DUMMY 14 and DUMMY 15 are short-circuited within the LSI. Available for measuring COG contact resistor.	Open
DUMMY 1~13, 16~30	28	-	Open	Dummy pads. Must be left open.	Open
IOVccDUM 1~3	3	O	Input pins	Output an internal IOVcc level. When neighboring input pins are fixed to IOVcc, short-circuit them.	Open
Vcc1DUM1 Vcc1DUM2	2	O	Input pins	Output an internal Vcc1 level. When neighboring input pins are fixed to Vcc1, short-circuit them.	Open
AGNDDUM 1-4	4	O	Input pins	Output an internal AGND level. When neighboring input pins are fixed to AGND, short-circuit them.	Open
TESTO1 TESTO2	2	O	Open	Test pins. Leave open.	-

HD66781 power-supply specification

Item			Voltage range	Specification
Input Voltage	IOVcc	Interface voltage 1	+1.7V~+3.3V	Power supply for signals interfacing with MPU or LCDC. Supply through the system. Power supply for CS*, RS, WR*/SCL, RD*, DB17-2, DB1/SDO, DB0/SDI, VSYNC, HSYNC, ENABLE, PD17-0. Connect on the FPC when using at the same electric potential with Vcc1.
	Vcc1	Interface voltage 2	+1.7V~+3.3V	Power supply for signals interfacing with a gate driver/power supply IC and a deep standby mode control circuit that halts the logic regulator. Supply with the same electric potential with Vcc of HD66783 or HD667P21 though the system. Power supply for FLM1, FLM2, CL11/SFTCLK11, CL12/SFTCLK12, SFTCLK21, SFTCLK22, M1, M2, EQ1, EQ2, DCCLK1, DCCLK2, GCL1, GCL2, GDA1, GDA2, GCS1*, GCS2*, RESET*, RESETO1, RESETO2, DACK*, BST, M3-1, IM0/ID. Connect on the FPC when using at the same potential with IOVcc.
	Vcc	Power supply for the logic regulator	+2.5V~+3.3V	Supply through the system. Connect on the FPC when using at the same electric potential with Vci of HD66783 or HD667P21.
	VDD	Power supply for the Internal logic	-	Generated from the internal logic regulator. Supply through the system is not required.
	GND	-	0V	GND for the internal logic circuit. Connect to GND on the FPC.
	RGND	-	0V	GND for the internal GRAM. Connect to GND on the FPC.
	AGND	-	0V	GND for the I/O side and analogue circuits other than logic circuits and the internal GRAM, which operate with VDD voltage. Connect to GND on the FPC.
LCD drive voltage	DDVDH	-	+4.5V~+5.9V	Connect to DDVDH of HD66783 or HD667P21.
Source driver grayscale reference voltage	VDH	-	+3.0V~ (DDVDH-0.5)V	Connect to VREG1OUT of HD66783 or HD667P21.
	VGS	-	-	Connect to GND or variable resistor.
LCD drive output	S1~ S720	V0~V63 grayscale level	-	-

HD667B81 PAD Arrangement

●Chip Size : 16.94mm × 2.99mm
●Chip Thickness : 400μm(typ.)
●PAD Coordinate : PAD center

●Coordinate Origin : Chip Center

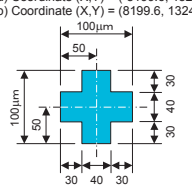
●Au Bump Size :
(1) 54μm × 106μm
NO.1~NO.200

(2)26μm × 90μm
NO.201~NO.281,NO.853~NO.933

(3)90μm × 26μm
NO.282~NO.852

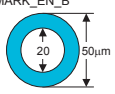
●Au Bump pitch : See PAD coordinate
●Au Bump height : 15μm(typ.)
●"No.X" in the Figure corresponds to the □ PAD No. in the PAD Coordinate Table.

●Alignment Mark
(1) Arranged Coordinate : 2 places
Cell Name : MARK_COGTGT
(1-a) Coordinate (X,Y) = (-8199.6, 1324.3)
(1-b) Coordinate (X,Y) = (8199.6, 1324.3)

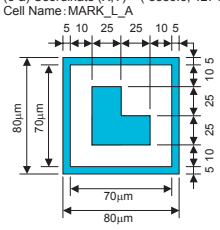


(2) Arrangement Coordinate
(2-a) Coordinate (X,Y) = (-8339.6, 1364.6)
Cell Name : MARK_EN_A

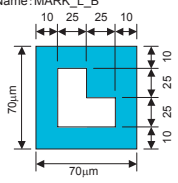
(2-b) Coordinate (X,Y) = (8339.6, 1364.6)
Cell Name : MARK_EN_B



(3) Arrangement Coordinate
(3-a) Coordinate (X,Y) = (-8339.6, 1274.3)
Cell Name : MARK_L_A

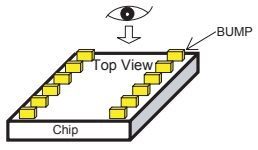


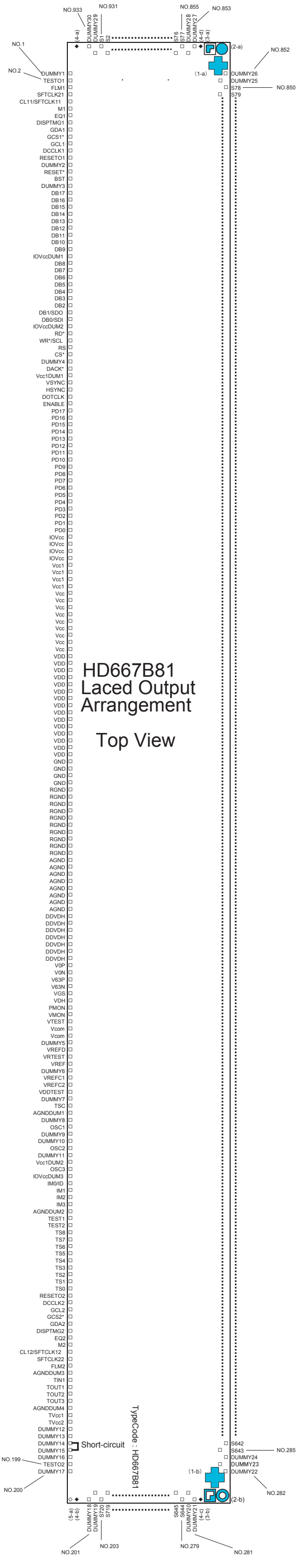
(3-b) Coordinate (X,Y) = (8339.6, 1274.3)
Cell Name : MARK_L_B



●Long cell : ◆
(4) Arrangement Coordinate : 4 places
Cell Name : ZBASFLONGSCALELCD
(4-a) Coordinate (X,Y) = (-8339.6, -1197.9)
(4-b) Coordinate (X,Y) = (8339.6, -1197.9)
(4-c) Coordinate (X,Y) = (8339.6, 1197.9)
(4-c) Coordinate (X,Y) = (-8339.6, 1197.9)

●Short cell : ◇
(5) Arrangement Coordinate : 1 place
(5-a) Coordinate (X,Y) = (8339.6, -1276.1)
Cell Name : ZBSHORTSCALE_L0106





HD667B81
Laced Output
Arrangement

Top View

Pad Coordinate

Unit : μm

pad No.	pad name	X	Y
1	DUMMY1	-7960.0	-1356.3
2	TESTO1	-7880.0	-1356.3
3	FLM1	-7800.0	-1356.3
4	SFTCLK21	-7720.0	-1356.3
5	CL11/SFTCLK11	-7640.0	-1356.3
6	M1	-7560.0	-1356.3
7	EQ1	-7480.0	-1356.3
8	DISPTMG1	-7400.0	-1356.3
9	GDA1	-7320.0	-1356.3
10	GCS1*	-7240.0	-1356.3
11	GCL1	-7160.0	-1356.3
12	DCCLK1	-7080.0	-1356.3
13	RESETO1	-7000.0	-1356.3
14	DUMMY2	-6920.0	-1356.3
15	RESET*	-6840.0	-1356.3
16	BST	-6760.0	-1356.3
17	DUMMY3	-6680.0	-1356.3
18	DB17	-6600.0	-1356.3
19	DB16	-6520.0	-1356.3
20	DB15	-6440.0	-1356.3
21	DB14	-6360.0	-1356.3
22	DB13	-6280.0	-1356.3
23	DB12	-6200.0	-1356.3
24	DB11	-6120.0	-1356.3
25	DB10	-6040.0	-1356.3
26	DB9	-5960.0	-1356.3
27	IOVccDUM1	-5880.0	-1356.3
28	DB8	-5800.0	-1356.3
29	DB7	-5720.0	-1356.3
30	DB6	-5640.0	-1356.3
31	DB5	-5560.0	-1356.3
32	DB4	-5480.0	-1356.3
33	DB3	-5400.0	-1356.3
34	DB2	-5320.0	-1356.3
35	DB1/SDO	-5240.0	-1356.3
36	DB0/SDI	-5160.0	-1356.3
37	IOVccDUM2	-5080.0	-1356.3
38	RD*	-5000.0	-1356.3
39	WR*/SCL	-4920.0	-1356.3
40	RS	-4840.0	-1356.3
41	CS*	-4760.0	-1356.3
42	DUMMY4	-4680.0	-1356.3
43	DACK*	-4600.0	-1356.3
44	Vcc1DUM1	-4520.0	-1356.3
45	VSYNC	-4440.0	-1356.3
46	HSYNC	-4360.0	-1356.3
47	DOTCLK	-4280.0	-1356.3
48	ENABLE	-4200.0	-1356.3
49	PD17	-4120.0	-1356.3
50	PD16	-4040.0	-1356.3
51	PD15	-3960.0	-1356.3
52	PD14	-3880.0	-1356.3
53	PD13	-3800.0	-1356.3
54	PD12	-3720.0	-1356.3
55	PD11	-3640.0	-1356.3
56	PD10	-3560.0	-1356.3
57	PD9	-3480.0	-1356.3
58	PD8	-3400.0	-1356.3
59	PD7	-3320.0	-1356.3
60	PD6	-3240.0	-1356.3
61	PD5	-3160.0	-1356.3
62	PD4	-3080.0	-1356.3
63	PD3	-3000.0	-1356.3
64	PD2	-2920.0	-1356.3
65	PD1	-2840.0	-1356.3
66	PD0	-2760.0	-1356.3
67	IOVcc	-2680.0	-1356.3
68	IOVcc	-2600.0	-1356.3
69	IOVcc	-2520.0	-1356.3
70	IOVcc	-2440.0	-1356.3
71	Vcc1	-2360.0	-1356.3
72	Vcc1	-2280.0	-1356.3
73	Vcc1	-2200.0	-1356.3
74	Vcc1	-2120.0	-1356.3
75	Vcc	-2040.0	-1356.3
76	Vcc	-1960.0	-1356.3
77	Vcc	-1880.0	-1356.3
78	Vcc	-1800.0	-1356.3
79	Vcc	-1720.0	-1356.3
80	Vcc	-1640.0	-1356.3
81	Vcc	-1560.0	-1356.3
82	Vcc	-1480.0	-1356.3
83	Vcc	-1400.0	-1356.3
84	VDD	-1320.0	-1356.3
85	VDD	-1240.0	-1356.3
86	VDD	-1160.0	-1356.3
87	VDD	-1080.0	-1356.3
88	VDD	-1000.0	-1356.3
89	VDD	-920.0	-1356.3
90	VDD	-840.0	-1356.3
91	VDD	-760.0	-1356.3
92	VDD	-680.0	-1356.3
93	VDD	-600.0	-1356.3
94	VDD	-520.0	-1356.3
95	VDD	-440.0	-1356.3
96	VDD	-360.0	-1356.3
97	VDD	-280.0	-1356.3
98	VDD	-200.0	-1356.3
99	GND	-120.0	-1356.3
100	GND	-40.0	-1356.3
101	GND	40.0	-1356.3
102	GND	120.0	-1356.3
103	RGND	200.0	-1356.3
104	RGND	280.0	-1356.3
105	RGND	360.0	-1356.3
106	RGND	440.0	-1356.3
107	RGND	520.0	-1356.3
108	RGND	600.0	-1356.3
109	RGND	680.0	-1356.3
110	RGND	760.0	-1356.3
111	RGND	840.0	-1356.3
112	RGND	920.0	-1356.3
113	AGND	1000.0	-1356.3
114	AGND	1080.0	-1356.3
115	AGND	1160.0	-1356.3
116	AGND	1240.0	-1356.3
117	AGND	1320.0	-1356.3
118	AGND	1400.0	-1356.3
119	AGND	1480.0	-1356.3
120	AGND	1560.0	-1356.3

pad No.	pad name	X	Y
121	DDVDH	1640.0	-1356.3
122	DDVDH	1720.0	-1356.3
123	DDVDH	1800.0	-1356.3
124	DDVDH	1880.0	-1356.3
125	DDVDH	1960.0	-1356.3
126	DDVDH	2040.0	-1356.3
127	DDVDH	2120.0	-1356.3
128	VIP	2200.0	-1356.3
129	V0N	2280.0	-1356.3
130	V63P	2360.0	-1356.3
131	V63N	2440.0	-1356.3
132	VGS	2520.0	-1356.3
133	VDH	2600.0	-1356.3
134	PMON	2680.0	-1356.3
135	VMON	2760.0	-1356.3
136	VTEST	2840.0	-1356.3
137	Vcom	2920.0	-1356.3
138	Vcom	3000.0	-1356.3
139	DUMMY5	3080.0	-1356.3
140	VREFD	3160.0	-1356.3
141	VRTEST	3240.0	-1356.3
142	VREF	3320.0	-1356.3
143	DUMMY6	3400.0	-1356.3
144	VREFC1	3480.0	-1356.3
145	VREFC2	3560.0	-1356.3
146	VDDTEST	3640.0	-1356.3
147	DUMMY7	3720.0	-1356.3
148	TSC	3800.0	-1356.3
149	AGNDDUM1	3880.0	-1356.3
150	DUMMY8	3960.0	-1356.3
151	OSC1	4040.0	-1356.3
152	DUMMY9	4120.0	-1356.3
153	DUMMY10	4200.0	-1356.3
154	OSC2	4280.0	-1356.3
155	DUMMY11	4360.0	-1356.3
156	Vcc1DUM2	4440.0	-1356.3
157	OSC3	4520.0	-1356.3
158	IOVccDUM3	4600.0	-1356.3
159	IM0/ID	4680.0	-1356.3
160	IM1	4760.0	-1356.3
161	IM2	4840.0	-1356.3
162	IM3	4920.0	-1356.3
163	AGNDDUM2	5000.0	-1356.3
164	TEST1	5080.0	-1356.3
165	TEST2	5160.0	-1356.3
166	TS8	5240.0	-1356.3
167	TS7	5320.0	-1356.3
168	TS6	5400.0	-1356.3
169	TS5	5480.0	-1356.3
170	TS4	5560.0	-1356.3
171	TS3	5640.0	-1356.3
172	TS2	5720.0	-1356.3
173	TS1	5800.0	-1356.3
174	TS0	5880.0	-1356.3
175	RESETO2	5960.0	-1356.3
176	DCCLK2	6040.0	-1356.3
177	GCL2	6120.0	-1356.3
178	GCS2*	6200.0	-1356.3
179	GDA2	6280.0	-1356.3
180	DISPTMG2	6360.0	-1356.3
181	EQ2	6440.0	-1356.3
182	M2	6520.0	-1356.3
183	CL12/SFTCLK12	6600.0	-1356.3
184	SFTCLK22	6680.0	-1356.3
185	FLM2	6760.0	-1356.3
186	AGNDDUM3	6840.0	-1356.3
187	TIN1	6920.0	-1356.3
188	TOUT1	7000.0	-1356.3
189	TOUT2	7080.0	-1356.3
190	TOUT3	7160.0	-1356.3
191	AGNDDUM4	7240.0	-1356.3
192	TVcc1	7320.0	-1356.3
193	TVcc2	7400.0	-1356.3
194	DUMMY12	7480.0	-1356.3
195	DUMMY13	7560.0	-1356.3
196	DUMMY14	7640.0	-1356.3
197	DUMMY15	7720.0	-1356.3
198	DUMMY16	7800.0	-1356.3
199	TESTO2	7880.0	-1356.3
200	DUMMY17	7960.0	-1356.3
201	DUMMY18	8339.6	-1132.4
202	DUMMY19	8204.6	-1104.4
203	S720	8339.6	-1076.4
204	S719	8204.6	-1048.4
205	S718	8339.6	-1020.4
206	S717	8204.6	-992.4
207	S716	8339.6	-964.4
208	S715	8204.6	-936.4
209	S714	8339.6	-908.4
210	S713	8204.6	-880.4
211	S712	8339.6	-852.4
212	S711	8204.6	-824.4
213	S710	8339.6	-796.4
214	S709	8204.6	-768.4
215	S708	8339.6	-740.4
216	S707	8204.6	-712.4
217	S706	8339.6	-684.4
218	S705	8204.6	-656.4
219	S704	8339.6	-628.4
220	S703	8204.6	-600.4
221	S702	8339.6	-572.4
222	S701	8204.6	-544.4
223	S700	8339.6	-516.4
224	S699	8204.6	-488.4
225	S698	8339.6	-460.4
226	S697	8204.6	-432.4
227	S696	8339.6	-404.4
228	S695	8204.6	-376.4
229	S694	8339.6	-348.4
230	S693	8204.6	-320.4
231	S692	8339.6	-292.4
232	S691	8204.6	-264.4
233	S690	8339.6	-236.4
234	S689	8204.6	-208.4
235	S688	8339.6	-180.4
236	S687	8204.6	-152.4
237	S686	8339.6	-124.4
238	S685	8204.6	-96.4
239	S684	8339.6	-68.4
240	S683	8204.6	-40.4

pad No.	pad name	X	Y
241	S682	8339.6	-12.4
242	S681	8204.6	15.6
243	S680	8339.6	43.6
244	S679	8204.6	71.6
245	S678	8339.6	99.6
246	S677	8204.6	127.6
247	S676	8339.6	155.6
248	S675	8204.6	183.6
249	S674	8339.6	211.6
250	S673	8204.6	239.6
251	S672	8339.6	267.6
252	S671	8204.6	295.6
253	S670	8339.6	323.6
254	S669	8204.6	351.6
255	S668	8339.6	379.6
256	S667	8204.6	407.6
257	S666	8339.6	435.6
258	S665	8204.6	463.6
259	S664	8339.6	491.6
260	S663	8204.6	519.6
261	S662	8339.6	547.6
262	S661	8204.6	575.6
263	S660	8339.6	603.6
264	S659	8204.6	631.6
265	S658	8339.6	659.6
266	S657	8204.6	687.6
267	S656	8339.6	715.6
268	S655	8204.6	743.6
269	S654	8339.6	771.6
270	S653	8204.6	799.6
271	S652	8339.6	827.6
272	S651	8204.6	855.6
273	S650	8339.6	883.6
274	S649	8204.6	911.6
275	S648	8339.6	939.6
276	S647	8204.6	967.6
277	S646	8339.6	995.6
278	S645	8204.6	1023.6
279	S644	8339.6	1051.6
280	DUMMY20	8204.6	1079.6
281	DUMMY21	8339.6	1107.6
282	DUMMY22	7980.0	1364.6
283	DUMMY23	7952.0	1229.6
284	DUMMY24	7924.0	1364.6
285	S643	7896.0	1229.6
286	S642	7868.0	1364.6
287	S641	7840.0	1229.6
288	S640	7812.0	1364.6
289	S639	7784.0	1229.6
290	S638	7756.0	1364.6
291	S637	7728.0	1229.6
292	S636	7700.0	1364.6
293	S635	7672.0	1229.6
294	S634	7644.0	1364.6
295	S633	7616.0	1229.6
296	S632	7588.0	1364.6
297	S631	7560.0	1229.6
298	S630	7532.0	1364.6
299	S629	7504.0	1229.6
300	S628	7476.0	1364.6
301	S627	7448.0	1229.6
302	S626	7420.0	1364.6
303	S625	7392.0	1229.6
304	S624	7364.0	1364.6
305	S623	7336.0	1229.6
306	S622	7308.0	1364.6
307	S621	7280.0	1229.6
308	S620	7252.0	1364.6
309	S619	7224.0	1229.6
310	S618	7196.0	1364.6
311	S617	7168.0	1229.6
312	S616	7140.0	1364.6
313	S615	7112.0	1229.6
314	S614	7084.0	1364.6
315	S613	7056.0	1229.6
316	S612	7028.0	1364.6
317	S611	7000.0	1229.6
318	S610	6972.0	1364.6
319	S609	6944.0	1229.6
320	S608	6916.0	1364.6
321	S607	6888.0	1229.6
322	S606	6860.0	1364.6
323	S605	6832.0	1229.6
324	S604	6804.0	1364.6
325	S603	6776.0	1229.6
326	S602	6748.0	1364.6
327	S601	6720.0	1229.6
328	S600	6692.0	1364.6
329	S599	6664.0	1229.6
330	S598	6636.0	1364.6
331	S597	6608.0	1229.6
332	S596	6580.0	1364.6
333	S595	6552.0	1229.6
334	S594	6524.0	1364.6
335	S593	6496.0	1229.6
336	S592	6468.0	1364.6
337	S591	6440.0	1229.6
338	S590	6412.0	1364.6
339	S589	6384.0	1229.6
340	S588	6356.0	1364.6
341	S587	6328.0	1229.6
342	S586	6300.0	1364.6
343	S585	6272.0	1229.6
344	S584	6244.0	1364.6
345	S583	6216.0	1229.6
346	S582	6188.0	1364.6
347	S581	6160.0	1229.6
348	S580	6132.0	1364.6
349	S579	6104.0	1229.6
350	S578	6076.0	1364.6
351	S577	6048.0	1229.6
352	S576	6020.0	1364.6
353	S575	5992.0	1229.6
354	S574	5964.0	1364.6
355	S573	5936.0	1229.6
356	S572	5908.0	1364.6
357	S571	5880.0	1229.6
358	S570	5852.0	1364.6
359	S569	5824.0	1229.6
360	S568	5796.0	1364.6

pad No.	pad name	X	Y
361	S567	5768.0	1229.6
362	S566	5740.0	1364.6
363	S565	5712.0	1229.6
364	S564	5684.0	1364.6
365	S563	5656.0	1229.6
366	S562	5628.0	1364.6
367	S561	5600.0	1229.6
368	S560	5572.0	1364.6
369	S559	5544.0	1229.6
370	S558	5516.0	1364.6
371	S557	5488.0	1229.6
372	S556	5460.0	1364.6
373	S555	5432.0	1229.6
374	S554	5404.0	1364.6
375	S553	5376.0	1229.6
376	S552	5348.0	1364.6
377	S551	5320.0	1229.6
378	S550	5292.0	1364.6
379	S549	5264.0	1229.6
380	S548	5236.0	1364.6
381	S547	5208.0	1229.6
382	S546	5180.0	1364.6
383	S545	5152.0	1229.6
384	S544	5124.0	1364.6
385	S543	5096.0	1229.6
386	S542	5068.0	1364.6
387	S541	5040.0	1229.6
388	S540	5012.0	1364.6
389	S539	4984.0	1229.6
390	S538	4956.0	1364.6
391	S537	4928.0	1229.6
392	S536	4900.0	1364.6
393	S535	4872.0	1229.6
394	S534	4844.0	1364.6
395	S533	4816.0	1229.6
396	S532	4788.0	1364.6
397	S531	4760.0	1229.6
398	S530	4732.0	1364.6
399	S529	4704.0	1229.6
400	S528	4676.0	1364.6
401	S527	4648.0	1229.6
402	S526	4620.0	1364.6
403	S525	4592.0	1229.6
404	S524	4564.0	1364.6
405	S523	4536.0	1229.6
406	S522	4508.0	1364.6
407	S521	4480.0	1229.6
408	S520	4452.0	1364.6
409	S519	4424.0	1229.6
410	S518	4396.0	1364.6
411	S517	4368.0	1229.6
412	S516	4340.0	1364.6
413	S515	4312.0	1229.6
414	S514	4284.0	1364.6
415	S513	4256.0	1229.6
416	S512	4228.0	1364.6
417	S511	4200.0	1229.6
418	S510	4172.0	1364.6
419	S509	4144.0	1229.6
420	S508	4116.0	1364.6
421	S507	4088.0	1229.6
422	S506	4060.0	1364.6
423	S505	4032.0	1229.6
424	S504	4004.0	1364.6
425	S503	3976.0	1229.6
426	S502	3948.0	1364.6
427	S501	3920.0	1229.6
428	S500	3892.0	1364.6
429	S499	3864.0	1229.6
430	S498	3836.0	1364.6
431	S497	3808.0	1229.6
432	S496	3780.0	1364.6
433	S495	3752.0	1229.6
434	S494	3724.0	1364.6
435	S493	3696.0	1229.6
436	S492	3668.0	1364.6
437	S491	3640.0	1229.6
438	S490	3612.0	1364.6
439	S489	3584.0	1229.6
440	S488	3556.0	1364.6
441	S487	3528.0	1229.6
442	S486	3500.0	1364.6
443	S485	3472.0	1229.6
444	S484	3444.0	1364.6
445	S483	3416.0	1229.6
446	S482	3388.0	1364.6
447	S481	3360.0	1229.6
448	S480	3332.0	1364.6
449	S479	3304.0	1229.6
450	S478	3276.0	1364.6
451	S477	3248.0	1229.6
452	S476	3220.0	1364.6
453	S475	3192.0	1229.6
454	S474	3164.0	1364.6
455	S473	3136.0	1229.6
456	S472	3108.0	1364.6
457	S471	3080.0	1229.6
458	S470	3052.0	1364.6
459	S469	3024.0	1229.6
460	S468	2996.0	1364.6
461	S467	2968.0	1229.6
462	S466	2940.0	1364.6
463	S465	2912.0	1229.6
464	S464	2884.0	1364.6
465	S463	2856.0	1229.6
466	S462	2828.0	1364.6
467	S461	2800.0	1229.6
468	S460	2772.0	1364.6
469	S459	2744.0	1229.6
470	S458	2716.0	1364.6
471	S457	2688.0	1229.6
472	S456	2660.0	1364.6
473	S455	2632.0	1229.6
474	S454	2604.0	1364.6
475	S453	2576.0	1229.6
476	S452	2548.0	1364.6
477	S451	2520.0	1229.6
478	S450	2492.0	1364.6
479	S449	2464.0	1229.6
480	S448	2436.0	1364.6

pad No.	pad name	X	Y
481	S447	2408.0	1229.6
482	S446	2380.0	1364.6
483	S445	2352.0	1229.6
484	S444	2324.0	1364.6
485	S443	2296.0	1229.6
486	S442	2268.0	1364.6
487	S441	2240.0	1229.6
488	S440	2212.0	1364.6
489	S439	2184.0	1229.6
490	S438	2156.0	1364.6
491	S437	2128.0	1229.6
492	S436	2100.0	1364.6
493	S435	2072.0	1229.6
494	S434	2044.0	1364.6
495	S433	2016.0	1229.6
496	S432	1988.0	1364.6
497	S431	1960.0	1229.6
498	S430	1932.0	1364.6
499	S429	1904.0	1229.6
500	S428	1876.0	1364.6
501	S427	1848.0	1229.6
502	S426	1820.0	1364.6
503	S425	1792.0	1229.6
504	S424	1764.0	1364.6
505	S423	1736.0	1229.6
506	S422	1708.0	1364.6
507	S421	1680.0	1229.6
508	S420	1652.0	1364.6
509	S419	1624.0	1229.6
510	S418	1596.0	1364.6
511	S417	1568.0	1229.6
512	S416	1540.0	1364.6
513	S415	1512.0	1229.6
514	S414	1484.0	1364.6
515	S413	1456.0	1229.6
516	S412	1428.0	1364.6
517	S411	1400.0	1229.6
518	S410	1372.0	1364.6
519	S409	1344.0	1229.6
520	S408	1316.0	1364.6
521	S407	1288.0	1229.6
522	S406	1260.0	1364.6
523	S405	1232.0	1229.6
524	S404	1204.0	1364.6
525	S403	1176.0	1229.6
526	S402	1148.0	1364.6
527	S401	1120.0	1229.6
528	S400	1092.0	1364.6
529	S399	1064.0	1229.6
530	S398	1036.0	1364.6
531	S397	1008.0	1229.6
532	S396	980.0	1364.6
533	S395	952.0	1229.6
534	S394	924.0	1364.6
535	S393	896.0	1229.6
536	S392	868.0	1364.6
537	S391	840.0	1229.6
538	S390	812.0	1364.6
539	S389	784.0	1229.6
540	S388	756.0	1364.6
541	S387	728.0	1229.6
542	S386	700.0	1364.6
543	S385	672.0	1229.6
544	S384	644.0	1364.6
545	S383	616.0	1229.6
546	S382	588.0	1364.6
547	S381	560.0	1229.6
548	S380	532.0	1364.6
549	S379	504.0	1229.6
550	S378	476.0	1364.6
551	S377	448.0	1229.6
552	S376	420.0	1364.6
553	S375	392.0	1229.6
554	S374	364.0	1364.6
555	S373	336.0	1229.6
556	S372	308.0	1364.6
557	S371	280.0	1229.6
558	S370	252.0	1364.6
559	S369	224.0	1229.6
560	S368	196.0	1364.6
561	S367	168.0	1229.6
562	S366	140.0	1364.6
563	S365	112.0	1229.6
564	S364	84.0	1364.6
565	S363	56.0	1229.6
566	S362	28.0	1364.6
567	S361	0.0	1229.6
568	S360	-28.0	1364.6
569	S359	-56.0	1229.6
570	S358	-84.0	1364.6
571	S357	-112.0	1229.6
572	S356	-140.0	1364.6
573	S355	-168.0	1229.6
574	S354	-196.0	1364.6
575	S353	-224.0	1229.6
576	S352	-252.0	1364.6
577	S351	-280.0	1229.6
578	S350	-308.0	1364.6
579	S349	-336.0	1229.6
580	S348	-364.0	1364.6
581	S347	-392.0	1229.6
582	S346	-420.0	1364.6
583	S345	-448.0	1229.6
584	S344	-476.0	1364.6
585	S343	-504.0	1229.6
586	S342	-532.0	1364.6
587	S341	-560.0	1229.6
588	S340	-588.0	1364.6
589	S339	-616.0	1229.6
590	S338	-644.0	1364.6
591	S337	-672.0	1229.6
592	S336	-700.0	1364.6
593	S335	-728.0	1229.6
594	S334	-756.0	1364.6
595	S333	-784.0	1229.6
596	S332	-812.0	1364.6
597	S331	-840.0	1229.6
598	S330	-868.0	1364.6
599	S329	-896.0	1229.6
600	S328	-924.0	1364.6

pad No.	pad name	X	Y
601	S327	-952.0	1229.6
602	S326	-980.0	1364.6
603	S325	-1008.0	1229.6
604	S324	-1036.0	1364.6
605	S323	-1064.0	1229.6
606	S322	-1092.0	1364.6
607	S321	-1120.0	1229.6
608	S320	-1148.0	1364.6
609	S319	-1176.0	1229.6
610	S318	-1204.0	1364.6
611	S317	-1232.0	1229.6
612	S316	-1260.0	1364.6
613	S315	-1288.0	1229.6
614	S314	-1316.0	1364.6
615	S313	-1344.0	1229.6
616	S312	-1372.0	1364.6
617	S311	-1400.0	1229.6
618	S310	-1428.0	1364.6
619	S309	-1456.0	1229.6
620	S308	-1484.0	1364.6
621	S307	-1512.0	1229.6
622	S306	-1540.0	1364.6
623	S305	-1568.0	1229.6
624	S304	-1596.0	1364.6
625	S303	-1624.0	1229.6
626	S302	-1652.0	1364.6
627	S301	-1680.0	1229.6
628	S300	-1708.0	1364.6
629	S299	-1736.0	1229.6
630	S298	-1764.0	1364.6
631	S297	-1792.0	1229.6
632	S296	-1820.0	1364.6
633	S295	-1848.0	1229.6
634	S294	-1876.0	1364.6
635	S293	-1904.0	1229.6
636	S292	-1932.0	1364.6
637	S291	-1960.0	1229.6
638	S290	-1988.0	1364.6
639	S289	-2016.0	1229.6
640	S288	-2044.0	1364.6
641	S287	-2072.0	1229.6
642	S286	-2100.0	1364.6
643	S285	-2128.0	1229.6
644	S284	-2156.0	1364.6
645	S283	-2184.0	1229.6
646	S282	-2212.0	1364.6
647	S281	-2240.0	1229.6
648	S280	-2268.0	1364.6
649	S279	-2296.0	1229.6
650	S278	-2324.0	1364.6
651	S277	-2352.0	1229.6
652	S276	-2380.0	1364.6
653	S275	-2408.0	1229.6
654	S274	-2436.0	1364.6
655	S273	-2464.0	1229.6
656	S272	-2492.0	1364.6
657	S271	-2520.0	1229.6
658	S270	-2548.0	1364.6
659	S269	-2576.0	1229.6
660	S268	-2604.0	1364.6
661	S267	-2632.0	1229.6
662	S266	-2660.0	1364.6
663	S265	-2688.0	1229.6
664	S264	-2716.0	1364.6
665	S263	-2744.0	1229.6
666	S262	-2772.0	1364.6
667	S261	-2800.0	1229.6
668	S260	-2828.0	1364.6
669	S259	-2856.0	1229.6
670	S258	-2884.0	1364.6
671	S257	-2912.0	1229.6
672	S256	-2940.0	1364.6
673	S255	-2968.0	1229.6
674	S254	-2996.0	1364.6
675	S253	-3024.0	1229.6
676	S252	-3052.0	1364.6
677	S251	-3080.0	1229.6
678	S250	-3108.0	1364.6
679	S249	-3136.0	1229.6
680	S248	-3164.0	1364.6
681	S247	-3192.0	1229.6
682	S246	-3220.0	1364.6
683	S245	-3248.0	1229.6
684	S244	-3276.0	1364.6
685	S243	-3304.0	1229.6
686	S242	-3332.0	1364.6
687	S241	-3360.0	1229.6
688	S240	-3388.0	1364.6
689	S239	-3416.0	1229.6
690	S238	-3444.0	1364.6
691	S237	-3472.0	1229.6
692	S236	-3500.0	1364.6
693	S235	-3528.0	1229.6
694	S234	-3556.0	1364.6
695	S233	-3584.0	1229.6
696	S232	-3612.0	1364.6
697	S231	-3640.0	1229.6
698	S230	-3668.0	1364.6
699	S229	-3696.0	1229.6
700	S228	-3724.0	1364.6
701	S227	-3752.0	1229.6
702	S226	-3780.0	1364.6
703	S225	-3808.0	1229.6
704	S224	-3836.0	1364.6
705	S223	-3864.0	1229.6
706	S222	-3892.0	1364.6
707	S221	-3920.0	1229.6
708	S220	-3948.0	1364.6
709	S219	-3976.0	1229.6
710	S218	-4004.0	1364.6
711	S217	-4032.0	1229.6
712	S216	-4060.0	1364.6
713	S215	-4088.0	1229.6
714	S214	-4116.0	1364.6
715	S213	-4144.0	1229.6
716	S212	-4172.0	1364.6
717	S211	-4200.0	1229.6
718	S210	-4228.0	1364.6
719	S209	-4256.0	1229.6
720	S208	-4284.0	1364.6

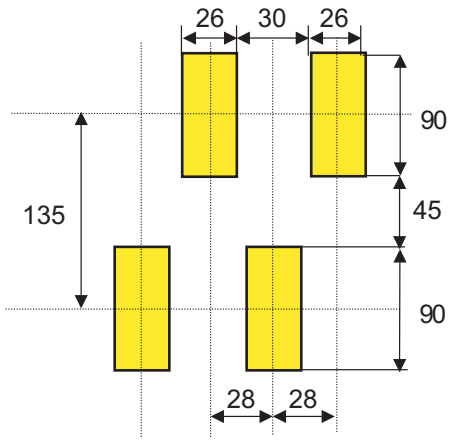
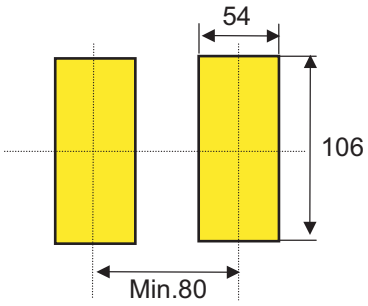
pad No.	pad name	X	Y
721	S207	-4312.0	1229.6
722	S206	-4340.0	1364.6
723	S205	-4368.0	1229.6
724	S204	-4396.0	1364.6
725	S203	-4424.0	1229.6
726	S202	-4452.0	1364.6
727	S201	-4480.0	1229.6
728	S200	-4508.0	1364.6
729	S199	-4536.0	1229.6
730	S198	-4564.0	1364.6
731	S197	-4592.0	1229.6
732	S196	-4620.0	1364.6
733	S195	-4648.0	1229.6
734	S194	-4676.0	1364.6
735	S193	-4704.0	1229.6
736	S192	-4732.0	1364.6
737	S191	-4760.0	1229.6
738	S190	-4788.0	1364.6
739	S189	-4816.0	1229.6
740	S188	-4844.0	1364.6
741	S187	-4872.0	1229.6
742	S186	-4900.0	1364.6
743	S185	-4928.0	1229.6
744	S184	-4956.0	1364.6
745	S183	-4984.0	1229.6
746	S182	-5012.0	1364.6
747	S181	-5040.0	1229.6
748	S180	-5068.0	1364.6
749	S179	-5096.0	1229.6
750	S178	-5124.0	1364.6
751	S177	-5152.0	1229.6
752	S176	-5180.0	1364.6
753	S175	-5208.0	1229.6
754	S174	-5236.0	1364.6
755	S173	-5264.0	1229.6
756	S172	-5292.0	1364.6
757	S171	-5320.0	1229.6
758	S170	-5348.0	1364.6
759	S169	-5376.0	1229.6
760	S168	-5404.0	1364.6
761	S167	-5432.0	1229.6
762	S166	-5460.0	1364.6
763	S165	-5488.0	1229.6
764	S164	-5516.0	1364.6
765	S163	-5544.0	1229.6
766	S162	-5572.0	1364.6
767	S161	-5600.0	1229.6
768	S160	-5628.0	1364.6
769	S159	-5656.0	1229.6
770	S158	-5684.0	1364.6
771	S157	-5712.0	1229.6
772	S156	-5740.0	1364.6
773	S155	-5768.0	1229.6
774	S154	-5796.0	1364.6
775	S153	-5824.0	1229.6
776	S152	-5852.0	1364.6
777	S151	-5880.0	1229.6
778	S150	-5908.0	1364.6
779	S149	-5936.0	1229.6
780	S148	-5964.0	1364.6
781	S147	-5992.0	1229.6
782	S146	-6020.0	1364.6
783	S145	-6048.0	1229.6
784	S144	-6076.0	1364.6
785	S143	-6104.0	1229.6
786	S142	-6132.0	1364.6
787	S141	-6160.0	1229.6
788	S140	-6188.0	1364.6
789	S139	-6216.0	1229.6
790	S138	-6244.0	1364.6
791	S137	-6272.0	1229.6
792	S136	-6300.0	1364.6
793	S135	-6328.0	1229.6
794	S134	-6356.0	1364.6
795	S133	-6384.0	1229.6
796	S132	-6412.0	1364.6
797	S131	-6440.0	1229.6
798	S130	-6468.0	1364.6
799	S129	-6496.0	1229.6
800	S128	-6524.0	1364.6
801	S127	-6552.0	1229.6
802	S126	-6580.0	1364.6
803	S125	-6608.0	1229.6
804	S124	-6636.0	1364.6
805	S123	-6664.0	1229.6
806	S122	-6692.0	1364.6
807	S121	-6720.0	1229.6
808	S120	-6748.0	1364.6
809	S119	-6776.0	1229.6
810	S118	-6804.0	1364.6
811	S117	-6832.0	1229.6
812	S116	-6860.0	1364.6
813	S115	-6888.0	1229.6
814	S114	-6916.0	1364.6
815	S113	-6944.0	1229.6
816	S112	-6972.0	1364.6
817	S111	-7000.0	1229.6
818	S110	-7028.0	1364.6
819	S109	-7056.0	1229.6
820	S108	-7084.0	1364.6
821	S107	-7112.0	1229.6
822	S106	-7140.0	1364.6
823	S105	-7168.0	1229.6
824	S104	-7196.0	1364.6
825	S103	-7224.0	1229.6
826	S102	-7252.0	1364.6
827	S101	-7280.0	1229.6
828	S100	-7308.0	1364.6
829	S99	-7336.0	1229.6
830	S98	-7364.0	1364.6
831	S97	-7392.0	1229.6
832	S96	-7420.0	1364.6
833	S95	-7448.0	1229.6
834	S94	-7476.0	1364.6
835	S93	-7504.0	1229.6
836	S92	-7532.0	1364.6
837	S91	-7560.0	1229.6
838	S90	-7588.0	1364.6
839	S89	-7616.0	1229.6
840	S88	-7644.0	1364.6

pad No.	pad name	X	Y
841	S87	-7672.0	1229.6
842	S86	-7700.0	1364.6
843	S85	-7728.0	1229.6
844	S84	-7756.0	1364.6
845	S83	-7784.0	1229.6
846	S82	-7812.0	1364.6
847	S81	-7840.0	1229.6
848	S80	-7868.0	1364.6
849	S79	-7896.0	1229.6
850	S78	-7924.0	1364.6
851	DUMMY25	-7952.0	1229.6
852	DUMMY26	-7980.0	1364.6
853	DUMMY27	-8339.6	1107.6
854	DUMMY28	-8204.6	1079.6
855	S77	-8339.6	1051.6
856	S76	-8204.6	1023.6
857	S75	-8339.6	995.6
858	S74	-8204.6	967.6
859	S73	-8339.6	939.6
860	S72	-8204.6	911.6
861	S71	-8339.6	883.6
862	S70	-8204.6	855.6
863	S69	-8339.6	827.6
864	S68	-8204.6	799.6
865	S67	-8339.6	771.6
866	S66	-8204.6	743.6
867	S65	-8339.6	715.6
868	S64	-8204.6	687.6
869	S63	-8339.6	659.6
870	S62	-8204.6	631.6
871	S61	-8339.6	603.6
872	S60	-8204.6	575.6
873	S59	-8339.6	547.6
874	S58	-8204.6	519.6
875	S57	-8339.6	491.6
876	S56	-8204.6	463.6
877	S55	-8339.6	435.6
878	S54	-8204.6	407.6
879	S53	-8339.6	379.6
880	S52	-8204.6	351.6
881	S51	-8339.6	323.6
882	S50	-8204.6	295.6
883	S49	-8339.6	267.6
884	S48	-8204.6	239.6
885	S47	-8339.6	211.6
886	S46	-8204.6	183.6
887	S45	-8339.6	155.6
888	S44	-8204.6	127.6
889	S43	-8339.6	99.6
890	S42	-8204.6	71.6
891	S41	-8339.6	43.6
892	S40	-8204.6	15.6
893	S39	-8339.6	-12.4
894	S38	-8204.6	-40.4
895	S37	-8339.6	-68.4
896	S36	-8204.6	-96.4
897	S35	-8339.6	-124.4
898	S34	-8204.6	-152.4
899	S33	-8339.6	-180.4
900	S32	-8204.6	-208.4
901	S31	-8339.6	-236.4
902	S30	-8204.6	-264.4
903	S29	-8339.6	-292.4
904	S28	-8204.6	-320.4
905	S27	-8339.6	-348.4
906	S26	-8204.6	-376.4
907	S25	-8339.6	-404.4
908	S24	-8204.6	-432.4
909	S23	-8339.6	-460.4
910	S22	-8204.6	-488.4
911	S21	-8339.6	-516.4
912	S20	-8204.6	-544.4
913	S19	-8339.6	-572.4
914	S18	-8204.6	-600.4
915	S17	-8339.6	-628.4
916	S16	-8204.6	-656.4
917	S15	-8339.6	-684.4
918	S14	-8204.6	-712.4
919	S13	-8339.6	-740.4
920	S12	-8204.6	-768.4
921	S11	-8339.6	-796.4
922	S10	-8204.6	-824.4
923	S9	-8339.6	-852.4
924	S8	-8204.6	-880.4
925	S7	-8339.6	-908.4
926	S6	-8204.6	-936.4
927	S5	-8339.6	-964.4
928	S4	-8204.6	-992.4
929	S3	-8339.6	-1020.4
930	S2	-8204.6	-1048.4
931	S1	-8339.6	-1076.4
932	DUMMY29	-8204.6	-1104.4
933	DUMMY30	-8339.6	-1132.4

Alignment Mark	X	Y
L-type (Positive)	-8339.6	1274.3
L-type (Negative)	8339.6	1274.3
Circle (Positive)	-8339.6	1364.6
Circle (Negative)	8339.6	1364.6
Cross	-8199.6	1324.3
	8199.6	1324.3

Unit : μm

Bump Arrangement

S1~S720	 S=2340um^2 Unit : um
I/O pins (No1 ~ 200)	 S=5724um^2 Unit : um

Example of connecting HD66781 and HD66783

Note:

This is an example of connecting HD66781 and HD66783 when these drivers are used as a set. The bottom views show an example of pin arrangements. See the pad cooridnation of each product for more accurate and detailed reference to the number of pads and the coordination.

The validity of this connection example is not confirmed. It is necessary to throughly check the operation and the display quality before use.

a-Si TFT

IOVcc = 1.7V~3.3V (HD66781)
Vcc1 = 1.7~3.3V (HD66781)
Vcc = 2.5~3.3V (HD66781)
VCC = 1.7~3.3V (HD667P21)
VCI = 2.5~3.3V (HD667P21)
Supply a same potential to Vcc1 of HD66781 and VCC of HD66783.
Make sure that IOVcc≦Vcc1≦Vcc (HD66781).

Source Electrode

Gate electrode

Gate electrode

To opposing electrodes on the panel(Vcom)

HD66781
(Bottom View)
Laced Output
Arrangement

HD667B83
(Bottom View)
Laced Output
Arrangement

80-system 18-bit interface

Short-circuit DUMMY14 and DUMMY15 Within LSI

Short-circuit DMY22 and DMY23 within LSI

Short-circuit TG328 and G328 within LSI

Connect on the FPC.

Connect on the FPC.

Connect on the FPC.

GND

1uF/3V/B

1.7~3.3V
Vcc1(781)=Vcc(783)

1.7~3.3V
IOVcc

> 200kΩ

1uF/6V/B

1uF/10V/B

1uF/10V/B

1uF/6V/B

1uF/6V/B

1uF/10V/B
VF<0.4V/20mA at 25℃, VR≧30V

1uF/25V/B

1uF/6V/B

1uF/6V/B

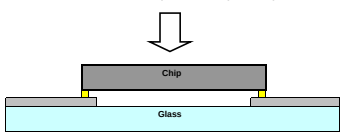
1uF/6V/B

1uF/6V/B

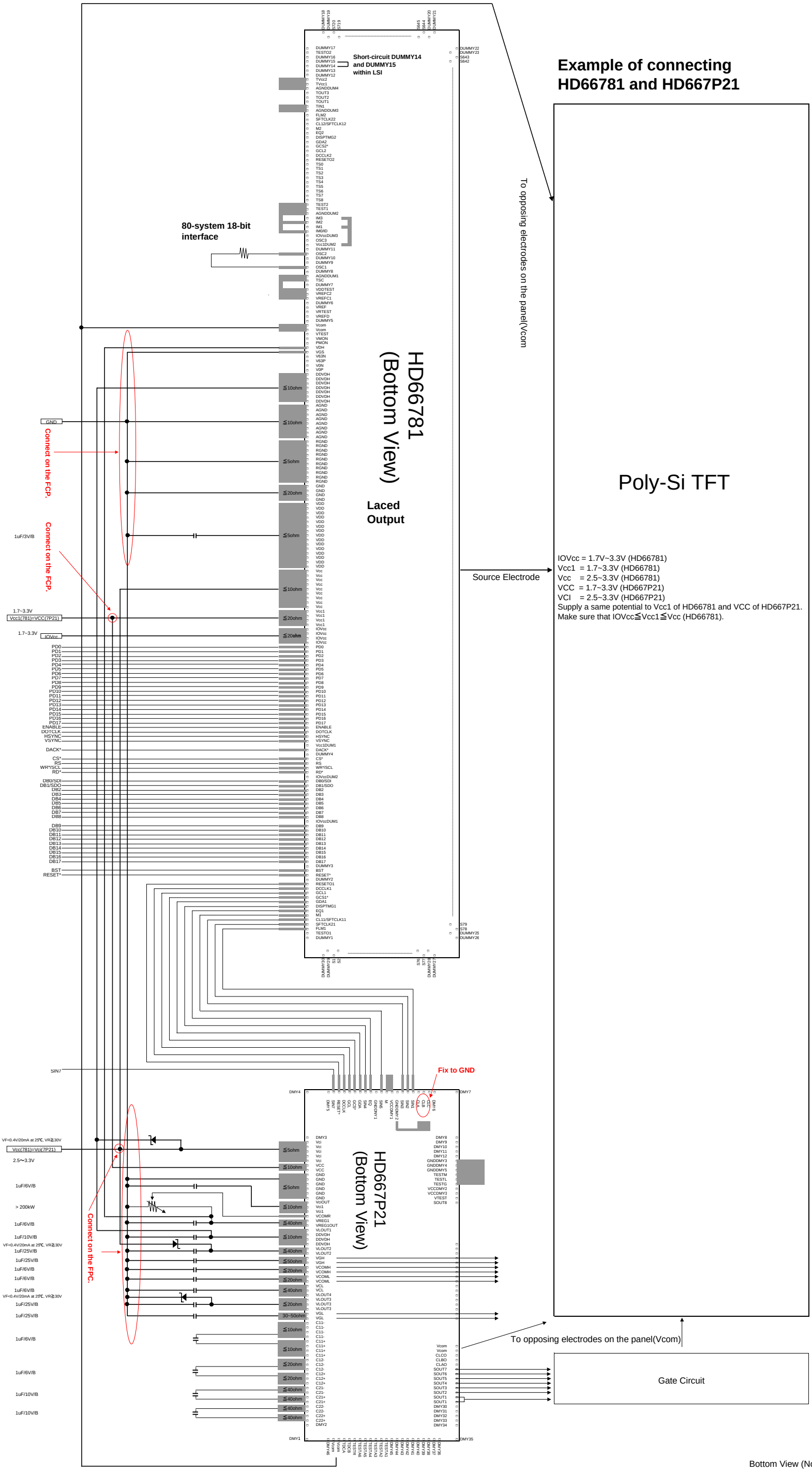
1uF/25V/B
VF<0.4V/20mA at 25℃, VR≧30V

Vcc(781)=Vci(783)
2.5~3.3V

Bottom View (Non Bump View)



Example of connecting HD66781 and HD667P21



Block Function

(1) System interface

The HD66781 has 2 kinds of high-speed system interfaces: 80-system 18-/16-/9-/8-bit bus interfaces and Serial Peripheral Interface (SPI) ports. The 8-bit bus interface is compliant to both big and little endian data outputs from the microcomputer. The interface mode is selected with the IM3-0 pins.

The HD66781 incorporates 16-bit index register (IR), write-data register (WDR), and 16-bit read-data register (RDR). The IR stores index information from the control register and GRAM. The WDR temporarily stores data to write into the control register and GRAM, and the RDR temporarily stores data read from GRAM. Data written into GRAM from MPU is first written into the WDR and then automatically written to GRAM by internal operation. Since data are read through the RDR from GRAM, the data that are read out first are invalid and the ensuing data are read out normally.

The execution time for the instructions other than oscillation start is 0-clock cycle, which enables writing instructions consecutively.

Table 1 Register Selection (8/9/16/18 parallel interface)

80-system bus			Operation
WR*	RD*	RS	
0	1	0	Write index to IR.
1	0	0	Read internal status
0	1	1	Write to control registers/GRAM through WDR
1	0	1	Read from GRAM through RDR

Table 2 Register Selection (SPI)

Start byte		Operation
RW	RS	
0	0	Write index to IR.
1	0	Read internal status
0	0	Write to control registers/GRAM through WDR
1	1	Read from GRAM through RDR

The HD66781 incorporates DMA single address mode interface to keep control on the bus occupation ratio when transferring a large volume of data. The DMA controller supporting a single address mode controls the DACK pin of HD66781 to recognize out-enable signal (OE) for SRAM as a write strobe signal. The HD66781 enables data transfer with less bus cycle by using a same bus cycle for a readout operation from an external SRAM and a write operation to HD66781. See "DMA transfer single address mode" (p.131) for details on controlling the execution of transfer and conditions in using this mode.

(2) External Display Interface (RGB I/F, VSYNC I/F)

The HD66781 incorporates RGB and VSYNC interfaces as an external interface for displaying moving pictures. When the RGB-I/F is selected, the operation is synchronized with externally supplied signals, VSYN C, HSYNC, and DOTCLK. The display data (PD17-0) are written in accordance with the data enable signal (ENABLE). Accordingly, the display on the screen does not flicker when RAM data are being updated internally.

When the VSYNC-I/F is selected, the operation is synchronized with internal clocks except frame synchronization, which is synchronized with VSYNC signal. The display data is written to GRAM through a system interface. In this case, there are constraints on the speed and methods of updating RAM data when the VSYNC I/F is selected. For details, see the "External Display Interface" section (p.139).

The switch from and to the system interface is made through instructions. An optimum interface can be selected for the kind of display (still and/or moving pictures). The display data are all written to GRAM through the RGB-I/F. This enables transmission of data only when the display on the screen is being updated, and thereby reduces the data transmission as well as consumption of power when a moving picture is displayed.

(3) Address Counter (AC)

The address counter (AC) assigns the address to GRAM. When a set-address instruction is written to the IR, the address information is sent from the IR to the AC. After writing data into GRAM, the AC is automatically incremented or decremented by 1, while after data are read form GRAM, the AC is not updated. Window address function enables data write only in the rectangular area of GRAM specified by the window address.

(4) Graphic RAM (GRAM)

GRAM is a graphics RAM that stores 224,640-byte bit-pattern data, where one pixel is expressed by 18 bits. Maximum 240 RGB x 320 can be displayed by using both main/sub panels. Besides data of 240 RGB x 320 lines for a base image, it can store OSD data of 240 RGB x 96 lines. The allocation of the numbers of lines for a base image and an OSD image is changeable.

(5) Grayscale Voltage Generation Circuit

The grayscale voltage generation circuit generates an LCD drive voltage according to the grayscale level set in the γ-correction register. Simultaneously 262,144 colors are available for display.

(6) Timing generator

Timing generator generates a timing signal for the operation of internal circuits such as GRAM. The timing for display operation such as RAM read and the internal operation timing such as access from MPU are generated in a way to avoid mutual interfere. Also the signals interfacing with gate driver/power supply IC (M, FLM, CL1/SFTCLK1, SFTCLK2, EQ, DCCLK, and DISPTMG) are generated.

(7) Oscillation Circuit (OSC)

The HD66781 generates R-C oscillation simply by placing an external oscillation-resistor between the OSC1 and OSC2 pins. The oscillation frequency is changeable with the value of external resistor. Adjust oscillation frequency in accordance to an operation voltage, display size, and frame frequency. During the standby mode, the R-C oscillation is halted to reduce power consumption. For details, see “Oscillation Circuit” (p.173).

(8) Liquid Crystal Display Driver Circuit

The LCD driver circuit consists of a 720-output source driver (S1 ~ S720). Display pattern data are latched when 720-bit data arrive. The latched data controls the source driver and generates drive waveforms. The shift direction of 720-bit output from source driver is changeable with SS bit. Select an appropriate shift direction for the assembly.

(9) Gate driver/power supply IC interfacing circuit

Gate driver/power supply IC interfacing circuit is a serial interface circuit to interface with the HD66783 and the HD667P21. When making settings for instructions to the HD66783 or the HD667P21 though the HD66781, values set in the register of HD66781 are transferred through this serial interface circuit. The transfer starts by making a serial transfer ENABLE setting. Both transfer of instruction to the HD66783/HD667P21 and read out from the HD66781 are impossible during standby mode. For details, see “Gate Driver/Power Supply IC interface control” (p.70).

(10) Internal Logic Power Supply Regulator

Internal logic power supply regulator generates power supply VDD for the internal logic.

GRAM Address MAP

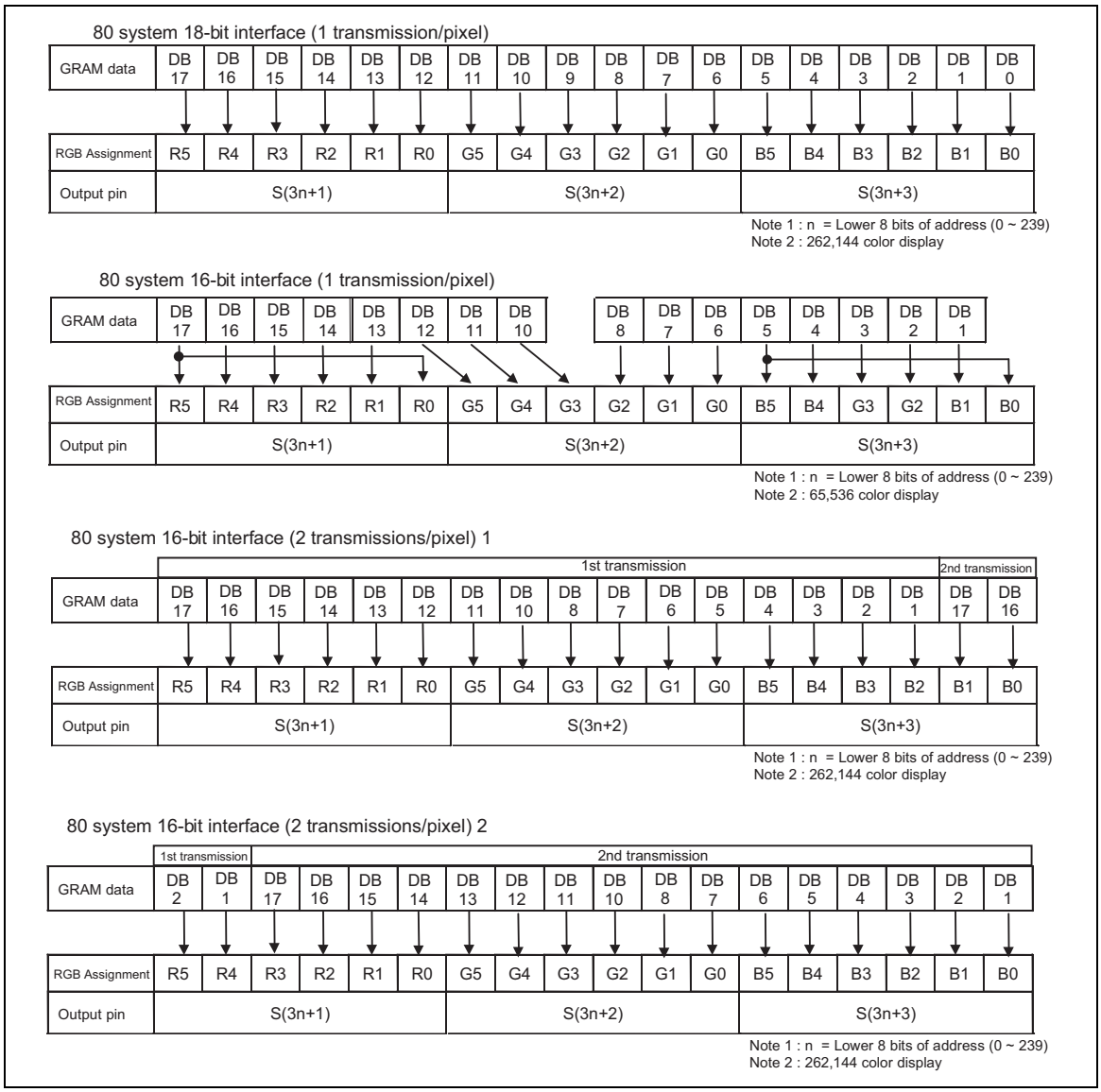
Relation between GRAM addresses and Screen positions (SS=0, BGR=0)

Table 3

S/ G pins		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	·····	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720
GS=0	GS=1	PD17-0			PD17-0			PD17-0			PD17-0			·····	PD17-0			PD17-0			PD17-0			PD17-0		
G1	G328	h00000			h00001			h00002			h00003			·····	h000EC			h000ED			h000EE			h000EF		
G2	G327	h00100			h00101			h00102			h00103			·····	h001EC			h001ED			h001EE			h001EF		
G3	G326	h00200			h00201			h00202			h00203			·····	h002EC			h002ED			h002EE			h002EF		
G4	G325	h00300			h00301			h00302			h00303			·····	h003EC			h003ED			h003EE			h003EF		
G5	G324	h00400			h00401			h00402			h00403			·····	h004EC			h004ED			h004EE			h004EF		
G6	G323	h00500			h00501			h00502			h00503			·····	h005EC			h005ED			h005EE			h005EF		
G7	G322	h00600			h00601			h00602			h00603			·····	h006EC			h006ED			h006EE			h006EF		
G8	G321	h00700			h00701			h00702			h00703			·····	h007EC			h007ED			h007EE			h007EF		
G9	G320	h00800			h00801			h00802			h00803			·····	h008EC			h008ED			h008EE			h008EF		
G10	G319	h00900			h00901			h00902			h00903			·····	h009EC			h009ED			h009EE			h009EF		
G11	G318	h00A00			h00A01			h00A02			h00A03			·····	h00AEC			h00AED			h00AEE			h00AEF		
G12	G317	h00B00			h00B01			h00B02			h00B03			·····	h00BEC			h00BED			h00BEE			h00BEF		
G13	G316	h00C00			h00C01			h00C02			h00C03			·····	h00CEC			h00CED			h00CEE			h00CEF		
G14	G315	h00D00			h00D01			h00D02			h00D03			·····	h00DEC			h00DED			h00DEE			h00DEF		
G15	G314	h00E00			h00E01			h00E02			h00E03			·····	h00EEC			h00EED			h00EEE			h00EEF		
G16	G313	h00F00			h00F01			h00F02			h00F03			·····	h00FEC			h00FED			h00FEE			h00FEF		
G17	G312	h01000			h01001			h01002			h01003			·····	h010EC			h010ED			h010EE			h010EF		
G18	G311	h01100			h01101			h01102			h01103			·····	h011EC			h011ED			h011EE			h011EF		
G19	G310	h01200			h01201			h01202			h01203			·····	h012EC			h012ED			h012EE			h012EF		
G20	G309	h01300			h01301			h01302			h01303			·····	h013EC			h013ED			h013EE			h013EF		
:	:	:			:			:			:															
:	:	:			:			:			:															
G301	G28	h12C00			h12C01			h12C02			h12C03			·····	h12CEC			h12CED			h12CEE			h12CEF		
G302	G27	h12D00			h12D01			h12D02			h12D03			·····	h12DEC			h12DED			h12DEE			h12DEF		
G303	G26	h12E00			h12E01			h12E02			h12E03			·····	h12EEC			h12EED			h12EEE			h12EEF		
G304	G25	h12F00			h12F01			h12F02			h12F03			·····	h12FEC			h12FED			h12FEE			h12FEF		
G305	G24	h13000			h13001			h13002			h13003			·····	h130EC			h130ED			h130EE			h130EF		
G306	G23	h13100			h13101			h13102			h13103			·····	h131EC			h131ED			h131EE			h131EF		
G307	G22	h13200			h13201			h13202			h13203			·····	h132EC			h132ED			h132EE			h132EF		
G308	G21	h13300			h13301			h13302			h13303			·····	h133EC			h133ED			h133EE			h133EF		
G309	G20	h13400			h13401			h13402			h13403			·····	h134EC			h134ED			h134EE			h134EF		
G310	G19	h13500			h13501			h13502			h13503			·····	h135EC			h135ED			h135EE			h135EF		
G311	G18	h13600			h13601			h13602			h13603			·····	h136EC			h136ED			h136EE			h136EF		
G312	G17	h13700			h13701			h13702			h13703			·····	h137EC			h137ED			h137EE			h137EF		
G313	G16	h13800			h13801			h13802			h13803			·····	h138EC			h138ED			h138EE			h138EF		
G314	G15	h13900			h13901			h13902			h13903			·····	h139EC			h139ED			h139EE			h139EF		
G315	G14	h13A00			h13A01			h13A02			h13A03			·····	h13AEC			h13AED			h13AEE			h13AEF		
G316	G13	h13B00			h13B01			h13B02			h13B03			·····	h13BEC			h13BED			h13BEE			h13BEF		
G317	G12	h13C00			h13C01			h13C02			h13C03			·····	h13CEC			h13CED			h13CEE			h13CEF		
G318	G11	h13D00			h13D01			h13D02			h13D03			·····	h13DEC			h13DED			h13DEE			h13DEF		
G319	G10	h13E00			h13E01			h13E02			h13E03			·····	h13EEC			h13EED			h13EEE			h13EEF		
G320	G9	h13F00			h13F01			h13F02			h13F03			·····	h13FEC			h13FED			h13FEE			h13FEF		

Relation between GRAM data and Display data (SS=0, BGR=0)

The following figure illustrates the relationship between data on GRAM and display data through each interface.



80-system 18/16-bit interface (SS = 0, BGR = 0)

80 system 9-bit interface (2 transmissions/pixel)

	1st transmission									2nd transmission								
GRAM data	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9
RGB Assignment	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Output pin	S(3n+1)						S(3n+2)						S(3n+3)					

Note 1 : n = Lower 8 bits of address (0 ~ 239)
Note 2 : 262,144 color display

80 system 8-bit interface (big endian)/ SPI (2 transmissions/pixel)

	1st transmission								2nd transmission							
GRAM data	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10
RGB Assignment	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Output pin	S(3n+1)						S(3n+2)						S(3n+3)					

Note 1 : n = lower 8 bits of address (0 ~ 239)
Note 2 : 65,536 color display

80 system 8-bit interface / (3 transmissions/pixel) 1

	1st transmission		2nd transmission								3rd transmission							
GRAM data	DB 11	DB 10	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10
RGB Assignment	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Output pin	S(3n+1)						S(3n+2)						S(3n+3)					

Note 1 : n = lower 8 bits of address (0 ~ 239)
Note 2 : 262,144 color display

80 system 8-bit interface / (3 transmissions/pixel) 2

	1st transmission						2nd transmission						3rd transmission					
GRAM data	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12
RGB Assignment	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Output pin	S(3n+1)						S(3n+2)						S(3n+3)					

Note 1 : n = lower 8 bits of address (0 ~ 239)
Note 2 : 262,144 color display
Note 3: Upper 2-bit data of each transmission are not used.

80 system 8-bit interface (little endian) / (2 transmissions/pixel)

	2nd transmission								1st transmission							
GRAM data	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10
RGB Assignment	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Output pin	S(3n+1)						S(3n+2)						S(3n+3)					

Note 1 : n = lower 8 bits of address (0 ~ 239)
Note 2 : 65,536 color display

80-system 9/8-bit interface (SS = 0, BGR = 0)

18 bit RGB interface (1 transmission/pixel)

GRAM data	PD 17	PD 16	PD 15	PD 14	PD 13	PD 12	PD 11	PD 10	PD 9	PD 8	PD 7	PD 6	PD 5	PD 4	PD 3	PD 2	PD 1	PD 0
RGB Assignment	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Output pin	S(3n+1)						S(3n+2)						S(3n+3)					

Note 1 : n = lower 8 bits of address (0 ~ 239)
Note 2 : 262,144 color display

16-bit RGB interface (1 transmission/pixel)

GRAM data	PD 17	PD 16	PD 15	PD 14	PD 13		PD 11	PD 10	PD 9	PD 8	PD 7	PD 6	PD 5	PD 4	PD 3	PD 2	PD 1	
RGB Assignment	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Output pin	S(3n+1)						S(3n+2)						S(3n+3)					

Note 1 : n = lower 8 bits of address (0 ~ 239)
Note 2 : 65,536 color display

6-bit RGB interface (3 transmissions/pixel)

	1st transmission						2nd transmission						3rd transmission					
GRAM data	PD 17	PD 16	PD 15	PD 14	PD 13	PD 12	PD 17	PD 16	PD 15	PD 14	PD 13	PD 12	PD 17	PD 16	PD 15	PD 14	PD 13	PD 12
RGB Assignment	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Output pin	S(3n+1)						S(3n+2)						S(3n+3)					

Note 1 : n = lower 8 bits of address (0 ~ 239)
Note 2 : 262,144 color display

RGB interface (SS = 0, BGR = 0)

Relation between GRAM address and Screen position (SS=1, BGR=1)

Table 4

S/ G pins		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	·····	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720
GS=0	GS=1	PD17-0			PD17-0			PD17-0			PD17-0			·····	PD17-0			PD17-0			PD17-0			PD17-0		
G1	G328	h000EF			h000EE			h000ED			h000EC			·····	h00003			h00002			h00001			h00000		
G2	G327	h001EF			h001EE			h001ED			h001EC			·····	h00103			h00102			h00101			h00100		
G3	G326	h002EF			h002EE			h002ED			h002EC			·····	h00203			h00202			h00201			h00200		
G4	G325	h003EF			h003EE			h003ED			h003EC			·····	h00303			h00302			h00301			h00300		
G5	G324	h004EF			h004EE			h004ED			h004EC			·····	h00403			h00402			h00401			h00400		
G6	G323	h005EF			h005EE			h005ED			h005EC			·····	h00503			h00502			h00501			h00500		
G7	G322	h006EF			h006EE			h006ED			h006EC			·····	h00603			h00602			h00601			h00600		
G8	G321	h007EF			h007EE			h007ED			h007EC			·····	h00703			h00702			h00701			h00700		
G9	G320	h008EF			h008EE			h008ED			h008EC			·····	h00803			h00802			h00801			h00800		
G10	G319	h009EF			h009EE			h009ED			h009EC			·····	h00903			h00902			h00901			h00900		
G11	G318	h00AEF			h00AEE			h00AED			h00AEC			·····	h00A03			h00A02			h00A01			h00A00		
G12	G317	h00BEF			h00BEE			h00BED			h00BEC			·····	h00B03			h00B02			h00B01			h00B00		
G13	G316	h00CEF			h00CEE			h00CED			h00CEC			·····	h00C03			h00C02			h00C01			h00C00		
G14	G315	h00DEF			h00DEE			h00DED			h00DEC			·····	h00D03			h00D02			h00D01			h00D00		
G15	G314	h00EEF			h00EEE			h00EED			h00EEC			·····	h00E03			h00E02			h00E01			h00E00		
G16	G313	h00FEF			h00FEE			h00FED			h00FEC			·····	h00F03			h00F02			h00F01			h00F00		
G17	G312	h010EF			h010EE			h010ED			h010EC			·····	h01003			h01002			h01001			h01000		
G18	G311	h011EF			h011EE			h011ED			h011EC			·····	h01103			h01102			h01101			h01100		
G19	G310	h012EF			h012EE			h012ED			h012EC			·····	h01203			h01202			h01201			h01200		
G20	G309	h013EF			h013EE			h013ED			h013EC			·····	h01303			h01302			h01301			h01300		
:	:	:			:			:			:															
:	:	:			:			:			:															
G301	G28	h12CEF			h12CEE			h12CED			h12CEC			·····	h12C03			h12C02			h12C01			h12C00		
G302	G27	h12DEF			h12DEE			h12DED			h12DEC			·····	h12D03			h12D02			h12D01			h12D00		
G303	G26	h12EEF			h12EEE			h12EED			h12EEC			·····	h12E03			h12E02			h12E01			h12E00		
G304	G25	h12FEF			h12FEE			h12FED			h12FEC			·····	h12F03			h12F02			h12F01			h12F00		
G305	G24	h130EF			h130EE			h130ED			h130EC			·····	h13003			h13002			h13001			h13000		
G306	G23	h131EF			h131EE			h131ED			h131EC			·····	h13103			h13102			h13101			h13100		
G307	G22	h132EF			h132EE			h132ED			h132EC			·····	h13203			h13202			h13201			h13200		
G308	G21	h133EF			h133EE			h133ED			h133EC			·····	h13303			h13302			h13301			h13300		
G309	G20	h134EF			h134EE			h134ED			h134EC			·····	h13403			h13402			h13401			h13400		
G310	G19	h135EF			h135EE			h135ED			h135EC			·····	h13503			h13502			h13501			h13500		
G311	G18	h136EF			h136EE			h136ED			h136EC			·····	h13603			h13602			h13601			h13600		
G312	G17	h137EF			h137EE			h137ED			h137EC			·····	h13703			h13702			h13701			h13700		
G313	G16	h138EF			h138EE			h138ED			h138EC			·····	h13803			h13802			h13801			h13800		
G314	G15	h139EF			h139EE			h139ED			h139EC			·····	h13903			h13902			h13901			h13900		
G315	G14	h13AEF			h13AEE			h13AED			h13AEC			·····	h13A03			h13A02			h13A01			h13A00		
G316	G13	h13BEF			h13BEE			h13BED			h13BEC			·····	h13B03			h13B02			h13B01			h13B00		
G317	G12	h13CEF			h13CEE			h13CED			h13CEC			·····	h13C03			h13C02			h13C01			h13C00		
G318	G11	h13DEF			h13DEE			h13DED			h13DEC			·····	h13D03			h13D02			h13D01			h13D00		
G319	G10	h13EEF			h13EEE			h13EED			h13EEC			·····	h13E03			h13E02			h13E01			h13E00		
G320	G9	h13FEF			h13FEE			h13FED			h13FEC			·····	h13F03			h13F02			h13F01			h13F00		

Relation between GRAM data and Display data (SS=1, BGR=1)

80 system 18-bit interface (1 transmission/pixel)

GRAM data	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
RGB Assignment	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Output pin	S(720- 3n)						S(719- 3n)						S(718 -3n)					

Note 1 : n = Lower 8 bits of address (0 ~ 239)
Note 2 : 262,144 color display

80 system 16-bit interface (1 transmission/pixel)

GRAM data	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1		
RGB Assignment	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	G3	G2	B1	B0
Output pin	S(720- 3n)						S(719 - 3n)						S(718 -3n)					

Note 1 : n = Lower 8 bits of address (0 ~ 239)
Note 2 : 65,536 color display

80 system 16 bit interface (2 transmissions/pixel) 1

	1st transmission																2nd transmission	
GRAM data	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 17	DB 16
RGB Assignment	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Output pin	S(720- 3n)						S(719- 3n)						S(718 -3n)					

Note 1 : n = Lower 8 bits of address (0 ~ 239)
Note 2 : 262,144 color display

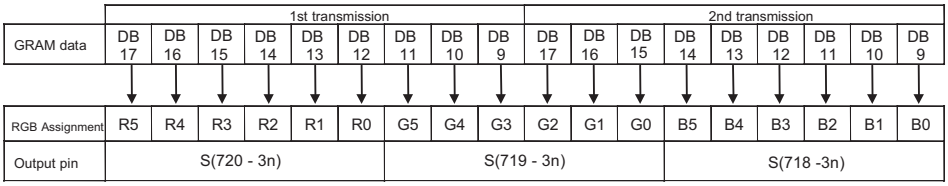
80 system 16 bit interface (2 transmissions/pixel) 2

	1st transmission		2nd transmission															
GRAM data	DB 2	DB 1	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1
RGB Assignment	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Output pin	S(720- 3n)						S(719- 3n)						S(718 -3n)					

Note 1 : n = Lower 8 bits of address (0 ~ 239)
Note 2 : 262,144 color display

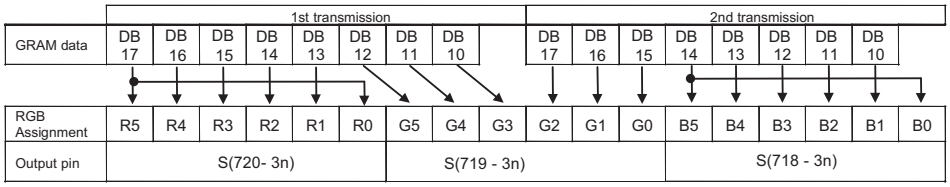
80-system18/16-bit interface (SS = 1, BGR = 1)

80 system 9-bit interface (2 transmissions/pixel)



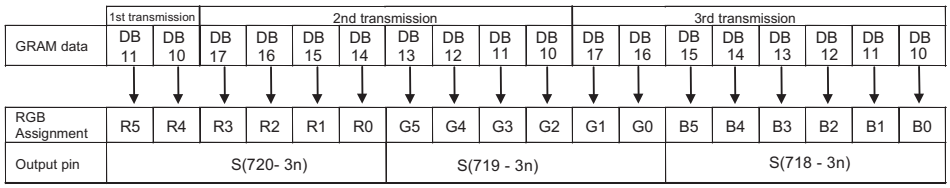
Note 1 : n = Lower 8 bits of address (0 ~ 239)
Note 2 : 262,144 color display

80 system 8-bit interface (big endian) / SPI (2 transmissions/pixel)



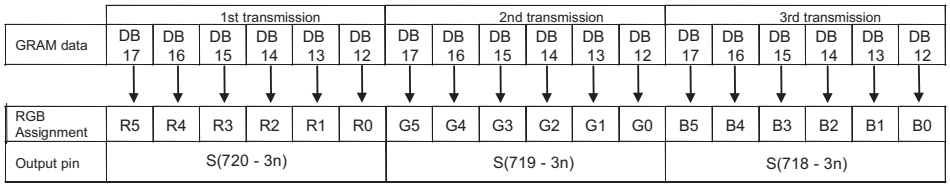
Note 1 : n = lower 8 bits of address (0 ~ 239)
Note 2 : 65,536 color display

80 system 8-bit interface / (3 transmissions/pixel) 1



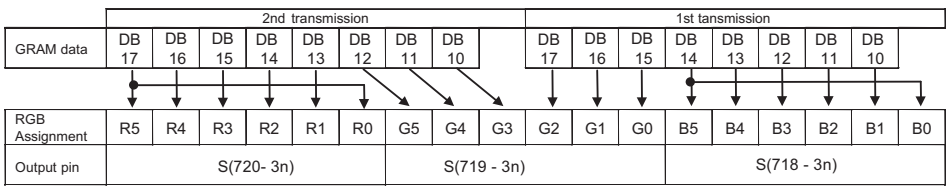
Note 1 : n = lower 8 bits of address (0 ~ 239)
Note 2 : 262,144 color display

80 system 8-bit interface / (3 transmissions/pixel) 2



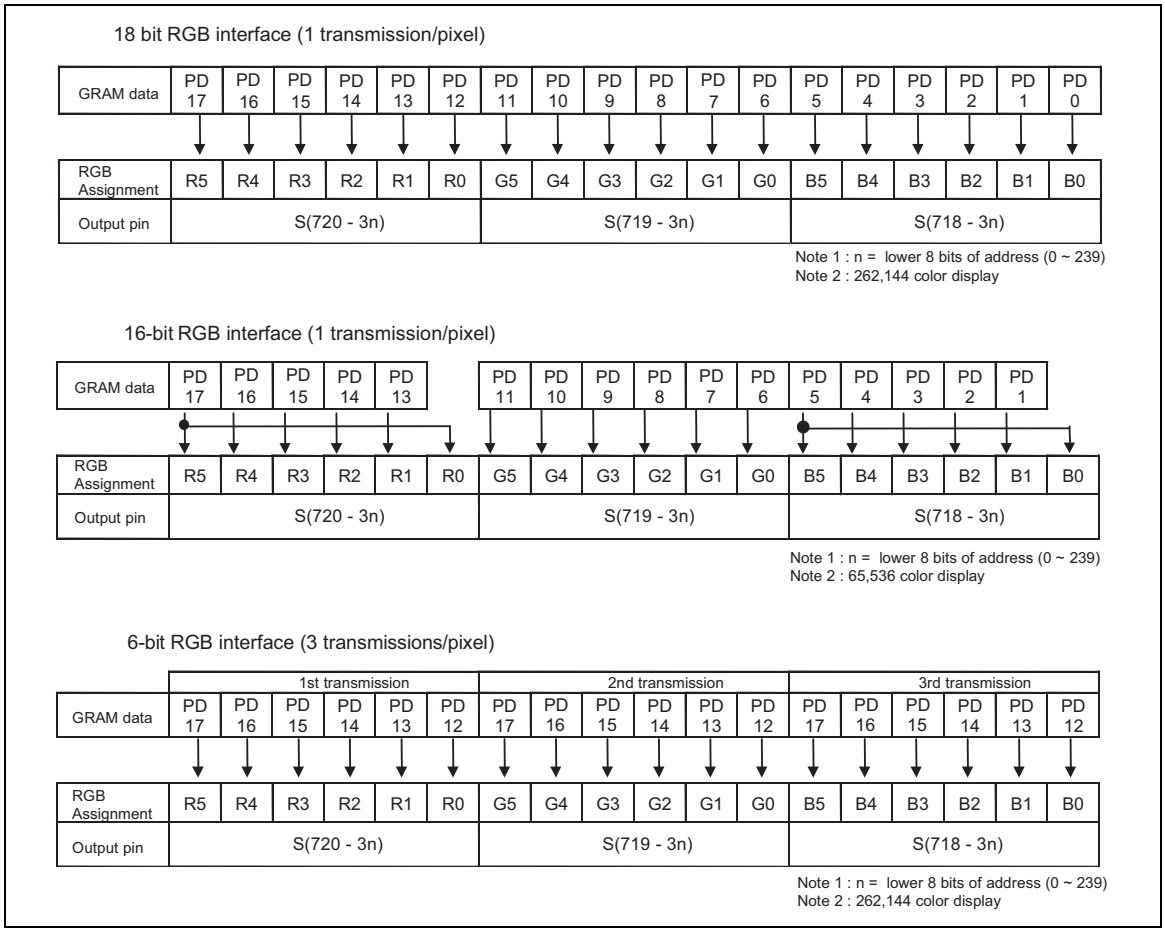
Note 1 : n = lower 8 bits of address (0 ~ 239)
Note 2 : 262,144 color display
Note 3 : Upper 2-bit data of each transmission are not used.

80 system 8-bit interface (little endian) / (2 transmissions/pixel)



Note 1 : n = lower 8 bits of address (0 ~ 239)
Note 2 : 65,536 color display

80-system 9/8-bit interface (SS = 1, BGR = 1)



RGB interface (SS = 1, BGR = 1)

Instruction

Outline

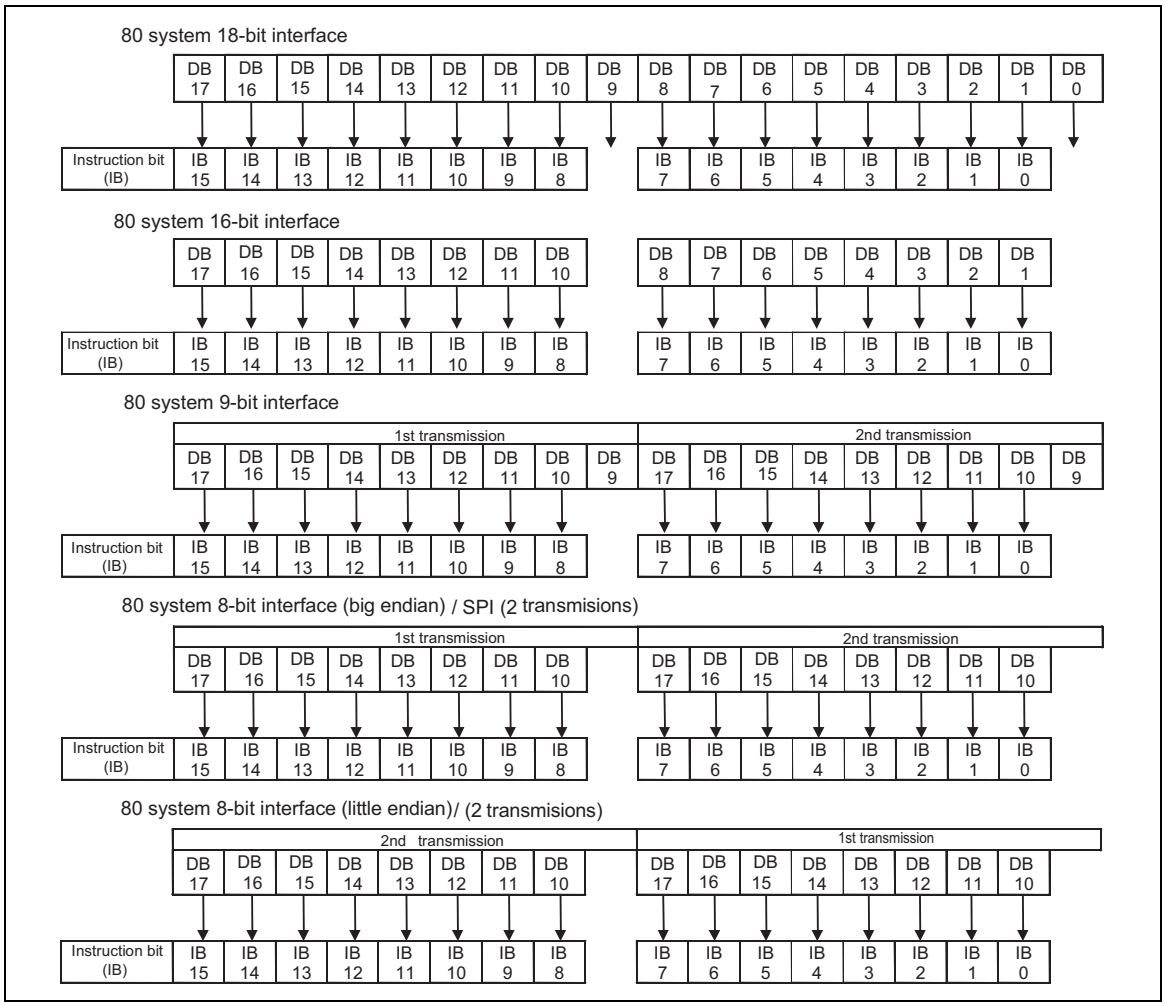
The HD66781 adapts an 18-bit bus architecture that enables high-speed interfacing with high-performance microcomputers. The HD66781 starts internal processing of 18/16/9/8/-bit data sent from external after storing control information in the instruction register (IR) and data register (DR). Since the internal operation of HD66781 is determined by signals sent from the microcomputer, register selection signal (RS), read/write signal (R/W), and internal 16-bit data bus signals (DB15 to DB0) are called instructions. GRAM is accessed through internal 18-bit data bus. The HD66781 has ten categories of instruction.

1. Specify index
2. Read status
3. Control display
4. Power management control
5. Graphics data processing
6. Set internal GRAM address
7. Transfer data to and from internal GRAM
8. Make an internal γ-adjustment
9. Control a panel
10. Control OSD display

Normally, the instruction to write data on GRAM is used the most often. The address of internal GRAM is updated automatically after data are written to the internal GRAM. With window address function, this reduces the amount of data transmission to minimum and thereby lightens the load on the program processed by the microcomputer. Since instructions are executed in 0 cycle, it is possible to write instructions consecutively.

Instruction data format

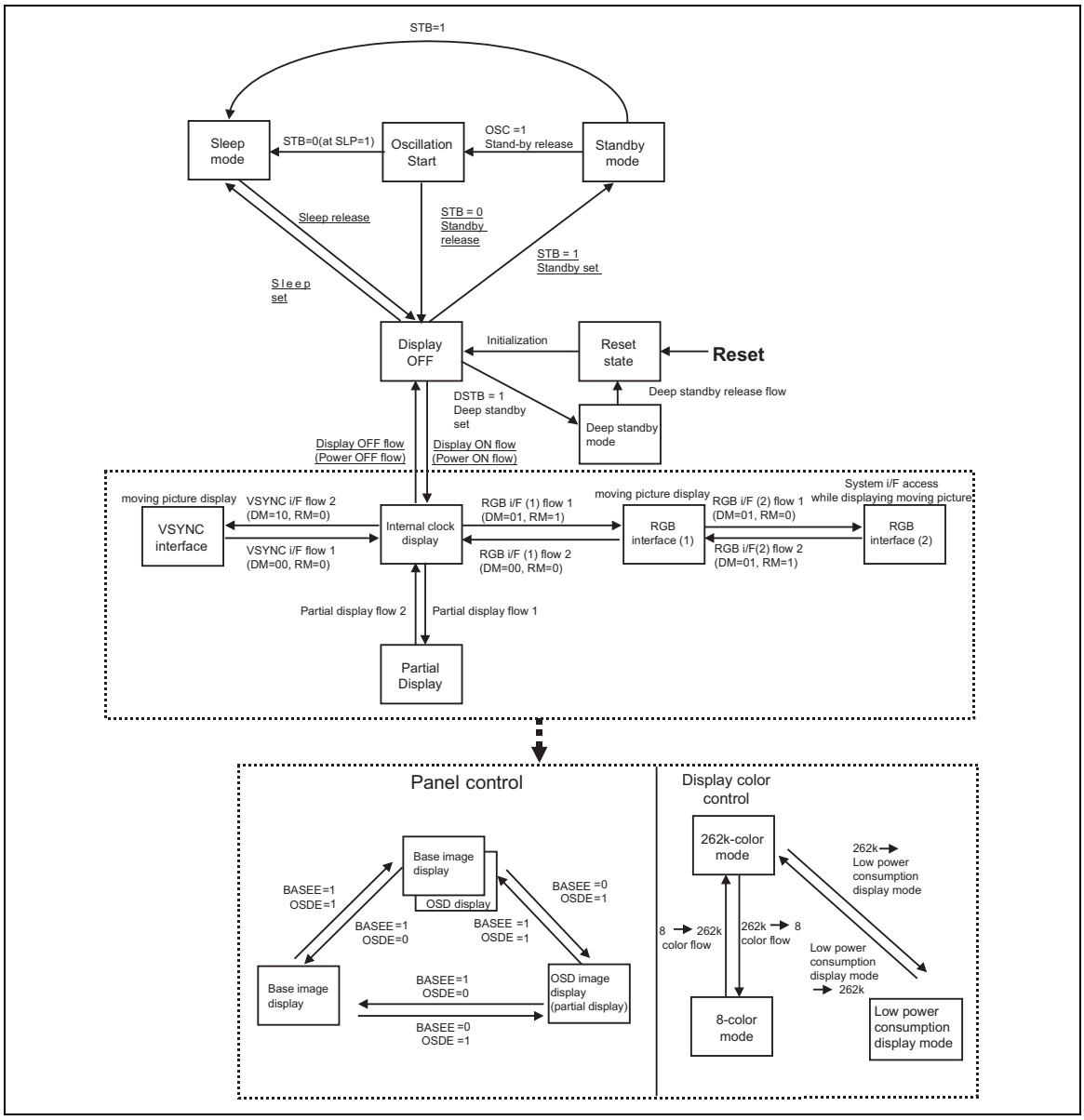
As the following figure shows, the assignment to the 16 instruction bits (IB15-0) varies according to the interface in use. An instruction must adopt the data format for each interface.



80-system interface instruction data format

Basic Operation modes

The basic operation modes of HD66781 and transitions between the modes are illustrated as follows. A transition between the modes must be made according to the instruction setting flow.



Basic operation modes

Instructions

The following are detail explanations of instructions with illustrations of instruction bits (IB15-0) assigned to each interface.

Index/Status/Display control instruction

Index (IR)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	*	*	*	*	*	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index instruction specifies the control register and the RAM control indexes that are accessed (R000h to R508h). The register number is set in binary from "000_0000_0000" to "101_0000_1000". Do not access to the registers and bits to which the index and the instruction bit are not assigned.

Status read (SR)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	0	0	0	0	0	0	0	0	L8	L7	L6	L5	L4	L3	L2	L1	L0

SR read the internal status of HD66781.

L[8:0]: Indicate the position of the raster-row driving liquid crystal.

Start Oscillation (R000h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1
R	1	0	0	0	0	0	1	1	1	1	0	0	0	0	1	0	0

The start oscillation instruction restarts the oscillator in a halt state during the standby mode. After executing this instruction, wait at least 10ms for stabilizing oscillation before issuing a next instruction. For details, see " Standby/Sleep mode" (p190.). The device code "0781"H is read out when this register is forced to read out.

Driver Output Control (R001h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	LTPS	0	0	0	SS	0	0	0	0	0	0	0	0

LTPS: Select the type of a panel. The output waveforms from SFTCLK1, 2 vary according to the setting of the panel. When LTPS = 0, a-Si TFT panel waveforms are output. When LTPS = 1, low temperature poly-Si TFT panel waveforms are output. See SFTCLK waveforms (p.67) for detail.

Make a setting for this register when D[1:0] = 2'h0.

SS: Select the correspondence between RAM write address and source driver output.
SS = "0": data written in H'00000 is output from S1.
SS = "1": data written in H'00000 is output from S720.
For details, see "GRAM Address Map".

By making settings for both SS and RGB bits, the assignment of RGB dots to the S1 ~ S720 pins is determined.

When SS = 0 and BGR = 0, R, G, B are assigned interchangeably in this order from S1 to S720.
When SS = 1 and BGR =1, R, G, B are assigned interchangeably in this order from S720 to S1.

Changes in the SS and BGR settings require RAM data rewrite.

LCD Driving Wave Control (R002h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	FLD1	FLD0	B/C	EOR	0	0	NW5	NW4	NW3	NW2	NW1	NW0

NW[5:0]: Specify "n", the number of raster-rows from 1 to 64, to alternate every n+1 raster-rows when C-pattern waveform is generated (B/C = 1).

EOR: When EOR = 1, alternations occur by applying EOR (exclusive OR) operation to an odd/even frame select signal and an n-raster-row inversion signal while a C-pattern waveform is generated (B/C =1). This instruction is used when liquid crystal alternate drive is not available due to a combination of numbers of LCD raster-rows and the value of "n". For details, see "n-raster-row inversion Alternate drive"(p.174).

B/C: When B/C =0, field alternating waveforms are generated. Alternation occurs every frame to drive liquid crystal. When B/C=1, alternation occurs every n raster-rows. For details, see the "n-raster-row Inversion alternating Drive" section.

FLD[1:0]: Specify the number of fields for n-field interlaced drive. For details, see the "Interlaced Drive"(p.175) section.

Table 5

FLD [1:0]	Numbers of fields
2'h0	Setting disabled
2'h1	1 field (= 1 frame)
2'h2	Setting disabled
2'h3	3 fields

Note 1) This instruction is not available with the external display interface. In the external display interface mode, make sure FLD[1:0] = 2'h1.

The following functions are not available during interlaced drive (FLD =2'h3).

Table 6

Unavailable functions when FLD = 2'h3
External display interface
OSD function (αblending)
Scroll function
Resizing function (vertical direction magnification)

Entry Mode 1 (R003h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	TRI	DFM	0	BGR	0	0	HWM	0	0	0	I/D1	I/D0	AM	0	OSD	ODF

This instruction is for writing data from the microcomputer to the internal GRAM of HD66781.

ODF: Set the format to write OSD data to the internal RAM. When ODF =0, assign transmission rate bits (α channel) to the LSB of RGB data. When ODF = 1, assign transmission rate bit (α channel) to the MSB. OSD bit must be "1" when writing OSD data.

Table 7 BGR = 0

OSD	ODF	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	*	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
1	0	R5	R4	R3	R2	R1	α2	G5	G4	G3	G2	G1	α1	B5	B4	B3	B2	B1	α0
1	1	α2	α1	α0	R4	R3	R2	R1	R0	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

Table 8 BGR =1

OSD	ODF	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	*	B5	B4	B3	B2	B1	B0	G5	G4	G3	G2	G1	G0	R5	R4	R3	R2	R1	R0
1	0	B5	B4	B3	B2	B1	α0	G5	G4	G3	G2	G1	α1	R5	R4	R3	R2	R1	α2
1	1	α0	α1	α2	B4	B3	B2	B1	B0	G4	G3	G2	G1	G0	R4	R3	R2	R1	R0

Table 9

α2	α1	α0	Transmission rate	Display screen
0	0	0	0%	Base picture display
0	0	1	-	Setting disabled
0	1	0	25%	Base picture (75%) + OSD image (25%) display
0	1	1	75%	Base picture (25%) + OSD image (75%) display
1	0	0	50%	Base picture (50%) + OSD image (50%) display
1	0	1	-	Setting disabled
1	1	0	100%	OSD image display
1	1	1	-	Setting disabled

OSD: Set RAM write data as OSD data. Set OSD =1, when writing OSD data. By setting OSD to 1, OSD data are written to the internal RAM according to the format set by ODF.

OSD =0: Write normal picture data (18-bit RGB) to RAM
OSD =1: Write OSD image data (18-bit (α+RGB)) to RAM

AM: Set the automatic updating method of address counter after data are written to GRAM.

AM =0, the address counter is updated in horizontal direction.
AM =1, the address counter is updated in vertical direction.

When a window-address range is specified, data are written in the window-address range specified within the GRAM in accordance with I/D1-0 and AM setting.

I/D[1:0]: I/D sets automatic increment (+1) and automatic decrement (-1) of address counter (AC) after data are written to GRAM. When I/D=0, the address counter is incremented or decremented in horizontal direction (lower address: AD7-0). When I/D =1, the address counter is incremented or decremented in vertical direction (upper address: AD16-8). The AM bit specifies the address transition direction when data are being written to GRAM.

HWM: When HWM =1, data are written to GRAM in high speed with low power consumption. In power saving high-speed write mode, the data in the horizontal line of rectangular area specified by the window address are stored in the line buffer and one-line data are written to GRAM at once. This minimizes the number of RAM access required to write data and thereby reduces power consumption.

When HWM =1, the data write in horizontal direction must be executed by line of the specified window-address range. If data write is terminated in the middle of the line, data in that line are not correctly written to GRAM.

Note 1) Insertion of dummy write is not required in high-speed write mode.
Note 2) Data in the buffer will be erased if RAM write is terminated in the middle of a line and other instruction set is executed.
Note 3) In the high-speed write mode, wait at least 2 write cycles (t_{cycw}) of the normal write mode after RAM write before making a transition from RAM write to index write.

BGR: Change the order of (R), (G), (B) dots to (B), (G), (R) when the dots are assigned to the 18-bit write data.

BGR=0, the dot order (R), (G), (B) is not changed when 18-bit data are written to GRAM.
BGR =1, the dot order changes from (R), (G), (B) to (B), (G), (R) when 18-bit data are written to GRAM. The assignment of α bit of OSD data is also changed.

DFM: Set the data format for 3-RAM-write 18-bit data transfers in 80-system 8-bit interface (big-endian) mode when IM3-0 = GND/GND/ Vcc1/Vcc1 in conjunction with TRI.

DFM =0, RGB 18-bit data are written to GRAM by byte-boundary 3 transfers.
DFM =1, RGB 18-bit data are written to GRAM by 3 x 6-bit transfer.

Set the data format for 2-RAM-write 18-bit data transfers in 80-system 16-bit interface mode when IM3-0 = GND/GND/Vcc1/GND in conjunction with TRI.

DFM =0, RGB 18-bit data are written to GRAM in the MSB format by 2 transfers.
DFM =1, RGB 18-bit data are written to GRAM in the LSB format by 2 transfers.

DFM must be set to 0, when not using 8- or16-bit interface.

TRI: Make the 3-RAM-write transfers available in 80-system 8-bit interface (big-endian) when IM3-0 = GND/GND/Vcc1/Vcc1.

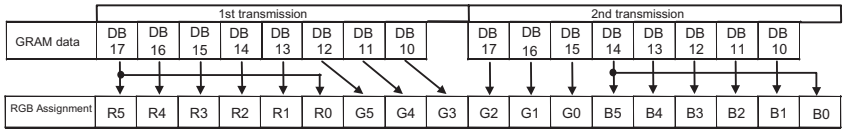
TRI =0, 16-bit RAM data are transferred in 2 transfers.
TRI =1, 18-bit RAM data are transferred in 3 transfers.

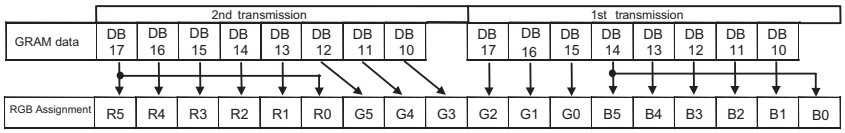
Make the 2-RAM-write transfers available in 80-system 16-bit interface (big-endian) when IM3-0 = GND/GND/Vcc1/GND.

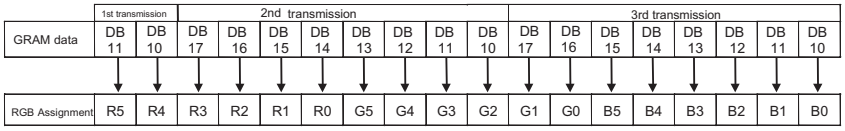
TRI =0, 16-bit RAM data are transferred in one transfer.
TRI =1, 18-bit RAM data are transferred in 2 transfers.

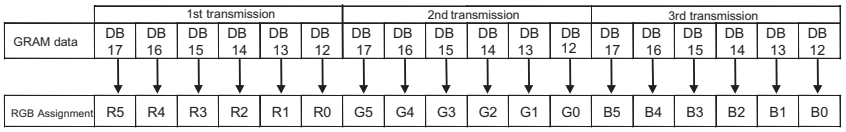
TRI must be set to 0, when not using 8- or 16-bit interface. During RAM read, set TRI = 0.

TRI	DFM	8-bit interface RAM write transmission formula
0	*	IM3-0 = (GND, GND, Vcc1, Vcc1) 80 system 8-bit interface(big endian) (2 transmissions/pixel) 65,536 colors
0	*	IM3-0 = (GND, Vcc1, Vcc1, Vcc1) 80 system 8-bit interface (little endian) (2 transmissions/pixel) 65,536 colors
1	0	IM3-0 = (GND, GND, Vcc1, Vcc1) 80 system 8-bit interface (3 transmissions/pixel) 262,144 colors
1	1	IM3-0 = (GND, GND, Vcc1, Vcc1) 80 system 8-bit interface (3 transmissions/pixel) 262,144 colors





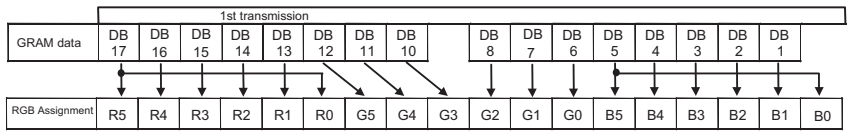


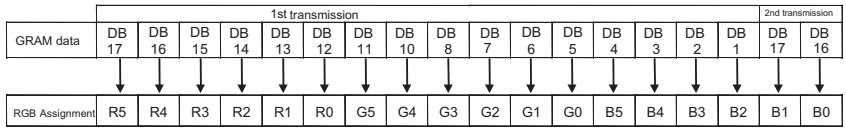


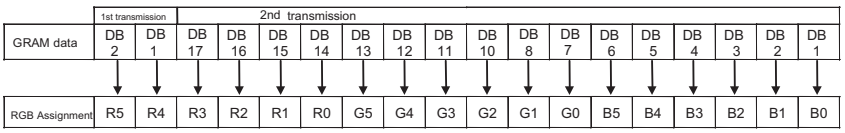
8-bit interface: RAM write transmission

Note 1) Instruction setting is transferred by 2 x 8-bit transmissions regardless of TRI and DFM settings.

TRI	DFM	16-bit interface RAM write transmission formula
0	*	80 system 16-bit interface (1 transmission/pixel) 65,536 colors
1	0	80 system 16-bit interface (2 transmissions/pixel) 262,144 colors
1	1	80 system 16-bit interface (2 transmissions/pixel) 262,144 colors







16-bit interface: RAM write transmission

Note 1) Instruction setting is transferred by 1 x 16-bit transmission regardless of TRI and DFM settings.

Direction Setting	I/D1-0 = "00" Horizontal: Decrement Vertical: Decrement	I/D1-0 = "01" Horizontal: Increment Vertical: Decrement	I/D1-0 = "10" Horizontal: Decrement Vertical: Increment	I/D1-0 = "11" Horizontal: Increment Vertical: Increment
AM = "0" Horizontal	17'00000 … 17'h19FEF	17'00000 … 17'h19FEF	17'00000 … 17'h19FEF	17'00000 … 17'h19FEF
AM = "1" Vertical	17'00000 … 17'h19FEF	17'00000 … 17'h19FEF	17'00000 … 17'h19FEF	17'00000 … 17'h19FEF

Address direction setting

Note 1) When a window-address range is specified, write operation is executed only within the specified window-address range of GRAM.

Resizing Control 1/2 (R004/R005h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	RCV1	RCV0	0	0	RCH1	RCH0	0	0	RSR1	RSR0
W	1	RSEV7	RSEV6	RSEV5	RSEV4	RSEV3	RSEV2	RSEV1	RSEV0	0	0	0	0	0	0	0	RSEH

RSR[1:0]: Set the contraction scale which is applied during RAM write. When the resizing scale is set, data are written to RAM according to this bit scale in horizontal and vertical directions. See the "Resizing Function" (p.105) section for details.

RCH[1:0]: RCH specifies the number of surplus pixels in the horizontal direction, which are made after resizing a picture. By specifying the number of surplus pixels, it is possible to disregard the surplus pixels when data are transferred. This instruction is only available with resizing function. Set RCH = 2'h0 when resizing function is not used (RSR = 2'h0).

RCV[1:0]: RCV specifies the number of surplus pixels in the vertical direction, which are made after resizing a picture. By specifying the number of surplus pixels, it is possible to disregard the surplus pixels when data are transferred. This instruction is only available with resizing function. Set RCV = 2'h0 when resizing function is not used (RSR = 2'h0).

RSEH: Set the magnifying scale in the horizontal direction of a picture. When the magnifying scale is set, data are written to RAM according to the bit scale in horizontal direction. See "Resizing Function" for details.

RSEV[7:0]: Set magnifying scale in the vertical direction of a picture. When the magnifying scale is set, the data in the internal RAM are magnified when displayed.

Note 1) When using picture magnification function, the picture resizing scale register (contraction) must be RSR1-0 = 2'h0.

Note 2) When using picture contraction function, the picture resizing scale (magnification) must be set RSEV7-0 = 8'h00, RSEH = 0.

Note 3) Base picture scrolling function and vertical-direction display magnification function cannot be used simultaneously.

Settings for resizing scales

Table 10 Resizing scale ratio setting (RSR)

RSR[1:0]	Resizing scale
2'h0	No resizing (x 1)
2'h1	x 1/2
2'h2	Setting disabled
2'h3	x 1/4

Table 11 Setting for the number of surplus pixel in the horizontal/vertical direction (RCV, RCH)

RCH [1:0] / RCV [1:0]	Number of pixel surplus in horizontal/vertical direction
2'h0	0 pixel
2'h1	1 pixel
2'h2	2 pixels
2'h3	3 pixels

Note 1) 1 pixel = 1RGB

Table 12 magnification in horizontal direction (RSEH)

RSEH	Magnification
2'h0	No resizing (x1)
2'h1	2 times (x2)

Table 13 BASE picture magnification in the vertical direction (RSEV)

RSEV [1:0]	Magnification
2'h0	No resizing (x1)
2'h1	2 times (x2)
2'h2	Setting disabled
2'h3	Setting disabled

Table 14 OSD image 1 magnification in the vertical direction (RSEV)

RSEV [3:2]	Magnification
2'h0	No resizing (x1)
2'h1	2 times (x2)
2'h2	4 times (x4)
2'h3	Setting disabled

Table 15 OSD image 2 magnification in the vertical direction (RSEV)

RSEV [5:4]	Magnification
2'h0	No resizing (x1)
2'h1	2 times (x2)
2'h2	4 times (x4)
2'h3	Setting disabled

Table 16 OSD image 3 magnification in the vertical direction (RSEV)

RSEV [7:6]	Magnification
2'h0	No resizing (x1)
2'h1	2 times (x2)
2'h2	4 times (x4)
2'h3	Setting disabled

Display Control 1 (R007h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	OSDE2	OSDE1	OSDE0	0	0	0	BASEE	0	0	0	DTE	0	0	D1	D0

D[1:0]: The graphics display is shown when D[1] = 1, and turned off when D[1] = 0. When setting D[1] = 0, the data are retained in GRAM. This means the graphics display is instantly shown when setting D[1] to 1. When D[1] is 0 (i.e. the display is not shown) all source outputs are set to the GND level. This reduces the charged/discharged current on LCD, which is generated during liquid crystal alternate drive.

When D= 2'b01, the display operation is being executed inside the HD66781 even while the external display is turned off. When D = 2'b00, both internal and external display operations are halted.

In combination with GON and DTE bits, D1-0 bits control ON/OFF of display. For details, see the "Instruction Setting"(p.185) section.

Table 17

D[1:0]	Source output	HD66781 internal operation	Gate control signal/Power supply IC, LCD panel control signal (FLM, CL1/SFTCLK1, 2, DCCLK, EQ)
2'h0	GND	Halt	Halt
2'h1	GND	Continue	Continue
2'h2	Non-lit display	Continue	Continue
2'h3	Display	Continue	Continue

Note 1) Data from the microcomputer can be written to GRAM irrespective of D bit setting.
Note 2) D = 2'h00 during the standby mode. In this case, the register setting of D bit is not changed.
Note 3) A picture displayed when D = 2'b11 is specified by the BASEE setting.

DTE: Control the DISPTMG output.

Table 18

DTE	DISPTMG
0	GND
1	Vcc1/GND

BASEE: Set display enable of a base image. The D-bit setting takes precedence over the BASEE-bit setting.

Table 19

D[1:0]	BASEE	Source Output (S1~S720)
2'h0	*	GND
2'h1	*	GND
2'h2	*	Non-lit level
2'h3	0	Non-lit display
	1	Display BASE image

Note 1) The source output at the "non-lit display" level is determined according to the PTS bit setting.
Note 2) Gate lines are scanned in the manner determined by the PTS bit setting during the non-lit display.

OSDE0: Display enable bit for OSD image 1.
OSDE1: Display enable bit for OSD image 2.
OSDE2: Display enable bit for OSD image 3.

OSDE0/OSDE1/OSDE2 = 0, the HD66781 does not display OSD images. Only base images are displayed.
OSDE0/OSDE1/OSDE2 = 1, the HD66781 displays OSD images according to the α channel bits in the pixel data of the OSD image.

When OSDE =1, while a base image is not displayed (BASEE =0), an OSD is displayed with 100% transmission rate.

Display Control 2 (R008h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0

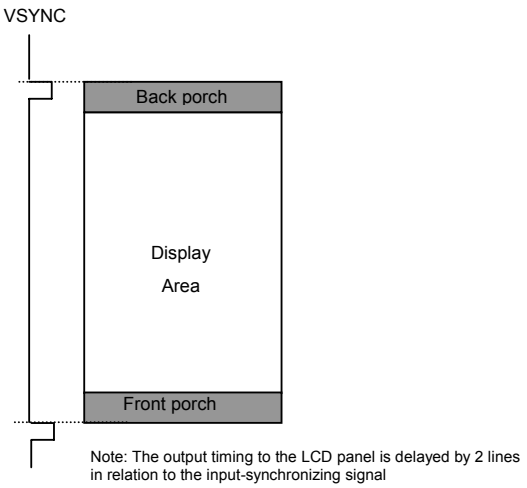
FP [3:0]: Set the number of lines for a front porch (a blank period made before the end of display).

BP [3:0]: Set the number of lines for a back porch (a blank period made after the beginning of display).

In the external display interface mode, a back porch (BP) period starts at the falling edge of VSYNC and display operation starts after the back porch period. A front porch (FP) period starts after the numbers of raster-rows set with NL bit are driven for display. After the front porch period, a blank period continues until the next VSYNC input.

Table 20

FP [3:0] BP [3:0]	Number of Front porch line Number of Back porch line
4'h0	Setting disabled
4'h1	Setting disabled
4'h2	2 lines
4'h3	3 lines
4'h4	4 lines
4'h5	5 lines
4'h6	6 lines
4'h7	7 lines
4'h8	8 lines
4'h9	9 lines
4'hA	10 lines
4'hB	11 lines
4'hC	12 lines
4'hD	13 lines
4'hE	14 lines
4'hF	Setting disabled



Set BP, FP, and MP within the range indicated below.

Table 21

Internal clock operation	**FLD = 2'h1**	BP ≥ 2 lines	FP ≥ 2 lines	FP+BP ≤ 16 lines
	FLD = 2'h3	BP = 3 lines	FP = 5 lines	
RGB interface		BP ≥ 2 lines	FP ≥ 2 lines	FP+BP ≤ 16 lines
VSYNC interface		BP ≥ 2 lines	FP ≥ 2 lines	FP+BP = 16 lines

Display Control 3 (R009h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	PTS2	PTS1	PTS0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0

ISC [3:0]: Specify the cycle to scan gate lines, when PTG bits set the scan mode in the non-display area to the interval scan mode. The scan cycle is always odd number of frames, and polarity inversion is applied each timing when gate lines are scanned.

Table 22

ISC [3:0]	Scan cycle	When (fFLM) = 60Hz
4'h0	Setting disabled	-
4'h1	3 frames	50ms
4'h2	5 frames	84ms
4'h3	7 frames	117ms
4'h4	9 frames	150ms
4'h5	11 frames	184ms
4'h6	13 frames	217ms
4'h7	15 frames	251ms
4'h8	17 frames	284ns
4'h9	19 frames	317ms
4'hA	21 frames	351ms
4'hB	23 frames	384ms
4'hC	25 frames	418ms
4'hD	27 frames	451ms
4'hE	29 frames	484ms
4'hF	31 frames	518ms

PTG [1:0]: Set the DISPTMG output to determine the gate bus line scan mode in non-display area. The setting is applied to all no-display areas and front/back porch periods of the entire panel.

Table 23

PTG[1:0]	DISPTMG output	Gate output in non-display area	Source output in non-display area
2'h0	Normal drive	Normal scan	PT setting
2'h1	GND	VGL (fixed)	PT setting
2'h2	Interval drive	Interval scan	PT setting
2'h3	Setting disabled	-	-

Note 1) Set alternating drive to frame cycle when using interval scan.

PTS [2:0]: Determine the kind of source outputs in the no-display area, which is applied to the front/back porch periods and non-display area of partial display. When PTS [2] =1, the grayscale voltage generating amplifiers are halted except those for the V0 and V63 levels during no-display area drive period to reduce power consumption.

Table 24

PTS[2:0]	Non-display source output		Non-display area	Non-display area
	Positive polarity	Negative polarity	Operation of grayscale amplifier	Step up clock frequency
3'h0	V63	V0	V0 to V63	DC0, DC1 setting
3'h1	Setting disabled	Setting disabled	-	DC0, DC1 setting
3'h2	GND	GND	V0 to V63	DC0, DC1 setting
3'h3	Hi-Z	Hi-Z	V0 to V63	DC0, DC1 setting
3'h4	V63	V0	V0, V63	DC0, DC1 setting x 1/2
3'h5	Setting disabled	Setting disabled	-	-
3'h6	GND	GND	V0, V63	DC0, DC1 setting x 1/2
3'h7	Hi-z	Hi-z	V0, V63	DC0, DC1 setting x 1/2

Note 1) Gate outputs in non-display area are controlled by the off-scan mode (PTG).

Note 2) Grayscale amplifier operation halt and slowdown of step-up clocks are applied to the non-display area.

Note 3) When DC[4:3]=2'h3, the frequency of step-up clocks in the non-display area are not slowed down half even if PTS[2:0] is set to 4, 6 or 7.

Display Control 4 (R00Bh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	FRC ON	D16 B	0	0	0	0	0	0	0	0	0	0	0	COL 1	COL 0

FRCON: Make a setting for the FRC mode. Control on and off of the FRC mode.

D16B: When FRCON=1, the FRC mode sets in. When COL[1:0]=2'h1 and the low-power display mode, where only 32 operational amplifiers are used, the FRC mode enables display with abundant colors. For details, see "low-power display mode"(p.169).

Set D16B to 1 when using a 16-bit interface (one-transfer 16-bit interface, 2-transfer 8-bit interface, 16-bit SPI, RGB interfaces).

Table 25

Interface mode	FRCON	D16B	Colors
18-bit, 16-bit x2, 9-bit x2, 8-bit x3, RGB 18-bit, 6-bit x3	0	*	262,144
	1	0	250,047
16-bit x1, 8-bit x2, SPI	0	*	65,536
	1	1	64,512

Note 1) When the FRC mode is on, do not switch the interface mode settings (M, TRI, D16B registers)

Note 2) When the FRC mode is on, 18-bit format data and 16-bit format data are not displayed simultaneously.

COL[1:0]: When COL=2'h1, 32 grayscale operational amplifiers are halted. When making a setting, it must follow the setting sequence in the "Low Power Consumption Display Mode" section.

When COL = 2'h2, 8-color mode sets in. When making a setting, it must follow the setting sequence in the "8-Color Display Mode" section. All operational amplifiers except V0 and V63 levels are halted for low power consumption display.

Table 26

COL[1:0]	Amplifiers in operation	Available colors for display	
		FRCON = 0	FRCON = 1
2'h0	64	262,144 colors/65,536 colors	-
2'h1	32	32,768 colors	250,047 colors/64,512 colors
2'h2	2	8 colors	-
2'h3	Setting disabled	Setting disabled	Setting disabled

Note 1) When COL[1:0] =2'h1 and FRCON = 0, do not write data that correspond to the grayscale levels the amplifiers of which are halted.

Table 27 grayscale level amplifiers in operation (when REV=0)

amplifier	COL[1:0]			GRAM data RGB	
	2'h0	2'h1	2'h2		
V0	*	*	*	6'h00	6'h3F
V1	*			6'h01	6'h3E
V2	*	*		6'h02	6'h3D
V3	*			6'h03	6'h3C
V4	*	*		6'h04	6'h3B
V5	*			6'h05	6'h3A
V6	*	*		6'h06	6'h39
V7	*			6'h07	6'h38
V8	*	*		6'h08	6'h37
V9	*			6'h09	6'h36
V10	*	*		6'h0A	6'h35
V11	*			6'h0B	6'h34
V12	*	*		6'h0C	6'h33
V13	*			6'h0D	6'h32
V14	*	*		6'h0E	6'h31
V15	*			6'h0F	6'h30
V16	*	*		6'h10	6'h2F
V17	*			6'h11	6'h2E
V18	*	*		6'h12	6'h2D
V19	*			6'h13	6'h2C
V20	*	*		6'h14	6'h2B
V21	*			6'h15	6'h2A
V22	*	*		6'h16	6'h29
V23	*			6'h17	6'h28
V24	*	*		6'h18	6'h27
V25	*			6'h19	6'h26
V26	*	*		6'h1A	6'h25
V27	*			6'h1B	6'h24
V28	*	*		6'h1C	6'h23
V29	*			6'h1D	6'h22
V30	*	*		6'h1E	6'h21
V31	*			6'h1F	6'h20

amplifier	COL[1:0]			GRAM data RGB	
	2'h0	2'h1	2'h2		
V32	*			6'h20	6'h1F
V33	*	*		6'h21	6'h1E
V34	*			6'h22	6'h1D
V35	*	*		6'h23	6'h1C
V36	*			6'h24	6'h1B
V37	*	*		6'h25	6'h1A
V38	*			6'h26	6'h19
V39	*	*		6'h27	6'h18
V40	*			6'h28	6'h17
V41	*	*		6'h29	6'h16
V42	*			6'h2A	6'h15
V43	*	*		6'h2B	6'h14
V44	*			6'h2C	6'h13
V45	*	*		6'h2D	6'h12
V46	*			6'h2E	6'h11
V47	*	*		6'h2F	6'h10
V48	*			6'h30	6'h0F
V49	*	*		6'h31	6'h0E
V50	*			6'h32	6'h0D
V51	*	*		6'h33	6'h0C
V52	*			6'h34	6'h0B
V53	*	*		6'h35	6'h0A
V54	*			6'h36	6'h09
V55	*	*		6'h37	6'h08
V56	*			6'h38	6'h07
V57	*	*		6'h39	6'h06
V58	*			6'h3A	6'h05
V59	*	*		6'h3B	6'h04
V60	*			6'h3C	6'h03
V61	*	*		6'h3D	6'h02
V62	*			6'h3E	6'h01
V63	*	*	*	6'h3F	6'h00

*: amplifier in operation

External Display interface Control 1 (R00Ch)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	RM	0	0	DM [1]	DM [0]	0	0	RIM [1]	RIM [0]

RIM[1:0] Make settings for the RGB interface mode when the RGB interface is selected with DM and RM bits. The setting must be made before the display through an external display interface. Do not make changes to the setting during display.

Table 28

RIM[1:0]	RGB interface mode	Colors
2'h0	18-bit RGB interface (1 transmission/pixel)	262,144
2'h1	16-bit RGB interface (1 transmission/pixel)	65,536
2'h2	6-bit RGB interface (3 transmission/pixel)	262,144
2'h3	Setting disabled	-

Note 1) The instruction register setting is made only through a system interface.

Note 2) Data transfer and DOTCLK input must be by the RGB unit when a 6-bit RGB interface is selected.

DM[1:0]: Set a display operation mode. An interface for display operation is selected by the DM setting. DM allows switching between the internal clock operation mode and the external display interface mode. Do not try to switch between the external interface modes (RGB-I/F and VSYNC-I/F).

Table 29

DM[1:0]	Display operation interface
2'h0	Internal clock operation
2'h1	RGB interface
2'h2	VSYNC interface
2'h3	Setting disabled-

RM: Set a RAM access interface. RAM access is made only through the interface specified by the RM setting. Set RM to 1 when writing display data through the RGB interface. This setting is valid irrespective of the display operation mode. Changes in display data can be made by setting RM to 0, which enables RAM data overwrite through a system interface, even while the screens are displayed through the RGB interface mode.

Table 30

RM	Display operation interface
0	Internal clock operation/VSYNC interface
1	RGB interface

As the following table shows, an optimum interface is selected for the kind of display by the external display interface control setting.

Write display data during moving picture display (through RGB and VSYNC interfaces) in the high-speed write mode (HWM=1), which enables high-speed RAM access with low power consumption.

Table 31

Kind of Display	Operation mode	RAM access setting (RM)	Display operation mode (DM)
still picture	internal clock operation only	system interface (RM = 0)	internal clock operation (DM = 2'h0)
moving picture	RGB interface (1)	RGB interface (RM = 1)	RGB interface (DM = 2'h1)
Write over still picture area during moving picture display	RGB interface (2)	system interface (RM = 0)	RGB interface (DM = 2'h1)
moving picture	VSYNC interface	system interface (RM = 0)	VSYNC interface (DM = 2'h2)

Note 1) The instruction register settings are made only through a system interface.
Note 2) No switching between the RGB and VSYNC interfaces is made.
Note 3) No change in the settings of RGB interface mode (RIM) is made during the RGB interface operation.
Note 4) See "External Display Interface" for reference to the transition flows between the modes.
Note 5) Use the RGB and VSYNC interfaces in the high-speed write mode (HWM =1).

Internal clock mode: All display operations are controlled by signals generated by the internal clock in internal clock operation mode. All inputs through the external display interface are invalid. The internal RAM is accessible only through a system interface.

RGB interface mode (1): Display operation is controlled by the frame synchronizing clock (VSYNC), line synchronizing signal (VSYNC), and dot clock (DOTCLK) in the RGB interface mode. These signals must be supplied throughout the display operation in this mode.

All display data are stored in the internal RAM, transmitted through DB17-0 bits by pixel. The combination with the window address function enables simultaneous display of both moving picture areas and the internal RAM area. The data are transmitted only when the screen is being updated, thereby reducing the overall data transmission to minimum.

The periods of the front (FP) and back (BP) porches and the display period (NL) are automatically generated in the HD66782 by counting the clock of line synchronizing signal (HSYNC) in accordance to the frame synchronizing signal (VSYNC). Transmit pixel data through DB17-0 bits in accordance with the aforementioned setting.

RGB interface mode (2): When RGB-I/F is selected, RAM data are changeable through the system interface. This write operation must be performed while display data are not being transmitted through the RGB-I/F (ENABLE = High). When reverting from the system interface mode to the data transmission through the RGB interface, make a new setting for the address set and index (R202h) after changing the aforementioned settings.

VSYNC interface mode: The internal display operation is synchronized with the frame-synchronizing signal (VSYNC) in the VSYNC interface mode. By writing data to RAM at a fixed speed on the falling edge of VSYNC, it enables moving pictures display with a system interface. In this case, there are some constraints in the RAM write speed and methods. For details, see "External Display Interface" (p.139).

In the VSYNC-I/F mode, only VSYNC input is valid. Other input signals for the external display interface are invalid.

The front porch (FP), back porch (BP) periods and display period (NL) are automatically generated in accordance to the frame synchronizing signal (VSYNC) according to the register setting of HD66781.

Frame Cycle Control (R00Dh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	DIVI1	DIVI0	0	0	0	RTNI 4	RTNI 3	RTNI 2	RTNI 1	RTNI 0

RTNI[4:0]: Set IH (line) period.

DIVI[1:0]: Set the division ratio of clocks for internal operations (DIV1-0). The internal operations are executed by the clocks, the frequency of which is divided according to the DIV1-0 setting. When changing the number of raster-rows to drive, adjust the frame frequency too. For details, see “Frame Frequency Adjustment Function”(p.178).

Table 32

RTNI[3:0]	clocks per line
5’h00	Setting disabled
:	:
5’h0F	Setting disabled
5’h10	16 clocks
5’h11	17 clocks
5’h12	18 clocks
5’h13	19 clocks
5’h14	20 clocks
5’h15	21 clocks
5’h16	22 clocks
5’h17	23 clocks
5’h18	24 clocks
5’h19	25 clocks
5’h1A	26 clocks
5’h1B	27 clocks
5’h1C	28 clocks
5’h1D	29 clocks
5’h1E	30 clocks
5’h1F	31 clocks

DIVI[1:0]	division ratio	internal operation clock frequency
2’h0	1/1	fosc / 1
2’h1	1/2	fosc / 2
2’h2	1/4	fosc / 4
2’h3	1/8	fosc / 8

Note 1) fosc : R-C oscillation frequency

Formula for frame frequency

$$\text{frame frequency} = \frac{fosc}{\text{Number of clock per line x division ratio x (Line +FP+BP)}} \quad [Hz]$$

fosc : R-C oscillation frequency

Line : Number of drive raster-rows (NL bit)

division ration : DIVI bit

clocks per line : RTNI bit

External Display Interface Control 2 (R00Eh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	DIVE 1	DIVE 0	0	RTNE 6	RTNE 5	RTNE 4	RTNE 3	RTNE 2	RTNE 1	RTNE 0

RTNE[6:0]: Specify the number of clocks for internal operation per 1H (line). Set the value of the number of DOTCLK input in 1H period, divided by the division ratio.

DIVE[1:0]: Set the internal division ratio of DOTCLK (DIVE). The internal operation is executed according to the clocks divided by the division ratio set by DIVE.

Table 33

RTNE[6:0]	Clocks per line
7'h00	Setting disabled
:	:
7'h0F	Setting disabled
7'h10	16 clocks
7'h11	17 clocks
7'h12	18 clocks
:	:
7'h7D	125 clocks
7'h7E	126 clocks
7'h7F	127 clocks

DIVE[1:0]	Division	Internal operation clock frequency
2'h0	Setting disabled	
2'h1	1/4	fdotclk / 4
2'h2	1/8	fdotclk / 8
2'h3	1/16	fdotclk / 16

fdotclk: DOTCLK frequency

External Display Interface Control 3 (R00Fh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL

DPL: Specify the polarities of signals on DOTCLK pin.

DPL=0: Input data on a rising edge of DOTCLK.
DPL=1: Input data on a falling edge of DOTCLK.

EPL: Specify the polarities of signals on ENABLE pin.

EDL = 0 Data are written to PD17 to PD 0 when ENABLE = 0. No data are written when ENABLE = 1.
EDL = 1 Data are written to PD17 to PD 0 when ENABLE = 1. No data are written when ENABLE = 0.

HSPL: Specify the polarities of signals on HSYNC pin.

HSPL=0: Low active.
HSPL=1: High active.

VSPL: Specify the polarities of signals on VSYNC pin.

VSPL=0: Low active.
VSPL=1: High active.

Gate Driver/LTPS LCD Panel Interface Control 1 (R010h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	FWI 4	FWI 3	FWI 2	FWI 1	FWI 0	0	0	0	0	0	FTI2	FTI1	FTI0

FTI[2:0]: FTI bits specify the rising position of FLM during display operation with internal clocks (DM = 2'h0 or 2'h2) when LTPS = 1. The setting of this register is invalid when LTPS = 0. In this case, the rising position of FLM is at a reference point.

FWI[4:0]: FWI bits specifies the width of "High" of FLM during display operation with internal clocks (DM = 2'h0 or 2'h2) when LTPS = 1. The setting of this register is invalid when LTPS = 0. In this case, the width of "High" of FLM is 1H.

See the figures (page 66, 67) with regard to how the signal waveform of each gate driver and LTPS LCD panel interface are controlled by these settings.

Table 34

FTI[2:0]	FLM Rising position
2'h0	0 clock
2'h1	1 clock
2'h2	2 clocks
2'h3	3 clocks

FWI[4:0]	FLM "High" width
5'h00	0 clock
5'h01	1 clock
5'h02	2 clocks
5'h03	3 clocks
:	:
5'h1D	29 clocks
5'h1E	30 clocks
5'h1F	31 clocks

Note 1) The clocks in the tables are measured from the reference point. The reference point is the position where SFTCLK rises when the rising position of SFTCLK is set to 0 clock.

Gate Driver/LTPS LCD Panel Interface Control 2 (R011h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	SWI 4	SWI 3	SWI 2	SWI 1	SWI 0	0	0	0	0	0	0	STI1	STI0

STI[1:0]: STI bits specifies the rising position of SFTCLK1/2 during display operation with internal clocks (DM = 2'h0 or 2'h2) when LTPS = 1. The setting of this register is invalid when LTPS = 0. In this case, the rising position of CL1 is 8 clocks away from a reference point.

SWI[4:0]: SWI bits specifies the width of "High" of SFTCLK1/2 during display operation with internal clocks (DM = 2'h0 or 2'h2) when LTPS = 1. The setting of this register is invalid when LTPS = 0. In this case, the falling position of CL1 is at a reference point.

See the figures (page 66, 67) with regard to how the signal waveform of each gate driver and LTPS LCD panel interface are controlled by these settings.

Table 35

STI[1:0]	CL1/SFTCLK1, 2 Rising position
2'h0	0 clock
2'h1	1 clock
2'h2	2 clocks
2'h3	3 clocks

SWI[4:0]	CL1/SFTCLK1, 2 "High" width
5'h00	0 clock
5'h01	1 clock
5'h02	2 clocks
5'h03	3 clocks
:	:
5'h1D	29 clocks
5'h1E	30 clocks
5'h1F	31 clocks

Note 1) The clocks in the tables are measured from a reference point. The reference point is the position where SFTCLK rises when the rising position of SFTCLK is set to 0 clock.

Gate Driver/LTPS LCD Panel Interface Control 3 (R012h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SDTI 1	SDTI 0

SDTI[1:0]: Specify the delay from a reference point of the source output during display operation with internal clocks (DM = 2'h0 or 2'h2).

See the figures (page 66, 67) with regard to how the signal waveform of each gate driver and LTPS LCD panel interface are controlled by these settings.

Table 36

SDTI[1:0]	Source output delay
2'h0	1 clock
2'h1	2 clocks
2'h2	3 clocks
2'h3	4 clocks

Note 1) The clocks in the tables are measured from a reference point. The reference point is the position where SFTCLK rises when the rising position of SFTCLK is set to 0 clock.

Gate Driver/LTPS LCD Panel Interface Control 4 (R013h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	DPWI4	DPWI3	DPWI2	DPWI1	DPWI0	0	0	0	0	0	0	DPTI1	DPTI0

DPTI[1:0]: Specify the rising position of DISPTMG during display operation with internal clocks (DM = 2'h0 or 2'h2).

DPWI[4:0]: DPWI bits specifies the width of "High" of DISPTMG during display operation with internal clocks (DM = 2'h0 or 2'h2) when LTPS = 1. The setting of this register is invalid when LTPS = 0. In this case, the falling position of CL1 is at a reference point.

See the figures (page 66, 67) with regard to how the signal waveform of each gate driver and LTPS LCD panel interface are controlled by these settings.

Table 37

DPTI[1:0]	DISPTMG Rising position
2'h0	0 clock
2'h1	1 clock
2'h2	2 clocks
2'h3	3 clocks

DPWI[4:0]	DISPTMG "High" width
5'h00	0 clock
5'h01	1 clock
5'h02	2 clocks
5'h03	3 clocks
:	:
5'h1D	29 clocks
5'h1E	30 clocks
5'h1F	31 clocks

Note 1) The clocks in the tables are measured from a reference point. The reference point is the position where SFTCLK rises when the rising position of SFTCLK is set to 0 clock.

Note 2) The gate non-overlap period can be set to 0 when DPTI = "2'h0" and DPWI is set to the number of clocks more than that of the 1H period.

Gate Driver/LTPS LCD Panel Interface Control 5 (R015h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	EQWI1	EQWI0	0	0	0	0	0	0	0	0

EQWI[1:0]: Specify the width of "High" of EQ during display operation with internal clocks (DM = 2'h0 or 2'h2).

See the figures (page 66, 67) with regard to how the signal waveform of each gate driver and LTPS LCD panel interface are controlled by these settings. Also see "Equalizing Function" for details on equalization.

Table 38

EQWI[1:0]	EQ "High" width
2'h0	0 clock
2'h1	1 clock
2'h2	2 clocks
2'h3	3 clocks

Note 1) The clocks in the tables are measured from the source output alternating point.

Gate Driver/LTPS LCD Panel Interface Control 6 (R016h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	FWE5	FWE4	FWE3	FWE2	FWE1	FWE0	0	0	0	0	0	FTE2	FTE1	FTE0

FTE[2:0]: FTE bits specifies the rising position of FLM during display operation with DOTCLK (DM = 2'h1) when LTPS = 1. The setting of this register setting is invalid when LTPS = 0. In this case, the rising position of FLM is at a reference point.

FWE[5:0]: FWE bits specifies the width of "High" of FLM during display operation with DOTCLK (DM = 2'h1) when LTPS = 1. The register setting is invalid when LTPS = 0. In this case, the width of "High" of FLM is 1H.

See the figures (page 66, 67) with regard to how the signal waveform of each gate driver and LTPS LCD panel interface are controlled by these settings.

Table 39

FTE[2:0]	FLM Rising position
3'h0	0 clock
3'h1	1 clock
3'h2	2 clocks
3'h3	3 clocks
3'h4	4 clocks
3'h5	5 clocks
3'h6	6 clocks
3'h7	7 clocks

FWE[5:0]	FLM "High" width
6'h00	0 clock
6'h01	1 clock
6'h02	2 clocks
6'h03	3 clocks
:	:
6'h3D	61 clocks
6'h3E	62 clocks
6'h3F	63 clocks

Note 1) The clocks in the tables are DOTCLK / division ratio for the 1H period, measured from a reference point. The reference point is the position where SFTCLK rises when the rising position of SFTCLK is set to 0 clock.

Gate Driver/LTPS LCD Panel Interface Control 7 (R017h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	SWE5	SWE4	SWE3	SWE2	SWE1	SWE0	0	0	0	0	0	STE2	STE1	STE0

STE[2:0]: STE bits specifies the rising position of SFTCLK1/2 during display operation with DOTCLK (DM = 2'h1) when LTPS = 1. The register setting is invalid when LTPS = 0. In this case, the rising position of CL1 is 8 clocks away from a reference point.

SWE[5:0]: SWE bits specifies the width of "High" of SFTCLK1/2 during display operation with DOTCLK (DM = 2'h1) when LTPS = 1. The register setting is invalid when LTPS = 0. In this case, the falling position of CL1 is at a reference point.

See the figures (page 66, 67) with regard to how the signal waveform of each gate driver and LTPS LCD panel interface are controlled by these settings.

Table 40

STE[2:0]	CL1/SFTCLK1,2 Rising position
3'h0	0 clock
3'h1	1 clock
3'h2	2 clocks
3'h3	3 clocks
3'h4	4 clocks
3'h5	5 clocks
3'h6	6 clocks
3'h7	7 clocks

SWE[5:0]	CL1/SFTCLK1,2 "High" width
6'h00	0 clock
6'h01	1 clock
6'h02	2 clocks
6'h03	3 clocks
:	:
6'h3D	61 clocks
6'h3E	62 clocks
6'h3F	63 clocks

Note 1) The clocks in the tables are DOTCLK / division ratio for the 1H period, measured from a reference point. The reference point is the position where SFTCLK rises when the rising position of SFTCLK is set to 0 clock.

Gate Driver/LTPS LCD Panel Interface Control 8 (R018h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	SDTE 2	SDTE 1	SDTE 0

SDTE[2:0]: Specify the delay from a reference point of the source output during display operation with DOTCLK (DM = 2'h1).

See the figures (page 66, 67) with regard to how the signal waveform of each gate driver and LTPS LCD panel interface are controlled by these settings.

Table 41

SDTE[2:0]	Source output delay
3'h0	1 clock
3'h1	2 clocks
3'h2	3 clocks
3'h3	4 clocks
3'h4	5 clocks
3'h5	6 clocks
3'h6	7 clocks
3'h7	Setting disabled

Note 1) The clocks in the tables are DOTCLK / division ratio for the 1H period, measured from a reference point. The reference point is the position where SFTCLK rises when the rising position of SFTCLK is set to 0 clock.

Gate Driver/LTPS LCD Panel Interface Control 9 (R019h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	DPWE5	DPWE4	DPWE3	DPWE2	DPWE1	DPWE0	0	0	0	0	0	DPTE2	DPTE1	DPTE0

DPTE[2:0]: Specify the rising position of DISPTMG during display operation with DOTCLK (DM = 2'h1).

DPWE[5:0]: DPWE specifies the width of "High" of DISPTMG during display operation with DOTCLK (DM = 2'h1) when LTPS = 1. The register setting is invalid when LTPS = 0. In this case, the falling position of CL1 is at a reference point.

See the figures (page 66, 67) with regard to how the signal waveform of each gate driver and LTPS LCD panel interface are controlled by these settings.

Table 42

DPTE[2:0]	DISPTMG Rising position
3'h0	0 clock
3'h1	1 clock
3'h2	2 clocks
3'h3	3 clocks
3'h4	4 clocks
3'h5	5 clocks
3'h6	6 clocks
3'h7	7 clocks

DPWE[5:0]	DISPTMG "High" width
6'h00	0 clock
6'h01	1 clock
6'h02	2 clocks
6'h03	3 clocks
:	:
6'h3D	61 clocks
6'h3E	62 clocks
6'h3F	63 clocks

Note 1) The clocks in the tables are DOTCLK / division ratio for the 1H period, measured from a reference point. The reference point is the position where SFTCLK rises when the rising position of SFTCLK is set to 0 clock.

Note 2) The gate non-overlap period can be set to 0 when DPTI = "2'h0" and DPWI is set to the number of clocks more than that of the 1H period.

Gate Driver/LTPS LCD Panel Interface Control 10 (R01Bh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	EQWE2	EQWE1	EQWE0	0	0	0	0	0	0	0	0

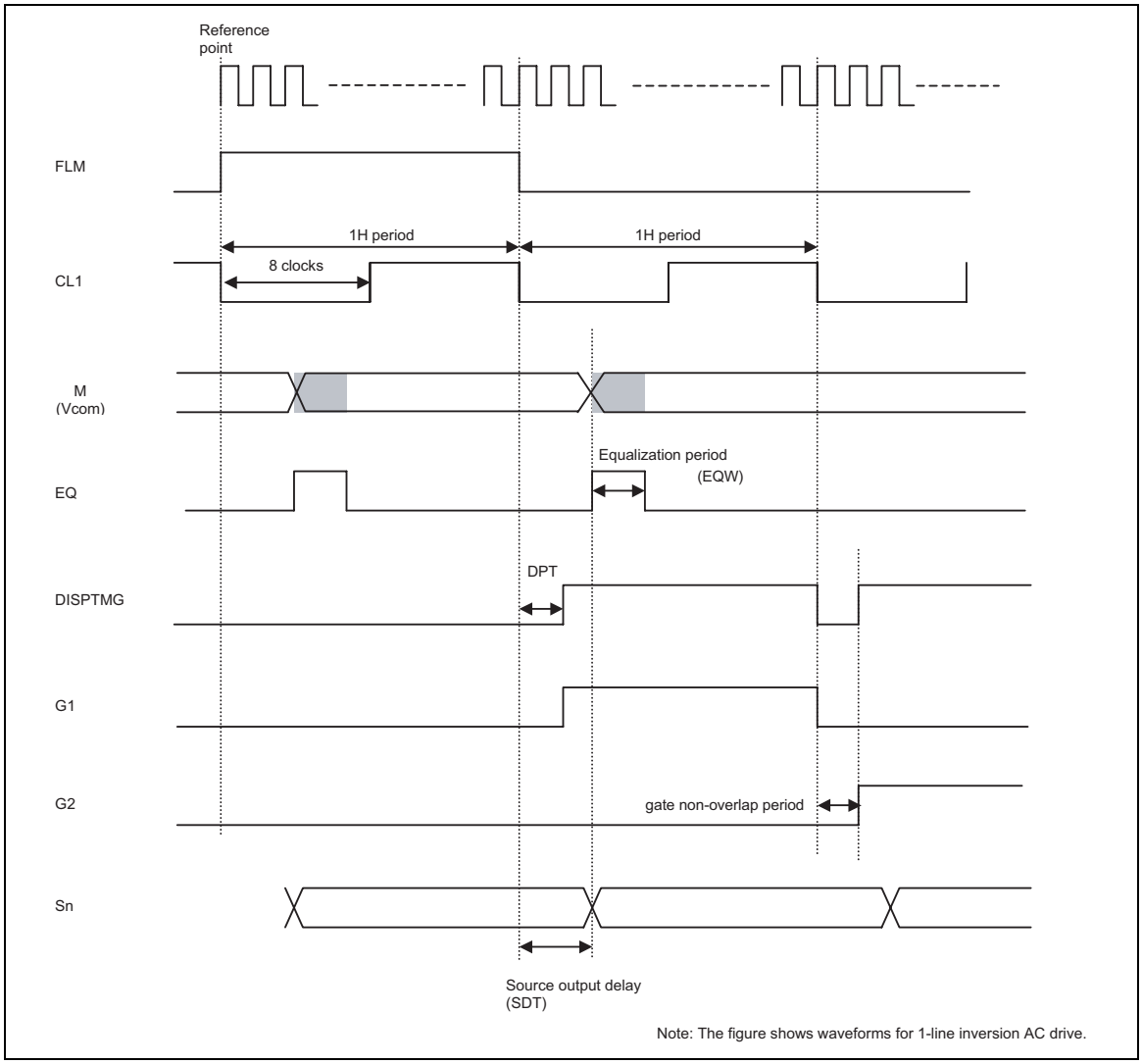
EQWE[2:0]: Specify the width of "High" of EQ DISPTMG during display operation with DOTCLK (DM = 2'h1).

See the figures (page 66, 67) with regard to how the signal waveform of each gate driver and LTPS LCD panel interface are controlled by these settings. Also see "Equalizing Function" for details on equalization.

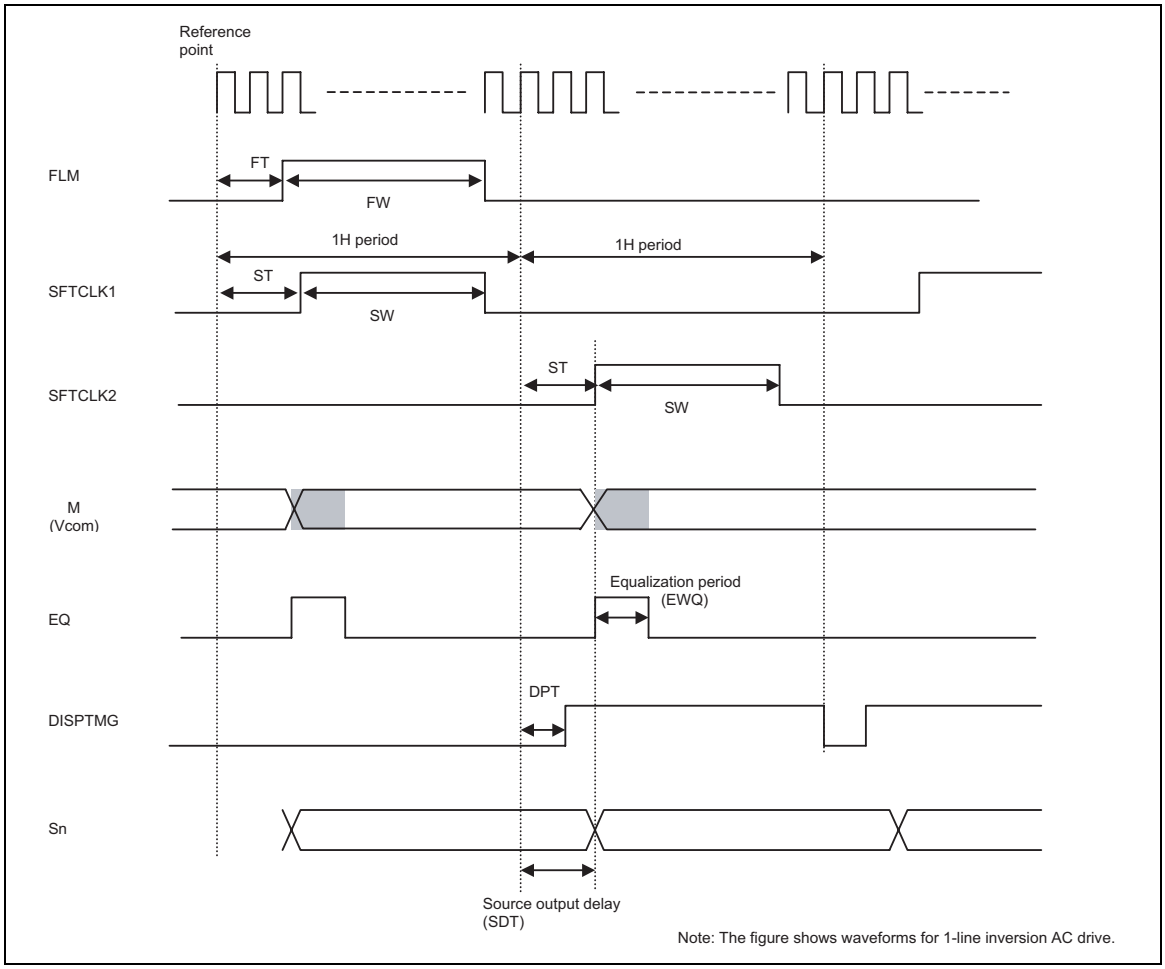
Table 43

EQWE[2:0]	EQ "High" width
3'h0	0 clock
3'h1	1 clock
3'h2	2 clocks
3'h3	3 clocks
3'h4	4 clocks
3'h5	5 clocks
3'h6	6 clocks
3'h7	7 clocks

Note 1) The clocks in the tables are DOTCLK / division ratio for the 1H period, measured from the source output change.



Output waveforms of a-Si TFT panel (LTPS = 0)



Output waveforms of low-temperature poly-Si TFT panel (LTPS = 1)

Power control 1 (R100h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	DC 4	DC 3	0	0	0	SAP 2	SAP 1	SAP 0	0	AP 2	AP 1	AP 0	0	DS TB	SLP	STB

STB: When STB = 1, the HD66781 enters into the standby mode. In the standby mode, display operation is completely halted, and all internal operations including the internal R-C oscillator and reception of external clock pulse, are halted. Only instructions to release from the standby mode (STB = 0) and to start oscillation are accepted during the standby mode.

In the standby mode, a serial transfer to the gate driver/power supply IC cannot be made and it requires retransfer after release from the standby mode. Also in the standby mode, any change in the GRAM data or instruction setting cannot be made, but GRAM data are retained.

SLP: When SLP = 1, the HD66781 enters into the sleep mode. In the sleep mode, internal display operation is halted except the R-C oscillator to reduce current consumption. No change is made to the GRAM data or instructions during the sleep mode, and the GRAM data and the instructions are retained.

DSTB: When DSTB = 1, the HD66781 enters into the deep standby mode, where the power supply for the internal logic is turned off to save more power than the standby mode. The GRAM data and the instruction setting are destroyed in the deep standby mode and it requires resetting after release from the deep standby mode. Also in the deep standby mode, a serial transfer to the gate driver cannot be made and it requires a retransfer after the release from the deep standby mode.

AP[2:0]: Adjust the amount of constant current in the operational amplifier in the liquid crystal drive power supply. When the amount of constant current is set large, the liquid crystal drive capacity will be enhanced and the display quality will improve, while the current consumption will increase. Select an optimum amount of current taking both the display quality and the current consumption into account. When no display operation is required, set AP[2:0] = "3'h0" to halt the operation of operational amplifier and step-up circuits to reduce the current consumption. Also if AP[2:0] is set to other than 0, the clock for the step-up circuit DCCLK is output.

SAP[2:0]: Adjust the amount of constant current in the operational amplifier of source driver. When the amount of constant current is set large, the liquid crystal drive capacity is enhanced and the display quality will improve, while the current consumption will increase. Select an optimum amount of current taking both the display quality and the current consumption into account. When no display operation is required, set SAP[2:0] = "3'h0" to halt the operation of operational amplifier and step-up circuits to reduce the current consumption.

DC[4:3]: Select the frequency of clocks for the step-up circuit (DCCLK). If the DCCLK frequency is set high, display quality is enhanced due to increased drive capacity of step-up circuit, while power consumption will be increased. Make an adjustment taking both display quality and power consumption into consideration.

Note: The AP[2:0] in the above description is the instruction bits for gate driver/power supply IC. The instruction setting in the AP[2:0] must be transferred to the gate driver/power supply IC before an instruction is executed. For details, see "Gate driver/power supply IC Serial Transfer".

Table 44 SAP setting

SAP[2:0]	Current in the operational amplifier
3'h0	operation halt : op-amp, step-up circuit
3'h1	op-amp constant current flow rate : 0.65
3'h2	op-amp constant current flow rate : 0.80
3'h3	op-amp constant current flow rate : 1.00
3'h4	op-amp constant current flow rate : 1.35
3'h5	op-amp constant current flow rate : 1.60
3'h6	Setting disabled
3'h7	Setting disabled

DC setting

DC[4:3]	DCCLK frequency
2'h0	Fosc / 4
2'h1	fosc / 8
2'h2	fosc / 16
2'h3	fosc / 32

Note 1) The amount of current in the above table is shown as a ratio against that of SAP[2:0] = 3'h3 as 1.

Gate Driver/ Power Supply IC Interface Control 1 (R110h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	TE	0	0	0	0	0	IDX 2	IDX 1	IDX 0
R	1	0	0	0	0	0	0	0	TE	0	0	0	0	0	IDX 2	IDX 1	IDX 0

Gate Driver/ Power Supply IC Interface Control 2 (R111h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	TB 12	TB 11	TB 10	TB 9	TB 8	TB 7	TB 6	TB 5	TB 4	TB 3	TB 2	TB 1	TB 0

IDX[2:0]: The index register of the instruction, which is transferred to the gate driver/power supply IC. The instruction that corresponds to the index as determined by the IDX[2:0] setting is transferred to the gate driver or power supply IC through a serial interface for the gate/power supply IC. The following figures illustrates the bit array with which instructions are transferred. The upper 3 bits in the figures corresponds to the IDX[2:0] bits. The instructions of the indexes determined by the IDX[2:0]settings as below are transferred to the gate driver/power supply IC.

When any change will be made to the instruction setting to the gate driver/power supply IC, the setting must be made first in the R111h register of HD 66781 before making a setting for IDX[2:0]. The transfer start (TE = 1) starts transferring the instructions, which is then followed by the execution.

TE: The ENABLE for the serial transfer to the gate driver/power supply IC. TE=0 enables a serial transfer. TE=1 starts a transfer to the gate driver/power supply IC. When the transfer is completed, TE=0 is returned.

A serial transfer takes 18 clocks at maximum (with reference to internal clocks). Do not make any changes to the instructions that are being transferred. Other instructions can be executable even during the instruction transfer.

Note 1) The transfer of the NL[5:0], AP[2:0], FLD[1:0] settings to the gate driver/power supply IC must be made right after the instruction setting of HD66781. Make a same setting to the HD66781 and HD66783/HD667P21 with regard to NL, AP, FLD registers. Otherwise, a proper operation is not guaranteed.

Note 2) As in the following figures, the bits to which no register is assigned must be overwritten with “0” or “1”.

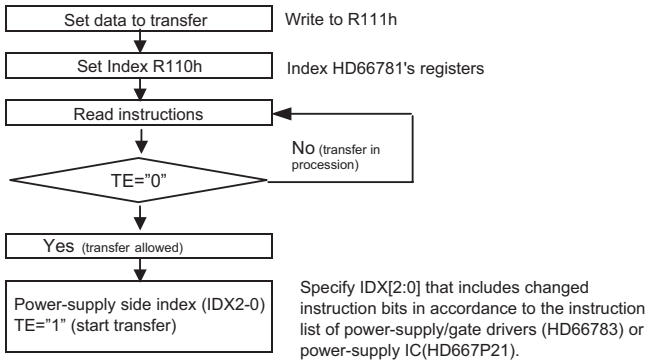
HD66783 Instructions

IDX2	IDX1	IDX0	TB12	TB11	TB10	TB9	TB8	TB7	TB6	TB5	TB4	TB3	TB2	TB1	TB0
0	0	0	0	GON	VCOMG	BT[2]	BT[1]	BT[0]	DC0[2]	DC0[1]	DC0[0]	AP[2]	AP[1]	AP[0]	0
0	0	1	0	DK	1	EQM	0	PON	VRH[3]	VRH[2]	VRH[1]	VRH[0]	VC[2]	VC[1]	VC[0]
0	1	0	DC1[2]	DC1[1]	DC1[0]	VDV[4]	VDV[3]	VDV[2]	VDV[1]	VDV[0]	VCM[4]	VCM[3]	VCM[2]	VCM[1]	VCM[0]
0	1	1	Setting disabled												
1	0	0	Setting disabled												
1	0	1	Setting disabled												
1	1	0	GS	NL[5]	NL[4]	NL[3]	NL[2]	NL[1]	NL[0]	SCN[5]	SCN[4]	SCN[3]	SCN[2]	SCN[1]	SCN[0]
1	1	1	0	0	0	0	0	0	0	0	0	0	0	NL[1]	NL[0]

HD667P21 Instructions

IDX2	IDX1	IDX0	TB12	TB11	TB10	TB9	TB8	TB7	TB6	TB5	TB4	TB3	TB2	TB1	TB0
0	0	0	0	GON	VCOMG	BT[2]	BT[1]	BT[0]	DC[2]	DC[1]	DC[0]	AP[2]	AP[1]	AP[0]	0
0	0	1	0	0	0	0	0	PON	VRH[3]	VRH[2]	VRH[1]	VRH[0]	VC[2]	VC[1]	VC[0]
0	0	1	0	1	0	DK[1]	DK[0]	0	0	0	0	0	0	0	0
0	1	0	0	0	0	VDV[4]	VDV[3]	VDV[2]	VDV[1]	VDV[0]	VCM[4]	VCM[3]	VCM[2]	VCM[1]	VCM[0]
0	1	1	Setting disabled												
1	0	0	Setting disabled												
1	0	1	Setting disabled												
1	1	0	Setting disabled												
1	1	1	0	0	VGL[4]	VGL[3]	VGL[2]	VGL[1]	VGL[0]	0	VGH[4]	VGH[3]	VGH[2]	VGH[1]	VGH[0]

HD66783 / HD667P21 instructions



Serial transfer sequence: gate driver/power supply IC interface

Setting examples

1. Set DC1[2:0], VDV[4:0], VCM of HD66783 to 3'h2, 5'h2, 5'h3 respectively.

   (1) Instruction set: R111h
   (2) Data write: 16'h0843 (DC1[2:0]=3'h2, VDV[4:0]=5'h2, VCM[4:0]=5'h3)
   (3) Instruction set: R110h
   (4) Data read: (make sure TE=0)
   (5) Data write: 16'h0102 (TE=1, IDX[2:0]=3'h2)

2. Set NL of HD66781 and HD66783 to 6'h20 (NL, AP, FLD are the registers that require a setting in both HD66781 and HD66783).

   (1) Instruction set: R400h
   (2) Data write: 16'h0020
   ↓
   (3) Instruction set: R111h
   (4) Data write: 16'h0800 (GS=0, NL[5:0]=6'h20, SCN[5:0]=6'h00)
   (5) Instruction set: R110h
   (6) Data read: (make sure TE=0)
   (7) Data write: 16'h0102 (TE=1, IDX[2:0]=3'h6)

Note 1) Make a same setting to the HD66781 and HD66783 at one time. (1) and (2) are the setting for the HD66781. (3)~(7) are the setting for the HD66783.

Common registers for HD66783 and HD667P21

BT[2:0]: Change the output scale of step-up circuits. Adjust the step-up scale according to the voltage in use. To set power consumption lower, it is necessary to set the step-up scale smaller. For details, see the datasheets of HD66783 and HD667P21.

VCOMG: Make settings for the output level of VcomL.

VCOMG = 0	The low-side output of Vcom is fixed to GND and the instruction (VDV) setting becomes invalid. Outputs from VcomL and VCL are halted. For this reason, the VCOMG setting is related to the power-supply startup sequence. Make a VCOMG setting by following the power-supply setting sequence.
VCOMG = 1	The low-side output of Vcom becomes VcomL. The output voltage of VcomL is set by instruction (VDV) setting. VCOMG = 1 is valid when PON = 1.

VC[2:0]: Adjust the reference voltages of VREG1OUT, VREG2OUT, and Vci1 voltages according to Vci as the reference voltage. For details, see the datasheets of HD66783 and HD667P21.

VRH[3:0]: Set the amplifying scale of VREG1OUT with the values set in VC bits (REGP) as an input. For details, see the datasheets of HD66783 and HD667P21.

VCM[4:0]: Make a setting for VcomH (the "High" of Vcom). VcomH can be amplified to VREG1OUT x 0.41 ~ 1.00. When VCM = 5'h01, VcomH is not adjusted by the internal volume adjustment but by an external resistor from VcomR. For details on whether to generate the VcomH level with internal electronic volume or an external resistor, see the datasheets of HD66783 and HD667P21.

VDV[4:0]: Set the Vcom alternating amplitude. The setting is invalid without Vcom alternating drive. For details, see the datasheets of HD66783 and HD667P21.

Registers of HD66783

AP[2:0]: Adjust the amount of constant current in the operational amplifier in the liquid crystal drive power supply. When the amount of constant current is set large, the liquid crystal drive capacity is enhanced and the display quality will improve, while the current consumption will increase. Select an optimum amount of current taking both the display quality and the current consumption into account. When no display operation is required, set AP[2:0] = "3'h0" to halt the operation of operational amplifiers and step-up circuits to reduce the current consumption. To set AP[2:0] otherwise, it starts step-up circuits to output VGH. For details, see the datasheets of HD66783.

DC0[2:0]: Select the operation frequency of step-up circuit 1. If the step-up operation frequency is set high, display quality will be enhanced due to increased drive capacity of step-up circuit, while power consumption will be increased. Make an adjustment taking both display quality and power consumption into consideration. For details, see the datasheets of HD66783.

GON: When GON=0, the output level of G1~G320 pins of HD66783 becomes VGH and the Vcom level becomes GND.

PON: Set start/halt of VGL, VCL operations. Set PON according to the power supply start sequence.

PON=0: Halt
PON=1: Start

EQM: Select the operation mode of Vcom2 output. Set EQM = 0.

DK: Control the start-up of DDVDH. See "Instruction Setting Flow" (p.185) for details on the setting.

VCM[4:0]: Make a setting for VcomH (the High voltage of Vcom). VcomH can be amplified to the level VREG1OUT x 0.40 ~ 0.98. When VCM[4:0] = 5'h0F, internal volume is halted and VcomH is adjusted by an external resistor from VcomR. See the datasheet of HD66783 whether to generate VcomH level with internal electronic volume or an external resistor.

DC1[2:0]: Select the operation frequency of step-up circuit 2. If the step-up operation frequency is set high, display quality will be enhanced due to increased drive capacity of step-up circuit, while power consumption will be increased. Make an adjustment taking both display quality and power consumption into consideration. See the datasheet of HD66783 for details.

SCN[5:0]: Set the start position of scanning gate bus line. For details, see the datasheets of HD66783.

NL[5:0]: Set the number of liquid crystal drive raster-rows. The number of raster-rows can be set to 8 multiples. The value should be set equal to or more than to drive the number of raster-rows required for the panel size.

Note: Set SCN[5:0] and NL[5:0] to satisfy the following equation:
(Output start position) + (Number of drive raster-rows) – 1 ≤ 320 (raster-rows)

GS: Set the scan direction of gate bus lines. The direction is changeable according to the gate driver's position on the assembly. For details, see the datasheets of HD66783.

FLD[1:0]: Set the number of valid lines to drive n-line interlacing. For details, see the datasheets of HD66783.

Registers of HD667P21

AP[2:0]: Adjust the amount of constant current in the operational amplifier in the liquid crystal drive power supply. When the amount of constant current is set large, the liquid crystal drive capacity will be enhanced and the display quality will improve, while the current consumption will increase. Select an optimum amount of current taking both the display quality and the current consumption into account. When no display operation is required, set AP[2:0] = "3'h0" to halt the operation of operational amplifier and step-up circuits to reduce the current consumption. If AP[2:0] is set otherwise, it starts step-up circuit to output VLOUT1, VLOUT2. For details, see the datasheets of HD667P21.

DC[2:0]: Select the operation frequency of step-up circuit 1. If the step-up operation frequency is set high, display quality will be enhanced due to increased drive capacity of step-up circuit, while power consumption will be increased. Make an adjustment taking both display quality and power consumption into consideration. For details, see the datasheets of HD66783.

GON: When GON=0, the Vcom level becomes GND.

PON: Set start/halt of VLOUT3 operation. Set PON according to the power supply start sequence.

PON=0: Halt
PON=1: Start

VCM[4:0]: Make a setting for VcomH (the High voltage of Vcom). VcomH can be amplified to the level VREG1OUT x 0.41 ~ 1.00. When VCM[4:0] = 5'h1F, internal volume is halted and VcomH is adjusted by an external resistor from VcomR. See the datasheet of HD667P21 whether to generate VcomH level with internal electronic volume or an external resistor.

VGH[4:0]: Set the VGH regulator output level. The setting can be made from 2.82 to 4.06 times of REGP voltage.

VGL[4:0]: Set the VGL regulator output level. The setting can be made from –1.60 to –2.84 times of REGP voltage.

RAM Address set in horizontal/vertical directions (R200h/R201h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	AD [7]	AD [6]	AD [5]	AD [4]	AD [3]	AD [2]	AD [1]	AD [0]
W	1	0	0	0	0	0	0	0	AD [16]	AD [15]	AD [14]	AD [13]	AD [12]	AD [11]	AD [10]	AD [9]	AD [8]

Note : Top R200h, Bottom R201h

AD[16:0]: Initialize GRAM address at AC (Address Counter). The address counter is automatically updated in accordance with AM, I/D settings after data are written to GRAM. Data can be written consecutively without making a new address setting. The address counter is not automatically updated when data are read out from GRAM.

Table 45 GRAM address range

AD[16:0]	GRAM Setting
17'h00000 – 17'h000EF	Bitmap data for G1
17'h00100 – 17'h001EF	Bitmap data for G2
17'h00200 – 17'h002EF	Bitmap data for G3
17'h00300 – 17'h003EF	Bitmap data for G4
17'h00400 – 17'h004EF	Bitmap data for G5
:	:
17'h13F00 – 17'h13CEF	Bitmap data for G317
17'h13F00 – 17'h13DEF	Bitmap data for G318
17'h13F00 – 17'h13EEF	Bitmap data for G319
17'h13F00 – 17'h13FEF	Bitmap data for G320

Note 1) An address set is made every frame within the GRAM address range set by AD[16:0] at the falling edge of VSYNC when RGB interface (RM=1) is selected.

Note 2) An address set is made when instructions are executed in the internal clock operation or the VSYNC interface mode (RM = 0).

Note 3) Register values are loaded in both horizontal/vertical address counters when a setting is made for either one of the R200h/R201h registers.

Write Data to GRAM (R202h)

R/W	RS	
W	1	The DB[17:0] pins are assigned to RAM write data (WD[17:0]) differently according to an interface.
RGB interface		The DB[17:0] pins are assigned to RAM write data (WD[17:0]) differently according to an interface .

WD[17:0]: All data are expanded into 18 bits internally before being written to GRAM. The way of expanding data into 18 bits is different according to the interface.

The grayscale level is selected according to the GRAM data. The address is automatically updated according to the setting with the AM and I/D bits after data are written to GRAM. During the standby mode, no access is allowed to GRAM. When the 8 or 16 bit interface modes are selected, the data in the MSB of R and B pixels are also written to the LSB of R and B pixels respectively to expand the 8/16- bit data into the 18-bit data internally.

During the RGB interface mode, when writing data to RAM through a system interface, make sure to avoid conflicts between writing through the RGB interface and writing through system interface.

When the 18-bit RGB interface is selected, the18-bit data in PD17-0 bits are written, and 262,144 colors are available. When the 16-bit RGB interface is selected, the data in the MSB of R and B pixels are also written to the LSB of R and B pixels respectively, and 65,536 colors are available.

The upper 3 bits of OSD image data are used as a transmission-rate bit (α channel).

Table 46 BGR = 0

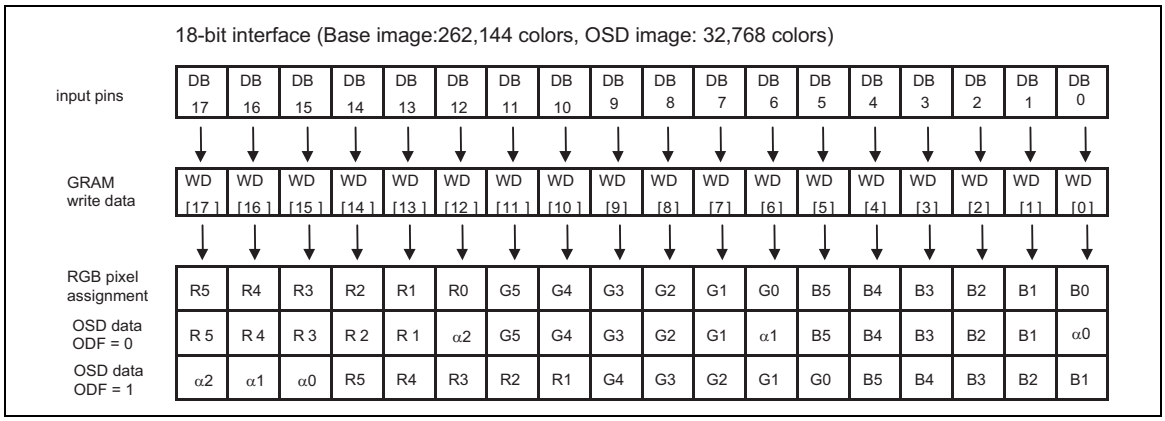
OSD	ODF	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	*	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
1	0	R5	R4	R3	R2	R1	α2	G5	G4	G3	G2	G1	α1	B5	B4	B3	B2	B1	α0
1	1	α2	α1	α0	R4	R3	R2	R1	R0	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

Table 47 BGR =1

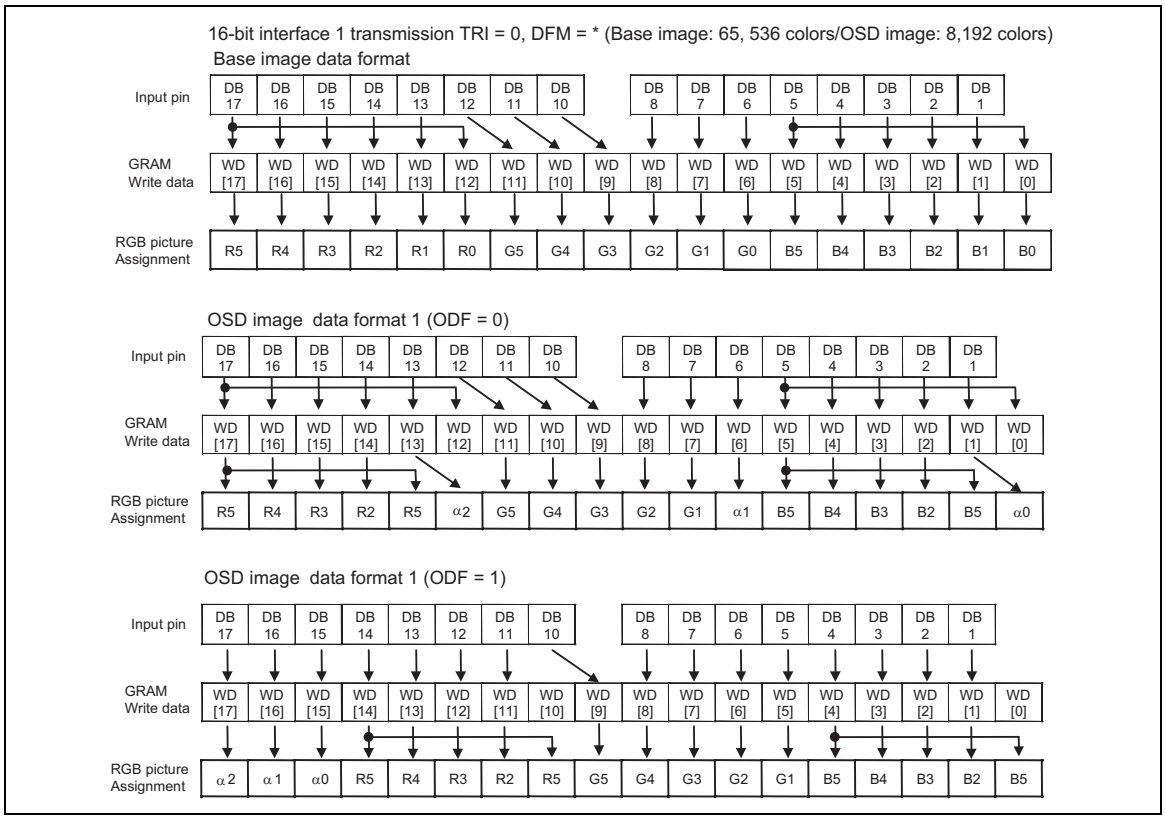
OSD	ODF	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	*	B5	B4	B3	B2	B1	B0	G5	G4	G3	G2	G1	G0	R5	R4	R3	R2	R1	R0
1	0	B5	B4	B3	B2	B1	α0	G5	G4	G3	G2	G1	α1	R5	R4	R3	R2	R1	α2
1	1	α0	α1	α2	B4	B3	B2	B1	B0	G4	G3	G2	G1	G0	R4	R3	R2	R1	R0

Table 48 α channel

α2	α1	α0	transmission rate	displayed picture
0	0	0	0%	Base image display
0	0	1		Setting disabled
0	1	0	25%	Base image 75%+OSD 25%
0	1	1	75%	Base image 25%+OSD 75%
1	0	0	50%	Base image 50%+OSD 50%
1	0	1		Setting disabled
1	1	0	100%	OSD image display
1	1	1		Setting disabled



RAM data write in 18-bit interface (Base image 262,144 colors/OSD image 8,192 colors)



RAM data write in 16-bit interface (Base image 65,536 colors/OSD image 32,768 colors)

16-bit interface 2 transmissions TRI = 1, DFM = 0 (Base image:262,144 colors, OSD image: 32,768 colors)

	1st transmission																2nd transmission	
input pins	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 17	DB 16
GRAM write data	WD [17]	WD [16]	WD [15]	WD [14]	WD [13]	WD [12]	WD [11]	WD [10]	WD [9]	WD [8]	WD [7]	WD [6]	WD [5]	WD [4]	WD [3]	WD [2]	WD [1]	WD [0]
RGB pixel assignment	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
OSD data ODF = 0	R 5	R 4	R 3	R 2	R 1	α2	G5	G4	G3	G2	G1	α1	B5	B4	B3	B2	B1	α0
OSD data ODF = 1	α2	α1	α0	R5	R4	R3	R2	R1	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1

16-bit interface 2 transmissions TRI = 1, DFM = 1 (Base image:262,144 colors, OSD image: 32,768 colors)

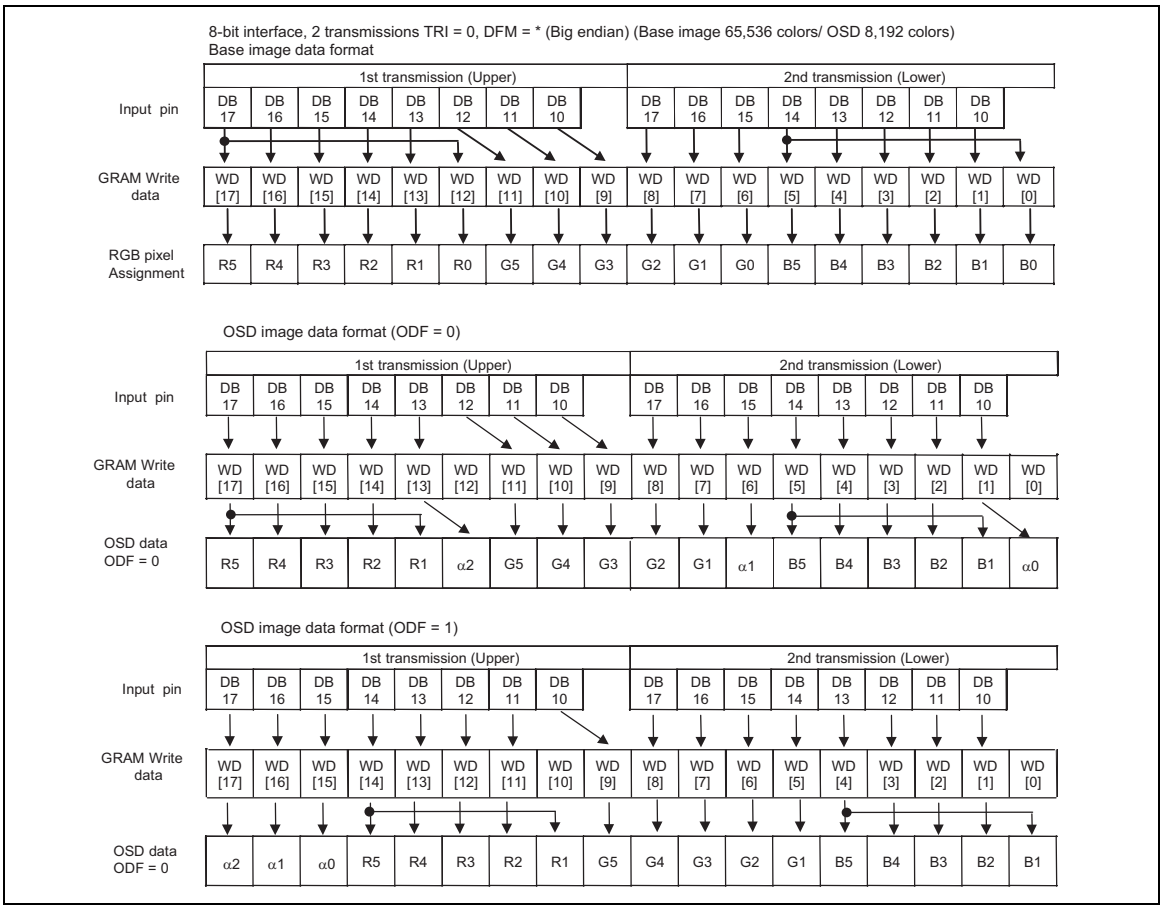
	1st transmission		2nd transmission															
input pins	DB 2	DB 1	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1
GRAM write data	WD [17]	WD [16]	WD [15]	WD [14]	WD [13]	WD [12]	WD [11]	WD [10]	WD [9]	WD [8]	WD [7]	WD [6]	WD [5]	WD [4]	WD [3]	WD [2]	WD [1]	WD [0]
RGB pixel assignment	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
OSD data ODF = 0	R 5	R 4	R 3	R 2	R 1	α2	G5	G4	G3	G2	G1	α1	B5	B4	B3	B2	B1	α0
OSD data ODF = 1	α2	α1	α0	R5	R4	R3	R2	R1	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1

RAM data write in 16-bit interface (Base image 262,144 colors/OSD image 32,768 colors)

9-bit interface (Base image 262,144 colors/OSD image 32,786 colors)

	1st transmission (Upper)									2nd transmission (Lower)								
Input pin	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9
GRAM Write data	WD [17]	WD [16]	WD [15]	WD [14]	WD [13]	WD [12]	WD [11]	WD [10]	WD [9]	WD [8]	WD [7]	WD [6]	WD [5]	WD [4]	WD [3]	WD [2]	WD [1]	WD [0]
RGB picture Assignment	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
OSD data ODF=0	R5	R4	R3	R2	R1	α 2	G5	G4	G3	G2	G1	α 1	B5	B4	B3	B2	B1	α 0
OSD data ODF=1	α2	α 1	α 0	R5	R4	R3	R2	R1	G5	G4	G3	G2	G1	B5	B4	B3	B2	B1

RAM data write in 9-bit interface (Base image 262,144 colors /OSD image 32,768 colors)



RAM data write in 8-bit interface, big endian (Base image/OSD image)

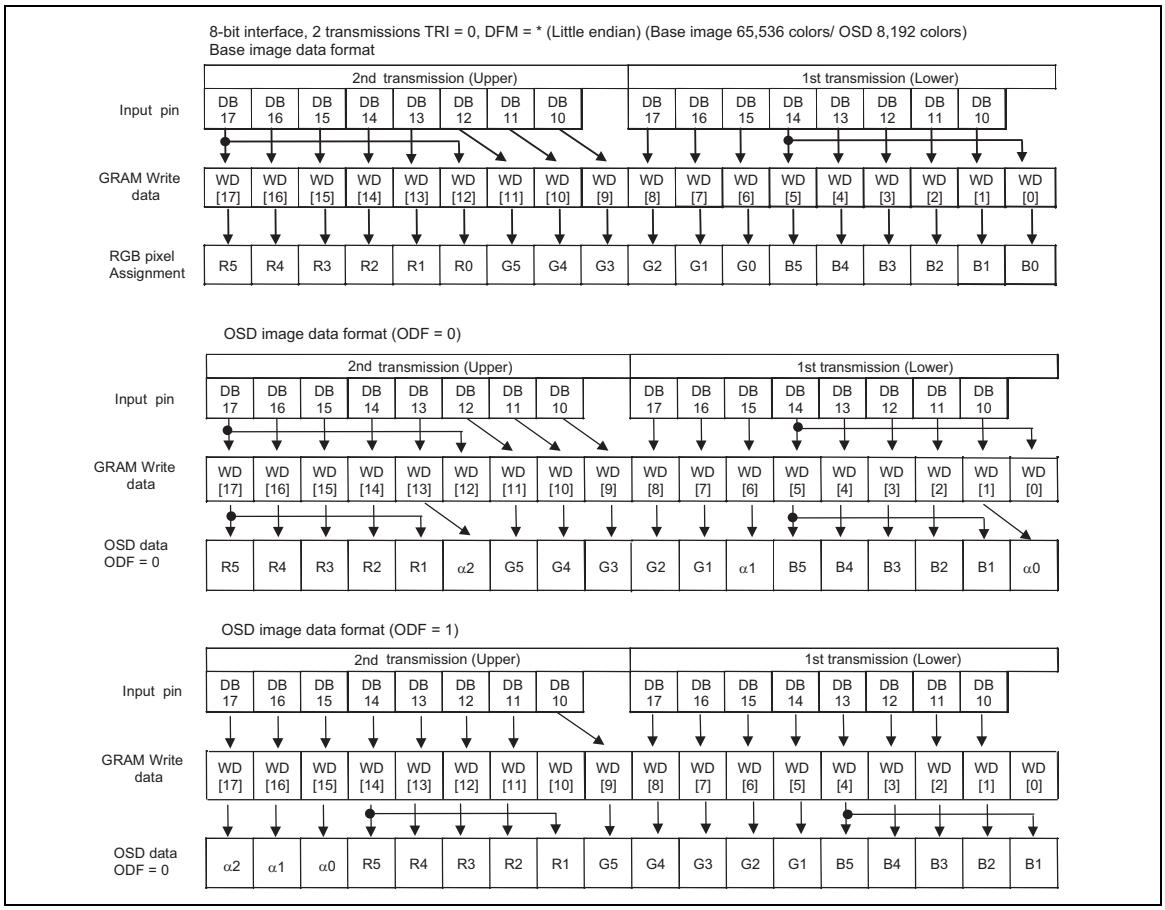
8-bit interface, 3 transmissions TRI = 1, DFM = 0 (Base image 262,144 colors/ OSD 32,768 colors)

	1st transmission		2nd transmission								3rd transmission							
Input pin	DB 11	DB 10	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10
GRAM Write data	WD [17]	WD [16]	WD [15]	WD [14]	WD [13]	WD [12]	WD [11]	WD [10]	WD [9]	WD [8]	WD [7]	WD [6]	WD [5]	WD [4]	WD [3]	WD [2]	WD [1]	WD [0]
RGB pixel assignment	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
OSD data ODF = 0	R5	R4	R3	R2	R1	α2	G5	G4	G3	G2	G1	α1	B5	B4	B3	B2	B1	α0
OSD data ODF = 1	α2	α1	α0	R5	R4	R3	R2	R1	G5	G4	G3	G2	G1	B5	B4	B3	B2	B1

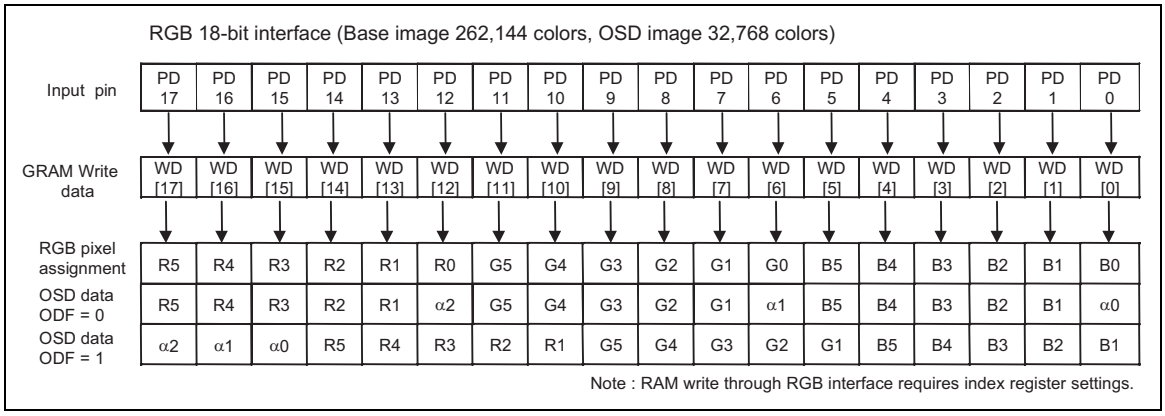
8-bit interface, 3 transmissions TRI = 1, DFM = 1 (Base image 262,144 colors/ OSD 32,768 colors)

	1st transmission						2nd transmission						3rd transmission					
Input pin	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12
GRAM Write data	WD [17]	WD [16]	WD [15]	WD [14]	WD [13]	WD [12]	WD [11]	WD [10]	WD [9]	WD [8]	WD [7]	WD [6]	WD [5]	WD [4]	WD [3]	WD [2]	WD [1]	WD [0]
RGB pixel assignment	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
OSD data ODF = 0	R5	R4	R3	R2	R1	α2	G5	G4	G3	G2	G1	α1	B5	B4	B3	B2	B1	α0
OSD data ODF = 1	α2	α1	α0	R5	R4	R3	R2	R1	G5	G4	G3	G2	G1	B5	B4	B3	B2	B1

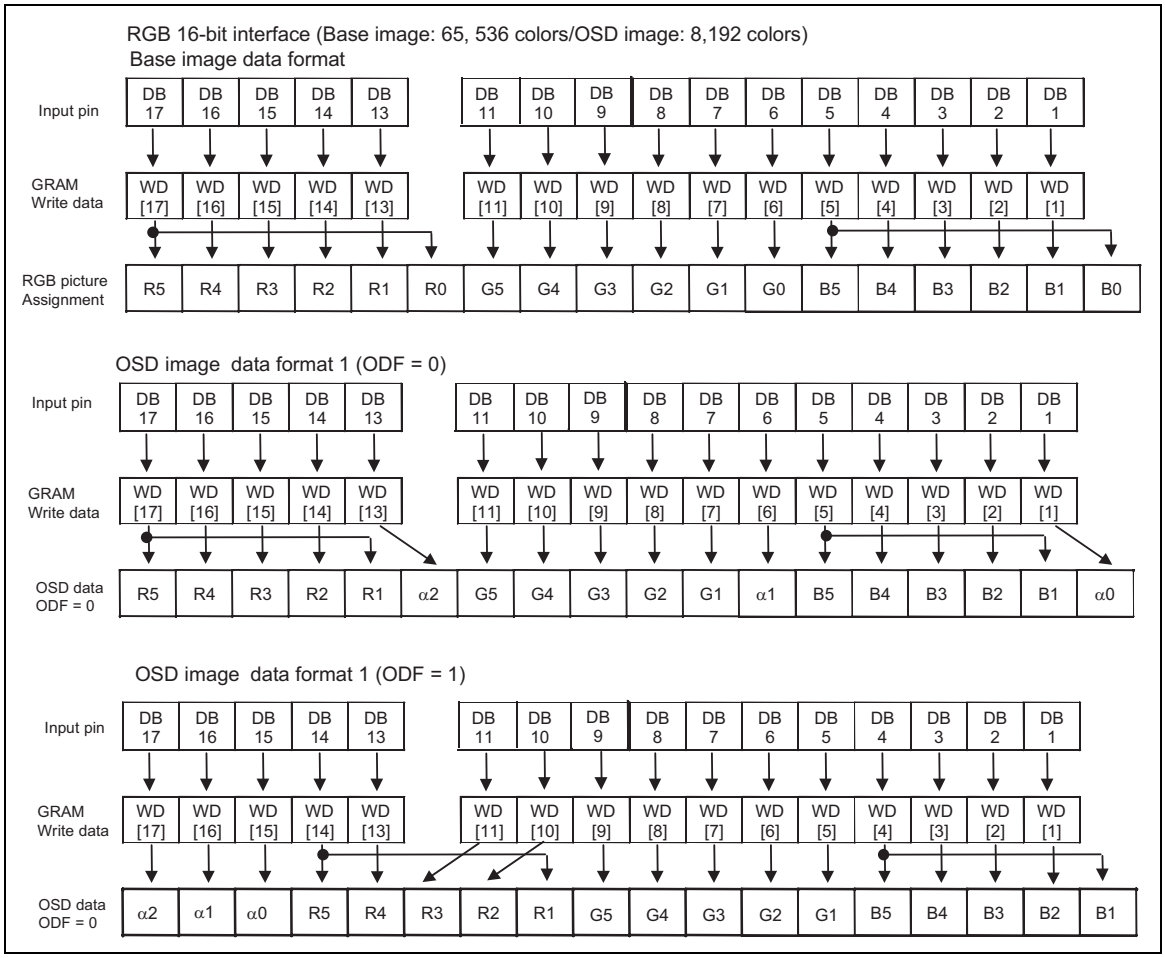
RAM data write in 8-bit interface, 3 transmissions (Base image/OSD image)



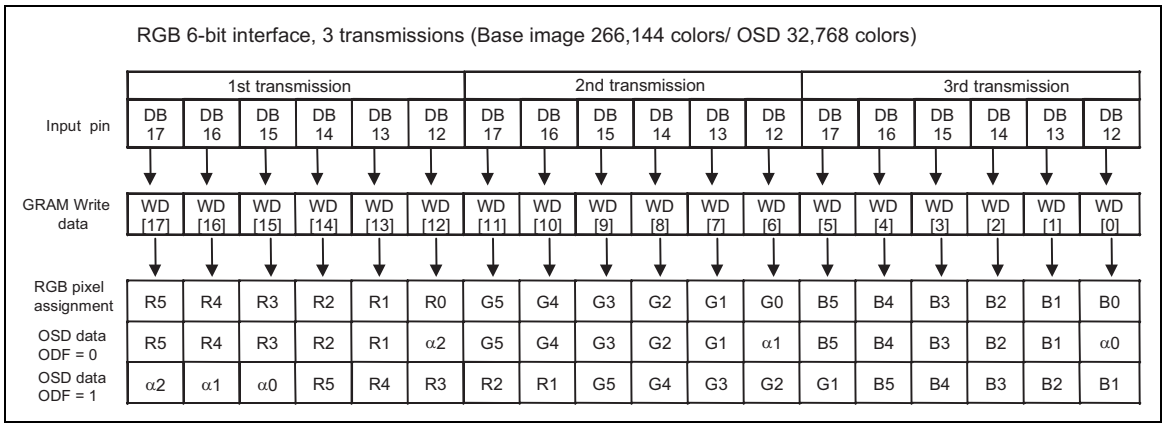
RAM data write in 8-bit interface, little endian (Base image/OSD image)



RGB 18-bit interface (Base/OSD image display)



RGB 16-bit interface (Base/OSD image display)



RGB 6-bit interface (Base/OSD image)

Table 49 GRAM data and LCD output level (REV = 0)

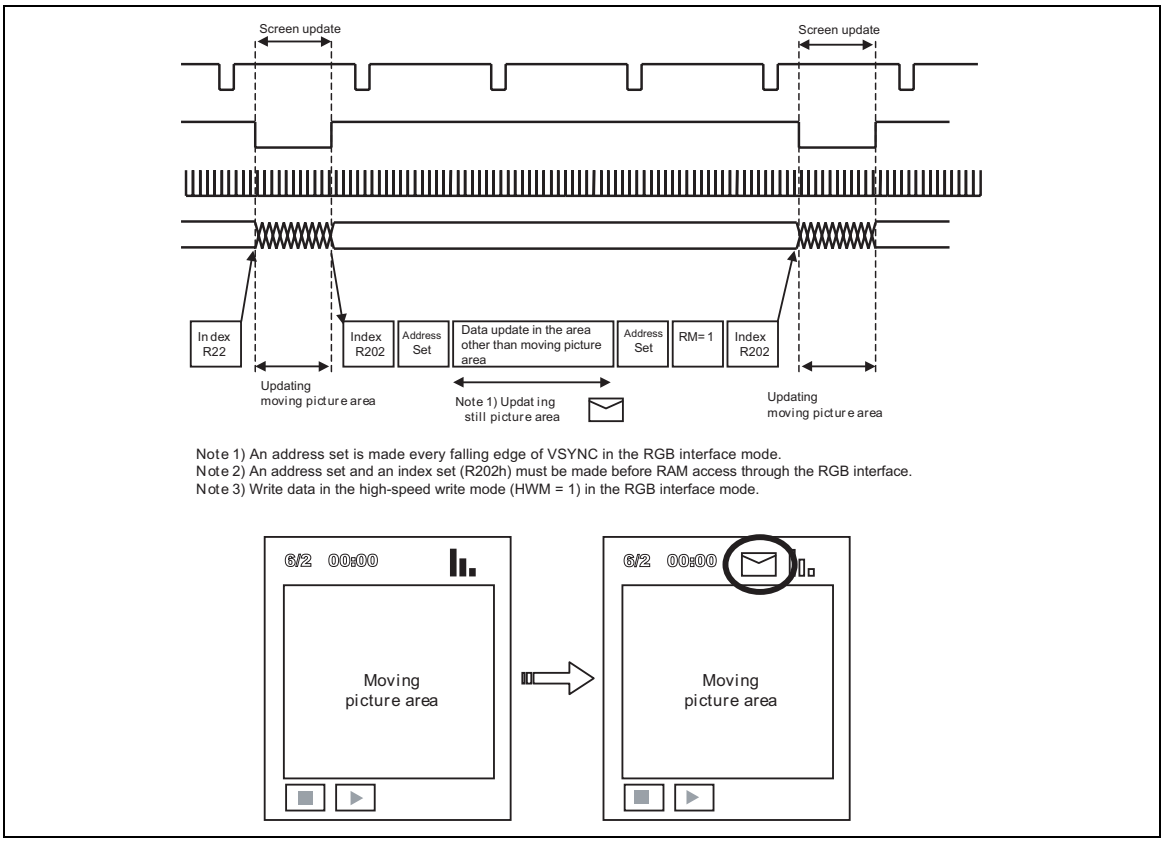
GRAM data RGB	Selected grayscale level	
	Positive	Negative
6'h00	V0	V63
6'h01	V1	V62
6'h02	V2	V61
6'h03	V3	V60
6'h04	V4	V59
6'h05	V5	V58
6'h06	V6	V57
6'h07	V7	V56
6'h08	V8	V55
6'h09	V9	V54
6'h0A	V10	V53
6'h0B	V11	V52
6'h0C	V12	V51
6'h0D	V13	V50
6'h0E	V14	V49
6'h0F	V15	V48
6'h10	V16	V47
6'h11	V17	V46
6'h12	V18	V45
6'h13	V19	V44
6'h14	V20	V43
6'h15	V21	V42
6'h16	V22	V41
6'h17	V23	V40
6'h18	V24	V39
6'h19	V25	V38
6'h1A	V26	V37
6'h1B	V27	V36
6'h1C	V28	V35
6'h1D	V29	V34
6'h1E	V30	V33
6'h1F	V31	V32

GRAM data RGB	Selected grayscale level	
	Positive	Negative
6'h20	V32	V31
6'h21	V33	V30
6'h22	V34	V29
6'h23	V35	V28
6'h24	V36	V27
6'h25	V37	V26
6'h26	V38	V25
6'h27	V39	V24
6'h28	V40	V23
6'h29	V41	V22
6'h2A	V42	V21
6'h2B	V43	V20
6'h2C	V44	V19
6'h2D	V45	V18
6'h2E	V46	V17
6'h2F	V47	V16
6'h30	V48	V15
6'h31	V49	V14
6'h32	V50	V13
6'h33	V51	V12
6'h34	V52	V11
6'h35	V53	V10
6'h36	V54	V9
6'h37	V55	V8
6'h38	V56	V7
6'h39	V57	V6
6'h3A	V58	V5
6'h3B	V59	V4
6'h3C	V60	V3
6'h3D	V61	V2
6'h3E	V62	V1
6'h3F	V63	V0

RAM Access through RGB-I/F and System I/F

The HD66781 writes all display data to the internal RAM even in the RGB-I/F mode. Through the RGB-I/F mode, only the data for the moving picture area as well as for the frames to update screens can be transmitted. By writing data in the high-speed write mode (HWM = 1) and with the window address function, the HD66781 achieves high-speed access to RAM with low power consumption while displaying moving pictures. In the frames other than the moving picture screen update, the display data in the area other than the moving picture area can be updated through a system interface.

RAM access is also possible through the system interface even in the RGB-I/F mode. In the RGB interface mode, data are written to RAM in synchronization with the DOTCLK input during ENABLE = "Low". When writing data in the RGB-I/F mode through the system interface, it is necessary to set ENABLE "High" to stop writing through the RGB interface. After accessing RAM through the system interface, wait an enough time for the write/read bus cycle before starting RAM access through the RGB interface.



Updating still picture area while displaying a moving picture

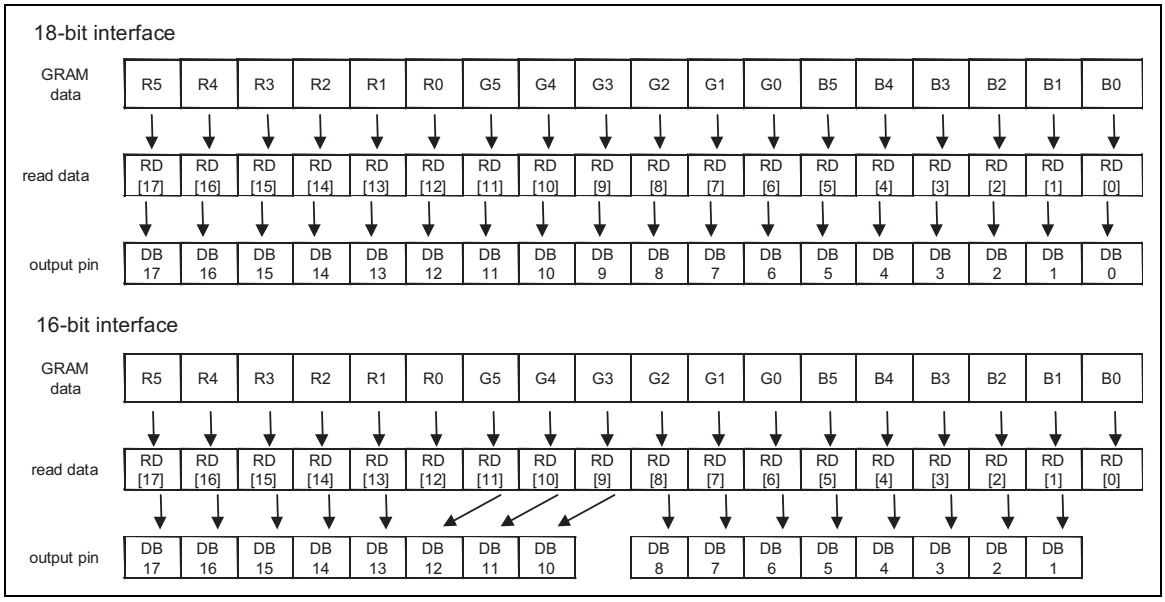
Read Data from GRAM (R202h)

R/W	RS	
R	1	RAM read data (RD[17:0]) are assigned differently to the DB[17:0] pins according to an interface .

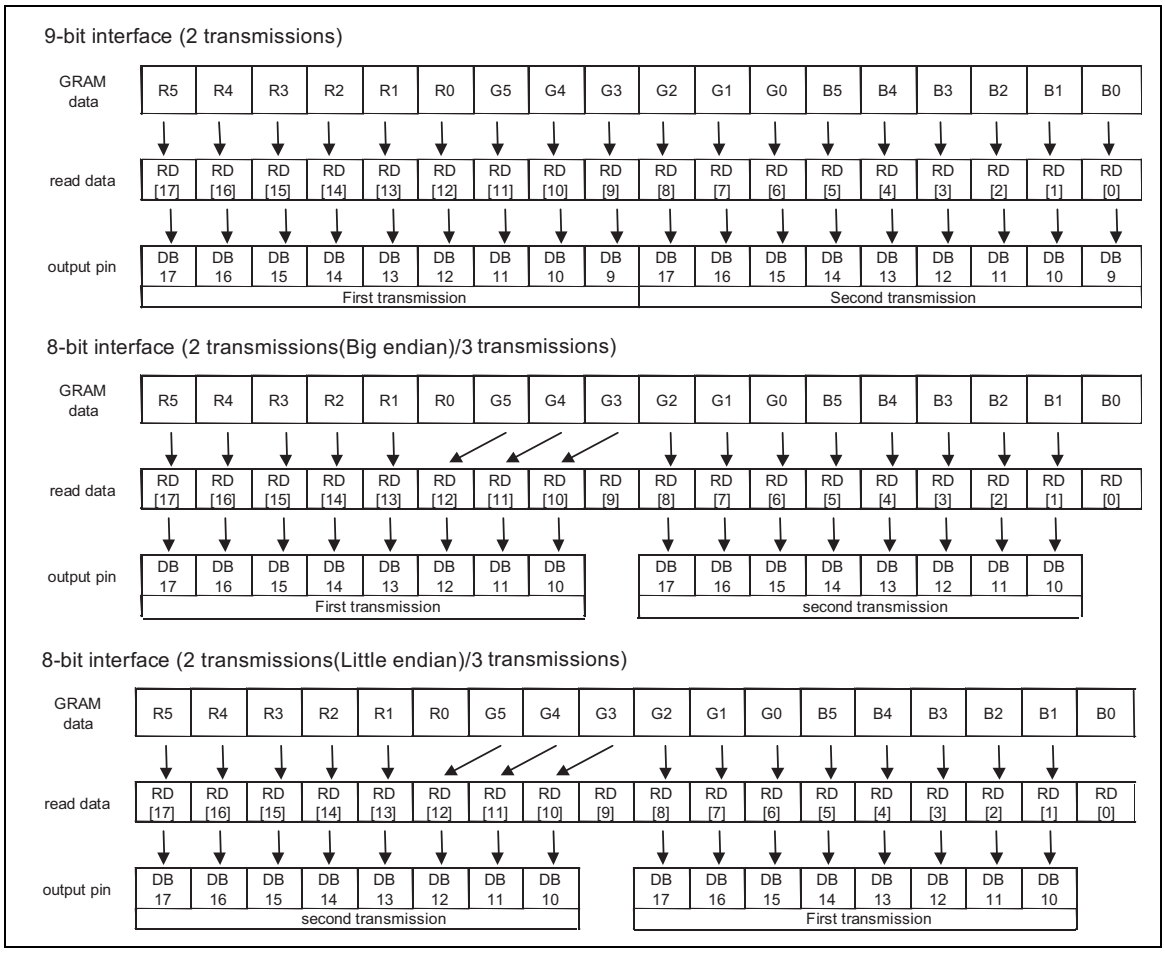
RD[17:0]: Read 18-bit data from GRAM. The RAM read data (RD[17:0]) are assigned differently to the DB[17:0] pins according to an interface.

When data are read out from GRAM to the microcomputer, the first-word data read immediately after the GRAM address set are latched in the internal read-data latch, and the data in the data bus (DB17–0) are nullified. The data are read as valid data from the second word.

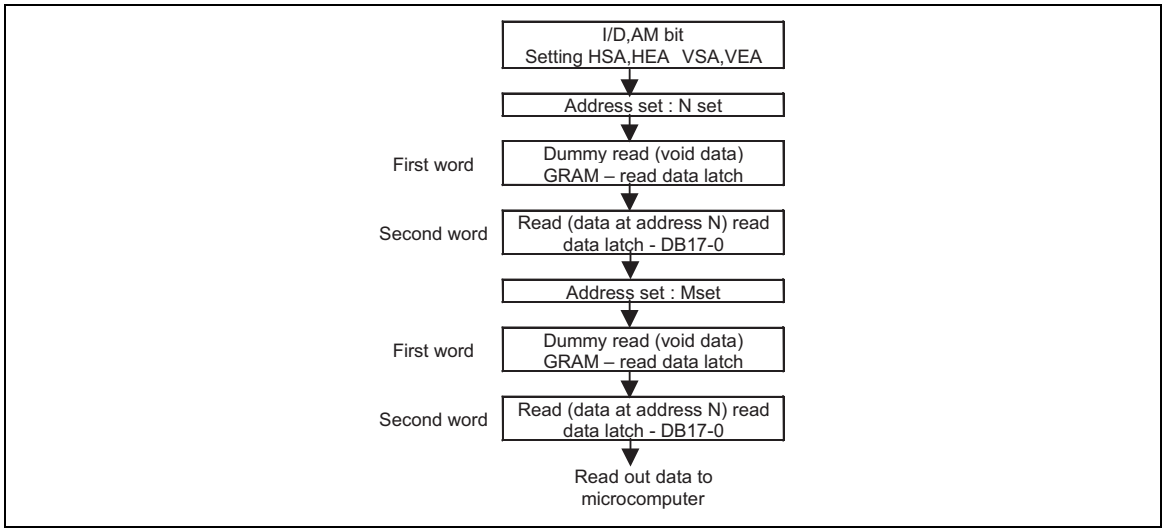
When the 8-/16-bit interfaces are selected, the GRAM data in the LSBs of R and B pixels are not read out. When reading out OSD data, it takes the data format when ODF = 0. This function is not available in the RGB interface mode. Set TRI = 0 while data read is executed.



Read data from GRAM: 18/16-bit interface



Read data from GRAM: 9/8-bit interface



GRAM read sequence

RAM Write Data Mask 1/2 (R203h/R204h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	WM [11]	WM [10]	WM [9]	WM [8]	WM [7]	WM [6]	0	0	WM [5]	WM [4]	WM [3]	WM [2]	WM [1]	WM [0]
W	1	0	0	0	0	0	0	0	0	0	0	WM [17]	WM [16]	WM [15]	WM [14]	WM [13]	WM [12]

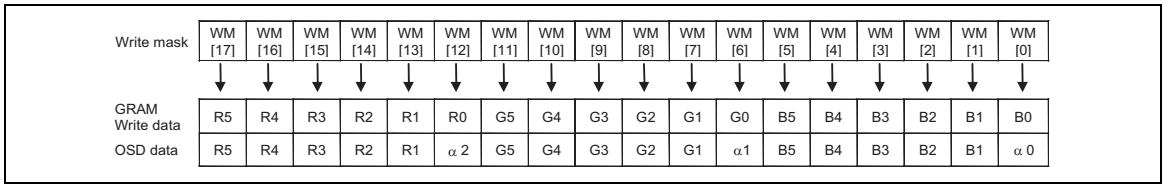
Note 1) Top R203, bottom R204

WM[17:0]: Write-mask data by bit when the data are written to GRAM. For example, if WM17 = 1, the WM17 write-mask the MSB of the data to write to GRAM so that the data in the MSB is not written to GRAM. The rest of WM16 ~ 0 bits also write-mask the data in the corresponding bits of GRAM write data as well when they are set to 1.

The WM17-0 bits write-mask the 18-bit data to write to GRAM.

Note 1) This function is not available in the RGB-I/F mode.

Note 2) OSD image data are written to RAM in the ODF = 0 format. The write-mask setting for OSD images must be made for the ODF = 0 format.



RAM write data mask

Window Address Control Instructions

Window horizontal RAM address Start/End (R210h/ R211h)
Window vertical RAM address Start/End (R212h/R213h)

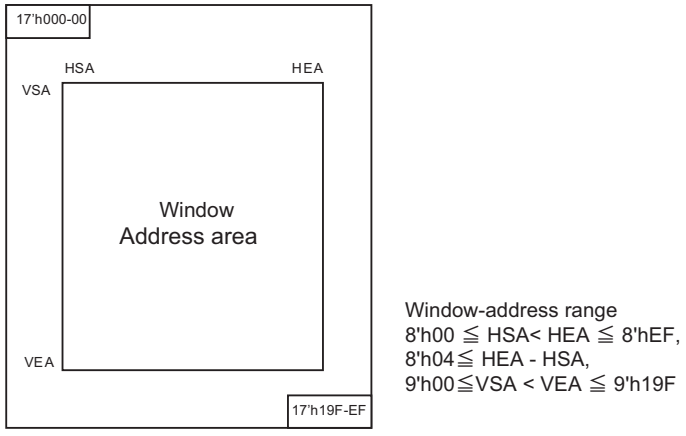
	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R50	W	1	0	0	0	0	0	0	0	0	HSA [7]	HSA [6]	HSA [5]	HSA [4]	HSA [3]	HSA [2]	HSA [1]	HSA [0]
R51	W	1	0	0	0	0	0	0	0	0	HEA [7]	HEA [6]	HEA [5]	HEA [4]	HEA [3]	HEA [2]	HEA [1]	HEA [0]
R52	W	1	0	0	0	0	0	0	0	VSA [8]	VSA [7]	VSA [6]	VSA [5]	VSA [4]	VSA [3]	VSA [2]	VSA [1]	VSA [0]
R53	W	1	0	0	0	0	0	0	0	VEA [8]	VEA [7]	VEA [6]	VEA [5]	VEA [4]	VEA [3]	VEA [2]	VEA [1]	VEA [0]

HSA[7:0] Specify the start position of a window-address range in the horizontal direction by address.

HEA[7:0] Specify the end position of a window-address range in the horizontal direction by address. Data are written to a rectangular area within GRAM from the address specified by HSA to the address specified by HEA. The setting of the address is required before writing data to RAM. Make sure the address is set to satisfy 8'h00≤ HSA< HEA ≤ 8'hEF and 8'h4≤ HEA - HSA.

VSA[7:0] Specify the start position of a window-address range in the vertical direction to access to RAM.

VEA[7:0] Specify the end position of a window-address range in the vertical direction to access to RAM. Data are written to a rectangular area within GRAM from the address specified by VSA to the address specified by VEA. The setting of addresses is required before writing data to RAM. Make sure the addresses are set to satisfy 9'h000≤ VSA< VEA ≤ 9'h19F.



GRAM address map and window-address range

Note 1) Set a window-address range within the GRAM address map.
Note 2) In the high-speed write mode, data are written to GRAM by one horizontal line. Write data to GRAM by horizontal line unit.
Note 3) Make an address set within the window address area. In the high-speed write mode, make an address set from the first line of the window address area.

γ Control (R300h ~ R309h)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R300	W	1	0	0	0	0	0	PK P1[2]	PK P1[1]	PK P1[0]	0	0	0	0	0	PK P0[2]	PK P0[1]	PK P0[0]
R301	W	1	0	0	0	0	0	PK P3[2]	PK P3[1]	PK P3[0]	0	0	0	0	0	PK P2[2]	PK P2[1]	PK P2[0]
R302	W	1	0	0	0	0	0	PK P5[2]	PK P5[1]	PK P5[0]	0	0	0	0	0	PK P4[2]	PK P4[1]	PK P4[0]
R303	W	1	0	0	0	0	0	PR P1[2]	PR P1[1]	PR P1[0]	0	0	0	0	0	PR P0[2]	PR P0[1]	PR P0[0]
R304	W	1	0	0	0	VR P1[4]	VR P1[3]	VR P1[2]	VR P1[1]	VR P1[0]	0	0	0	0	VR P0[3]	VR P0[2]	VR P0[1]	VR P0[0]
R305	W	1	0	0	0	0	0	PK N1[2]	PK N1[1]	PK N1[0]	0	0	0	0	0	PK P0[2]	PK P0[1]	PK P0[0]
R306	W	1	0	0	0	0	0	PK N3[2]	PK N3[1]	PK N3[0]	0	0	0	0	0	PK N2[2]	PK N2[1]	PK N2[0]
R307	W	1	0	0	0	0	0	PK N5[2]	PK N5[1]	PK N5[0]	0	0	0	0	0	PK N4[2]	PK N4[1]	PK N4[0]
R308	W	1	0	0	0	0	0	PR N1[2]	PR N1[1]	PR N1[0]	0	0	0	0	0	PR N0[2]	PR N0[1]	PR N0[0]
R309	W	1	0	0	0	VR N1[4]	VR N1[3]	VR N1[2]	VR N1[1]	VR N1[0]	0	0	0	0	VR N0[3]	VR N0[2]	VR N0[1]	VR N0[0]

PKP5-0[2:0]: γ fine adjustment registers for positive polarity
PRP1-0[2:0]: γ gradient adjustment registers for positive polarity
VRP(N)0[3:0]: amplitude adjustment resistor for positive polarity
PKN5-0[2:0]: γ fine adjustment registers for negative polarity
PRN1-0[2:0]: γ gradient adjustment registers for negative polarity
VRP(N)1[4:0]: amplitude average adjustment resistor for negative polarity

Base image display control instructions

Number of Line (R400h)
Base image display position (R401h)
Base picture RAM Address (R402h)
Base picture RAM Address (R403h)
Vertical scroll Control (R404h)
Base image expansion area/start line address (R405h)
Base image expansion area/end line address (R406h)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R400	W	1	0	0	0	0	0	0	0	0	0	0	NL1 [5]	NL1 [4]	NL1 [3]	NL1 [2]	NL1 [1]	NL1 [0]
R401	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	VLE	REV
R402	W	1	0	0	0	0	0	0	0	BSA [8]	BSA [7]	BSA [6]	BSA [5]	BSA [4]	BSA [3]	BSA [2]	BSA [1]	BSA [0]
R403	W	1	0	0	0	0	0	0	0	BEA [8]	BEA [7]	BEA [6]	BEA [5]	BEA [4]	BEA [3]	BEA [2]	BEA [1]	BEA [0]
R404	W	1	0	0	0	0	0	0	0	VL [8]	VL [7]	VL [6]	VL [5]	VL [4]	VL [3]	VL [2]	VL [1]	VL [0]
R405	W	1	0	0	0	0	0	0	0	ESA [8]	ESA [7]	ESA [6]	ESA [5]	ESA [4]	ESA [3]	ESA [2]	ESA [1]	ESA [0]
R406	W	1	0	0	0	0	0	0	0	EEA [8]	EEA [7]	EEA [6]	EEA [5]	EEA [4]	EEA [3]	EEA [2]	EEA [1]	EEA [0]

Base image control instructions

NL0[5:0]: Set the number of liquid crystal drive raster-rows. The number of raster-rows can be set to 8 multiples. The GRAM address mapping is made irrespective of the value set for the number of raster-rows to drive liquid crystal. The value should be set equal to or more than to drive the number of raster-rows required for the panel size.

REV: When REV = 1, a reverse display is shown within the display area. The grayscale level inversion enables to use same data to display on both normally white and normally black panels. The REV setting is effective for both OSD and base image areas.

The source outputs during front and back porches and a blank period during partial display mode depend on the setting of PTS bits.

Table 50

REV0	GRAM data	Source output level in display area	
		Positive polarity	Negative polarity
0	18'h00000	V63	V0
	:	:	:
	18'h3FFFF	V0	V63
1	18'h00000	V0	V63
	:	:	:
	18'h3FFFF	V63	V0

Note 1) The source outputs during front and back porches and a blank period during partial display mode depend on the setting of PTS bits.

VLE: When VLE = 1, settings for the vertical scroll display is made valid. The start line is displayed according to the VL[8:0] setting. The raster-rows that display a base image are scrolled by the number of lines set by VL bits. OSD area is not affected by the base-picture scrolling. This function is not available while external display interface is selected. While external display interface is selected, make sure that VLE= 0.

Table 51

VLE	Base image
0	Fixed display
1	Scrolling display

Note 1) Scroll function is not available during the interlaced drive (FLD = 2'h3)

BSA[8:0]/BEA[8:0]: Set the start line address (BSA) and the end line address (BEA) of the base image display RAM area.

Display RAM data from the one set at BSA bits from the first line. Make sure that base image display RAM area (BSA/BEA) is equal to or more than the number of raster-rows driving a panel (= NL ≤ BSA – BEA). In case of BSA – BEA ≤ NL, outside the base image area becomes non-lit display.

VL[8:0] Set the number of raster-rows that are scrolled for a base image. The numbers of raster-rows set by VL bits are scrolled within the base image.

ESA[8:0]/EEA[8:0] Set the start line address (ESA) and the end line address (EEA) of the area which is magnified in the base image display RAM area.

A base image in the area specified with ESA and EEA is magnified on display. Make sure that BSA ≤ ESA ≤ EEA ≤ BEA. A magnified base image is not available with the scrolling function.

Table 52 Liquid crystal drive raster-rows

NL[5:0]	Number of raster-rows
6'h00	Setting disabled
6'h01	16
6'h02	24
6'h03	32
6'h04	40
6'h05	48
6'h06	56
6'h07	64
6'h08	72
6'h09	80
6'h0A	88
6'h0B	96
6'h0C	104
6'h0D	112
6'h0E	120
6'h0F	128
6'h10	136
6'h11	144
6'h12	152
6'h13	160

NL[5:0]	Number of raster-rows
6'h14	168
6'h15	176
6'h16	184
6'h17	192
6'h18	200
6'h19	208
6'h1A	216
6'h1B	224
6'h1C	232
6'h1D	240
6'h1E	248
6'h1F	256
6'h20	264
6'h21	272
6'h22	280
6'h23	288
6'h24	296
6'h25	304
6'h26	312
6'h27	320

OSD control instructions

OSD image 1 display position (R500h)
OSD image 1 RAM Address /Start line Address (R501h)
OSD image 1 RAM Address /End line Address (R502h)
OSD image 2 display position (R503h)
OSD image 2 RAM Address/Start line Address (R504h)
OSD image 2 RAM Address/End line Address (R505h)
OSD image 3 display position (R506h)
OSD image 3 RAM Address/Start line Address (R507h)
OSD image 3 RAM Address/End line Address (R508h)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R500	W	1	0	0	0	0	0	0	0	ODP 0 [8]	ODP 0 [7]	ODP 0 [6]	ODP 0 [5]	ODP 0 [4]	ODP 0 [3]	ODP 0 [2]	ODP 0 [1]	ODP 0 [0]
R501	W	1	0	0	0	0	0	0	0	OSA 0 [8]	OSA 0 [7]	OSA 0 [6]	OSA 0 [5]	OSA 0 [4]	OSA 0 [3]	OSA 0 [2]	OSA 0 [1]	OSA 0 [0]
R502	W	1	0	0	0	0	0	0	0	OEA 0 [8]	OEA 0 [7]	OEA 0 [6]	OEA 0 [5]	OEA 0 [4]	OEA 0 [3]	OEA 0 [2]	OEA 0 [1]	OEA 0 [0]
R503	W	1	0	0	0	0	0	0	0	ODP 1 [8]	ODP 1 [7]	ODP 1 [6]	ODP 1 [5]	ODP 1 [4]	ODP 1 [3]	ODP 1 [2]	ODP 1 [1]	ODP 1 [0]
R504	W	1	0	0	0	0	0	0	0	OSA 1 [8]	OSA 1 [7]	OSA 1 [6]	OSA 1 [5]	OSA 1 [4]	OSA 1 [3]	OSA 1 [2]	OSA 1 [1]	OSA 1 [0]
R505	W	1	0	0	0	0	0	0	0	OEA 1 [8]	OEA 1 [7]	OEA 1 [6]	OEA 1 [5]	OEA 1 [4]	OEA 1 [3]	OEA 1 [2]	OEA 1 [1]	OEA 1 [0]
R506	W	1	0	0	0	0	0	0	0	ODP 2 [8]	ODP 2 [7]	ODP 2 [6]	ODP 2 [5]	ODP 2 [4]	ODP 2 [3]	ODP 2 [2]	ODP 2 [1]	ODP 2 [0]
R507	W	1	0	0	0	0	0	0	0	OSA 2 [8]	OSA 2 [7]	OSA 2 [6]	OSA 2 [5]	OSA 2 [4]	OSA 2 [3]	OSA 2 [2]	OSA 2 [1]	OSA 2 [0]
R508	W	1	0	0	0	0	0	0	0	OEA 2 [8]	OEA 2 [7]	OEA 2 [6]	OEA 2 [5]	OEA 2 [4]	OEA 2 [3]	OEA 2 [2]	OEA 2 [1]	OEA 2 [0]

ODP0[8:0]: ODP0 : Set the display position of OSD image 1.
ODP1[8:0]: ODP1 : Set the display position of OSD image 2.
ODP2[8:0]: ODP2 : Set the display position of OSD image 3.

The display areas for OSD images 1, 2, 3 should not overlap one another. Set each area as follows.

Display area of OSD image 1: ODP0, ODP0+(OEA0 – OSA0)
Display area of OSD image 2: ODP1, ODP1+(OEA1 – OSA1)
Display area of OSD image 3: ODP2, ODP2+(OEA2 – OSA2)

Make sure that
display area of OSD image 1 < Display area of OSD image 2 < Display area of OSD image 3.

If ODP0 is set "9'h000", OSD image 1 is displayed from the start line of the base image on the first panel. The OSD is not available during interlaced drive (FLD = 2'h3).

OSA0[8:0] OEA0[8:0]: OSA0, OEA0 : Set the start line address and end line address for display RAM area of the OSD image 1.

OSA1[8:0] OEA1[8:0]: OSA1, OEA1 : Set the start line address and end line address for display RAM area of the OSD image 2.

OSA2[8:0] OEA2[8:0]: OSA2, OEA2 : Set the start line address and end line address for display RAM area of the OSD image 3.

Instruction list

Main Category		Sub Category		Upper Code								Lower Code								Note
Upper bits of Index		Index	Command	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	
-	Index	—	Index	*	*	*	*	*	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID21	ID0	
SR	Status Read	—	Status Read	0	0	0	0	0	0	0	L8	L7	L6	L5	L4	L3	L2	L1	L0	
0**	Display Control System	000h	Start Oscillation	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1	
			Device Code Read	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	1	
		001h	Driver Output Control	0	0	0	LTPS (0)	0	0	0	SS (0)	0	0	0	0	0	0	0	0	
		002h	Liquid Crystal Drive Alternating Control	0	0	0	0	FLD[1] (0)	FLD[0] (1)	B/C (0)	EOR (0)	0	0	NW[5] (0)	NW[4] (0)	NW[3] (0)	NW[2] (0)	NW[1] (0)	NW[0] (0)	
		003h	Entry Mode	TRI (0)	DFM (0)	0	BGR (0)	0	0	HWM (0)	0	0	0	ID[1] (1)	ID[0] (1)	AM (0)	0	OSD (0)	ODF (0)	
		004h	Resizing Control (1)	0	0	0	0	0	0	RCV[1] (0)	RCV[0] (0)	0	0	RCH[1] (0)	RCH[0] (0)	0	0	RSR[1] (0)	RSR[0] (0)	
		005h	Resizing Control (2)	RSEV[7] (0)	RSEV[6] (0)	RSEV[5] (0)	RSEV[4] (0)	RSEV[3] (0)	RSEV[2] (0)	RSEV[1] (0)	RSEV[0] (0)	0	0	0	0	0	0	0	RSEH (0)	
		006h	Setting Disabled																	
		007h	Display Control (1)	0	OSDE[2] (0)	OSDE[1] (0)	OSDE[0] (0)	0	0	0	BASEE (0)	0	0	0	DTE (0)	0	0	D[1] (0)	D[0] (0)	
		008h	Display Control (2)	0	0	0	0	FP[3] (1)	FP[2] (0)	FP[1] (0)	FP[0] (0)	0	0	0	0	BP[3] (1)	BP[2] (0)	BP[1] (0)	BP[0] (0)	
		009h	Display Control (3)	0	0	0	0	0	PTS[2] (0)	PTS[1] (0)	PTS[0] (0)	0	0	PTG[1] (0)	PTG[0] (0)	ISC[3] (0)	ISC[2] (0)	ISC[1] (0)	ISC[0] (0)	
		00Ah	Setting Disabled																	
		00Bh	Display Control (4)	0	FRCON (0)	D16B (0)	0	0	0	0	0	0	0	0	0	0	0	COL[1] (0)	COL[0] (0)	
		00Ch	External Display Interface Control (1	0	0	0	0	0	0	0	RM (0)	0	0	DM[1] (0)	DM[0] (0)	0	0	RIM[1] (0)	RIM[0] (0)	
		00Dh	Frame Cycle Adjustment Contro	0	0	0	0	0	0	DIVI[1] (0)	DIVI[0] (0)	0	0	0	RTNI[4] (1)	RTNI[3] (0)	RTNI[2] (0)	RTNI[1] (0)	RTNI[0] (0)	
		00Eh	External Display Interface Control (2	0	0	0	0	0	0	DIVE[1] (1)	DIVE[0] (0)	0	RTNE[6] (0)	RTNE[5] (0)	RTNE[4] (1)	RTNE[3] (1)	RTNE[2] (1)	RTNE[1] (1)	RTNE[0] (0)	
		00Fh	External Display Interface Control (3	0	0	0	0	0	0	0	0	0	0	0	VSPL (0)	HSPL (0)	0	EPL (0)	DPL (0)	
		010h	Gate Driver/LTPS Liquid Crystal Panel Interface Control (1)	0	0	0	FWI[4] (0)	FWI[3] (0)	FWI[2] (0)	FWI[1] (0)	FWI[0] (0)	0	0	0	0	0	0	FTI[1] (0)	FTI[0] (0)	
		011h	Gate Driver/LTPS Liquid Crystal Panel Interface Control (2)	0	0	0	SWI[4] (0)	SWI[3] (0)	SWI[2] (0)	SWI[1] (0)	SWI[0] (0)	0	0	0	0	0	0	STI[1] (0)	STI[0] (0)	
		012h	Gate Driver/LTPS Liquid Crystal Panel Interface Control (3)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SDTI[1] (0)	SDTI[0] (0)	
		013h	Gate Driver/LTPS Liquid Crystal Panel Interface Control (4)	0	0	0	DPWI[4] (0)	DPWI[3] (0)	DPWI[2] (0)	DPWI[1] (0)	DPWI[0] (0)	0	0	0	0	0	0	DPTI[1] (0)	DPTI[0] (0)	
		014h	Setting Disabled																	
		015h	Gate Driver/LTPS Liquid Crystal Panel Interface Control (5)	0	0	0	0	0	0	EQWI[1] (0)	EQWI[0] (0)	0	0	0	0	0	0	0	0	
		016h	Gate Driver/LTPS Liquid Crystal Panel Interface Control (6)	0	0	FWE[5] (0)	FWE[4] (0)	FWE[3] (0)	FWE[2] (0)	FWE[1] (0)	FWE[0] (0)	0	0	0	0	0	FTE[2] (0)	FTE[1] (0)	FTE[0] (0)	
		017h	Gate Driver/LTPS Liquid Crystal Panel Interface Control (7)	0	0	SWE[5] (0)	SWE[4] (0)	SWE[3] (0)	SWE[2] (0)	SWE[1] (0)	SWE[0] (0)	0	0	0	0	0	STE[2] (0)	STE[1] (0)	STE[0] (0)	
		018h	Gate Driver/LTPS Liquid Crystal Panel Interface Control (8)	0	0	0	0	0	0	0	0	0	0	0	0	0	SDTE[2] (0)	SDTE[1] (0)	SDTE[0] (0)	
		019h	Gate Driver/LTPS Liquid Crystal Panel Interface Control (9)	0	0	DPWE[5] (0)	DPWE[4] (0)	DPWE[3] (0)	DPWE[2] (0)	DPWE[1] (0)	DPWE[0] (0)	0	0	0	0	0	DPTE[2] (0)	DPTE[1] (0)	DPTE[0] (0)	
		01Ah	Setting Disabled																	
		01Bh	Gate Driver/LTPS Liquid Crystal Panel Interface Control (10)	0	0	0	0	0	EQWE[2] (0)	EQWE[1] (0)	EQWE[0] (0)	0	0	0	0	0	0	0	0	
		01Ch-0FFh	Setting Disabled																	
1**	Power Control System	100h	Power Control (1)	DC[4] (0)	DC[3] (0)	0	0	0	SAP[2] (0)	SAP[1] (0)	SAP[0] (0)	0	AP[2] (0)	AP[1] (0)	AP[0] (0)	0	DSTB (0)	SLP (0)	STB (0)	
		102h-10Fh	Setting Disabled																	
	(Gate Driver / Power Supply IC Interface)	110h	Gate Driver / Power Supply IC I/F Control (1)	0	0	0	0	0	0	0	TE (0)	0	0	0	0	0	IDX[2] (0)	IDX[1] (0)	IDX[0] (0)	
		111h	Gate Driver / Power Supply IC I/F Control (2)	0	0	0	TB[12] (0)	TB[11] (0)	TB[10] (0)	TB[9] (0)	TB[8] (0)	TB[7] (0)	TB[6] (0)	TB[5] (0)	TB[4] (0)	TB[3] (0)	TB[2] (0)	TB[1] (0)	TB[0] (0)	
		112h-1FFh	Setting Disabled																	
2**	RAM Access System	200h	RAM Address Set (1)	0	0	0	0	0	0	0	0	AD[7] (0)	AD[6] (0)	AD[5] (0)	AD[4] (0)	AD[3] (0)	AD[2] (0)	AD[1] (0)	AD[0] (0)	
		201h	RAM Address Set (2)	0	0	0	0	0	0	0	AD[16] (0)	AD[15] (0)	AD[14] (0)	AD[13] (0)	AD[12] (0)	AD[11] (0)	AD[10] (0)	AD[9] (0)	AD[8] (0)	
		202h	RAM Data Write / Read	RAM Write Data (WD17-0) or RAM Read Data (RD17-0) Bit assignment will change according to the selected interface.																
		203h	RAM Write Data Mask (1)	0	0	WM[11] (0)	WM[10] (0)	WM[9] (0)	WM[8] (0)	WM[7] (0)	WM[6] (0)	0	0	WM[5] (0)	WM[4] (0)	WM[3] (0)	WM[2] (0)	WM[1] (0)	WM[0] (0)	
		204h	RAM Write Data Mask (2)	0	0	0	0	0	0	0	0	0	0	WM[17] (0)	WM[16] (0)	WM[15] (0)	WM[14] (0)	WM[13] (0)	WM[12] (0)	
		205h-20Fh	Setting Disabled																	
	Window Address Control System	210h	Horizontal RAM Address Poseition (1)	0	0	0	0	0	0	0	0	HSA[7] (0)	HSA[6] (0)	HSA[5] (0)	HSA[4] (0)	HSA[3] (0)	HSA[2] (0)	HSA[1] (0)	HSA[0] (0)	
		211h	Horizontal RAM Address Poseition (2)	0	0	0	0	0	0	0	0	HEA[7] (1)	HEA[6] (1)	HEA[5] (1)	HEA[4] (1)	HEA[3] (1)	HEA[2] (1)	HEA[1] (1)	HEA[0] (1)	
		212h	Vertical RAM Address Poseition (1)	0	0	0	0	0	0	0	VSA[8] (0)	VSA[7] (0)	VSA[6] (0)	VSA[5] (0)	VSA[4] (0)	VSA[3] (0)	VSA[2] (0)	VSA[1] (0)	VSA[0] (0)	
		213h	Vertical RAM Address Poseition (2)	0	0	0	0	0	0	0	VEA[8] (1)	VEA[7] (0)	VEA[6] (0)	VEA[5] (1)	VEA[4] (1)	VEA[3] (1)	VEA[2] (1)	VEA[1] (1)	VEA[0] (1)	
		214h-2FFh	Setting Disabled																	
3**	γ Control	300h	Control (1)	0	0	0	0	0	PKP1[2] (0)	PKP1[1] (0)	PKP1[0] (0)	0	0	0	0	0	PKP0[2] (0)	PKP0[1] (0)	PKP0[0] (0)	
		301h	Control (2)	0	0	0	0	0	PKP3[2] (0)	PKP3[1] (0)	PKP3[0] (0)	0	0	0	0	0	PKP2[2] (0)	PKP2[1] (0)	PKP2[0] (0)	
		302h	Control (3)	0	0	0	0	0	PKP5[2] (0)	PKP5[1] (0)	PKP5[0] (0)	0	0	0	0	0	PKP4[2] (0)	PKP4[1] (0)	PKP4[0] (0)	
		303h	Control (4)	0	0	0	0	0	PRP1[2] (0)	PRP1[1] (0)	PRP1[0] (0)	0	0	0	0	0	PRP0[2] (0)	PRP0[1] (0)	PRP0[0] (0)	
		304h	Control (5)	0	0	0	VRP1[4] (0)	VRP1[3] (0)	VRP1[2] (0)	VRP1[1] (0)	VRP1[0] (0)	0	0	0	0	VRP0[3] (0)	VRP0[2] (0)	VRP0[1] (0)	VRP0[0] (0)	
		305h	Control (6)	0	0	0	0	0	PKN1[2] (0)	PKN1[1] (0)	PKN1[0] (0)	0	0	0	0	0	PKN0[2] (0)	PKN0[1] (0)	PKN0[0] (0)	
		306h	Control (7)	0	0	0	0	0	PKN3[2] (0)	PKN3[1] (0)	PKN3[0] (0)	0	0	0	0	0	PKN2[2] (0)	PKN2[1] (0)	PKN2[0] (0)	
		307h	Control (8)	0	0	0	0	0	PKN5[2] (0)	PKN5[1] (0)	PKN5[0] (0)	0	0	0	0	0	PKN4[2] (0)	PKN4[1] (0)	PKN4[0] (0)	
		308h	Control (9)	0	0	0	0	0	PRN1[2] (0)	PRN1[1] (0)	PRN1[0] (0)	0	0	0	0	0	PRN0[2] (0)	PRN0[1] (0)	PRN0[0] (0)	
		309h	Control (10)	0	0	0	VRN1[4] (0)	VRN1[3] (0)	VRN1[2] (0)	VRN1[1] (0)	VRN1[0] (0)	0	0	0	0	VRN0[3] (0)	VRN0[2] (0)	VRN0[1] (0)	VRN0[0] (0)	
		30Ah-3FFh	Setting Disabled																	
4**	Coordinate Control System	400h	Line Number Control	0	0	0	0	0	0	0	0	0	0	NL[5] (1)	NL[4] (0)	NL[3] (0)	NL[2] (1)	NL[1] (1)	NL[0] (1)	
		401h	Screen Control	0	0	0	0	0	0	0	0	0	0	0	0	0	0	VLE (0)	REV (0)	
		402h	Base Picture RAM Area (Start Line)	0	0	0	0	0	0	0	BSA[8] (0)	BSA[7] (0)	BSA[6] (0)	BSA[5] (0)	BSA[4] (0)	BSA[3] (0)	BSA[2] (0)	BSA[1] (0)	BSA[0] (0)	
		403h	Base Picture RAM Area (End Line)	0	0	0	0	0	0	0	BEA[8] (1)	BEA[7] (0)	BEA[6] (0)	BEA[5] (1)	BEA[4] (1)	BEA[3] (1)	BEA[2] (1)	BEA[1] (1)	BEA[0] (1)	
		404h	Vertical Scroll Control	0	0	0	0	0	0	0	VL[8] (0)	VL[7] (0)	VL[6] (0)	VL[5] (0)	VL[4] (0)	VL[3] (0)	VL[2] (0)	VL[1] (0)	VL[0] (0)	
		405h	Base Picture 1RAM Magnified Area (Start Line)	0	0	0	0	0	0	0	ESA[8] (0)	ESA[7] (0)	ESA[6] (0)	ESA[5] (0)	ESA[4] (0)	ESA[3] (0)	ESA[2] (0)	ESA[1] (0)	ESA[0] (0)	
		406h	Base Picture 2RAM Magnified Area (End Line)	0	0	0	0	0	0	0	EEA[8] (0)	EEA[7] (0)	EEA[6] (0)	EEA[5] (0)	EEA[4] (0)	EEA[3] (0)	EEA[2] (0)	EEA[1] (0)	EEA[0] (0)	
		407h-4Fh	Setting Disabled																	
5**	OSD Control	500h	OSD Picture 1 Display Position	0	0	0	0	0	0	0	ODP0[8] (0)	ODP0[7] (0)	ODP0[6] (0)	ODP0[5] (0)	ODP0[4] (0)	ODP0[3] (0)	ODP0[2] (0)	ODP0[1] (0)	ODP0[0] (0)	
		501h	OSD Picture1 RAM Area (Start Line)	0	0	0	0	0	0	0	OSA0[8] (0)	OSA0[7] (0)	OSA0[6] (0)	OSA0[5] (0)	OSA0[4] (0)	OSA0[3] (0)	OSA0[2] (0)	OSA0[1] (0)	OSA0[0] (0)	
		502h	OSD Picture 1 RAM Area (End Line)	0	0	0	0	0	0	0	OEA0[8] (0)	OEA0[7] (0)	OEA0[6] (0)	OEA0[5] (0)	OEA0[4] (0)	OEA0[3] (0)	OEA0[2] (0)	OEA0[1] (0)	OEA0[0] (0)	
		503h	OSD Picture 2 Display Position	0	0	0	0	0	0	0	ODP1[8] (0)	ODP1[7] (0)	ODP1[6] (0)	ODP1[5] (0)	ODP1[4] (0)	ODP1[3] (0)	ODP1[2] (0)	ODP1[1] (0)	ODP1[0] (0)	
		504h	OSD Picture 2 RAM Area (Start Line)	0	0	0	0	0	0	0	OSA1[8] (0)	OSA1[7] (0)	OSA1[6] (0)	OSA1[5] (0)	OSA1[4] (0)	OSA1[3] (0)	OSA1[2] (0)	OSA1[1] (0)	OSA1[0] (0)	
		505h	OSD Picture 2 RAM Area (End Line)	0	0	0	0	0	0	0	OEA1[8] (0)	OEA1[7] (0)	OEA1[6] (0)	OEA1[5] (0)	OEA1[4] (0)	OEA1[3] (0)	OEA1[2] (0)	OEA1[1] (0)	OEA1[0] (0)	
		506h	OSD Picture 3 Display Position	0	0	0	0	0	0	0	ODP2[8] (0)	ODP2[7] (0)	ODP2[6] (0)	ODP2[5] (0)	ODP2[4] (0)	ODP2[3] (0)	ODP2[2] (0)	ODP2[1] (0)	ODP2[0] (0)	
		507h	OSD Picture 3 RAM Area (Start Line)	0	0	0	0	0	0	0	OSA2[8] (0)	OSA2[7] (0)	OSA2[6] (0)	OSA2[5] (0)	OSA2[4] (0)	OSA2[3] (0)	OSA2[2] (0)	OSA2[1] (0)	OSA2[0] (0)	
		508h	OSD Picture 3 RAM Area (End Line)	0	0	0	0	0	0	0	OEA2[8] (0)	OEA2[7] (0)	OEA2[6] (0)	OEA2[5] (0)	OEA2[4] (0)	OEA2[3] (0)	OEA2[2] (0)	OEA2[1] (0)	OEA2[0] (0)	
		509h-5FFh	Setting Disabled																	
6**		600h-6FFh	Setting Disabled																	

Note 1) Numerals in parentheses in instruction bit cells are initial value. 。
Note 2) Do not try to access to the index where setting is disabled.

HD66783 Instruction Table

IDX[2]	IDX[1]	IDX[0]	TB[12]	TB[11]	TB[10]	TB[9]	TB[8]	TB[7]	TB[6]	TB[5]	TB[4]	TB[3]	TB[2]	TB[1]	TB[0]
0	0	0	0	GON	VCOMG	BT[2]	BT[1]	BT[0]	DC0[2]	DC0[1]	DC0[0]	AP[2]	AP[1]	AP[0]	0
0	0	1	0	DK	1	EQM	0	PON	VRH[3]	VRH[2]	VRH[1]	VRH[0]	VC[2]	VC[1]	VC[0]
0	1	0	DC1[2]	DC1[1]	DC1[0]	VDV[4]	VDV[3]	VDV[2]	VDV[1]	VDV[0]	VCM[4]	VCM[3]	VCM[2]	VCM[1]	VCM[0]
0	1	1	Setting Disabled												
1	0	0	Setting Disabled												
1	0	1	Setting Disabled												
1	1	0	GS	NL[5]	NL[4]	NL[3]	NL[2]	NL[1]	NL[0]	SCN[5]	SCN[4]	SCN[3]	SCN[2]	SCN[1]	SCN[0]
1	1	1	0	0	0	0	0	0	0	0	0	0	0	FLD[1]	FLD[0]

HD667P21 Instruction Table

IDX[2]	IDX[1]	IDX[0]	TB[12]	TB[11]	TB[10]	TB[9]	TB[8]	TB[7]	TB[6]	TB[5]	TB[4]	TB[3]	TB[2]	TB[1]	TB[0]
0	0	0	0	GON	VCOMG	BT[2]	BT[1]	BT[0]	DC[2]	DC[1]	DC[0]	AP[2]	AP[1]	AP[0]	0
0	0	1	0	0	0	0	0	PON	VRH[3]	VRH[2]	VRH[1]	VRH[0]	VC[2]	VC[1]	VC[0]
0	0	1	0	1	0	DK[1]	DK[0]	0	0	0	0	0	0	0	0
0	1	0	0	0	0	VDV[4]	VDV[3]	VDV[2]	VDV[1]	VDV[0]	VCM[4]	VCM[3]	VCM[2]	VCM[1]	VCM[0]
0	1	1	Setting Disabled												
1	0	0	Setting Disabled												
1	0	1	Setting Disabled												
1	1	0	Setting Disabled												
1	1	1	0	0	VGL[4]	VGL[3]	VGL[2]	VGL[1]	VGL[0]	0	VGH[4]	VGH[3]	VGH[2]	VGH[1]	VGH[0]

AP and NL require a same and separate setting for each HD66781
and the register to transfer (Different Setting Disabled).

1. Setting for AP register of 781
2. Setting for AP register of 783/7P21 (R111h,TB[3]-[1])
3. Serial Transfer to 783/7P21 (IDX000)

1. Setting for NL register of 781
2. Setting for NL register of 783 (R111h TB[11]-[6])
3. Serial Transfer to 783 (IDX110)

1. Setting for FLD register of 781
2. Setting for FLD register of 783 (R111h TB[1]-[0])
3. Serial Transfer to 783 (IDX111)

Reset Function

The HD66781 is internally initialized by RESET input. During the reset period, internal settings are initialized. No access to instructions or GRAM data from the MPU is accepted during the reset period. The gate driver and the power supply are also automatically initialized when RESET input enters into the HD66781. The RESET period must be secured for at least 1 ms. In case of resetting by turning on the power supply (power-on reset), wait until the R-C oscillation frequency becomes stable after power is supplied (10 ms). During this period, do not access GRAM or make any initial instruction setting.

Instruction Set Initialization

See the parenthetic number in each bit in the instruction list for the initial value.

RAM Data Initialization

The RAM data are not automatically initialized by RESET input and must be initialized by software during the display-off period (D1–0 = 00).

Output Pin Initialization

1. LCD driver output pins (source outputs) : Output GND level (All pins)
2. Vcom : Halt (Output GND)
3. Gate driver control signal : Halt (Output GND)
   (FLM1, FLM2, CL11/SFTCLK11, CL12/SFTCLK12, SFTCLK21, SFTCLK22, M1, M2, DISPTMG1, DISPTMG2, EQ1, EQ2, DCCLK1, DCCLK2)
4. Gate driver serial interface : Halt GCS, GCL, GDA (Vcc1 output)
5. Oscillator output pin : Oscillate
6. Synchronizing signal (BST) : Output GND
7. RESET signal output : Same polarity with the RESET* input

RAM Address and Display Position on the Panel

The HD66781 incorporates a memory for 240RGB x 416-line display, and enables to drive QVGA-size panel (240RGB x 320 lines). Unused display memory is available for a partial OSD area. These features realize various ways of display with a single chip.

The HD66781 allows independent settings for the display panel and the drive position, where the RAM area of each image is specified in relation to the display panel that is assigned to gate pins to fit into the assembly. Accordingly, in designing a panel, it is not necessary to take the assembly position into account.

The HD66781 allows realizes various ways of display with the following settings:

1. Specify the RAM area of a base image (BSA, BEA)
2. Specify the RAM area of an OSD image (OSAx, OEAx)
3. Specify the display position of the OSD image (step 2) on the panel (ODPx).
4. Specify the gate pins for driving the panel displaying a base image (SCN, NL) and the scan order (GS).
5. Execute display ENABLE (BASEE, OSDE0/1/2) for each image after turning on display.

A base image is a display that is set to be a basic display on each panel. An OSD image is a picture that is set to display on the base image. The panel-drive settings are made with gate scan starting position (SCN), the number of raster-rows to drive (NL), and scan direction (GS). The gate scan direction can be set differently for each panel to fit into the assembly. To change the display position horizontally, the setting of SS bit is required during RAM write.

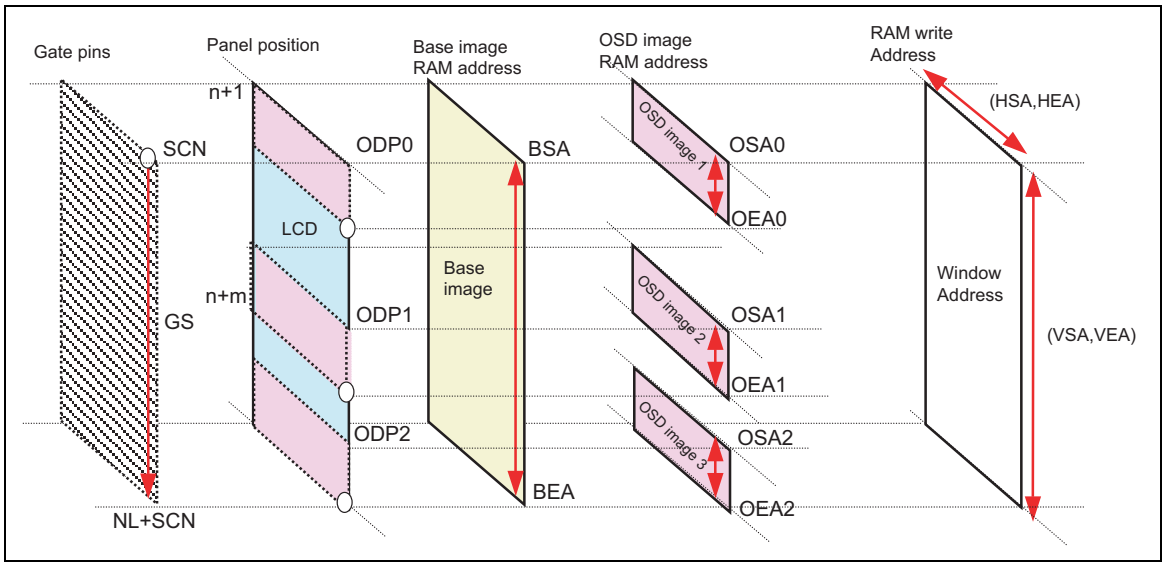
Table 53

	Display ENABLE	**Numbers of lines**	**RAM area**
(Base image 1)	BASEE	NL	(BSA, BEA)

Note 1) The base image is displayed from the start line of each panel.
Note 2) Make sure that base image RAM area is NL ≤ BEA – BSA.

Table 54

	Display ENABLE	**Display position**	**RAM area**
OSD image 1	OSDE0	ODP0	(OSA0, OEA0)
OSD image 2	OSDE1	ODP1	(OSA1, OEA1)
OSD image 3	OSDE2	ODP2	(OSA2, OEA2)



RAM Address, display position and drive position

Notes to the setting of panel control registers

The HD66781 has some constrains in setting the coordinate with regard to the display data, position, and OSD.

Screen settings

The following equation must be observed in making a setting for the screen.

$NL \leq 320$ lines
$0 \leq SCN < SCN+NL \leq 320$ lines

Base image display

Base image is displayed from the first line of each panel. Base image display start position: SCN = BSA

Set the base image RAM area (BSA, BEA) equal to or more than the number of lines (NL) required driving a panel. $NL \leq BEA - BSA$

OSD image display

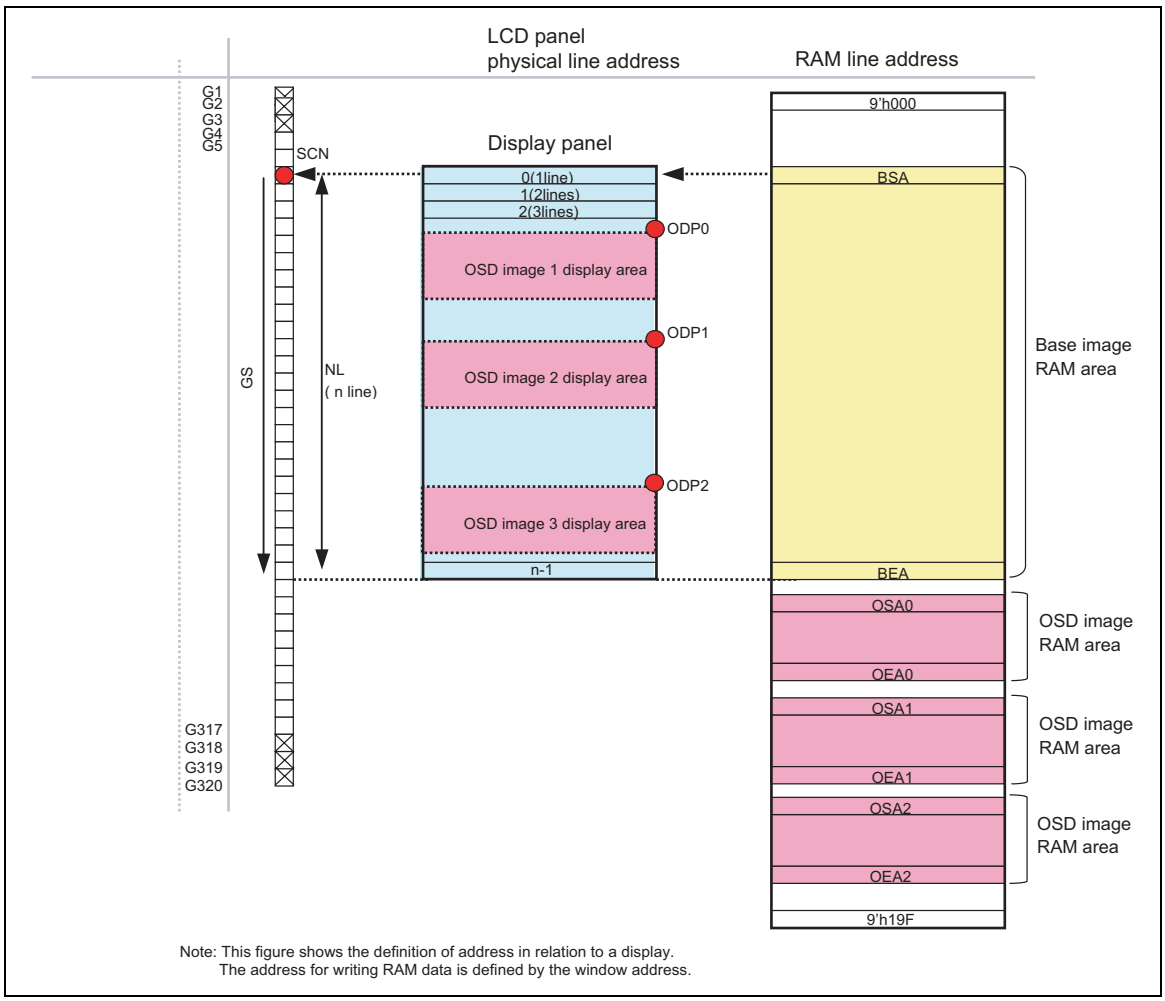
Set the OSD image RAM area (OSAx, OEAx) not to overlap one another. Set the OSD positions not to overlap one another.

$0 \leq ODP0 \leq ODP0 + n \times (OEA0 - OSA0 + 1) - 1 <$
$ODP1 \leq ODP1 + n \times (OEA1 - OSA1 + 1) - 1 <$
$ODP2 \leq ODP2 + n \times (OEA2 - OSA2 + 1) - 1 \leq NL$

n: OSD image magnification scale

The OSD images are displayed 100% when base image is turned off (BASEE = 0). The arrangement of α channels is also changed when changing RGB order to BGR. The OSD data are read out in the format when ODF is set to 0. During interlaced drive (FLD = 2'h3), OSD and α blending functions are not available.

Following figure shows the relationship among RAM address, display position, and panel drive.



Display RAM address and panel display position

OSD and α blending functions

The HD66781 incorporates OSD and α blending functions. The OSD image data has 3 α bits to select transmission rates among 0, 25, 50, 75, 100%. The HD66781 not only handles 32,678-color OSD at maximum but also enables picture display data as OSD, in addition to usual single color text display. The HD66781 realizes various ways of display with a single-chip configuration.

The HD66781 eliminates the processing of OSD and α blending from the microcomputer. Just transmitting OSD image data including α bits into the LCD driver as usual enables OSD and α blending display.

OSD and α blending processing

The HD66781 writes data to RAM as an OSD image according to the setting of OSD bit. An image read out as OSD according to the OSD image display setting is displayed after being processed according to the transmission rate set by α bits. OSD and α blending settings can be made by pixels (RGB).

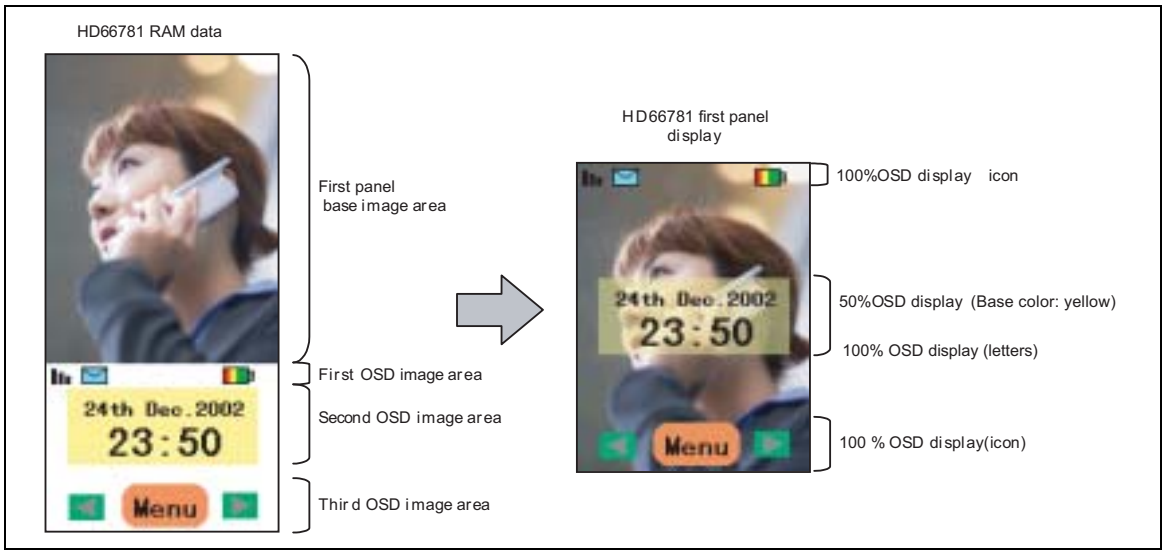
Table 55

α2	α1	α0	Transmission rate	Picture processing (Display data)	Picture processing (Display data)
0	0	0	0%	Base image display	Base image x 1.0 + OSD image x 0
0	0	1	-	Setting disabled	-
0	1	0	25%	Base image (75%) + OSD image (25%) display	25% transmission
0	1	1	75%	Base image (25%) + OSD image (75%) display	75% transmission
1	0	0	50%	Base image (50%) + OSD image (50%) display	Base image x 0.5 + OSD image x 0.5
1	0	1	-	Setting disabled	-
1	1	0	100%	OSD image display	Base image x 0 + OSD image x 1.0
1	1	1	-	Setting disabled	-

Note 1) The OSD image is displayed 100% when base image is turned off (BASEE = 0).

OSD and α blending processing

The following is an example of display with OSD and α blending functions with the HD66781. In the following example, the unused RAM area, which is not used for base image display, is used for OSD and α blending RAM area.



Display with OSD and α blending

OSD image data format

OSD image data format (α bit arrangement) is changeable with ODF bits. Select an appropriate format for the system to process. When writing an OSD image to RAM, set OSD to 1 beforehand. Specify the RAM write area by the window address.

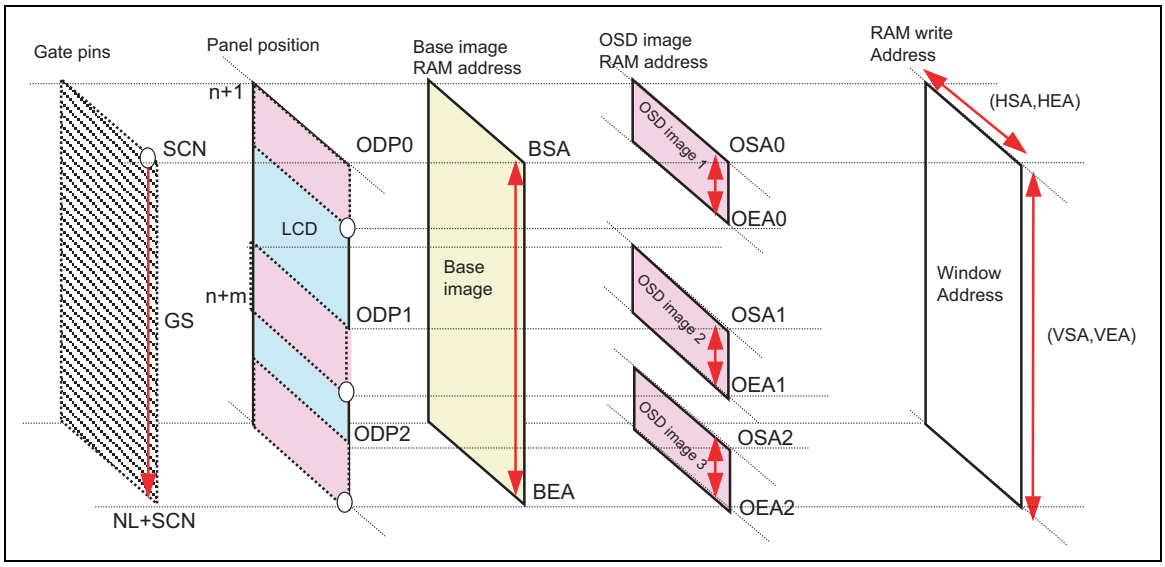
OSD image data format

ODF	D 17	D 16	D 15	D 14	D 13	D 12	D 11	D 10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	R5	R4	R3	R2	R1	α2	G5	G4	G3	G2	G1	α1	B5	B4	B3	B2	B1	α0
1	α2	α1	α0	R4	R3	R2	R1	R0	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
Normal data	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

OSD image display setting

To make a setting for OSD image display,

1. Specify OSD RAM area (OSA, OEA)
2. Specify OSD position
3. Set OSD ENABLE (OSDE)



RAM Address, display position, drive position

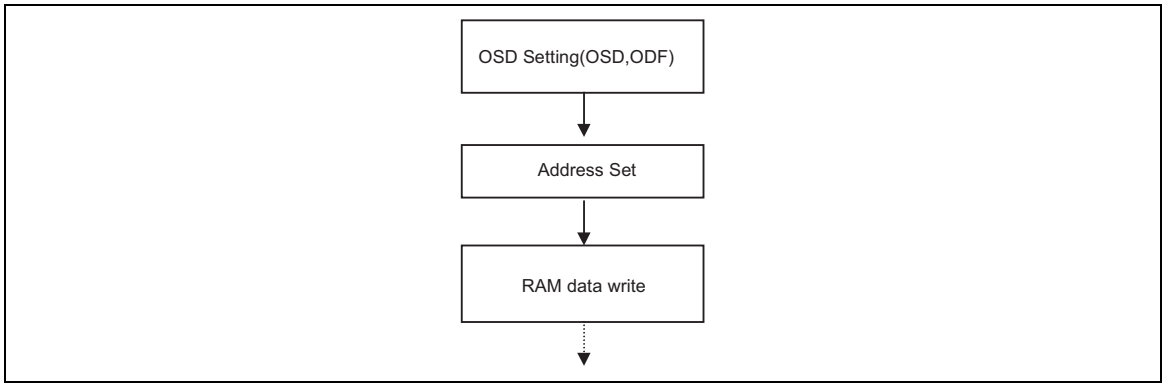
Whenever making an OSD image setting, the following must be observed.

1. Set the OSD RAM area with OSAx, OEAx not to overlap one another.
2. Set the OSD position so that an OSD image does not overlap one another.

$$0 \le ODP0 \le ODP0+n \times (OEA0 - OSA0+1) - 1 <$$
$$ODP1 \le ODP1+ n \times (OEA1 - OSA1+1) - 1 <$$
$$ODP2 \le ODP2+ n \times (OEA2 - OSA2+1) - 1 \le NL$$

"n" is a magnification scale of an OSD image.

3. An OSD image is displayed 100% when the base image is turned off (BASEE = 0).
4. During the interlaced drive (FLD = 2'h3), the OSD and α blending functions are not available.



OSD data write flow

Resizing function

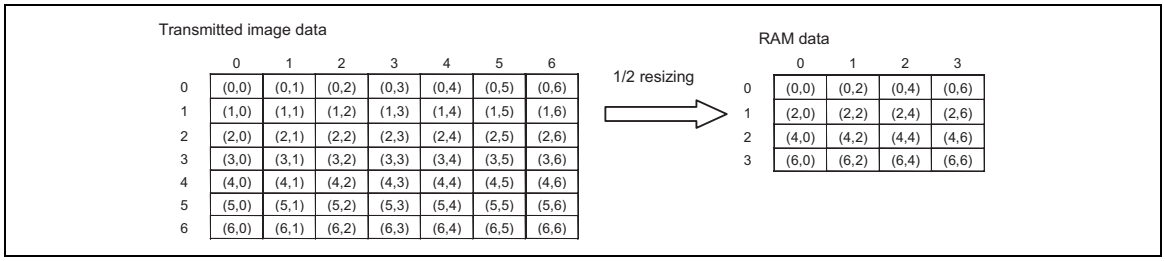
The HD66781 incorporates resizing function (contraction: x 1/2, x 1/4, magnification: x2) available when writing picture data.

Contraction

The HD66781 enables to write resized image data to RAM by simply transmitting original image data to the window address as usual with the setting of RSR bit that specifies the contraction rate.

This means the HD66781 allows the system simply to transmit data as usual even if resizing is required, and therefore makes resized images easily available on cameras, sub panels, or as a thumbnail display of a picture.

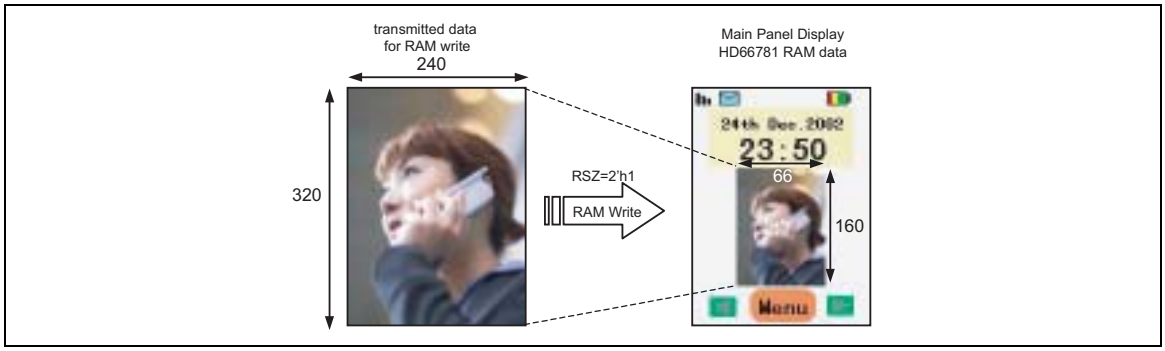
The HD66781 performs contraction resizing simply by selecting pixels. The resized image may seem distorted from the original image. Check the resized image before use.



	0	1	2	3	4	5	6
0	(0,0)	(0,1)	(0,2)	(0,3)	(0,4)	(0,5)	(0,6)
1	(1,0)	(1,1)	(1,2)	(1,3)	(1,4)	(1,5)	(1,6)
2	(2,0)	(2,1)	(2,2)	(2,3)	(2,4)	(2,5)	(2,6)
3	(3,0)	(3,1)	(3,2)	(3,3)	(3,4)	(3,5)	(3,6)
4	(4,0)	(4,1)	(4,2)	(4,3)	(4,4)	(4,5)	(4,6)
5	(5,0)	(5,1)	(5,2)	(5,3)	(5,4)	(5,5)	(5,6)
6	(6,0)	(6,1)	(6,2)	(6,3)	(6,4)	(6,5)	(6,6)

	0	1	2	3
0	(0,0)	(0,2)	(0,4)	(0,6)
1	(2,0)	(2,2)	(2,4)	(2,6)
2	(4,0)	(4,2)	(4,4)	(4,6)
3	(6,0)	(6,2)	(6,4)	(6,6)

Resizing: contraction



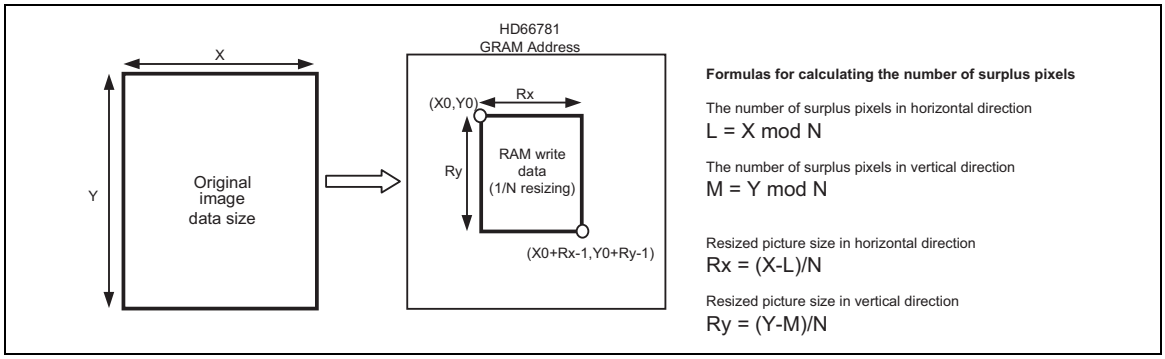
Resizing transmission, display example

Table 56

Original image size (X x Y)	Resized image size	
	1/2 (RSZ = 2'h1)	1/4 (RSZ = 2'h3)
640x480(VGA)	320x240	160x120
352x268 (CIF)	176x144	88x72
320x240 (QVGA)	160x120	80x60
176x144 (QCIF)	88x72	44x36
120x160	60x80	30x40
132x176	66x88	33x44

Resizing setting

The HD66781 selects resizing (contraction) rate according to the setting of RSR bit. Specify the RAM window-address range to fit into the resized picture. If resizing creates surplus pixels according to the result of calculation using the following formulas, set them in RCV, RCH registers before writing data to RAM.



Resizing Setting, surplus pixel calculation

Table 57

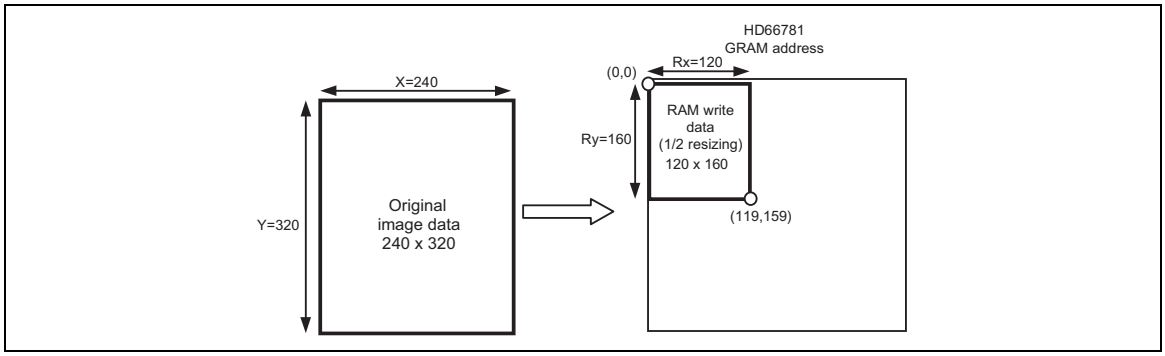
Original image (before resizing)

number of data in horizontal direction	X
number of data in vertical direction	Y
resizing ratio	1/N

HD66781 settings

Resizing setting	RSR	N-1
number of data in horizontal direction	RCV	L
number of data in vertical direction	RCH	M

RAM writing start address	AD	(X0, Y0)
RAM window address	HSA	X0
	HEA	X0+Rx - 1
	VSA	Y0
	VEA	Y0+Ry - 1



Resizing setting example (1/2 size)

Table 58

Original image (before resizing)

number of data in horizontal direction	X	240
number of data in vertical direction	Y	320
resizing ratio	1/N	1/2

HD66781 settings

Resizing setting	RSR	2'h1
number of data in horizontal direction	RCV	2'h0
number of data in vertical direction	RCH	2'h0

RAM writing start address	AD	17'h00000
RAM window address	HSA	8'h00
	HEA	8'h77
	VSA	8'h00
	VEA	8'h9F

Instructions for Resizing

Table 59 Resizing ratio

RSR[1:0]	ratio
2h'0	No resizing (x 1)
2h'1	1/2 resizing (x 1/2)
2h'2	setting disabled
2h'3	1/4 resizing (x 1/4)

Table 60 Surplus pixels

vertical direction

RCV[1:0]	surplus pixels
2h'0	0
2h'1	1 pixel
2h'2	2 pixels
2h'3	3 pixels

1 pixel = 1 RGB

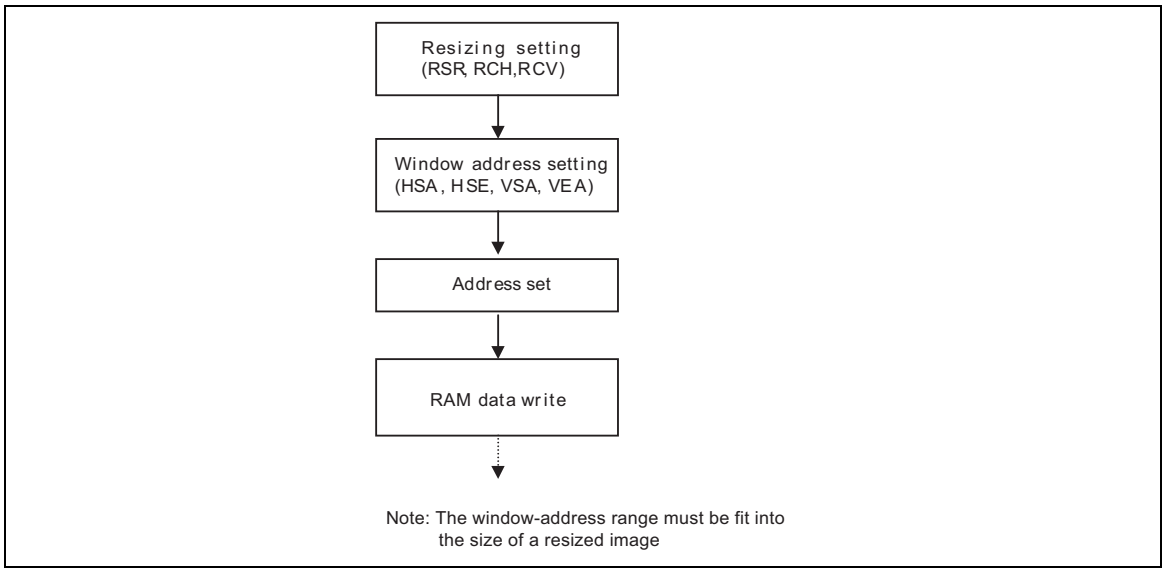
horizontal direction

RCH[1:0]	surplus pixels
2h'0	0
2h'1	1 pixel
2h'2	2 pixels
2h'3	3 pixels

1 pixel = 1 RGB

Notes to the resizing function

1. Make settings for resizing instructions (RSR, RCV, and RCH) before writing data to RAM.
2. Write data to RAM from the start position of the window address by line when using resizing function.
3. Fit the window-address range into the size of the resized picture.
4. Make an address set before writing data to RAM when using resizing function.
5. Settings for RCH, RCV are only required when using resizing function. Otherwise (RSR = 2'h0), set RCH = RCV = 2'h0.



RAM Writing flow when using resizing

Magnification

The HD66781 enables to write resized image data to RAM by simply transmitting original image data to the window address as usual with the settings of RESH/RESEV[7:0] bits that specify the magnification rate each for the base and OSD images. The magnification rate is specified each for the base and OSD images. Also, only a part of RAM area of a base image can be magnified on display in the vertical direction. This means the HD66781 allows the system simply to transmit an original data as usual even when displaying a magnified image on a large screen, and therefore enables to reduce the data transmission required for a large screen display.

The display magnification in the vertical direction should be specified by line.

Base image: The image specified by ESA[8:0] and EEA[8:0] on RAM is magnified on display by the scale set by the RSEV[1:0] setting.

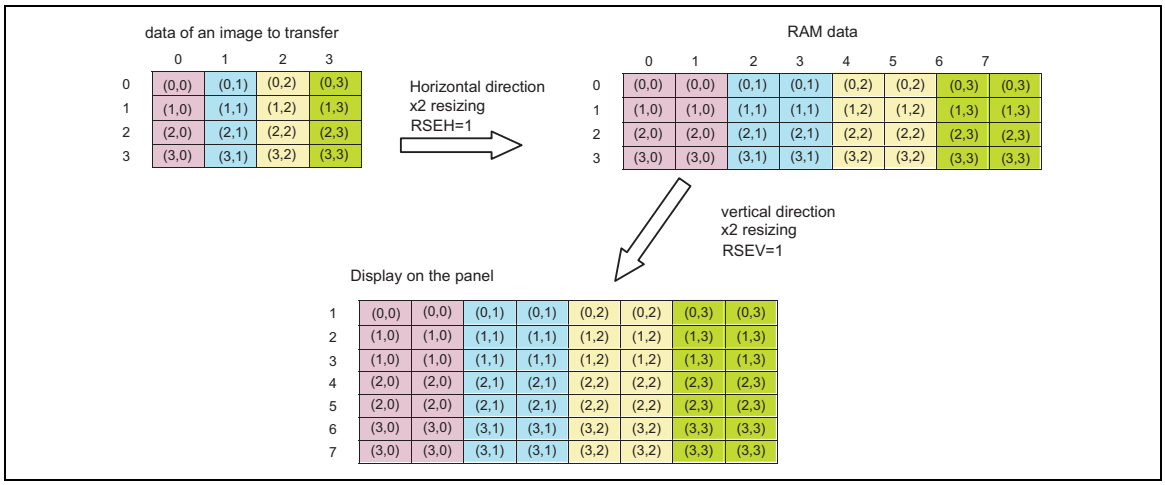
OSD image: The image specified by OSAx[8:0] and OEAx[8:0] on RAM is magnified on display in the manner set by the RSEV[7:2] setting.

When magnifying in the horizontal direction, the window-address settings (HSA[0], HEA[0]), RAM address set (AD[0]), and horizontal incremental direction of the counter (I/D[0]) as follows.

Table 61

Registers	Register setting
HSA[0]	1'b0
HEA[0]	1'b1
AD[0]	1'b0 when I/D[0]=0
	1'b1 when I/D[0]=1

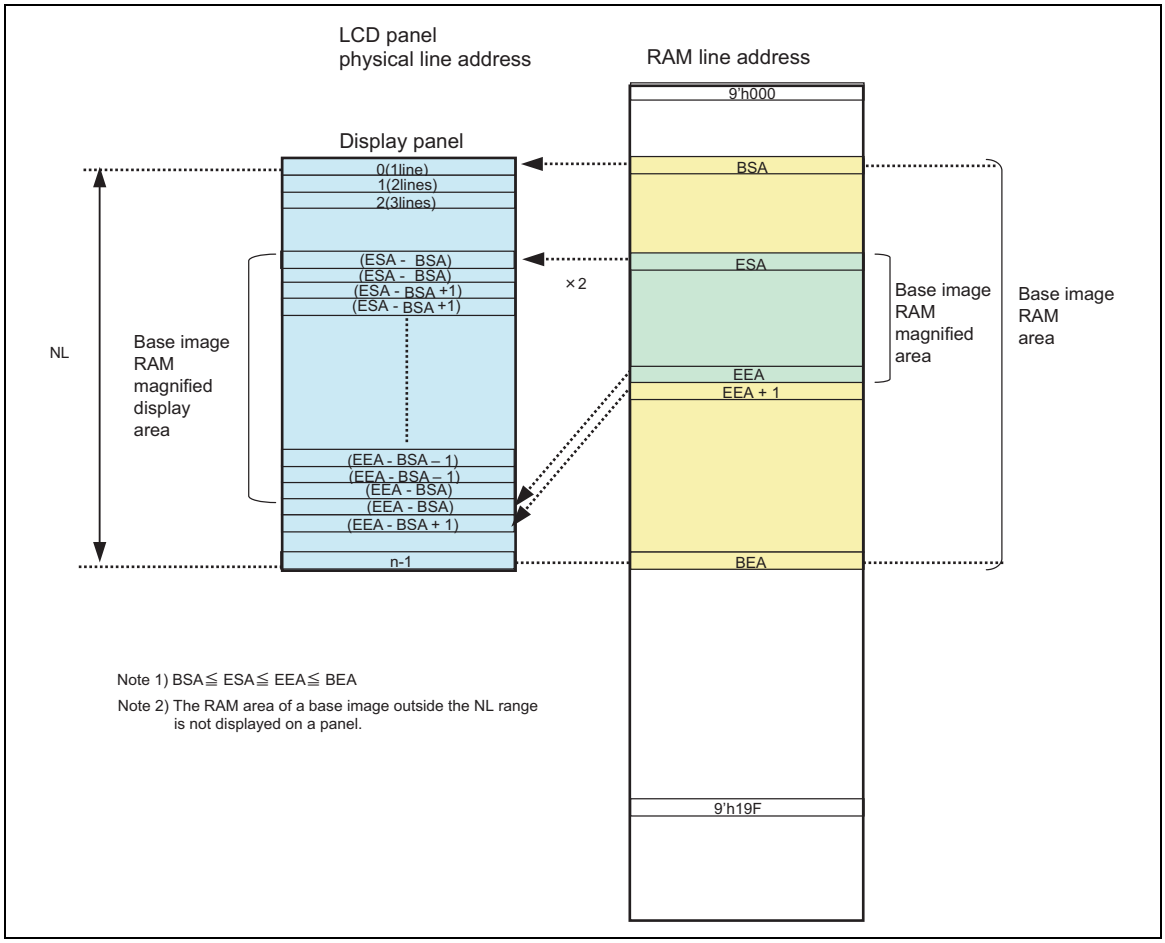
The HD66781 performs magnification resizing simply by inserting pixels. The resized image is an extended original image in both horizontal and vertical direction. Check the resized image before use.



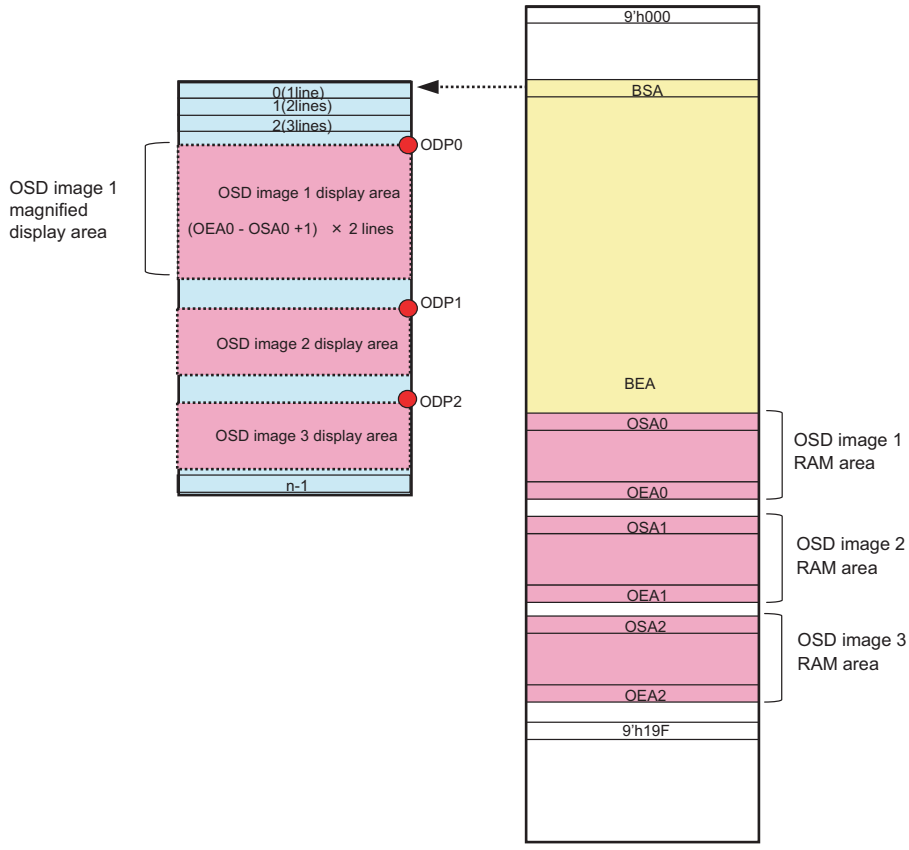
Resizing: magnification

The following figure illustrates the relationship of RAM address, display position and panel driving position when a base image is magnified in the vertical direction.

RESV[1:0] = 2'h1



RSEV[3:2] = 2'h1, RSEV[5:4] = 2'h0, RSEV[7:6] = 2'h0



Note: The OSD display positions must be designated not to overlap one another.

$0 \leqq ODP0 \leqq ODP0 + n \times (OEA0 - OSA0 + 1) - 1 <$
$ODP1 \leqq ODP1 + n \times (OEA1 - OSA1 + 1) - 1 <$
$ODP2 \leqq ODP2 + n \times (OEA2 - OSA2 + 1) - 1 \leqq NL$

n: magnification scale of OSD display

Interface specification

The HD66781 incorporates a system interface to make settings for instructions and an external display interface to display moving pictures. The HD66781 allows selecting an optimum interface for display (moving or still picture, or both) to transmit data efficiently.

The external display interface includes RGB interface and VSYNC interface, which enable flicker-free screen update.

In the RGB-I/F mode, the display operation is performed in synchronization with the signals (VSYNC, HSYNC, and DOTCLK). The display data are written according to the values of the data enable signal (ENABLE), and PD17-0 bits in synchronization with the VSYNC, HSYNC, and DOTCLK signals. The display data are written to GRAM to reduce the data transmission to minimum, i.e. only when the displays are being changed. With the window address function, only the RAM area used for moving picture display is overwritten, and therefore the simultaneous display of moving picture area, which is overwritten, and the RAM data in the area other than the moving picture area, which is not overwritten, is possible. In the RGB and VSYNC interface modes, write data to GRAM in the high speed write mode (HWM = 1) during displaying moving pictures to access to GRAM in high speed with low power consumption.

In the VSYNC interface mode, the frame synchronization signal (VSYNC) synchronizes internal display operations. By writing data in synchronization with the falling edge of VSYNC at a fixed speed to GRAM through a system interface, moving pictures are displayed with the system interface in use. In this case, there are some constraints in the speed and method to write data to RAM.

The HD66781 handles the following 4 operational modes according to the type of display. All settings are made through the external display interface. Transition between the modes must be done according to the transitional flow charts.

Table 62

Operation Mode	RAM Access Setting (RM)	Display Operation Mode (DM1-0)
Internal operating clock only (Displaying still picture)	System interface (RM = 0)	Internal operating clock (DM1-0 = 00)
RGB interface (1) (Displaying moving picture)	RGB interface (RM = 1)	RGB interface (DM1-0 = 01)
RGB interface (2) (Rewriting still picture while displaying moving pictures)	System interface (RM = 0)	RGB interface (DM1-0 = 01)
VSYNC interface (Displaying moving pictures)	System interface (RM = 0)	VSYNC interface (DM1-0 = 10)

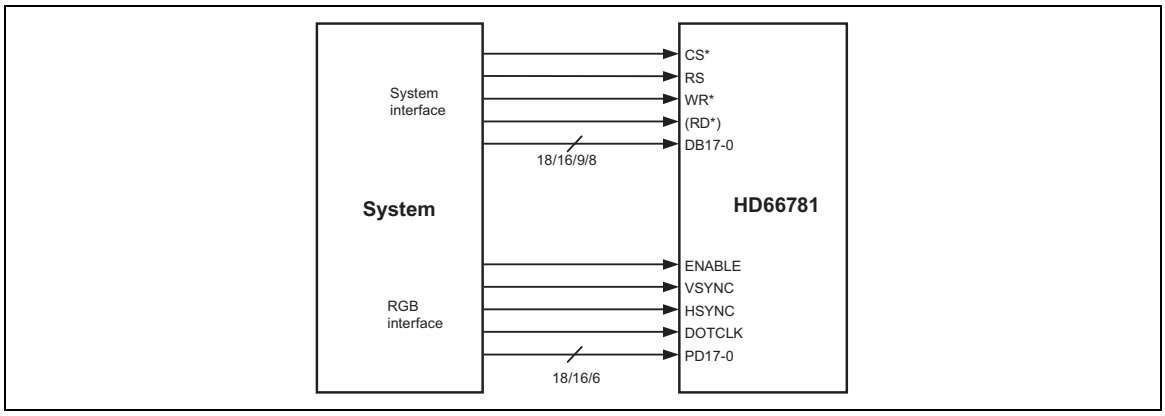
Note 1) Instructions are set only through a system interface.

Note 2) RGB-I/F and VSYNC-I/F are not used simultaneously.

Note 3) Do not make a change to the RGB-I/F mode (RIM-0) while the RGB I/F is operating.

Note 4) When making transitions between the interfaces, see the “External Display Interface” (p.139) for the transition flow chart

Note 5) RGB-I/F and VSYNC-I/F modes should be used with the high-speed write mode (HWM = 1).



HD66781 Interface

System Interface

The setting with IM3/2/1/0 pins allows selecting among the following system interfaces. The system interface enables instruction settings and RAM access.

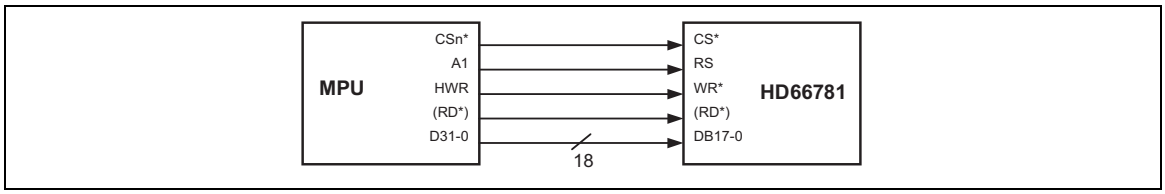
Table 63 IM bits settings and system interface

IM3	IM2	IM1	IM0	Interfacing mode with MPU	DB Pin	Colors
0	0	0	0	Setting disabled		
0	0	0	1	Setting disabled		
0	0	1	0	80-system 16-bit interface	DB17 to 10 and 8 to 1	65,536 (262,144) Note 2)
0	0	1	1	80-system 8-bit interface (Big endian)	DB17 to 10	65,536 (262,144) Note 2)
0	1	0	*	Serial Peripheral interface (SPI)	DB1 to 0	65,536
0	1	1	0	Setting disabled		
0	1	1	1	80-system 8-bit interface (Little endian)	DB17 to 10	65,536 (262,144) Note 2)
1	0	0	0	Setting disabled		
1	0	0	1	Setting disabled		
1	0	1	0	80-system 18-bit interface	DB17 to 0	262,144
1	0	1	1	80-system 9-bit interface	DB17 to 9	262,144
1	1	*	*	Setting disabled		

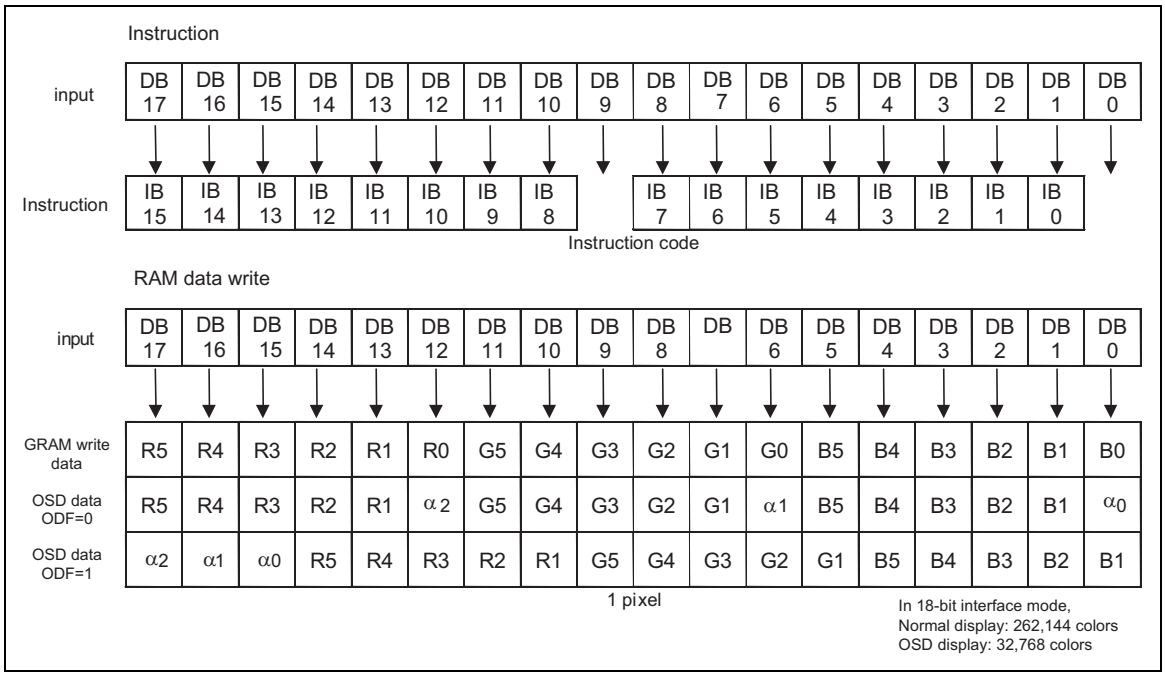
Note 1) 262,144 colors in 16-bit data bus 2-transmission mode.
Note 2) 262,144 colors in 8-bit data bus 3-transmission mode.

80-system 18-bit interface

80-system 18-bit parallel data transmission is selected by setting IM3/2/1/0 pins to Vcc1/GND/Vcc1/GND levels.



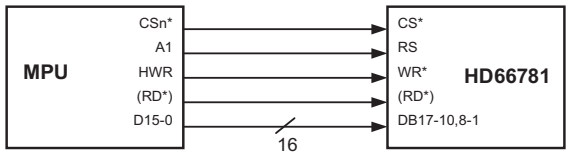
Example of Interface with the 18-bit Microcomputer



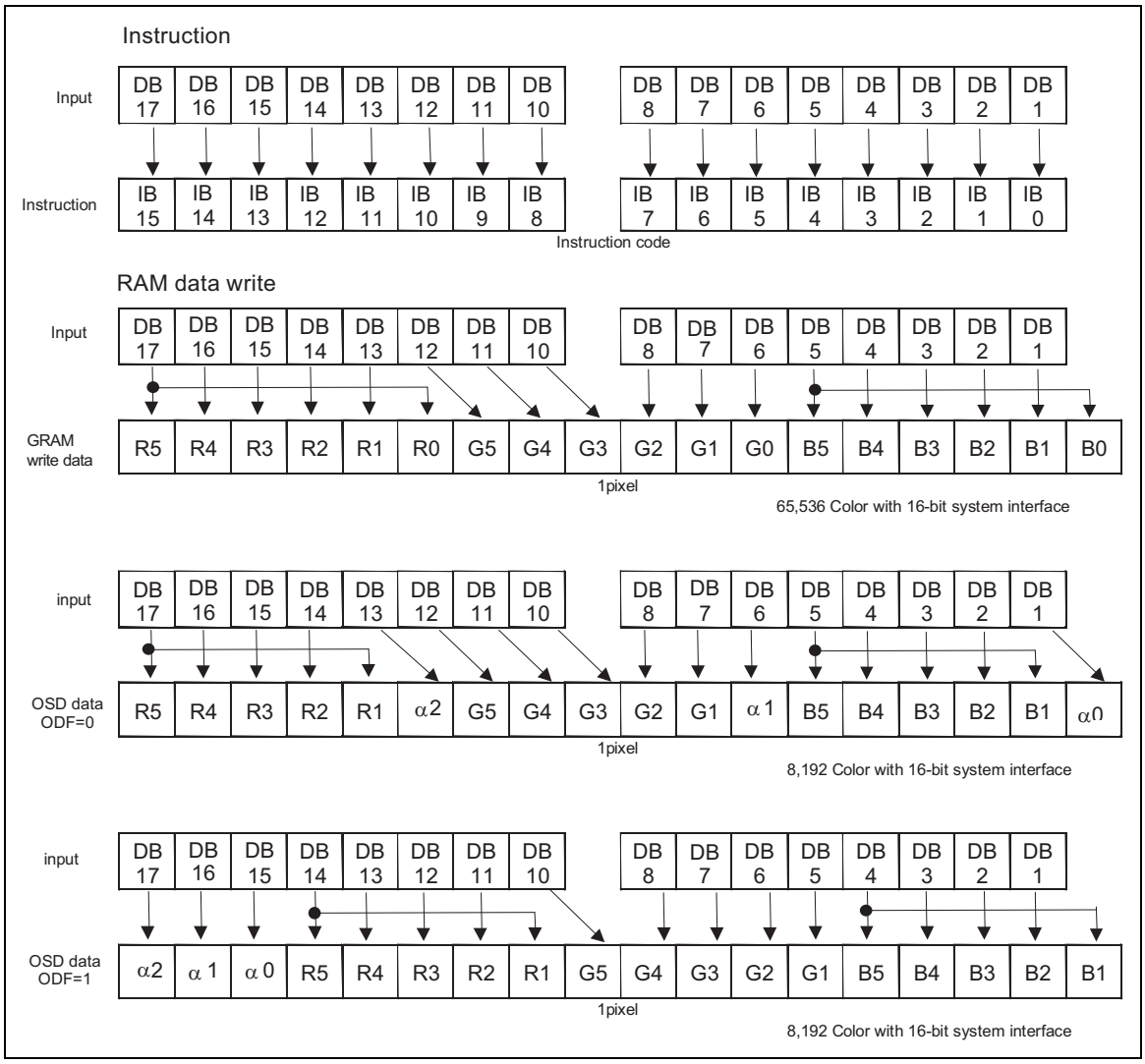
18-bit interface data format (Instruction / RAM write data)

80-system 16-bit interface

80-system 16-bit parallel data transmission is selected by setting IM3/2/1/0 pins to GND/GND/Vcc1/GND levels.

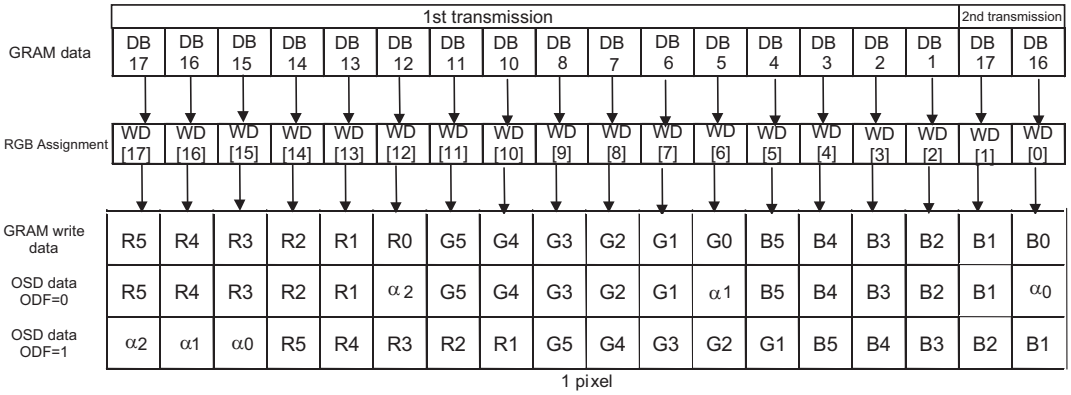


16-bit microcomputer and interface (example)



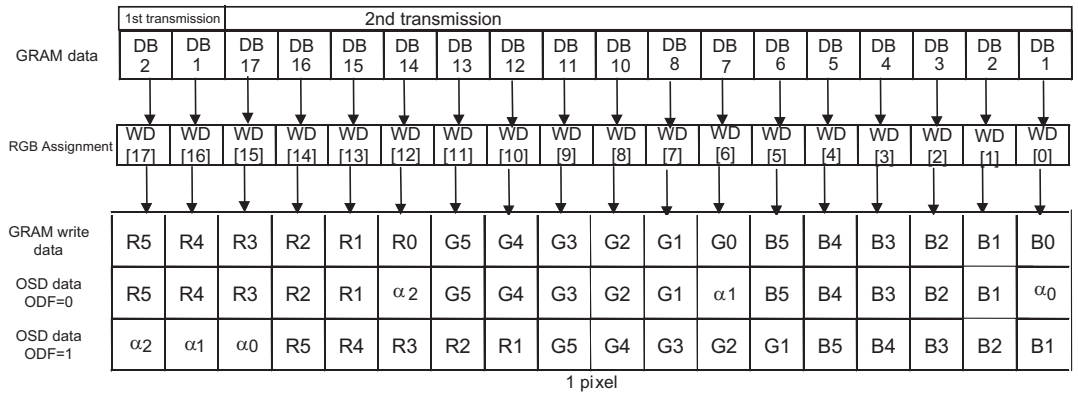
16-bit interface data format (Instruction / RAM write data)

80 system 16 bit interface (2 transmissions: TRI = 1, DFM = 0)



Note: Normal display in 262,144 colors, OSD display in 32,768 colors in16-bit system interface, 2-transmission mode.

80 system 16 bit interface (2 transmissions: TRI =1, DFM = 1)

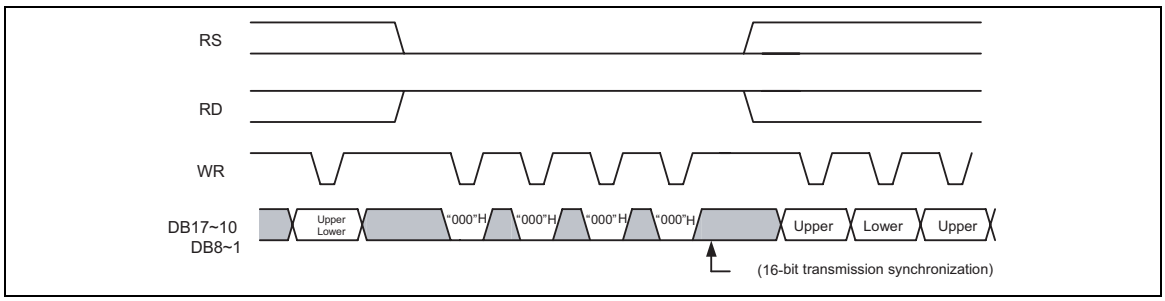


Note: Normal display in 262,144 colors, OSD display in 32,768 colors in16-bit system interface, 2-transmission mode.

16-bit interface data format (RAM write data in 2-transmission mode)

Data transmission synchronization in 16-bit bus interface mode

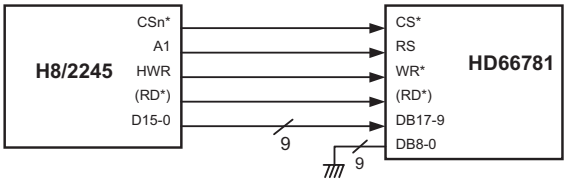
The HD66781 supports the data transmission synchronization function, which resets the counter that counts the number of data transmission of upper 2 bits and lower 16 bits or upper 16 bits and lower 2 bits in the 16-bit data bus interface 2-transmission mode. When a discrepancy occurs in the data transmission of the upper/lower bits due to effects from noise and so on, the "000" H instruction is written 4 times consecutively to reset the upper/lower counters so that data transmission restarts with the upper bit transmission. Periodical execution of synchronization function allows the display system to recover from excursion.



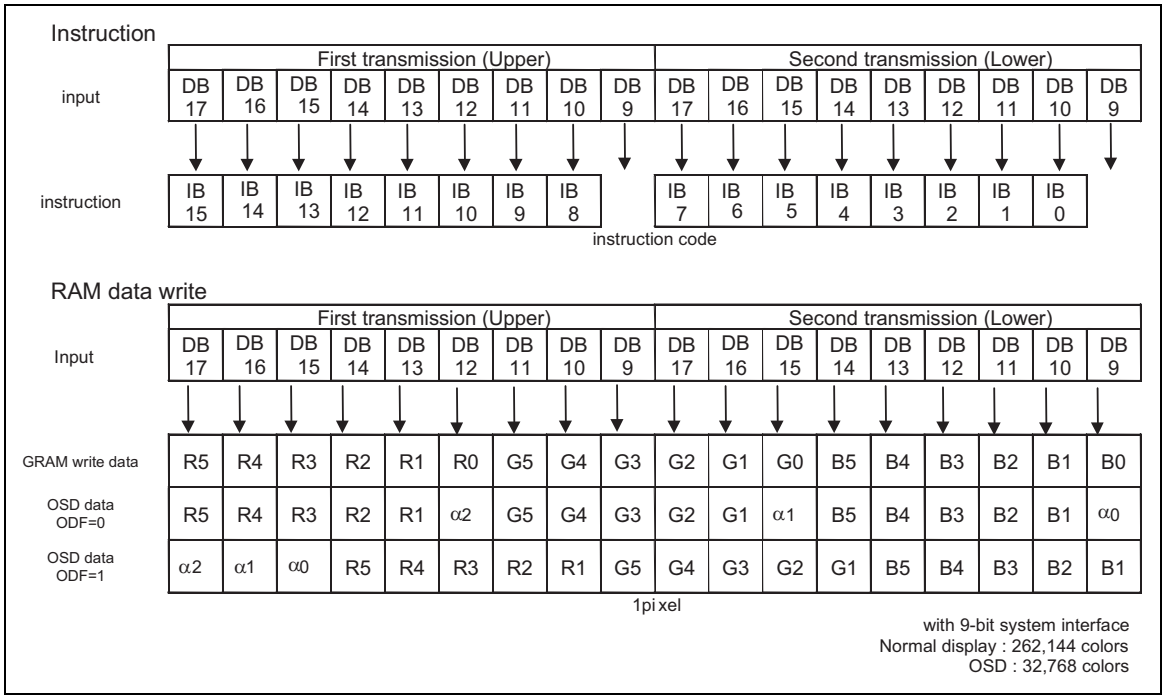
Data Transmission Synchronization

80-system 9-bit interface

The 80-system 9-bit parallel data transmission through DB17-9 pins is selected by setting IM3/2/1/0 pins to Vcc1/GND/Vcc1/Vcc1 levels respectively. When transmitting a 16-bit instruction, it is divided into upper and lower 8 bits (the LSB is not used) and the upper 8 bits are transmitted first. The RAM data is also divided into the upper and lower 9 bits, and the upper bits are transmitted first. The DB8-0 pins, that are not used, must be fixed to either IOVcc level. When writing the index register, the upper byte (8 bits) must be written.



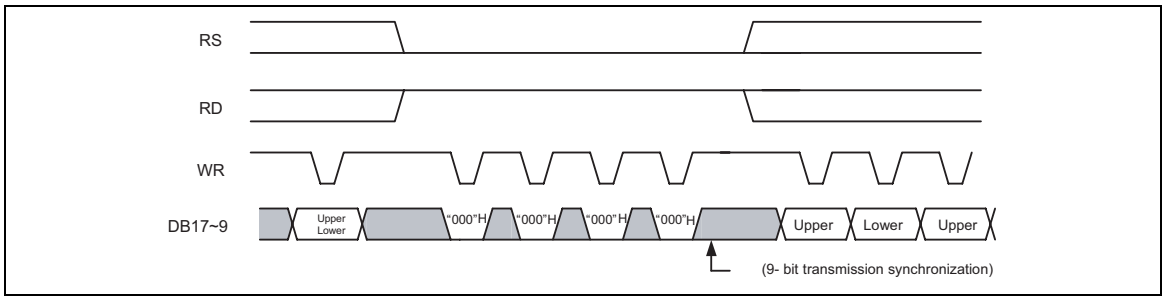
Example of Interface with the 9-bit Microcomputer



9-bit interface data format

Data transmission synchronization in 9-bit bus interface mode

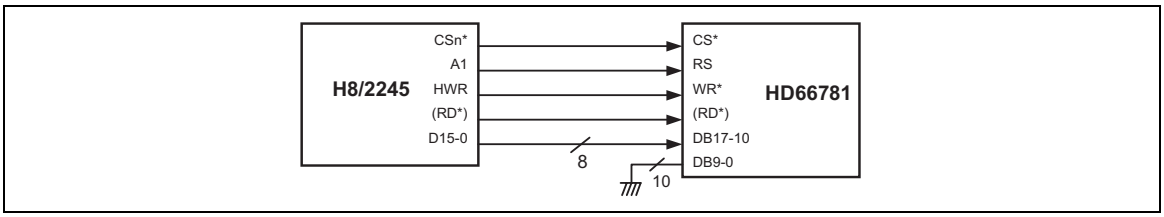
The HD66781 supports the data transmission synchronization function, which resets the upper/lower counters that count the number of data transmission of upper/lower 9 bits in the 9-bit bus interface mode. When a discrepancy occurs in the data transmission of the upper/lower 9 bits due to effects from noise and so on, the "000" H instruction is written 4 times consecutively to reset the upper/lower counters so that data transmission restarts with the upper 9-bit transmission. Periodical execution of synchronization function allows the display system to recover from excursion.



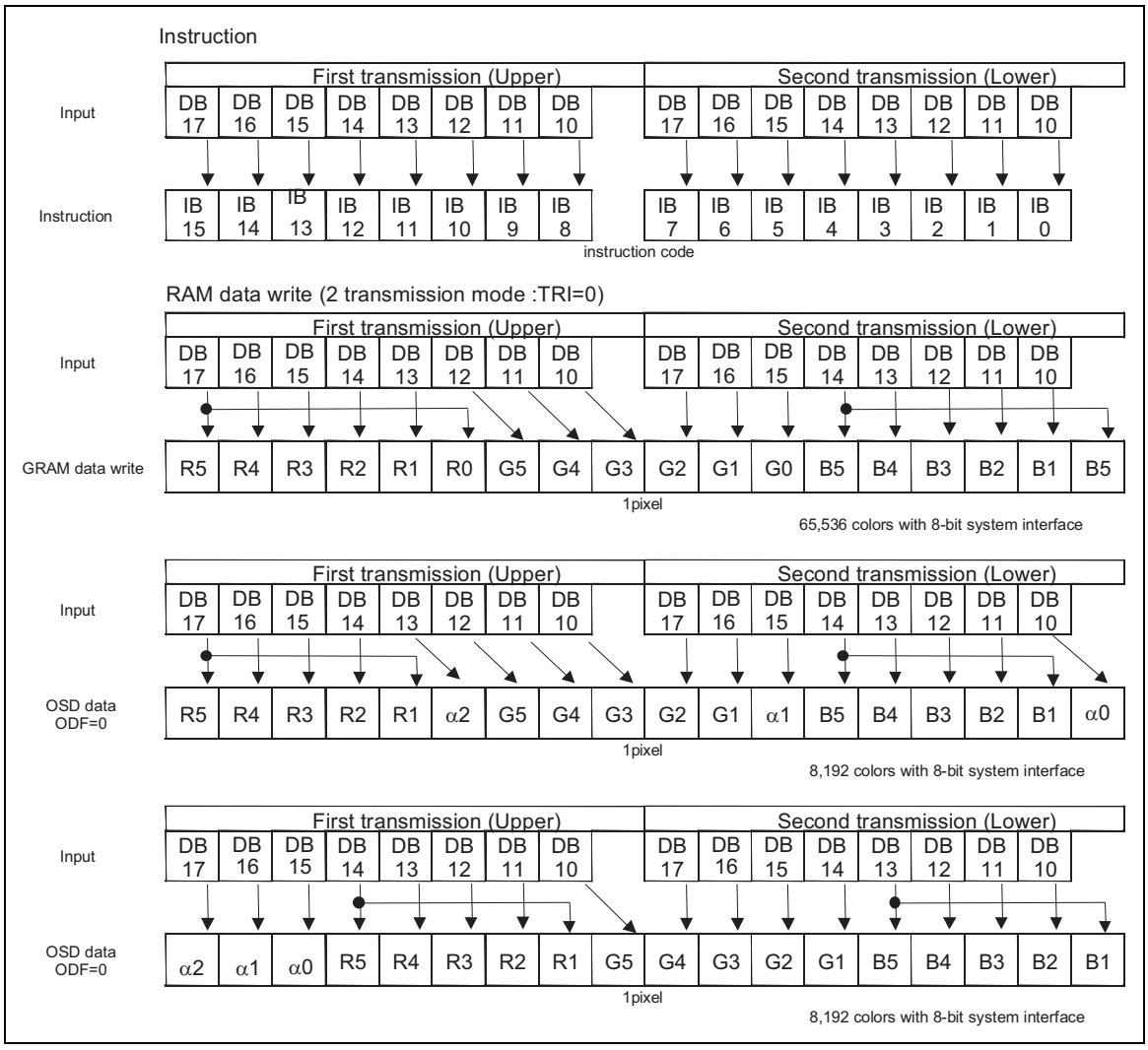
9-bit Transfer Synchronization

80-system 8-bit interface (Big endian)

The 80-system 8-bit parallel data transmission is selected by setting IM3/2/1/0 pins to GND/GND/Vcc1/Vcc1 levels respectively. When transmitting a 16-bit instruction, it is divided into upper and lower 8 bits and the upper 8 bits are transmitted first. The RAM data is also divided into the upper and lower 8 bits, and the upper bits are transmitted first. The data to write to RAM are expanded into 18 bits internally. The DB9-0 pins, that are not used, must be fixed to either IOVcc level. When writing the index register, the upper byte (8 bits) must be written.



Example of Interface with the 8-bit Microcomputer



8-bit interface data format, RAM data write (2-transmission mode)

RAM data write(3 transmission mode : TRI =1, DFM =0)

	first transmission		second transmission								third transmission							
input	DB 11	DB 10	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10
GRAM data write	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
OSD data ODF=0	R5	R4	R3	R2	R1	α 2	G5	G4	G3	G2	G1	α 1	B5	B4	B3	B2	B1	α 0
OSD data ODF=1	α 2	α 1	α 0	R5	R4	R3	R2	R1	G5	G4	G3	G2	G1	B5	B4	B3	B2	B1

1 pixel

with 8-bit system interface
Normal display : 262,144 colors
OSD : 32,786 colors

RAM data write (3 transmission mode :TRI =1, DFM =1)

	first transmission						second transmission				third transmission							
input	DB 11	DB 10	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10
GRAM data write	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
OSD data ODF=0	R5	R4	R3	R2	R1	α 2	G5	G4	G3	G2	G1	α 1	B5	B4	B3	B2	B1	α 0
OSD data ODF=1	α 2	α 1	α 0	R5	R4	R3	R2	R1	G5	G4	G3	G2	G1	B5	B4	B3	B2	B1

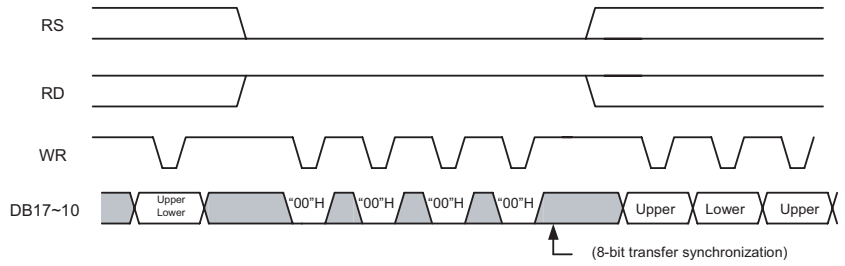
1 pixel

with 8-bit system interface
Normal display : 262,144 colors
OSD : 32,768 colors

8-bit interface data format, RAM data write (3-transmission mode)

Data transmission synchronization in 8-bit bus interface mode

The HD66781 supports the data transmission synchronization function, which resets the upper/lower counters that count the number of data transmission of upper/lower 8 bits in the 8-bit bus interface mode. When a discrepancy occurs in the data transmission of the upper/lower 8 bits due to effects from noise and so on, the "00" H instruction is written 4 times consecutively to reset the upper/lower counters so that data transmission restarts with the upper 8-bit transmission. Periodical execution of synchronization function allows the display system to recover from excursion.



8-bit data transmission synchronization

Serial Peripheral interface (SPI)

The Serial Peripheral Interface (SPI) is selected by setting IM3/2/1 pins to GND/Vcc1/GND levels respectively. The SPI is available through the chip select line (CS), serial transfer clock line (SCL), serial data input (SDI), and serial data output (SDO). In the SPI mode, the IM0/ID pin functions as ID pin. In the SPI mode, the DB17-2 pins, which are not used, must be fixed at either IOVcc level.

The HD66781 recognizes the start of data transfer at the falling edge of CS input to initiate the transfer of start byte. It recognizes the end of data transfer at the rising edge of CS input. The HD66781 is selected when the 6-bit chip address in the start byte transferred from the transmission device and the 6-bit device identification code assigned to the HD66781 are compared and both 6-bit data correspond. When selected, the HD66781 starts taking in the subsequent data string. The setting for the least significant bit of the identification code is made with the ID pin. The five upper bits of the identification code must be 01110. Two different chip addresses must be assigned to the HD66781 because the seventh bit of the start byte is assigned to a register select bit (RS). When RS = 0, index register write or status read is executed. When RS = 1, instruction write or RAM read/write is executed. The eighth bit of the start byte is to specify read or write (R/W bit). The data are received when the R/W bit is 0, and are transmitted when the R/W bit is 1.

In the SPI mode, the data are written to GRAM after two-byte data transmission. The data are expanded into 18 bits by adding one bit (the same data as the MSB of RB) to the LSB of RB data.

After receiving the start byte, the HD66781 starts to transmit or receive data by byte. The data transmission adopts a format by which the MSB is first transmitted. All HD66781 instructions consist of 16 bits and they are executed internally after two bytes are transmitted with the MSB first (DB15 to 0). The data to write to RAM are expanded into 18-bit data. After the start byte is received, the first byte is always fetched as the upper eight bits of the instruction and the second byte is fetched as the lower eight bits of the instruction. The 4-byte data that are read from RAM right after the start byte are made invalid. The HD66781 reads as valid data from the 5th-byte data.

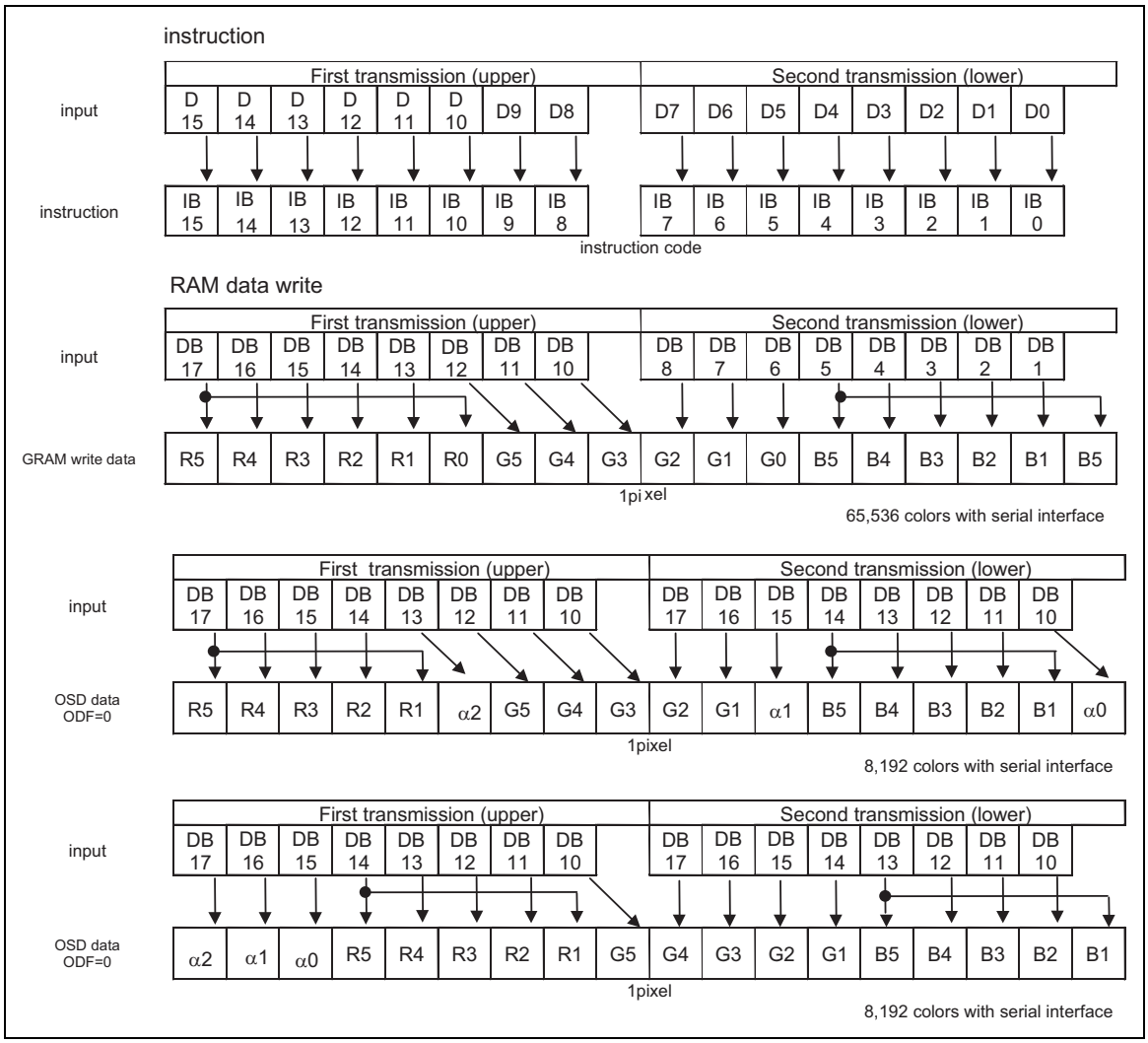
Start Byte Format

Transmitted bits	S	1	2	3	4	5	6	7	8
Start byte format	Transmission start	Device ID code						RS	R/W
		0	1	1	1	0	ID		

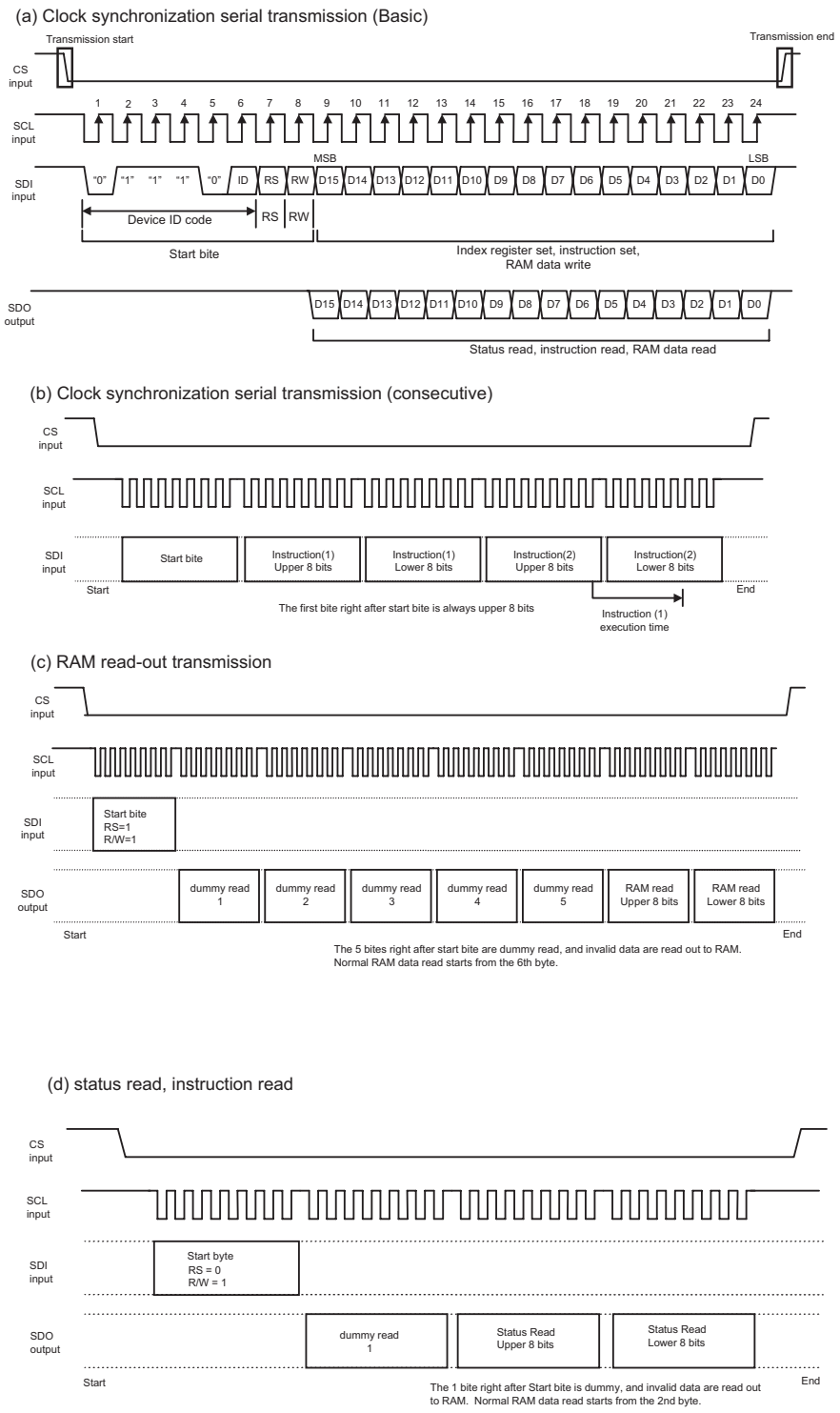
Note 1) ID bit is selected with the IM0/ID pin.

Table 64

RS	R/W	Function
0	0	Set index register
0	1	Read status
1	0	Write instruction or RAM data
1	1	Read instruction or RAM data



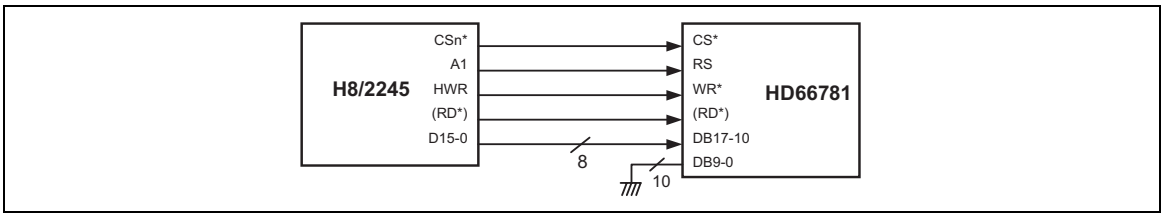
Data format for Serial Peripheral Interface



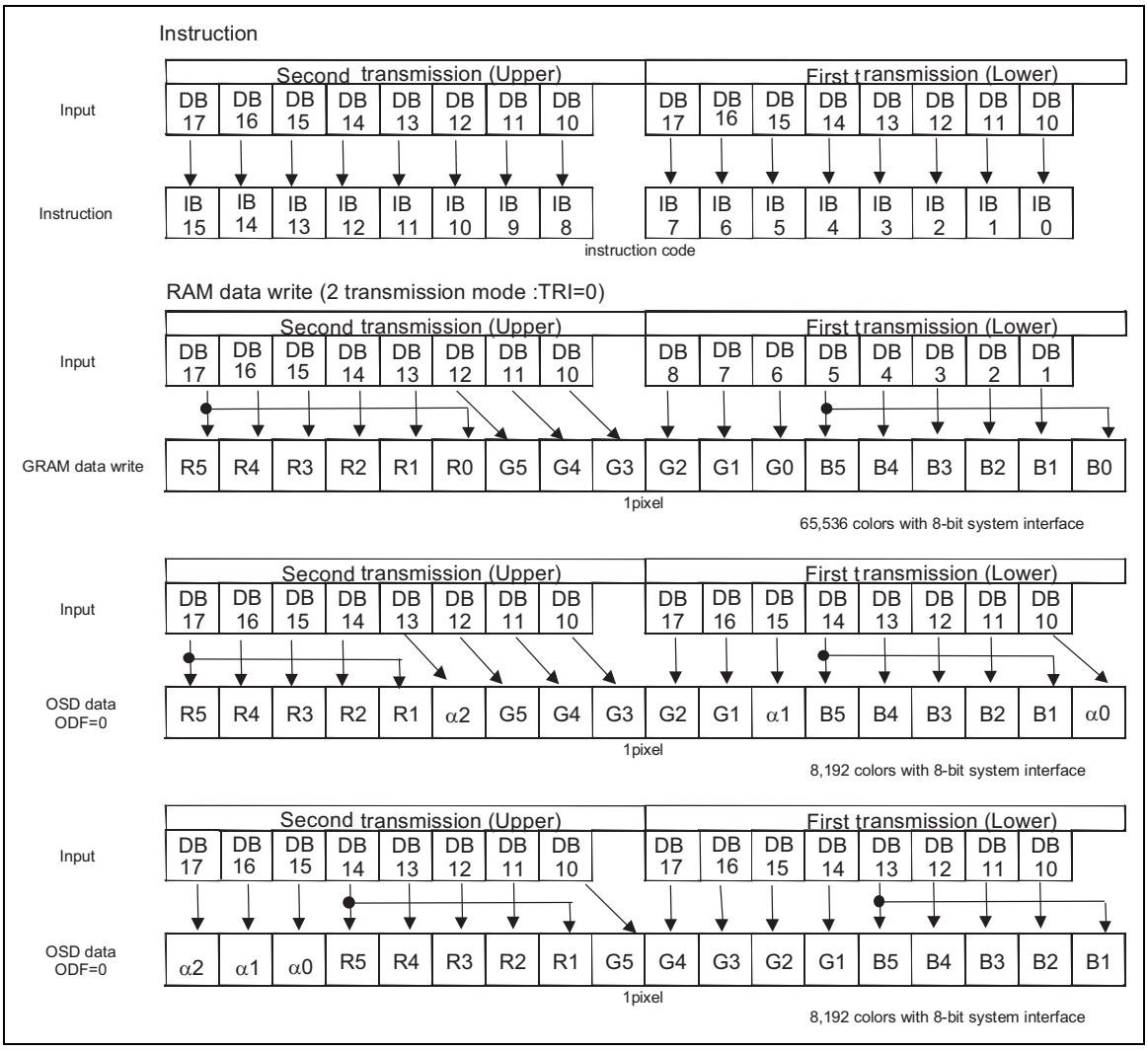
Serial Peripheral Interface: data transfer

80-system 8-bit interface (Little endian)

The 80-system 8-bit parallel data transmission is selected by setting IM3/2/1/0 pins to GND/Vcc1/Vcc1/Vcc1 levels respectively. When transmitting a 16-bit instruction, it is divided into upper and lower 8 bits and the upper 8 bits are transmitted first. The RAM data is also divided into the upper and lower 8 bits, and the upper bits are transmitted first. The data to write to RAM are expanded into 18 bits internally. The DB9-0 pins, that are not used, must be fixed to either IOVcc level. When writing into the index register, the upper byte (8 bits) must be written.



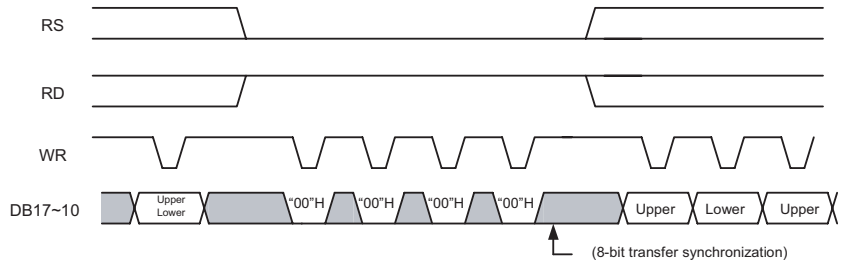
Example of Interface with the 8-bit Microcomputer



8-bit interface data format, RAM data write (2-transmission mode)

Data transmission synchronization in 8-bit bus interface mode

The HD66781 supports the data transmission synchronization function, which resets the upper/lower counters that count the number of data transmission of upper/lower 8 bits in the 8-bit bus interface mode. When a discrepancy occurs in the data transmission of the upper/lower 8 bits due to effects from noise and so on, the "00" H instruction is written 4 times consecutively to reset the upper/lower counters so that data transmission restarts with the upper 8-bit transmission. Periodical execution of synchronization function allows the display system to recover from excursion.



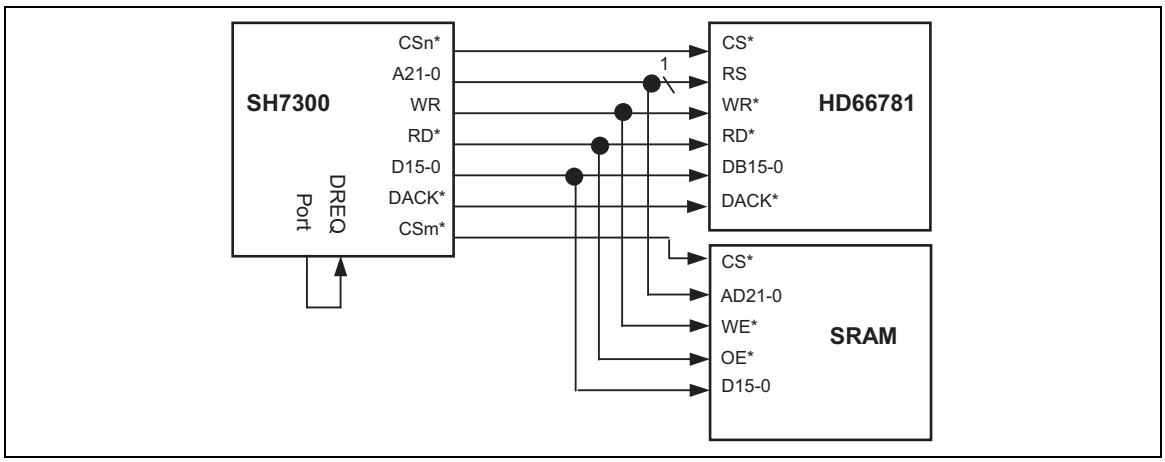
8-bit data transmission synchronization

DMA transfer Single Address mode

When connecting a microcomputer or an application processor, which are compliant to DMA transfer single address mode, with the HD66781, and SRAM or pseudo SRAM, the HD66781 allows using same bus cycle for data read from memory and data write to the HD66781. This reduces transfer time and controls bus occupation ratio when transferring a large volume of data from external memory to a LCD driver.

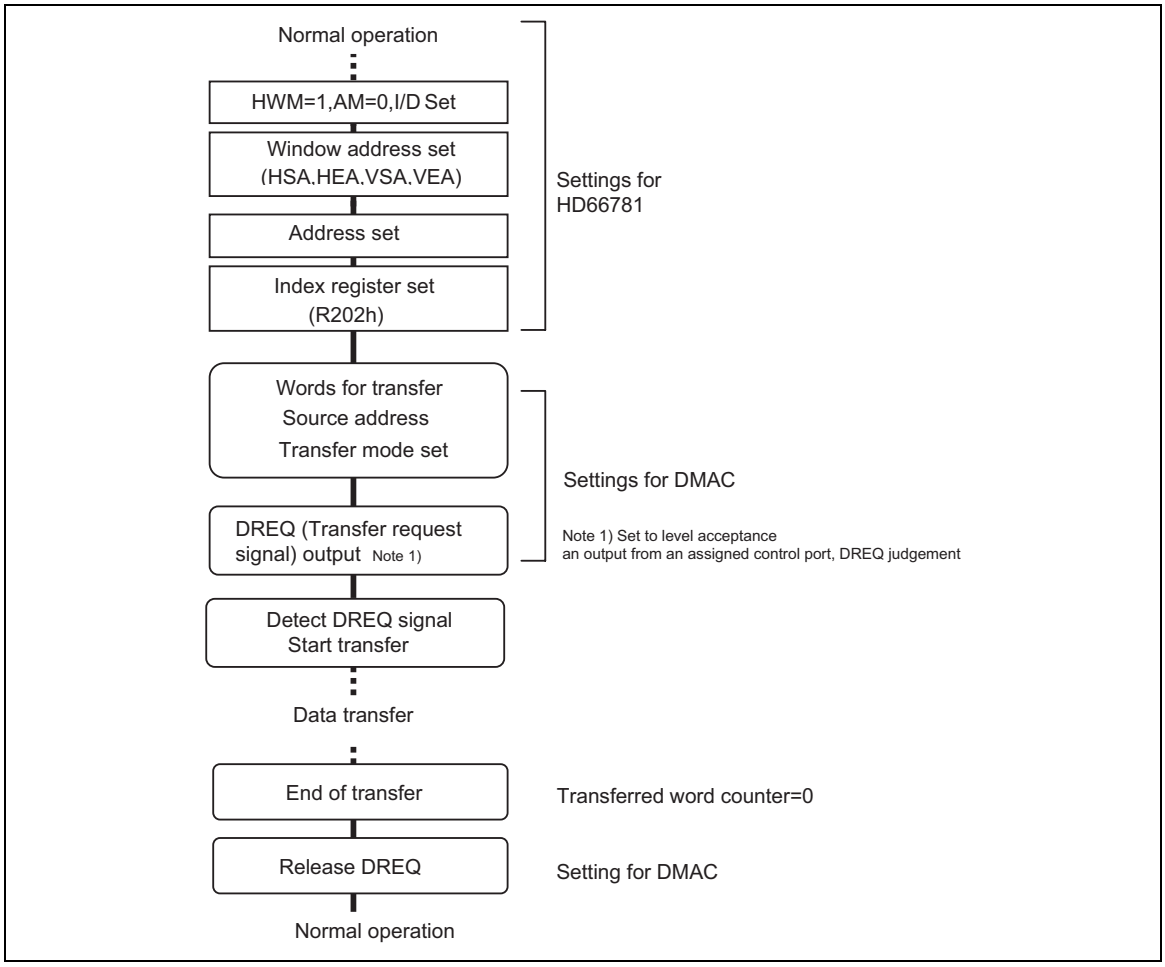
1. Pin functions in DMA single address mode

DACK: In DMA single address mode, it has the same function as CS in normal operation mode.
RD: Recognize write strobe (WR) internally when DACK is at the low level (active).
WR: Fix to High.
CS: Fix to High.
RS: Recognize a high level (data transfer) inside the HD66781 under any condition when DACK is at the low level (active).



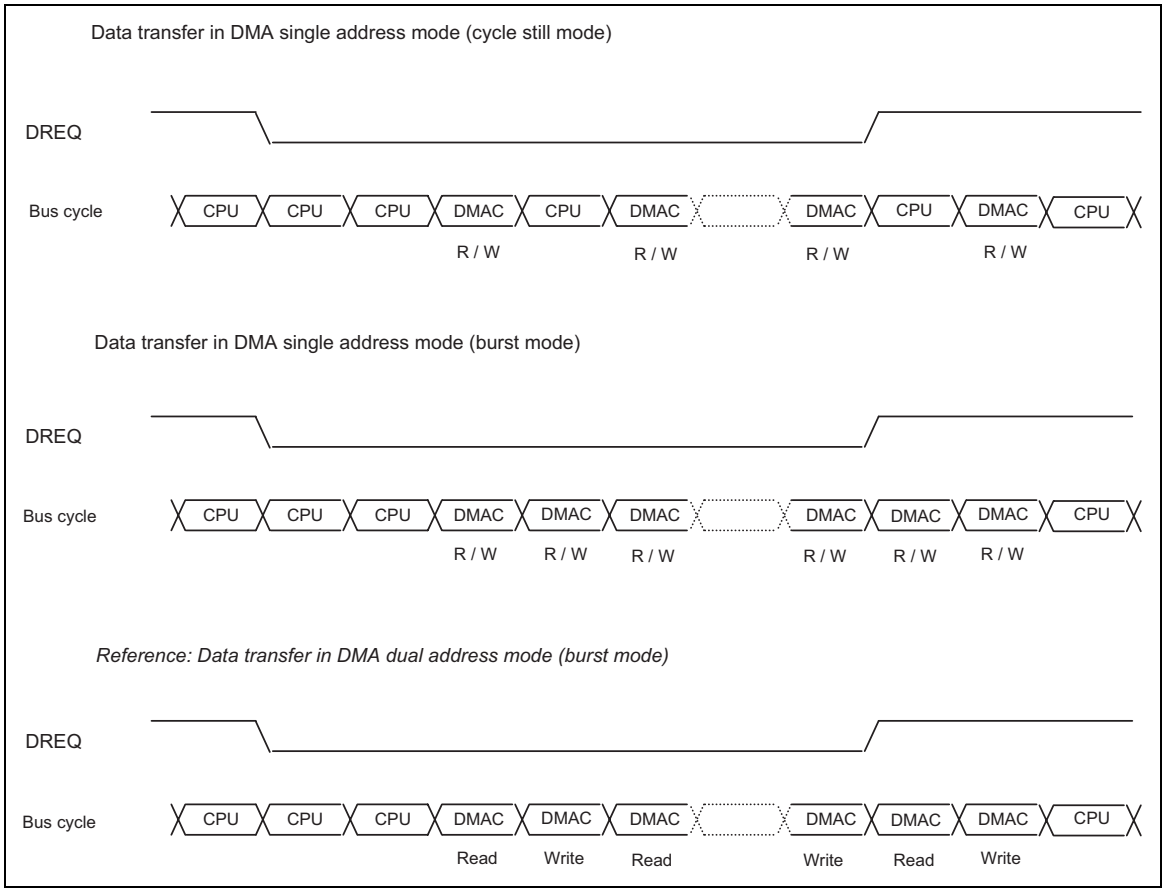
Interfacing with microcomputer and SRAM

2. Transfer procedure in DMA single address mode



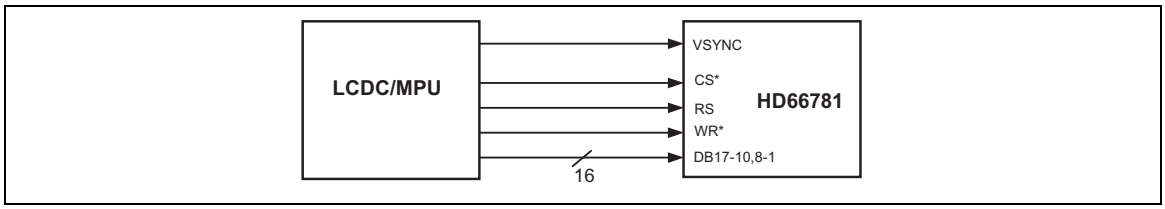
3. Notes to the DMA single address mode

1. DACK*pin and CS*pin cannot be made at a low level (active) simultaneously.
2. Once starting a transfer in the DMA single address mode, no command access to the HD66781 will be allowed until the end of the transfer.
3. The DMA single adders mode must be used with the window address function to make sure the number of data transfer in the DMA mode and the numbers of data in the specified window address area correspond. .
4. After transferring in the DMA mode, wait at least for RAM write execution time (bus cycle time in the normal write mode, t_{cycw}) before issuing a next instruction.
5. It is not possible to make a transfer form the HD66781 to external memory in the DMA single address mode.
6. The DMA single address mode is compatible with the normal cycle still mode and the burst mode.



VSYNC Interface

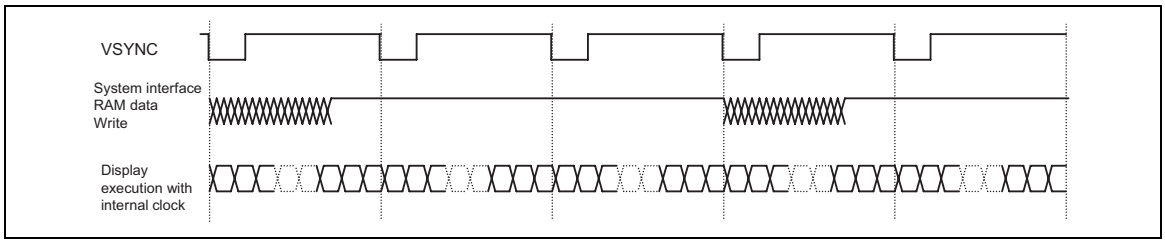
The HD66781 incorporates a VSYNC-I/F, which enables moving picture display with a system interface and the frame synchronization signal (VSYNC) only. This interface enables the display of moving pictures with minimum modification to the conventional system.



VSYNC interface

The VSYNC-I/F is selected by setting DM1-0 = 10 and RM = 0. In the VSYNC I/F mode, the internal display operations are synchronized with VSYNC. By writing data to RAM through the system interface in a speed that is higher for more than a fixed speed than the internal display operation speed, it enables moving picture display through a system interface and flicker-free screen update.

Display operations are executed by the internal clock generated by the internal oscillator and the VSYNC input. All display data are stored in RAM. Therefore, it only requires transfer of the data that is written over to update the screen, thereby minimizing the numbers of data transfers while displaying moving picture. The use of high-speed write mode (HWM = 1) with VSYNC interface enables RAM access in high speed with low power consumption.



Moving picture data transmission through VSYNC interface

Note 1) Data must be written to RAM in the high-speed write mode (HWM = 1) in VSYNC interface mode.

The VSYNC-I/F has limits on the minimum speed for RAM write through the system interface and the frequency of the internal clock. It requires RAM write speed more than the calculated result from the following formula.

Internal clock frequency (fosc) [Hz]
= Frame frequency × (Display raster-row (NL) + Front porch (FP) +Back porch (BP)) × 16 clocks
× Fluctuation

RAM writing speed (min.) [Hz]
> 320× Display lines (NL)/{[(Back porch (BP)+Display lines (NL) – margin) x 16 clocks] /fosc}

When RAM write does not start immediately after the falling edge of VSYNC, the period from the falling edge of VSYNC to the start of RAM write must also be taken into consideration.

An example of calculations for the internal clock frequency and RAM write speed in the VSYNC interface mode is as follows.

- Calculation Example: moving picture display in VSYNC I/F
- Panel size 240 RGB × 320 raster-rows (NL0 = 6'27)
- Total number of raster-rows(NL) 320 raster-rows
- Back, Front porches 14, 2, raster-rows (BP = 4'hE, FP = 4'h2)
- Frame frequency 60Hz

Internal clock frequency (fosc) Hz
= 60 Hz × (320 + 2 + 14) raster-rows × 16 clocks × 1.1 / 0.9 = 394 [kHz]

When calculating an internal clock frequency, possible causes of fluctuations must also be taken into consideration. The allowance for this fluctuation is ± 10 % from the center value, and the range of the frequency must be within the VSYNC cycle.

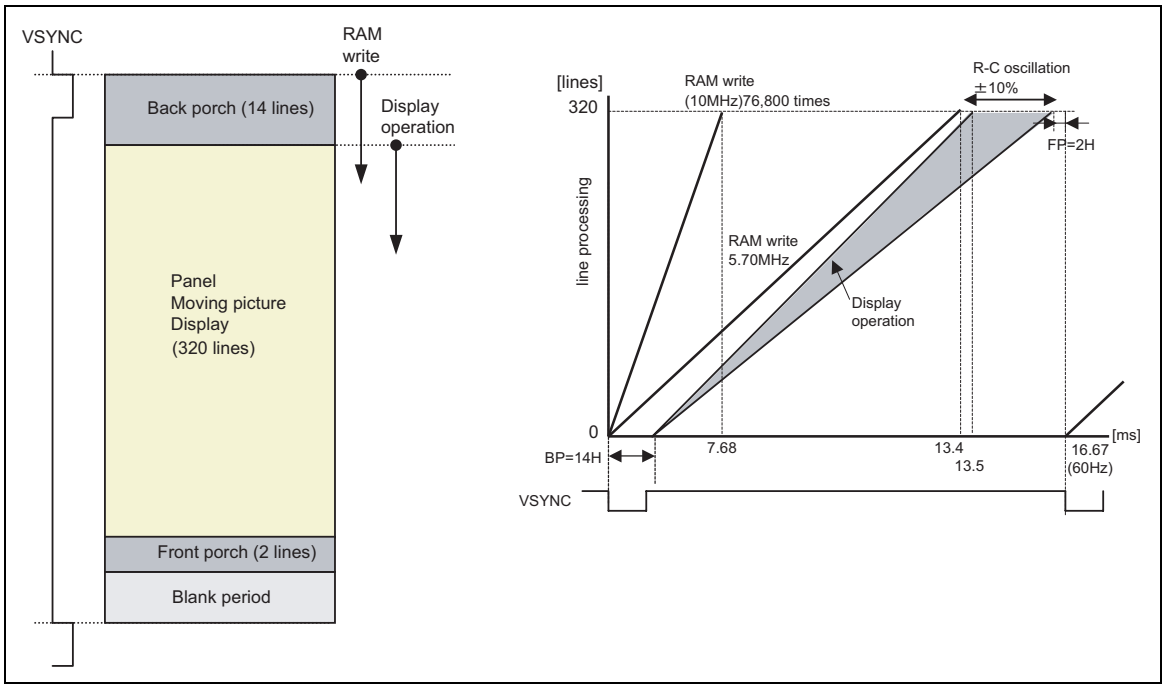
As the causes of fluctuations, the above example takes the variation in the LSI fabrication and the room temperature into account. Other possible causes of fluctuations, such as variation in the external resistors or the voltage change are not considered in the above calculation. It is necessary to make a setting with enough margins to include the allowances for these factors.

Minimum RAM writing speed [Hz]
> 240 × 320 / {((14 + 320 - 2) raster-rows × 16 clocks) / 394 kHz} = 5.70 [MHz]

In this case, RAM write is performed on the input of VSYNC.

When the data for one frame are written to RAM completely, there must be 2 raster-rows or more of a margin before the display raster-rows.

According to the above calculation results, writing data to RAM on the input of VSYNC at the speed of 5.7 MHz or more, the data for the entire screen on RAM are overwritten before the display operation starts. Accordingly, the flicker due to moving picture update can be avoided even if displaying a moving picture.

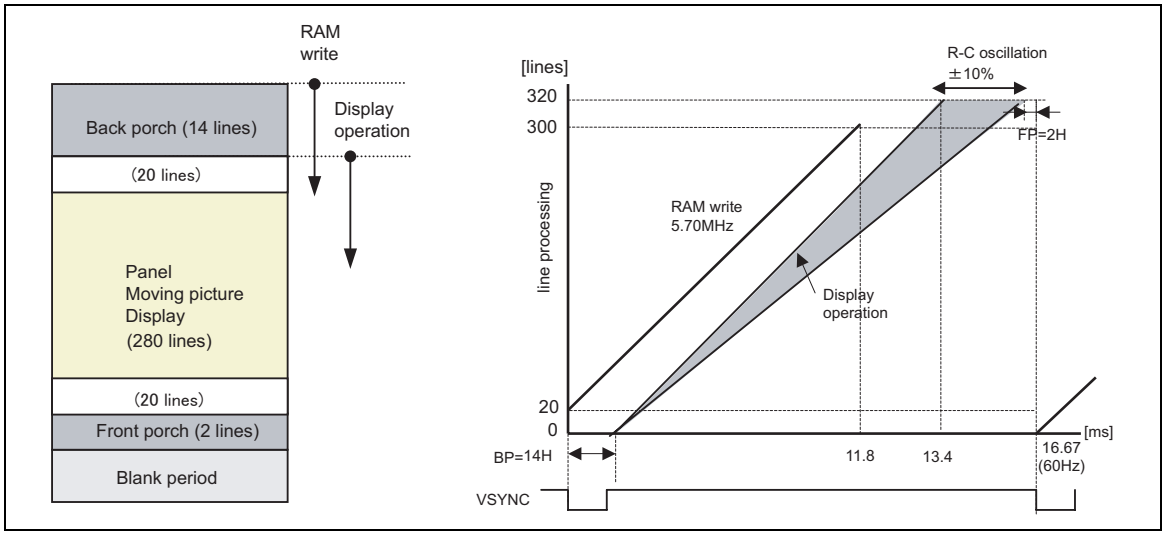


Minimum RAM write speed and internal clock frequency in VSYNC interface

Notes to the VSYNC interface

1. The aforementioned example of calculation is just a result of calculation. In the actual settings, causes for the fluctuations such as internal oscillators and so on should be taken into consideration. It is necessary to make a setting for RAM write speed with enough margins.

2. The aforementioned example of calculation is the value in case of writing over the entire screen. Limiting the area for the moving picture display will create more margins for the RAM write speed.



Condition on using VSYNC interface

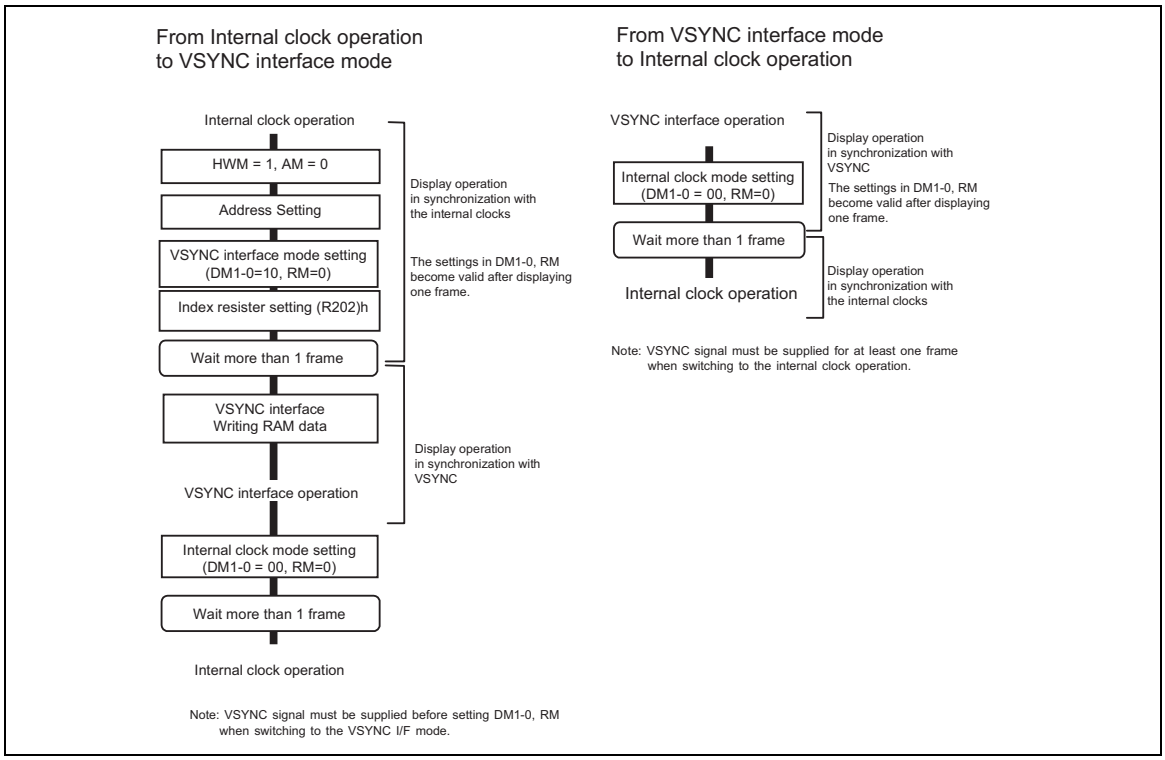
3. A front porch period continues after the completion of 1 frame display and until the next input of VSYNC.

4. The transition between the internal clock operation mode (DM1-0 = 00) and the VSYNC interface mode becomes effective after displaying one frame made during instruction setting.

5. In the VSYNC interface mode, the partial display, vertical scroll, and interlaced drive functions are not available.

6. In the VSYNC interface mode, set AM to 0 to transmit display data in the aforementioned method.

7. In the VSYNC interface mode, write display data to RAM in the high speed write mode (HWM = 1)



Transition between VSYNC and Internal clock operation modes

External Display Interface

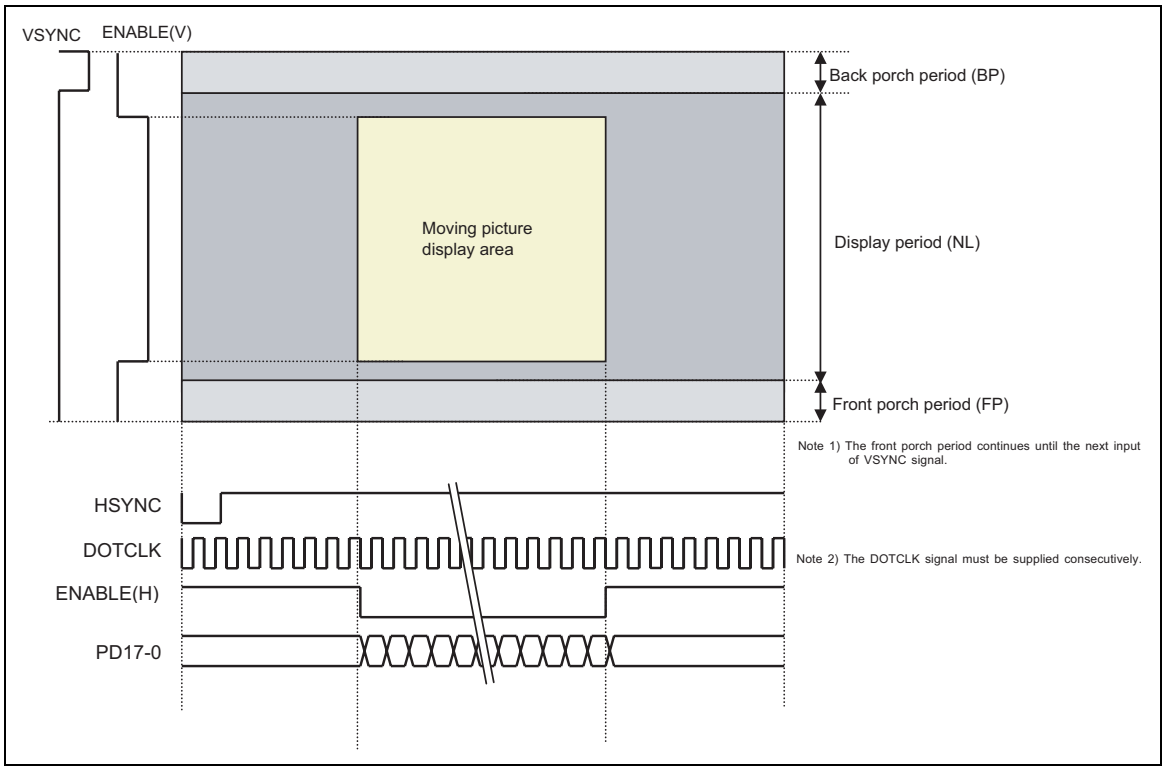
The following interfaces are available as an external display interface (RGB interface). The interface is selected by setting RIM1-0 bits. The RGB interface allows RAM access.

Table 65

RIM1	RIM0	RGB Interface	PD Pin
0	0	18-bit RGB interface	PD17-0
0	1	16-bit RGB interface	PD17-13, 11-1
1	0	6-bit RGB interface	PD17-12
1	1	Setting disabled	-

Note 1) It is not possible to use multiple interfaces at the same time.

Through the RGB-I/F, the display operation is in synchronization with VSYNC, HSYNC, and DOTCLK. The RGB interface enables data transmission in high speed with low power consumption by only overwriting the area that is needed to update in the high-speed write mode in combination with window address function. Front and back porches must be set before and after the display period.



VSYNC: Frame synchronization signal
HSYNC: Line synchronization signal
DOTCLK: DOT clock
ENABLE: Data enable signal
PD17-0: RGB(6:6:6)display data

Back porch period (BP):	14H≥BP≥2H
Front porch period (FP):	14H≥FP≥2H
	FP + BP = 16H
Display Period	NL≤320H
The numbers of raster-rows for 1 frame	FP+NL+BP

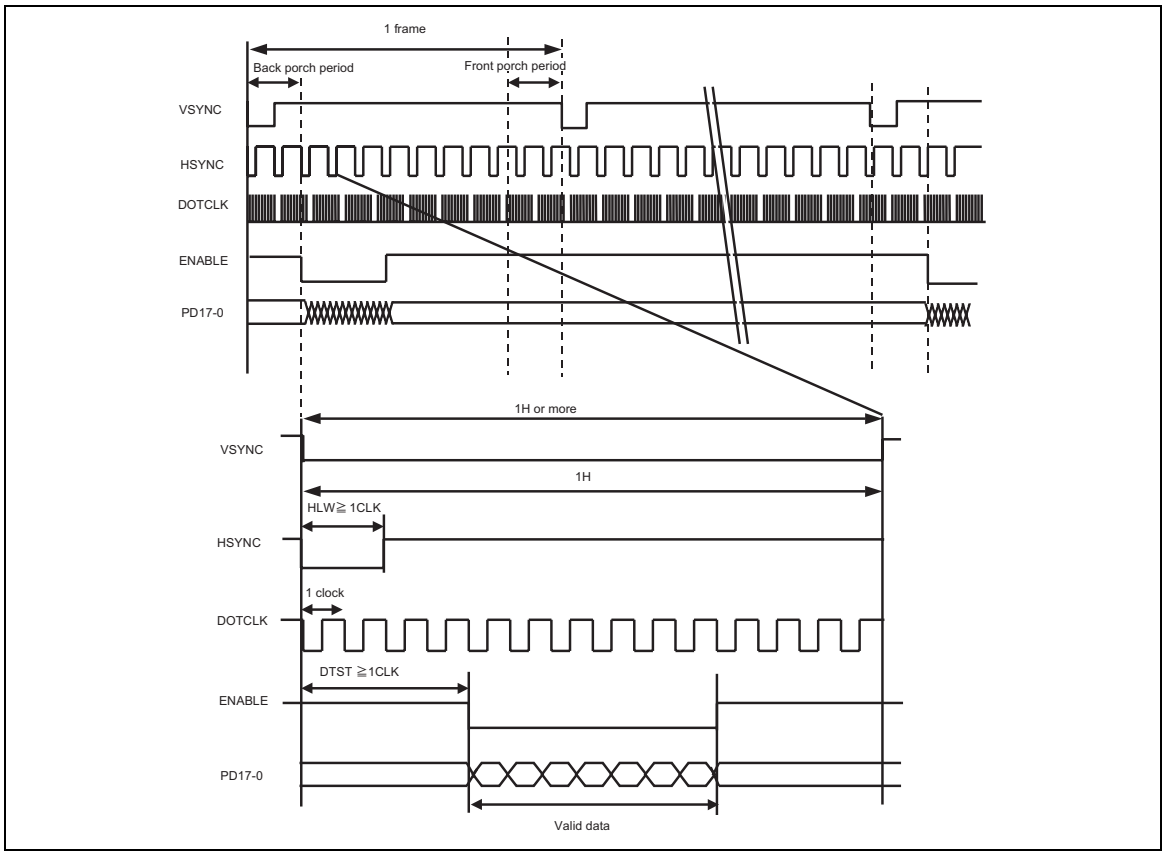
In the RGB interface mode, VYSNC, HSYNC and DOTCLK must be supplied more than to achieve the resolution on the liquid crystal panels.

Polarities of VSYNC, HSYNC, ENABLE, DOTCLK signals

The polarities of VSYNC, HSYNC, ENABLE, DOTCLK signals are changeable by instruction settings (DPL, EPL, HSPL, and VSPL) to conform to the system.

RGB interface timing

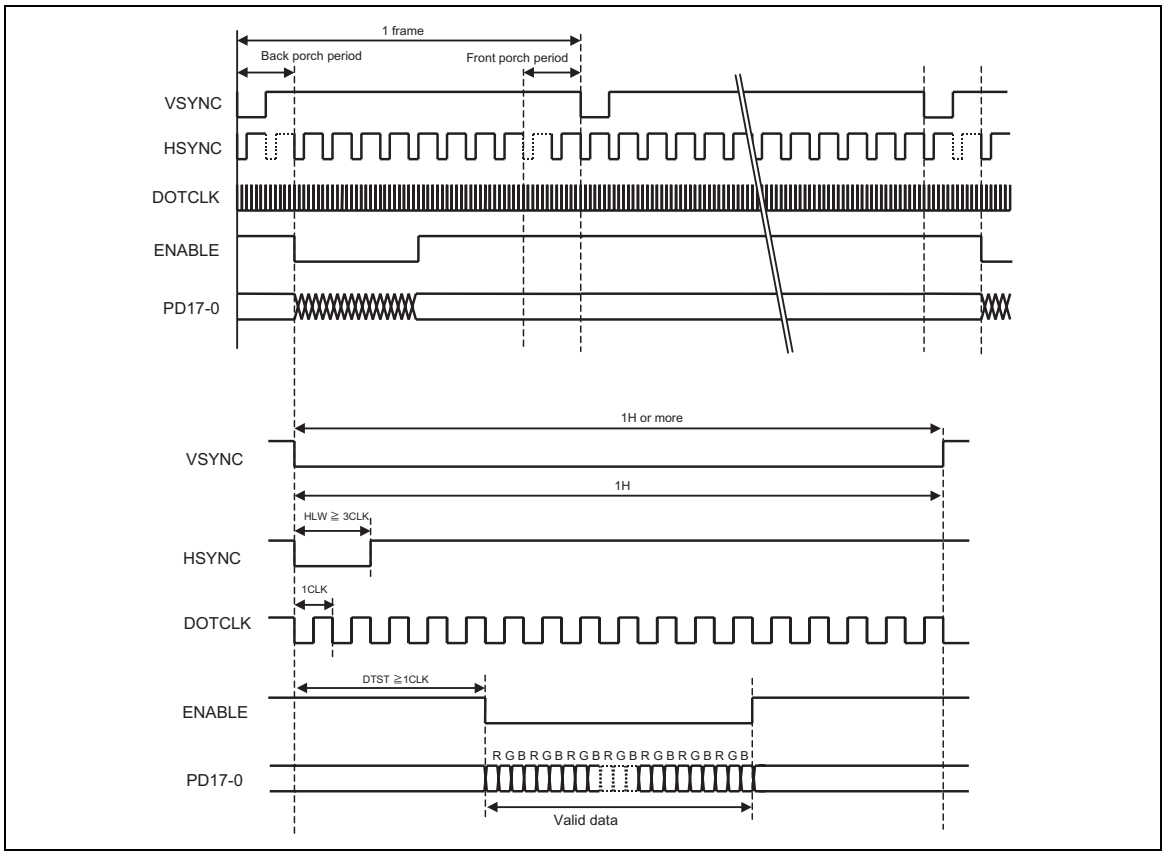
Timing chart of signals in 16/18-bit RGB interface mode



Note 1)VLW: VSYNC “Low” period
HLW: HSYNC “Low” period
DTST: Setup time for data transfer

Note 2) Write data in the high speed write mode (HWM = 1) in the RGB I/F mode.

Timing chart of signals in 6-bit RGB interface mode



Note 1) VLW: VSYNC “Low” period
HLW: HSYNC “Low” period
DTST: Setup time for data transfer

Note 2) Write data in the high speed write mode (HWM = 1) in the RGB I/F mode.

Note 3) VSYNC, HSYNC, EVABLE, DOTCLK, and PD17-0 must be transmitted by 3 clocks.

Moving picture display in RGB Interface

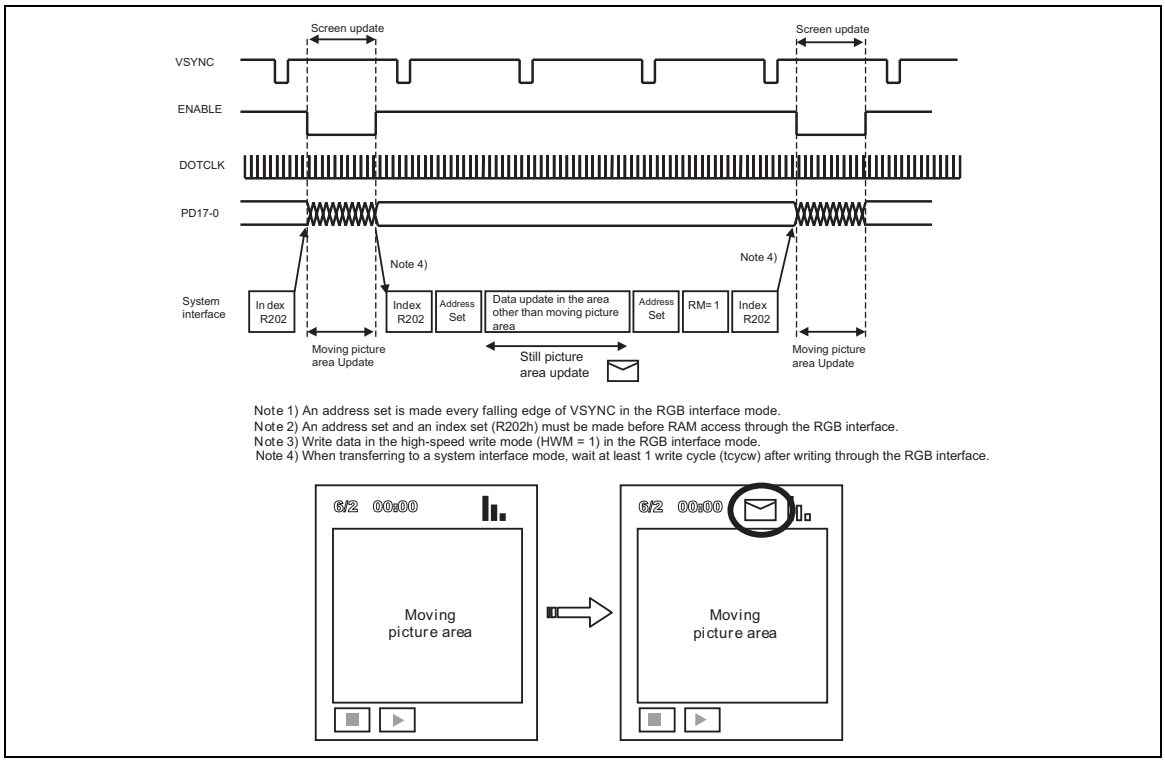
The HD66781 incorporates the RGB interface to display moving pictures and RAM to store display data, which provides the following merits in displaying moving pictures.

- The window address function enables the transfer of only data for the moving picture area.
- The high-speed write modes enables high-speed access to RAM with low power consumption
- Only transfer data that are written over the moving picture area.
- Reduced transmission contributes to the reduction of power consumption of the entire system.
- In combination with the system interface, the still picture area, such as an icon, can be updated while displaying moving pictures.

RAM access through the system interface in RGB-I/F mode

RAM is accessible through the system interface in the RGB-I/F mode. In the RGB interface mode, data are being written to RAM in synchronization with the DOTCLK input while the ENABLE is "Low". When writing data to RAM through the system interface, it is necessary to set ENABLE to "High" to stop data write through the RGB-I/F. Setting RM = 0 allows RAM access through the system interface. When reverting to the RGB interface mode, wait a write/read bus cycle. Then, set RM = 1 and the index to R202h to start RAM access though the RGB-I/F. When RAM write through the RGB and system interfaces conflicts, it is not guaranteed that the data are properly written to RAM.

The following is an example of moving picture display through the RGB-I/F and updating still picture area through the system interface.

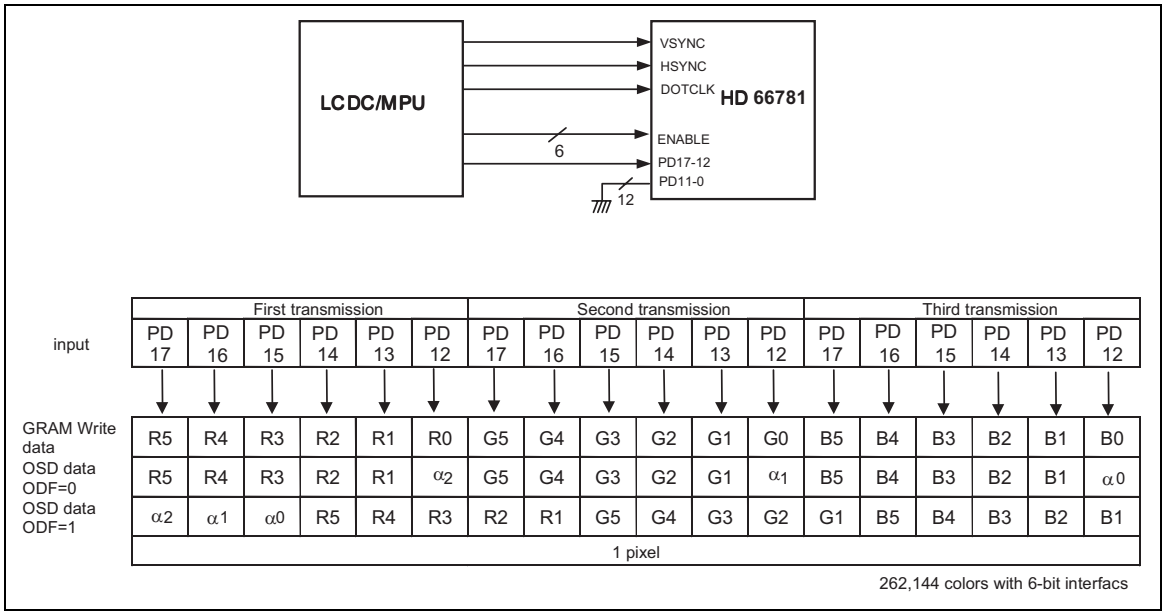


Updating still picture area during moving picture display

6-bit RGB interface

The 6-bit RGB interface is selected by setting RIM1-0 bits to 10. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transmitted to RAM in synchronization with the display operation through 6-bit RGB data bus (PD17-12) according to the data enable signal (ENABLE). Unused pins (PD11 to 0) must be fixed to either IOVcc or GND level.

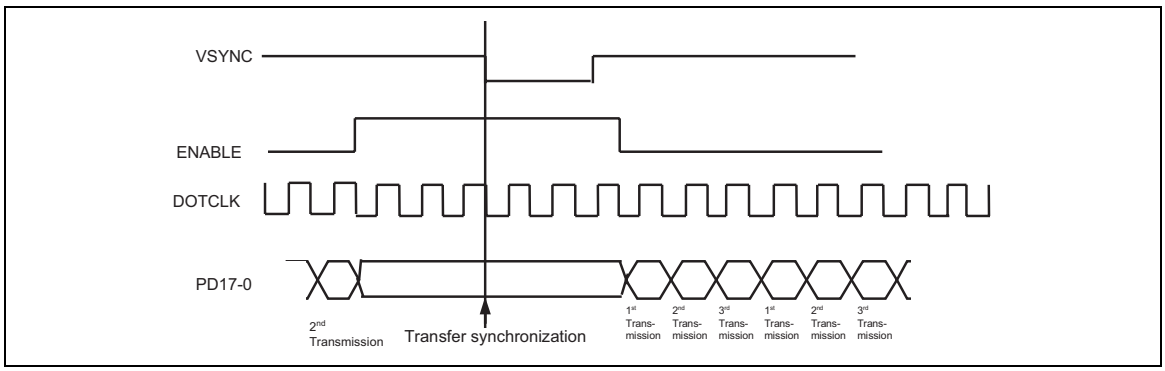
The instructions are set only through the system interface.



Example of 6-Bit RGB Interface and data format

Transfer synchronization function for a 6-bit bus interface

The HD66781 incorporates a transmission counter to count the first, second, third data transmissions in 6-bit RBG interface mode. The transmission counter is always reset to the first transmission on the falling edge of the VSYNC. When a discrepancy occurs in the transmission of first, second and third data, the counter is reset to the first data transmission at the start of each frame (the falling edge of VSYNC) and the data transmission restarts in the correct order from the next frame. In case of displaying moving pictures, which requires consecutive data transfer, this function minimizes the effect from the discrepancy in the data transmission and facilitates to return to the normal display.

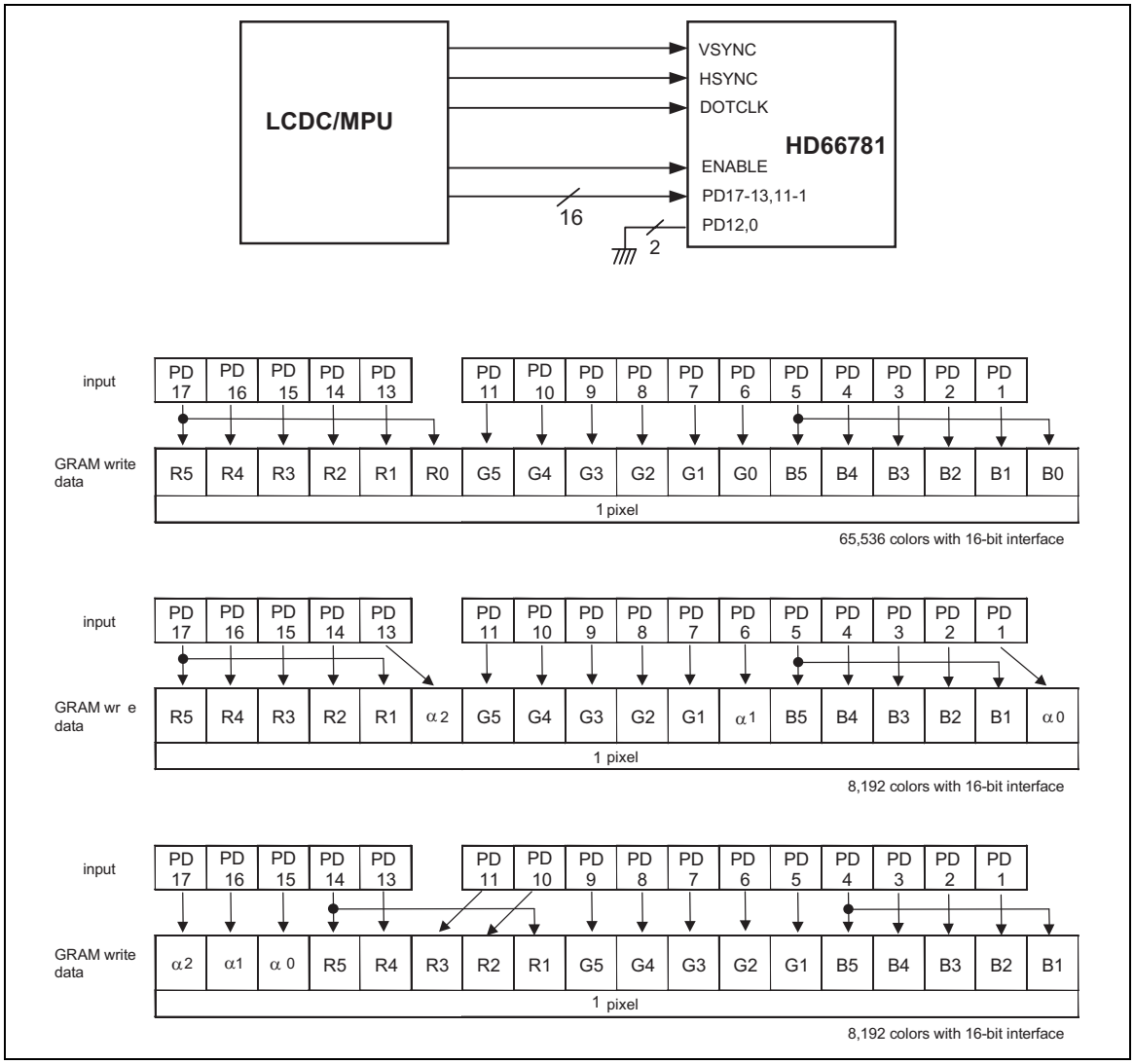


6-bit Transfer Synchronization

16-bit RGB interface

The 16-bit RGB interface is selected by setting RIM1-0 bits to 01. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transmitted to RAM in synchronization with the display operation through16-bit RGB data bus (PD17-13, 11-1) according to the data enable signal (ENABLE).

The instructions are set only through the system interface.

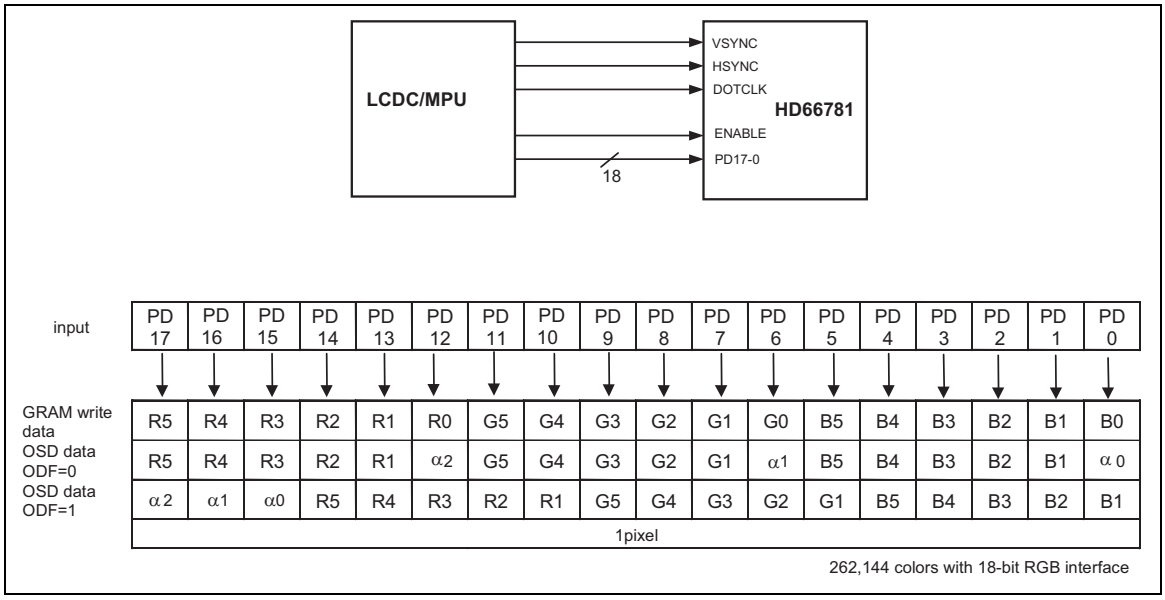


Example of 16-Bit RGB Interface and data format

18-bit RGB interface

The 18-bit RGB interface is selected by setting RIM1-0 bits to 10. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transmitted to RAM in synchronization with the display operation through 18-bit RGB data bus (PD17-0) according to the data enable signal (ENABLE).

The instructions are set only through the system interface.



Example of 18-Bit RGB Interface and data format

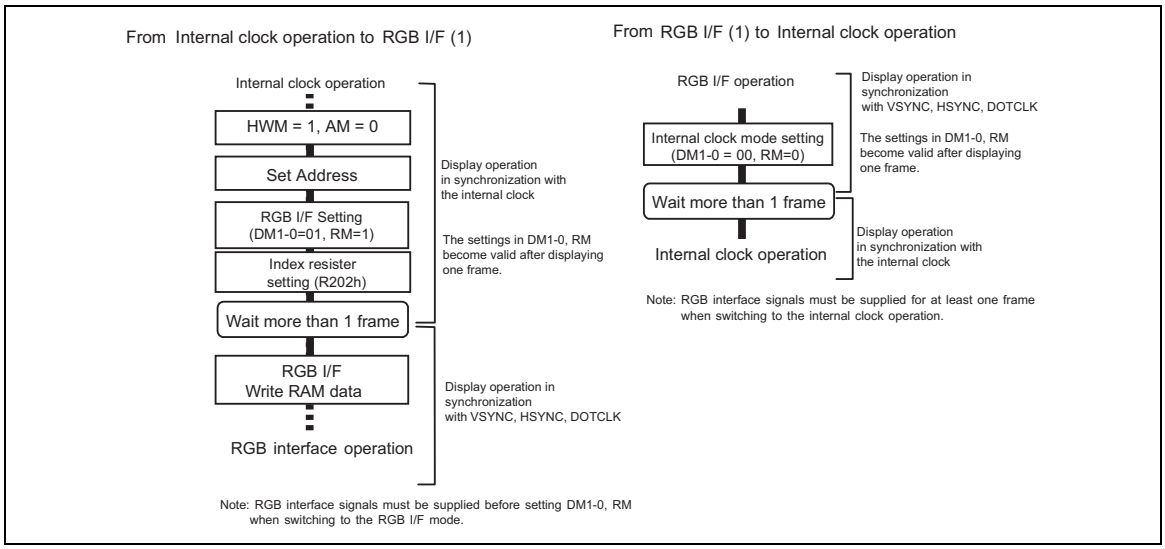
Notes to the external display interface

1. While an external display interface is selected, the following functions are not available.

Table 66

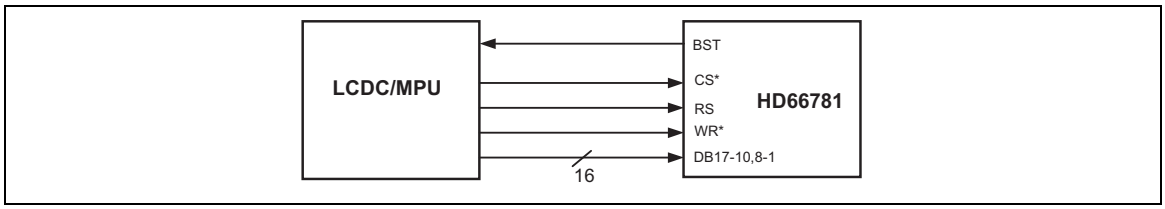
Function	External Display Interface	Internal Display Operation
Partial display	Not available	Available
Scroll function	Not available	Available
Interlaced drive	Not available	Available

2. The VSYNC, HSYNC, and DOTCLK signals must be supplied through the display operation through the RGB-I/F.
3. When making settings for gate driver/LTPS panel controlling signal in the RGB-I/F modes, the reference clock is DOTCLK, not the internal operation clocks.
4. In the 6-bit RGB-I/F mode, the RGB (pixels) data are transmitted by three clocks.
5. In the 6-bit RGB-I/F mode, the interface signals, VSYNC, HSYNC, DOTCL, ENABLE, and PD17-0, should be set by RGB (pixels) unit in convenience for the transmitting RGB pixels.
6. The transitions between the internal operation mode and external display interface should be made according to the mode switching sequence below.
7. In the RGB-I/F mode, the front porch period continues after displaying one frame data until the next VSYNC signal input.
8. In the RGB-I/F mode, the data must be written in the high-speed write mode (HWM = 1).
9. In the RGB-I/F mode, the address is set every frame on the falling edge of VSYNC.



Display Synchroniaing Data Transfer

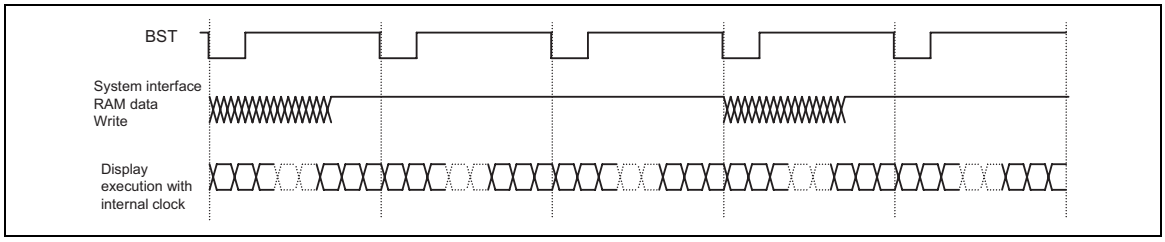
The HD66781 outputs BST signal that indicates the start of vertical retrace line period for flicker-free screen update. The BST signal is used as trigger to start internal GRAM write so that data transfer is synchronized with display scan.



Display synchronizing data transfer: Interface example

By writing data to RAM through the system interface in a speed that is higher for more than a fixed speed than the internal display operation speed, it enables moving picture display through an conventional interface and flicker-free screen update.

All display data are stored in RAM. Therefore, it only requires transfer of the data that is written over to update the screen, thereby minimizing the numbers of data transfers while displaying moving picture. The use of high-speed write mode (HWM = 1) with VSYNC interface enables RAM access in high speed with low power consumption.



Moving picture data transmission through VSYNC interface

Note 1) Data must be written to RAM in the high-speed write mode (HWM = 1) in VSYNC interface mode.

The display synchronizing data transfer mode has limits on the minimum speed for RAM write through the system interface and the frequency of the internal clock. It requires RAM write speed more than the calculated result from the following formula.

Internal clock frequency (fosc) [Hz]
= Frame frequency × (Display raster-row (NL) + Front porch (FP) +Back porch (BP)) × 16 clocks
× Fluctuation

RAM writing speed (min.) [Hz]
> 320× Display lines (NL)/{[(Front porch (FP)+Back porch (BP)+Display lines (NL) – margin) x 16 clocks] /fosc}

When RAM write does not start immediately after the rising edge of BST, the period from the rising edge of BST to the start of RAM write must also be taken into consideration.

An example of calculations for the internal clock frequency and RAM write speed in the display synchronizing data transfer mode is as follows.

- Calculation Example: moving picture display in VSYNC I/F
- Panel size 240 RGB × 320 raster-rows (NL0 = 6'27)
- Total number of raster-rows(NL) 320 raster-rows
- Back, Front porches 14, 2, raster-rows (BP = 4'hE, FP = 4'h2)
- Frame frequency 60Hz

Internal clock frequency (fosc) Hz
= 60 Hz × (320 + 2 + 14) raster-rows × 16 clocks × 1.1 / 0.9 = 394 [kHz]

When calculating an internal clock frequency, possible causes of fluctuations must also be taken into consideration. The allowance for this fluctuation is ± 10 % from the center value, and the range of the frequency must be within the BST signal cycle.

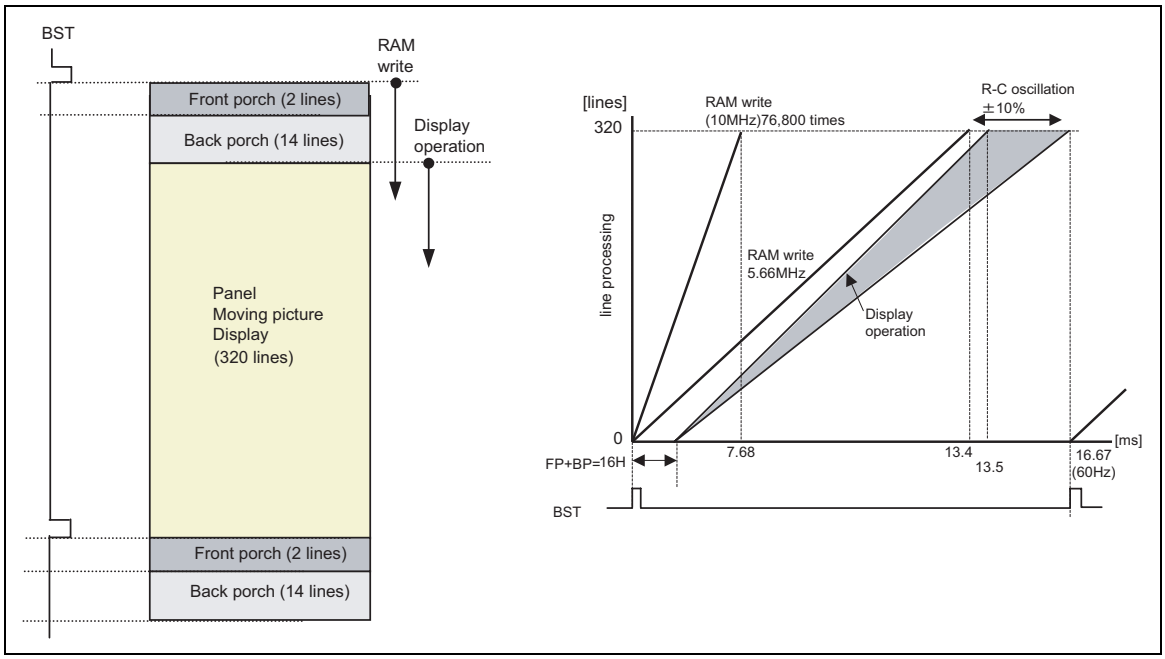
As the causes of fluctuations, the above example takes the variation in the LSI fabrication and the room temperature into account. Other possible causes of fluctuations, such as variation in the external resistors or the voltage change are not considered in the above calculation. It is necessary to make a setting with enough margins to include the allowances for these factors.

Minimum RAM writing speed [Hz]
> 240 × 320 / {((2+14 + 320 - 2) raster-rows × 16 clocks) / 394 kHz} = 5.66 [MHz]

In this case, RAM write is performed on the rising edge of BST.

When the data for one frame are written to RAM completely, there must be 2 raster-rows or more of a margin before the display raster-rows.

According to the above calculation results, writing data to RAM on the rising of BST at the speed of 5.66 MHz or more, the data for the entire screen on RAM are overwritten before the display operation starts. Accordingly, the flicker due to moving picture update can be avoided even if displaying a moving picture.



Minimum RAM write speed and internal clock frequency in VSYNC interface

Notes to the display synchronizing GRAM data transfer mode

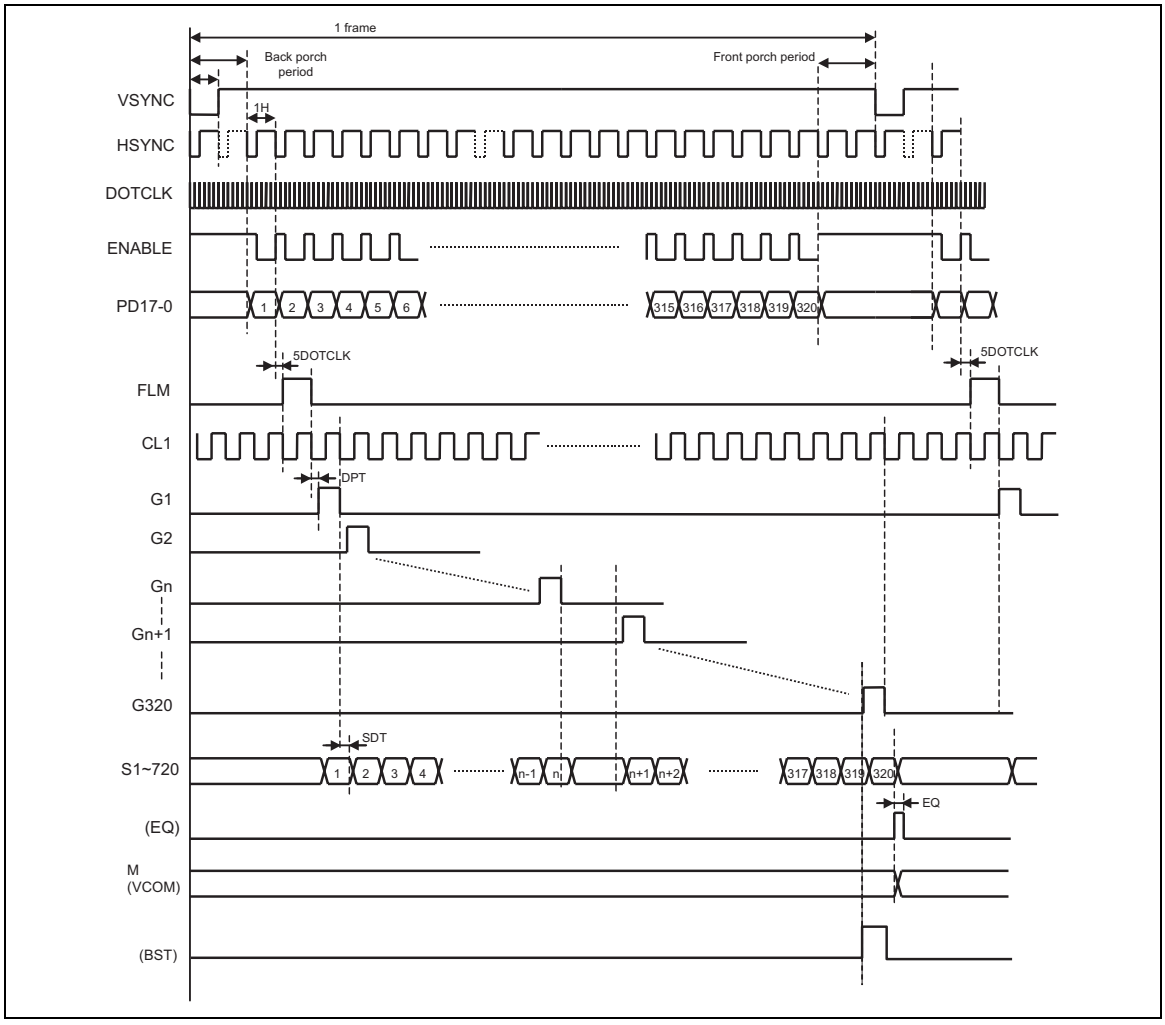
1. The aforementioned example of calculation is just a result of calculation. In the actual settings, causes for the fluctuations such as internal oscillators and so on should be taken into consideration. It is necessary to make a setting for RAM write speed with enough margins.

2. In the display synchronizing GRAM data transfer mode, write display data to RAM in the high speed write mode (HWM = 1)

Timing interfacing with LCD panel signals

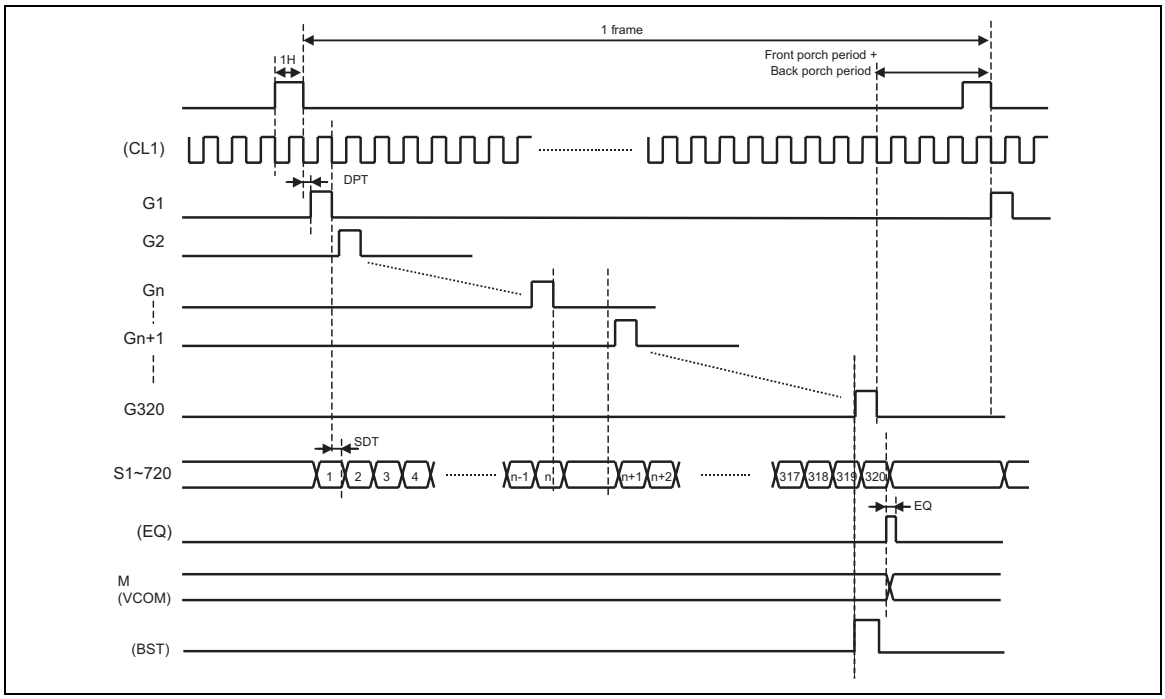
The relationship between RGB I/F signals and LCD panel signals during internal operation is as follows.

Timing interfacing with liquid crystal panel signals in RGB interface mode



Note 1) This figure is the example when DIVE[1:0] = 2'h2

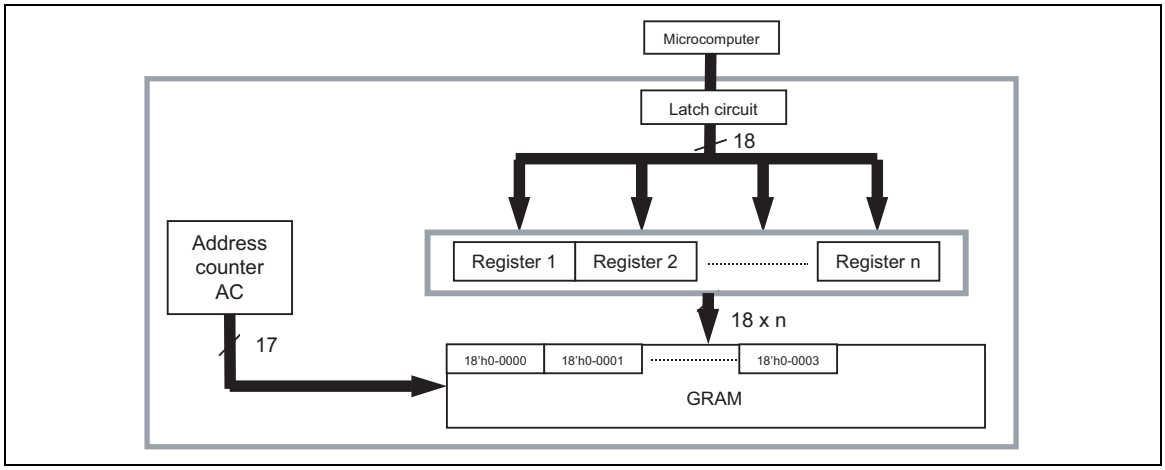
Timing interfacing with liquid crystal panel signals in internal clock operation mode



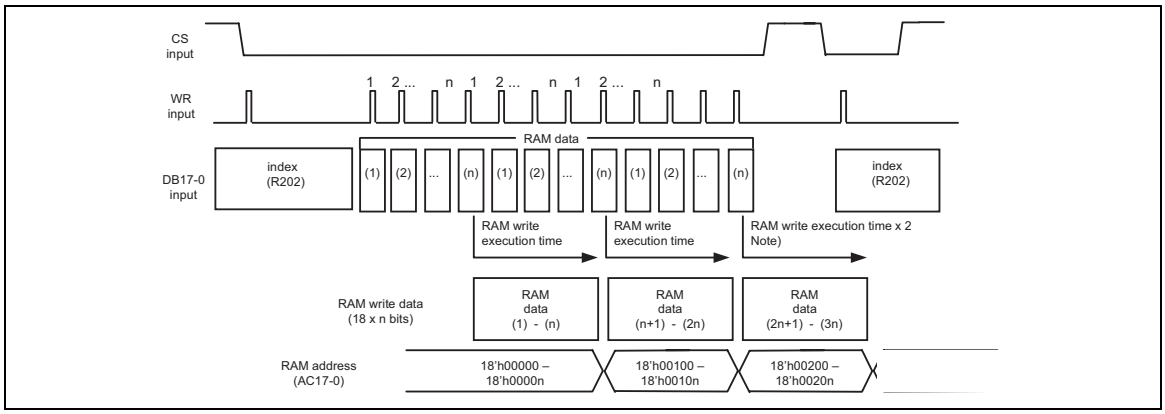
High-Speed Burst RAM Write Function

The HD66781 incorporates high-speed burst RAM-write function, which writes data to RAM about half the time required for the normal RAM write. This function is especially useful for applications, which require high-speed display data rewrite, such as colored moving picture display and so on.

In the high-speed RAM-write mode (HWM=1), data to write to RAM is temporarily stored to the internal register of HD66781 and then written to RAM by horizontal line in the area specified by the window address. Since the data stored in the register are written to RAM at once, it is possible to write next data to the internal register while data are being written from the internal register to RAM. This reduces the frequency of RAM access to minimum and enables consecutive high-speed access to the internal RAM with low power consumption, which is required for moving picture display.

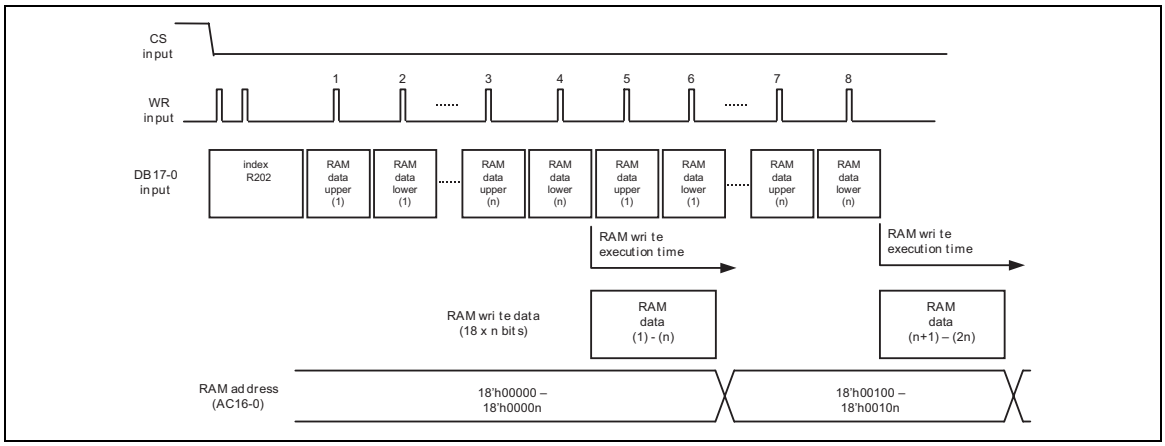


High-speed consecutive access to RAM, operational flow



High-speed consecutive access to RAM (HWM = "1")

Note 1) When making a transition from the high-speed RAM write to the index write, wait at least 2 bus cycle time (t_{cycw}) in the normal write mode after RAM write before executing next instructions.



High-speed consecutive access to RAM (9-bit interface)

Note 1) The high-speed RAM write mode (HWM=1) writes data to RAM by n words. In the 9-bit interface mode, data are written to RAM 2xn times per line.

Notes to the high-speed RAM write mode

1. RAM write is executed by line. If write operation is terminated before it reaches the end of horizontal line of the window-address area, it is not guaranteed that data are properly written on that line.

2. The index register for the RAM data write (202H), if selected, executes the first data write operation. This setting does not allow RAM data read. HWM must be set to 0 during RAM read.

3. The high-speed RAM write mode is not compatible with the normal RAM write mode. Whenever switching to the other mode, it is necessary to set the address before starting RAM write.

Table 67

	Normal RAM Write (HWM=0)	**High-Speed RAM Write (HWM=1)**
BGR function	Available	Available
Write mask function	Available	Available
RAM address set	Set by words	Set by words
RAM read	Set by words	Not available
RAM write	Set by words	Set by lines
Window address	Set by words (minimum range: 1 word x 1 line)	Set by words (minimum range: 8 word x 1 line)
External display interface	Available	Available
AM	AM = 1/0	AM = 0

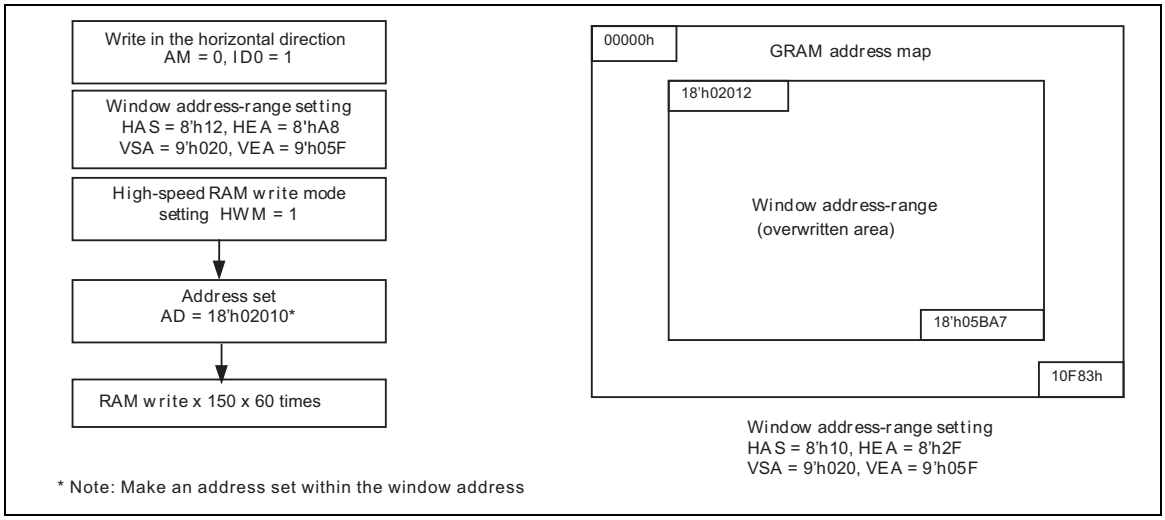
High-Speed RAM Write with Window Address Function

Specifying a window-address range (minimum range: 8 words x 1 word) enables consecutive high-speed RAM data write in an arbitrary rectangular area on RAM.

In the high-speed write mode, data must be written to RAM by horizontal lines. If RAM write is terminated in the middle of the line, there is no guarantee that data are properly written on that line.

The following figure illustrates an example of high-speed RAM write in the window-address range on RAM.

By setting the window address specifying bits (HSA = 8'h10, HEA = 8'h2F, VSA = 9'h020, VEA = 9'h05F), data are written consecutively in high speed in the window-address range specified by these bits.



Window Address Function

The window address function writes data consecutively to the on-chip GRAM within the rectangular window-address range specified by the horizontal address registers (start: HSA7-0, end: HEA 7-0) and the vertical address registers (start: VSA7-0, end: VEA7-0).

The address transition direction is determined by AM bit (either increment or decrement). This allows writing data, including picture data, consecutively without taking the data wrap position into consideration.

The window-address range must be specified within the GRAM address area. An address set must be made within the window-address range.

[Conditions on setting window-address range]

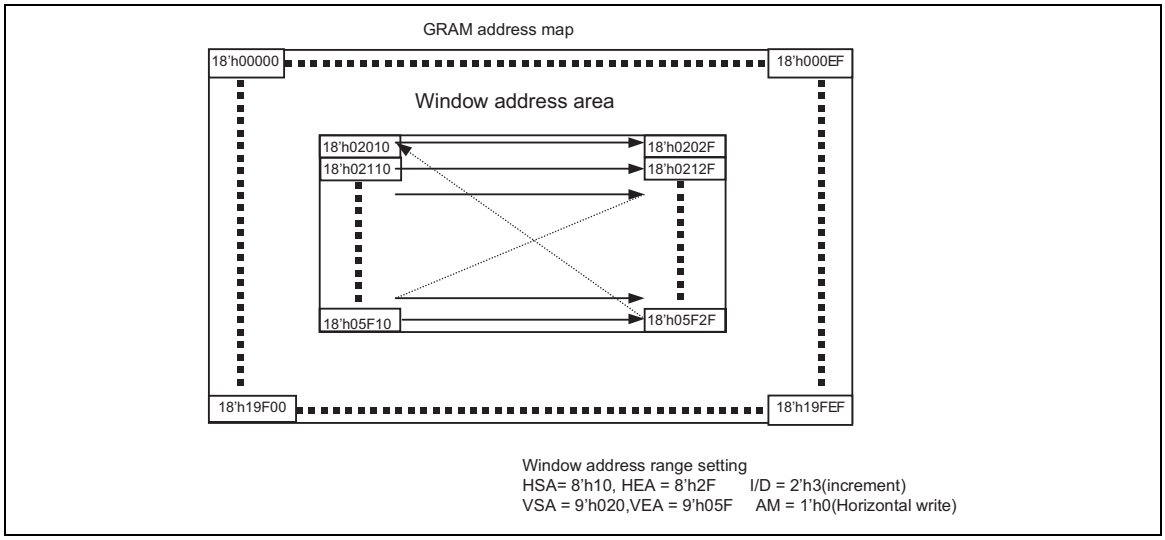
(horizontal direction) 8'h00 ≤ HSA ≤ HEA ≤ 8'hEF

(vertical direction) 9'h000≤ VSA ≤ VEA ≤ 9'h19F

[Conditions on making an address set within the window-address range]

(RAM address) HSA ≤ AD7-0 ≤ HEA

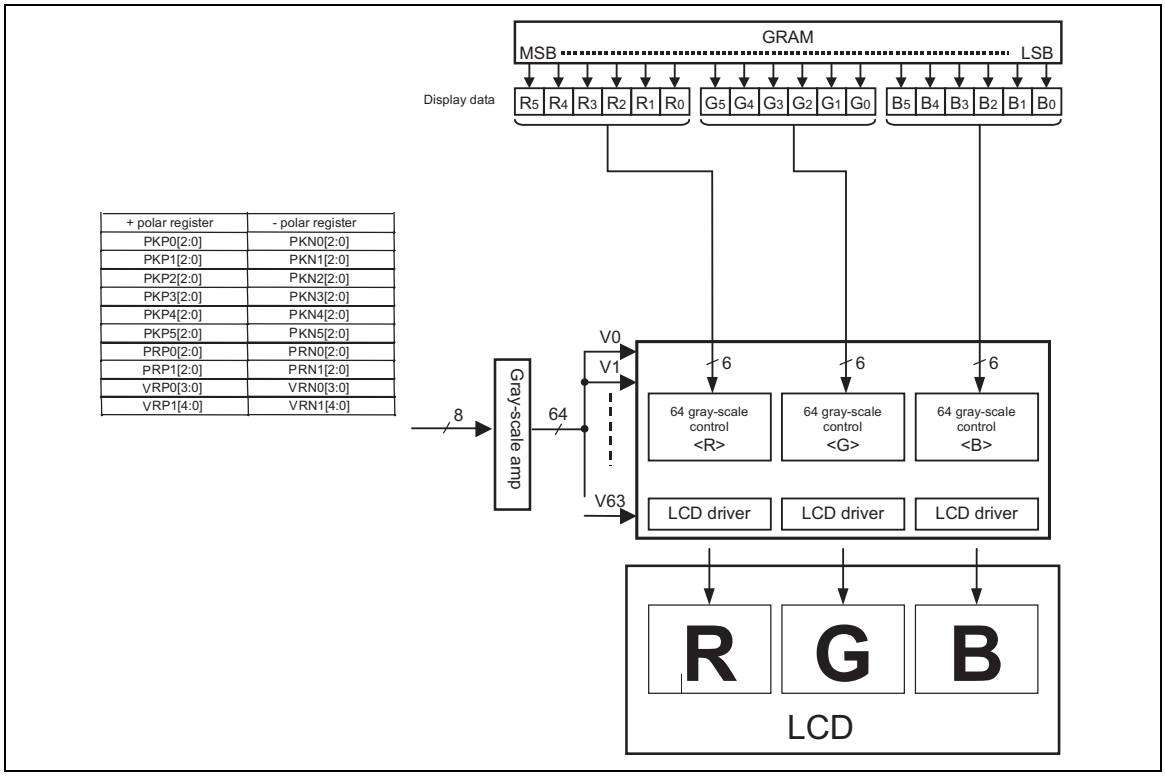
VSA ≤ AD16-8 ≤ VEA



Address transition direction in specified window-address range

γ-Correction Function

The HD66781 incorporates γ-correction function to simultaneously display 262,144 colors, by which 8-level grayscale is determined by the gradient-adjustment and fine-adjustment registers. The HD66781 incorporates gradient-adjustment and fine-adjustment registers for both positive and negative polarities and allows selecting either positive or negative polarity according to the characteristics of a liquid crystal panel.

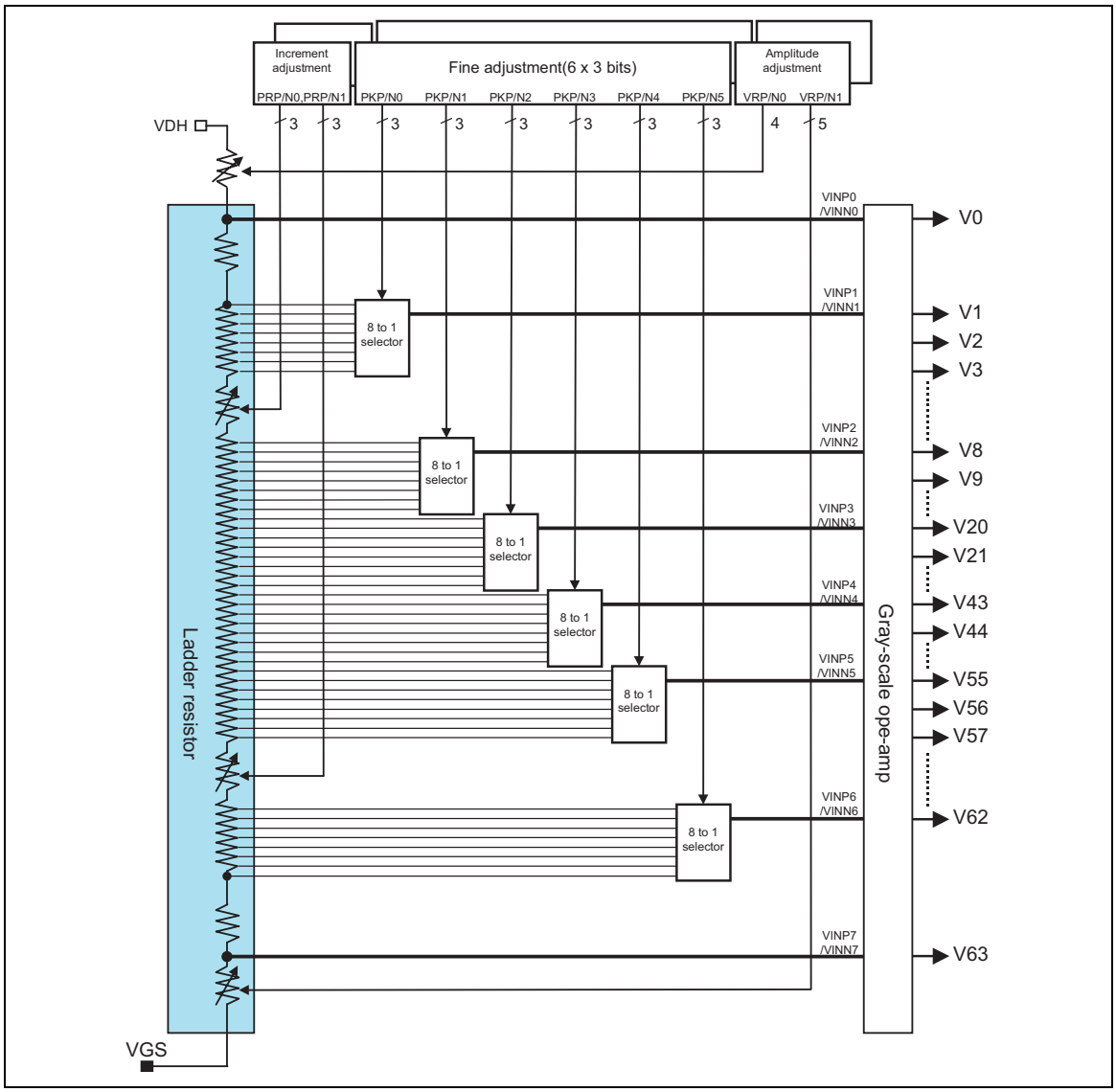


Grayscale control

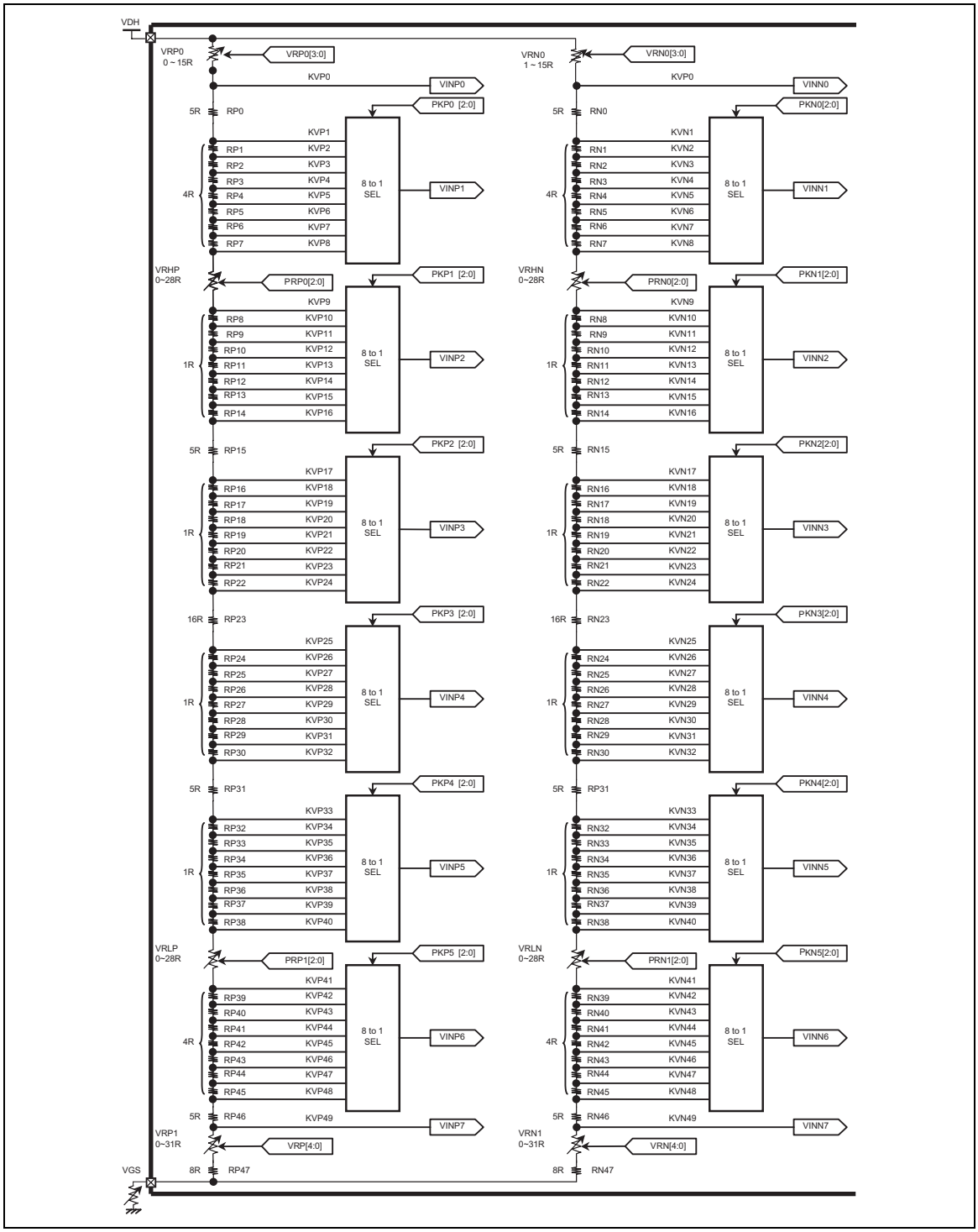
Grayscale Amplifier Configuration

The following figure illustrates the configuration of grayscale amplifier.

The eight-level grayscales (VIN0-7) are determined by the gradient adjustment and fine adjustment registers. The 8 levels are then divided by the ladder resistors placed between each level into 64 levels (V0-63).



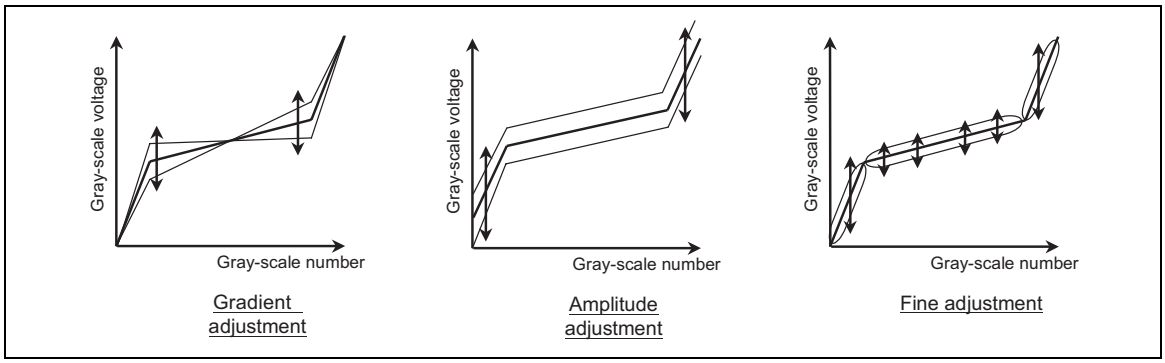
Grayscale amplifier



Ladder Resistors and 8 to 1 Selectors

γ-Correction Registers

The γ-adjustment register is a group of registers to set an appropriate grayscale voltage for the γ-characteristics of a liquid crystal panel. The register group is categorized into the ones adjusting gradient, amplitude, and reference value and fine-tuning in relation to grayscale number and grayscale voltage characteristics. Each register group can make an independent setting for the positive/negative polarity. The reference value and RGB are common to both polarities.



Gradient, Amplitude, Fine Adjustments

1. Gradient adjustment registers

The gradient adjustment registers are used to adjust the gradient around the middle of the grayscale number and voltage characteristics without changing a dynamic range. To adjust a gradient, the values of the variable resistors (VRHP (N)/VRLP (N)) in the ladder resistor block for grayscale voltage generation are controlled. The registers incorporate separate registers for positive and negative polarities to be compatible with asymmetric drive.

2. Amplitude adjustment registers

The amplitude adjustment registers are used to adjust the amplitude of the grayscale voltage. To adjust the amplitude, the values of the variable resistors (VRP(N)1/0) in the upper and lower parts of the ladder resistor block for grayscale voltage generation are adjusted. Same with the gradient registers, the amplitude adjustment registers also incorporate separate registers for positive and negative polarities.

3. Fine adjustment registers

The fine adjustment register is to fine-adjust the grayscale voltage level. To fine-adjust the grayscale voltage level, 8-to-1 selectors control each level of 8-level reference voltages generated from the ladder registers. Same with the other registers, the fine adjustment registers also incorporate separate registers for positive and negative polarities.

Table 68 List of output signals

Register Groups	Positive Polarity	Negative Polarity	Description
Gradient adjustment	PRP0 [2:0]	PRN0 [2:0]	Variable resistor VRHP (N)
	PRP1 [2:0]	PRN1 [2:0]	Variable resistor VRLP (N)
Amplitude adjustment	VRP0 [3:0]	VRN0 [3:0]	Variable resistor VRP (N) 0
	VRP1 [4:0]	VRN1 [4:0]	Variable resistor VRP (N) 1
Fine adjustment	PKP0 [2:0]	PKN0 [2:0]	8-to-1 selector (voltage level of grayscale 1)
	PKP1 [2:0]	PKN1 [2:0]	8-to-1 selector (voltage level of grayscale 8)
	PKP2 [2:0]	PKN2 [2:0]	8-to-1 selector (voltage level of grayscale 20)
	PKP3 [2:0]	PKN3 [2:0]	8-to-1 selector (voltage level of grayscale 43)
	PKP4 [2:0]	PKN4 [2:0]	8-to-1 selector (voltage level of grayscale 55)
	PKP5 [2:0]	PKN5 [2:0]	8-to-1 selector (voltage level of grayscale 62)

Ladder resistors and 8 to 1 selector

Block configuration

The block configuration of page **159** consists of two ladder resistors including variable resistors, and 8 to 1 selectors, which select the voltage generated by the ladder resistors, to output the reference voltage for the grayscale voltage. The γ–correction registers control the variable resistors and the 8 to 1 selectors. Pins that are connected to a variable resistor are also provided to compensate the variation among the panels.

Variable resistors

There are three kinds of variable resistors for the gradient adjustment (VRHP(N)/VRLP(N)), the amplitude adjustment (VRP(N)), and the reference adjustment (VDR). The resistance is determined by the gradient adjustment and amplitude adjustment registers as is shown below.

Table 69

Gradient adjustment

Register PRP(N)0/1[2:0]	Resistance VRHP(N) VRLP(N)
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Amplitude adjustment

Register VRP(N)0[3:0]	Resistance VRP(N)0
0000	0R
0001	1R
0010	2R
:	:
:	:
1101	13R
1110	14R
1111	15R

Reference adjustment

Register VRP(N)1[4:0]	Resistance VRP(N)1
00000	0R
00001	1R
00010	2R
:	:
:	:
11101	29R
11110	30R
11111	31R

8 to 1 selector

The 8-to-1 selectors select a voltage level generated by the ladder resistors according to the fine adjustment registers, and output as a reference voltage of either one of the following VIN1 ~ VIN 6. The relationship between the fine adjustment register and the selected voltage is as follows

Table 70

Contents of Register	Selected Voltage					
PKP(N) 0/1 [2:0]	VINP(N)1	VINP(N)2	VINP(N)3	VINP(N)4	VINP(N)5	VINP(N)6
000	KVP(N)1	KVP(N)9	KVP(N)17	KVP(N)25	KVP(N)33	KVP(N)41
001	KVP(N)2	KVP(N)10	KVP(N)18	KVP(N)26	KVP(N)34	KVP(N)42
010	KVP(N)3	KVP(N)11	KVP(N)19	KVP(N)27	KVP(N)35	KVP(N)43
011	KVP(N)4	KVP(N)12	KVP(N)20	KVP(N)28	KVP(N)36	KVP(N)44
100	KVP(N)5	KVP(N)13	KVP(N)21	KVP(N)29	KVP(N)37	KVP(N)45
101	KVP(N)6	KVP(N)14	KVP(N)22	KVP(N)30	KVP(N)38	KVP(N)46
110	KVP(N)7	KVP(N)15	KVP(N)23	KVP(N)31	KVP(N)39	KVP(N)47
111	KVP(N)8	KVP(N)16	KVP(N)24	KVP(N)32	KVP(N)40	KVP(N)48

The gray scale levels (V0-V63) are calculated according to the following formulas.

Formulas for calculating voltage (Positive polarity) (1)

Pins	Formula	Fine-adjustment registers	Reference voltage
KVP0	VDH-ΔV*VxP0/SUMRP	—	VINP0
KVP1	VDH-ΔV*(VxRP0+5R)/SUMRP	PKP0[2:0]="000"	VINP1
KVP2	VDH-ΔV*(VxRP0+9R)/SUMRP	PKP0[2:0]="001"	
KVP3	VDH-ΔV*(VxRP0+13R)/SUMRP	PKP0[2:0]="010"	
KVP4	VDH-ΔV*(VxRP0+17R)/SUMRP	PKP0[2:0]="011"	
KVP5	VDH-ΔV*(VxRP0+21R)/SUMRP	PKP0[2:0]="100"	
KVP6	VDH-ΔV*(VxRP0+25R)/SUMRP	PKP0[2:0]="101"	
KVP7	VDH-ΔV*(VxRP0+29R)/SUMRP	PKP0[2:0]="110"	
KVP8	VDH-ΔV*(VxRP0+33R)/SUMRP	PKP0[2:0]="111"	
KVP9	VDH-ΔV*(VxRP0+33R+VRHP)/SUMRP	PKP1[2:0]="000"	VINP2
KVP10	VDH-ΔV*(VxRP0+34R+VRHP)/SUMRP	PKP1[2:0]="001"	
KVP11	VDH-ΔV*(VxRP0+35R+VRHP)/SUMRP	PKP1[2:0]="010"	
KVP12	VDH-ΔV*(VxRP0+36R+VRHP)/SUMRP	PKP1[2:0]="011"	
KVP13	VDH-ΔV*(VxRP0+37R+VRHP)/SUMRP	PKP1[2:0]="100"	
KVP14	VDH-ΔV*(VxRP0+38R+VRHP)/SUMRP	PKP1[2:0]="101"	
KVP15	VDH-ΔV*(VxRP0+39R+VRHP)/SUMRP	PKP1[2:0]="110"	
KVP16	VDH-ΔV*(VxRP0+40R+VRHP)/SUMRP	PKP1[2:0]="111"	
KVP17	VDH-ΔV*(VxRP0+45R+VRHP)/SUMRP	PKP2[2:0]="000"	VINP3
KVP18	VDH-ΔV*(VxRP0+46R+VRHP)/SUMRP	PKP2[2:0]="001"	
KVP19	VDH-ΔV*(VxRP0+47R+VRHP)/SUMRP	PKP2[2:0]="010"	
KVP20	VDH-ΔV*(VxRP0+48R+VRHP)/SUMRP	PKP2[2:0]="011"	
KVP21	VDH-ΔV*(VxRP0+49R+VRHP)/SUMRP	PKP2[2:0]="100"	
KVP22	VDH-ΔV*(VxRP0+50R+VRHP)/SUMRP	PKP2[2:0]="101"	
KVP23	VDH-ΔV*(VxRP0+51R+VRHP)/SUMRP	PKP2[2:0]="110"	
KVP24	VDH-ΔV*(VxRP0+52R+VRHP)/SUMRP	PKP2[2:0]="111"	
KVP25	VDH-ΔV*(VxRP0+68R+VRHP)/SUMRP	PKP3[2:0]="000"	VINP4
KVP26	VDH-ΔV*(VxRP0+69R+VRHP)/SUMRP	PKP3[2:0]="001"	
KVP27	VDH-ΔV*(VxRP0+70R+VRHP)/SUMRP	PKP3[2:0]="010"	
KVP28	VDH-ΔV*(VxRP0+71R+VRHP)/SUMRP	PKP3[2:0]="011"	
KVP29	VDH-ΔV*(VxRP0+72R+VRHP)/SUMRP	PKP3[2:0]="100"	
KVP30	VDH-ΔV*(VxRP0+73R+VRHP)/SUMRP	PKP3[2:0]="101"	
KVP31	VDH-ΔV*(VxRP0+74R+VRHP)/SUMRP	PKP3[2:0]="110"	
KVP32	VDH-ΔV*(VxRP0+75R+VRHP)/SUMRP	PKP3[2:0]="111"	
KVP33	VDH-ΔV*(VxRP0+80R+VRHP)/SUMRP	PKP4[2:0]="000"	VINP5
KVP34	VDH-ΔV*(VxRP0+81R+VRHP)/SUMRP	PKP4[2:0]="001"	
KVP35	VDH-ΔV*(VxRP0+82R+VRHP)/SUMRP	PKP4[2:0]="010"	
KVP36	VDH-ΔV*(VxRP0+83R+VRHP)/SUMRP	PKP4[2:0]="011"	
KVP37	VDH-ΔV*(VxRP0+84R+VRHP)/SUMRP	PKP4[2:0]="100"	
KVP38	VDH-ΔV*(VxRP0+85R+VRHP)/SUMRP	PKP4[2:0]="101"	
KVP39	VDH-ΔV*(VxRP0+86R+VRHP)/SUMRP	PKP4[2:0]="110"	
KVP40	VDH-ΔV*(VxRP0+87R+VRHP)/SUMRP	PKP4[2:0]="111"	
KVP41	VDH-ΔV*(VxRP0+87R+VRHP+VRLP)/SUMRP	PKP4[2:0]="000"	VINP6
KVP42	VDH-ΔV*(VxRP0+91R+VRHP+VRLP)/SUMRP	PKP5[2:0]="001"	
KVP43	VDH-ΔV*(VxRP0+95R+VRHP+VRLP)/SUMRP	PKP5[2:0]="010"	
KVP44	VDH-ΔV*(VxRP0+99R+VRHP+VRLP)/SUMRP	PKP5[2:0]="011"	
KVP45	VDH-ΔV*(VxRP0+103R+VRHP+VRLP)/SUMRP	PKP5[2:0]="100"	
KVP46	VDH-ΔV*(VxRP0+107R+VRHP+VRLP)/SUMRP	PKP5[2:0]="101"	
KVP47	VDH-ΔV*(VxRP0+111R+VRHP+VRLP)/SUMRP	PKP5[2:0]="110"	
KVP48	VDH-ΔV*(VxRP0+115R+VRHP+VRLP)/SUMRP	PKP5[2:0]="111"	
KVP49	VDH-ΔV*(VxRP0+120R+VRHP+VRLP)/SUMRP	—	VINP7

Note 1) Sum of ladder resistors with positive polarities = 128R+VRHP+VRLP+VRP0+VRP1

Note 2) Sum of ladder resistors with negative polarities = 128R+VRHN+VRLN+VRN0+VRN1

Note 3) ΔV :Electric potential difference between VDH and VGS

Formulas for calculating voltage (Positive polarity) (2)

Grayscale voltage	Formula
V0	VINP0
V1	VINP1
V2	V8+(V1-V8)*(30/48)
V3	V8+(V1-V8)*(23/48)
V4	V8+(V1-V8)*(16/48)
V5	V8+(V1-V8)*(12/48)
V6	V8+(V1-V8)*(8/48)
V7	V8+(V1-V8)*(4/48)
V8	VINP2
V9	V20+(V8-V20)*(22/24)
V10	V20+(V8-V20)*(20/24)
V11	V20+(V8-V20)*(18/24)
V12	V20+(V8-V20)*(16/24)
V13	V20+(V8-V20)*(14/24)
V14	V20+(V8-V20)*(12/24)
V15	V20+(V8-V20)*(10/24)
V16	V20+(V8-V20)*(8/24)
V17	V20+(V8-V20)*(6/24)
V18	V20+(V8-V20)*(4/24)
V19	V20+(V8-V20)*(2/24)
V20	VINP3
V21	V43+(V20-V43)*(22/23)
V22	V43+(V20-V43)*(21/23)
V23	V43+(V20-V43)*(20/23)
V24	V43+(V20-V43)*(19/23)
V25	V43+(V20-V43)*(18/23)
V26	V43+(V20-V43)*(17/23)
V27	V43+(V20-V43)*(16/23)
V28	V43+(V20-V43)*(15/23)
V29	V43+(V20-V43)*(14/23)
V30	V43+(V20-V43)*(13/23)
V31	V43+(V20-V43)*(12/23)

Grayscale voltage	Formula
V32	V43+(V20-V43)*(11/23)
V33	V43+(V20-V43)*(10/23)
V34	V43+(V20-V43)*(9/23)
V35	V43+(V20-V43)*(8/23)
V36	V43+(V20-V43)*(7/23)
V37	V43+(V20-V43)*(6/23)
V38	V43+(V20-V43)*(5/23)
V39	V43+(V20-V43)*(4/23)
V40	V43+(V20-V43)*(3/23)
V41	V43+(V20-V43)*(2/23)
V42	V43+(V20-V43)*(1/23)
V43	VINP4
V44	V55+(V43-V55)*(22/24)
V45	V55+(V43-V55)*(20/24)
V46	V55+(V43-V55)*(18/24)
V47	V55+(V43-V55)*(16/24)
V48	V55+(V43-V55)*(14/24)
V49	V55+(V43-V55)*(12/24)
V50	V55+(V43-V55)*(10/24)
V51	V55+(V43-V55)*(8/24)
V52	V55+(V43-V55)*(6/24)
V53	V55+(V43-V55)*(4/24)
V54	V55+(V43-V55)*(2/24)
V55	VINP5
V56	V62+(V55-V62)*(44/48)
V57	V62+(V55-V62)*(40/48)
V58	V62+(V55-V62)*(36/48)
V59	V62+(V55-V62)*(32/48)
V60	V62+(V55-V62)*(25/48)
V61	V62+(V55-V62)*(18/48)
V62	VINP6
V63	VINP7

Note 1) Make sure DDVDH – V0 > 0.5V, DDVDH – V4 > 1.1V, V55-GND > 1.1V

Formulas for calculating voltage (Negative polarity) (1)

Pins	Formula	Fine-adjustment registers	Reference voltage
KVN0	VDH-ΔV*VxRN0/SUMRN	—	VINN0
KVN1	VDH-ΔV*(VxRN0+5R)/SUMRN	PKN0[2:0]="000"	VINN1
KVN2	VDH-ΔV*(VxRN0+9R)/SUMRN	PKN0[2:0]="001"	
KVN3	VDH-ΔV*(VxRN0+13R)/SUMRN	PKN0[2:0]="010"	
KVN4	VDH-ΔV*(VxRN0+17R)/SUMRN	PKN0[2:0]="011"	
KVN5	VDH-ΔV*(VxRN0+21R)/SUMRN	PKN0[2:0]="100"	
KVN6	VDH-ΔV*(VxRN0+25R)/SUMRN	PKN0[2:0]="101"	
KVN7	VDH-ΔV*(VxRN0+29R)/SUMRN	PKN0[2:0]="110"	
KVN8	VDH-ΔV*(VxRN0+33R)/SUMRN	PKN0[2:0]="111"	
KVN9	VDH-ΔV*(VxRN0+33R+VRHN)/SUMRN	PKN1[2:0]="000"	VINN2
KVN10	VDH-ΔV*(VxRN0+34R+VRHN)/SUMRN	PKN1[2:0]="001"	
KVN11	VDH-ΔV*(VxRN0+35R+VRHN)/SUMRN	PKN1[2:0]="010"	
KVN12	VDH-ΔV*(VxRN0+36R+VRHN)/SUMRN	PKN1[2:0]="011"	
KVN13	VDH-ΔV*(VxRN0+37R+VRHN)/SUMRN	PKN1[2:0]="100"	
KVN14	VDH-ΔV*(VxRN0+38R+VRHN)/SUMRN	PKN1[2:0]="101"	
KVN15	VDH-ΔV*(VxRN0+39R+VRHN)/SUMRN	PKN1[2:0]="110"	
KVN16	VDH-ΔV*(VxRN0+40R+VRHN)/SUMRN	PKN1[2:0]="111"	
KVN17	VDH-ΔV*(VxRN0+45R+VRHN)/SUMRN	PKN2[2:0]="000"	VINN3
KVN18	VDH-ΔV*(VxRN0+46R+VRHN)/SUMRN	PKN2[2:0]="001"	
KVN19	VDH-ΔV*(VxRN0+47R+VRHN)/SUMRN	PKN2[2:0]="010"	
KVN20	VDH-ΔV*(VxRN0+48R+VRHN)/SUMRN	PKN2[2:0]="011"	
KVN21	VDH-ΔV*(VxRN0+49R+VRHN)/SUMRN	PKN2[2:0]="100"	
KVN22	VDH-ΔV*(VxRN0+50R+VRHN)/SUMRN	PKN2[2:0]="101"	
KVN23	VDH-ΔV*(VxRN0+51R+VRHN)/SUMRN	PKN2[2:0]="110"	
KVN24	VDH-ΔV*(VxRN0+52R+VRHN)/SUMRN	PKN2[2:0]="111"	
KVN25	VDH-ΔV*(VxRN0+68R+VRHN)/SUMRN	PKN3[2:0]="000"	VINN4
KVN26	VDH-ΔV*(VxRN0+69R+VRHN)/SUMRN	PKN3[2:0]="001"	
KVN27	VDH-ΔV*(VxRN0+70R+VRHN)/SUMRN	PKN3[2:0]="010"	
KVN28	VDH-ΔV*(VxRN0+71R+VRHN)/SUMRN	PKN3[2:0]="011"	
KVN29	VDH-ΔV*(VxRN0+72R+VRHN)/SUMRN	PKN3[2:0]="100"	
KVN30	VDH-ΔV*(VxRN0+73R+VRHN)/SUMRN	PKN3[2:0]="101"	
KVN31	VDH-ΔV*(VxRN0+74R+VRHN)/SUMRN	PKN3[2:0]="110"	
KVN32	VDH-ΔV*(VxRN0+75R+VRHN)/SUMRN	PKN3[2:0]="111"	
KVN33	VDH-ΔV*(VxRN0+80R+VRHN)/SUMRN	PKN4[2:0]="000"	VINN5
KVN34	VDH-ΔV*(VxRN0+81R+VRHN)/SUMRN	PKN4[2:0]="001"	
KVN35	VDH-ΔV*(VxRN0+82R+VRHN)/SUMRN	PKN4[2:0]="010"	
KVN36	VDH-ΔV*(VxRN0+83R+VRHN)/SUMRN	PKN4[2:0]="011"	
KVN37	VDH-ΔV*(VxRN0+84R+VRHN)/SUMRN	PKN4[2:0]="100"	
KVN38	VDH-ΔV*(VxRN0+85R+VRHN)/SUMRN	PKN4[2:0]="101"	
KVN39	VDH-ΔV*(VxRN0+86R+VRHN)/SUMRN	PKN4[2:0]="110"	
KVN40	VDH-ΔV*(VxRN0+87R+VRHN)/SUMRN	PKN4[2:0]="111"	
KVN41	VDH-ΔV*(VxRN0+87R+VRHN+VRLN)/SUMRN	PKN4[2:0]="000"	VINN6
KVN42	VDH-ΔV*(VxRN0+91R+VRHN+VRLN)/SUMRN	PKN5[2:0]="001"	
KVN43	VDH-ΔV*(VxRN0+95R+VRHN+VRLN)/SUMRN	PKN5[2:0]="010"	
KVN44	VDH-ΔV*(VxRN0+99R+VRHN+VRLN)/SUMRN	PKN5[2:0]="011"	
KVN45	VDH-ΔV*(VxRN0+103R+VRHN+VRLN)/SUMRN	PKN5[2:0]="100"	
KVN46	VDH-ΔV*(VxRN0+107R+VRHN+VRLN)/SUMRN	PKN5[2:0]="101"	
KVN47	VDH-ΔV*(VxRN0+111R+VRHN+VRLN)/SUMRN	PKN5[2:0]="110"	
KVN48	VDH-ΔV*(VxRN0+115R+VRHN+VRLN)/SUMRN	PKN5[2:0]="111"	
KVN49	VDH-ΔV*(VxRN0+120R+VRHN+VRLN)/SUMRN	—	VINN7

Note 1) Sum of ladder resistors with positive polarities = 128R+VRHP+VRLP+VRP0+VRP1

Note 2) Sum of ladder resistors with negative polarities = 128R+VRHN+VRLN+VRN0+VRN1

Note 3) ΔV :Electric potential difference between VDH and VGS

Formulas for calculating voltage (Negative polarity) (2)

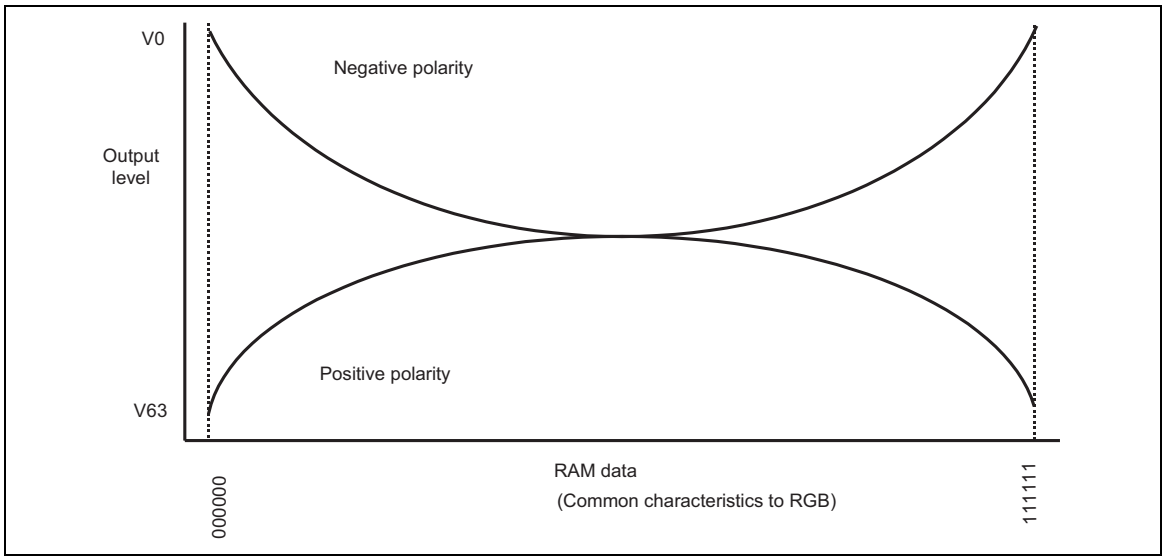
Grayscale voltage	Formula
V0	VINN0
V1	VINN1
V2	V8+(V1-V8)*(30/48)
V3	V8+(V1-V8)*(23/48)
V4	V8+(V1-V8)*(16/48)
V5	V8+(V1-V8)*(12/48)
V6	V8+(V1-V8)*(8/48)
V7	V8+(V1-V8)*(4/48)
V8	VINN2
V9	V20+(V8-V20)*(22/24)
V10	V20+(V8-V20)*(20/24)
V11	V20+(V8-V20)*(18/24)
V12	V20+(V8-V20)*(16/24)
V13	V20+(V8-V20)*(14/24)
V14	V20+(V8-V20)*(12/24)
V15	V20+(V8-V20)*(10/24)
V16	V20+(V8-V20)*(8/24)
V17	V20+(V8-V20)*(6/24)
V18	V20+(V8-V20)*(4/24)
V19	V20+(V8-V20)*(2/24)
V20	VINN3
V21	V43+(V20-V43)*(22/23)
V22	V43+(V20-V43)*(21/23)
V23	V43+(V20-V43)*(20/23)
V24	V43+(V20-V43)*(19/23)
V25	V43+(V20-V43)*(18/23)
V26	V43+(V20-V43)*(17/23)
V27	V43+(V20-V43)*(16/23)
V28	V43+(V20-V43)*(15/23)
V29	V43+(V20-V43)*(14/23)
V30	V43+(V20-V43)*(13/23)
V31	V43+(V20-V43)*(12/23)

Grayscale voltage	Formula
V32	V43+(V20-V43)*(11/23)
V33	V43+(V20-V43)*(10/23)
V34	V43+(V20-V43)*(9/23)
V35	V43+(V20-V43)*(8/23)
V36	V43+(V20-V43)*(7/23)
V37	V43+(V20-V43)*(6/23)
V38	V43+(V20-V43)*(5/23)
V39	V43+(V20-V43)*(4/23)
V40	V43+(V20-V43)*(3/23)
V41	V43+(V20-V43)*(2/23)
V42	V43+(V20-V43)*(1/23)
V43	VINN4
V44	V55+(V43-V55)*(22/24)
V45	V55+(V43-V55)*(20/24)
V46	V55+(V43-V55)*(18/24)
V47	V55+(V43-V55)*(16/24)
V48	V55+(V43-V55)*(14/24)
V49	V55+(V43-V55)*(12/24)
V50	V55+(V43-V55)*(10/24)
V51	V55+(V43-V55)*(8/24)
V52	V55+(V43-V55)*(6/24)
V53	V55+(V43-V55)*(4/24)
V54	V55+(V43-V55)*(2/24)
V55	VINN5
V56	V62+(V55-V62)*(44/48)
V57	V62+(V55-V62)*(40/48)
V58	V62+(V55-V62)*(36/48)
V59	V62+(V55-V62)*(32/48)
V60	V62+(V55-V62)*(25/48)
V61	V62+(V55-V62)*(18/48)
V62	VINN6
V63	VINN7

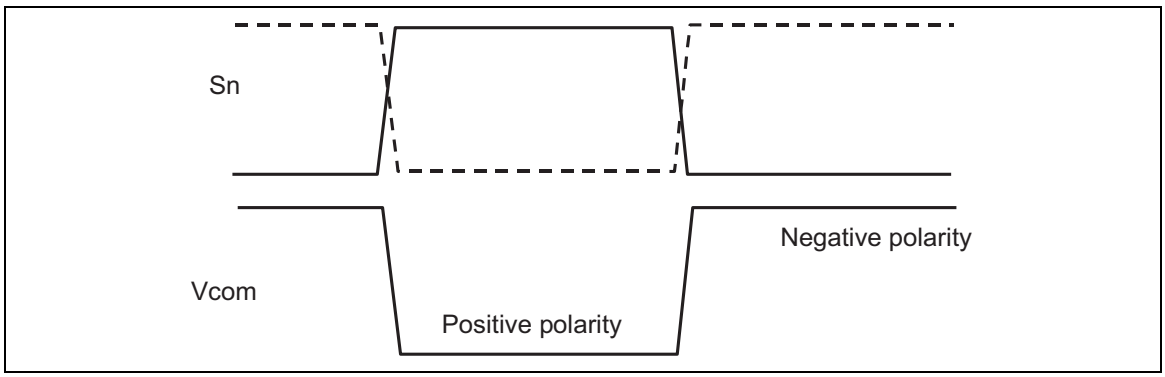
Note 1) Make sure DDVDH – V0 > 0.5V, DDVDH – V4 > 1.1V, V55-GND > 1.1V

Relationship between RAM data and output level (REV =0)

The relationship between the RAM data and the source output level is as follows.



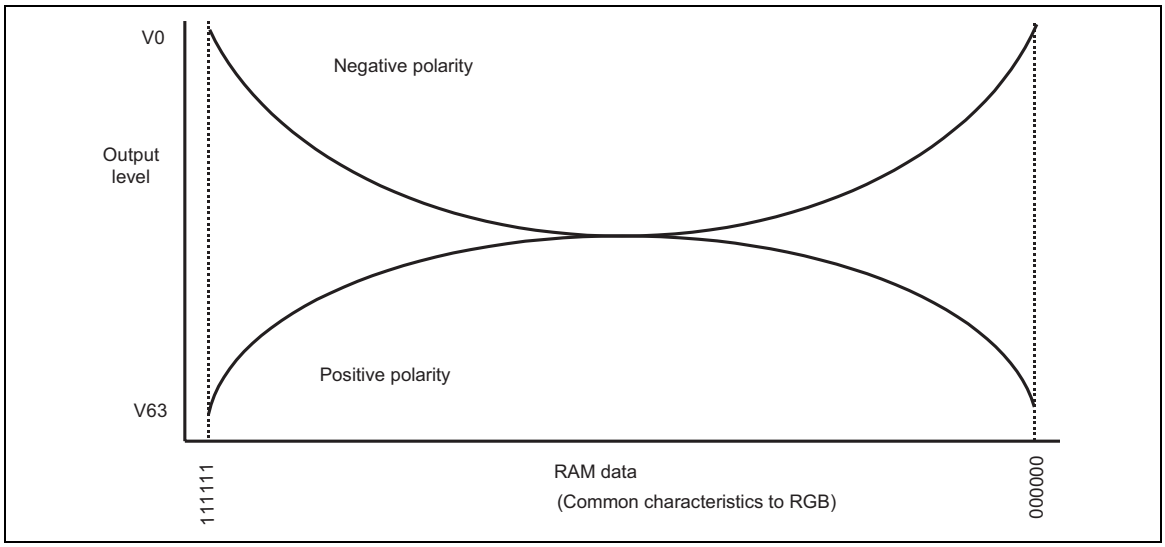
RAM data and the output voltage (REV = 0)



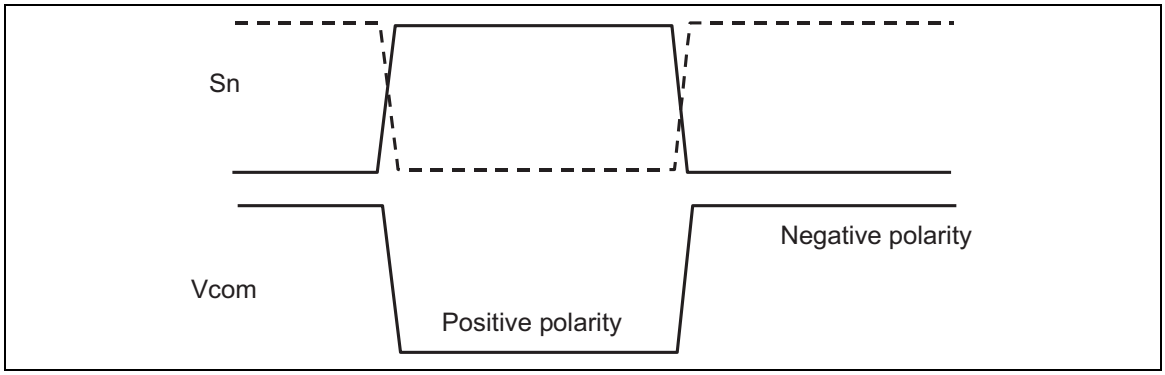
Source output and Vcom

Relationship between RAM data and output level (REV =1)

The relationship between the RAM data and the source output level is as follows.



RAM data and the output voltage (REV = 1)



Source output and Vcom

Low Power Consumption Display Mode

Setting COL[1:0] to 2'h1 halts 32 amplifiers among V0 ~ V63 grayscale amplifiers to display with low power consumption. In combination with the FRC mode setting, it is possible to realize display with low power consumption in abundant colors.

To make a setting for the low power consumption display, set in accordance to the following table according to the interface in use. The setting must be made in accordance to the setting sequence for low power consumption display mode.

Using this mode with short screen refreshing cycle may affect the quality of display. Consider the trade-off between the display quality and power-saving effects before use.

Table 71

Interface mode	FRCON	D16B	Available colors
18 bit, 16 bit x2, 9 bit x2, 8 bit x3, RGB18bit, 6 bit x3	0	*	262,144
	1	0	250,047
16bit x1, 8 bit x2, SPI	0	*	65,536
	1	1	64,512

Note 1) When the FRC mode is on, do not switch the interface mode settings (M, TRI, D16B registers)

Note 2) When the FRC mode is on, 18-bit format data and 16-bit format data are not displayed simultaneously.

Table 72

COL[1:0]	Amplifiers in operation	Available colors for display	
		FRCON = 0	FRCON = 1
2'h0	64	262,144 colors/65,536 colors	-
2'h1	32	32,768 colors	250,047 colors/64,512 colors
2'h2	2	8 colors	-
2'h3	Setting disabled	Setting disabled	Setting disabled

Note 1) When COL[1:0] =2'h1 and FRCON = 0, do not write data that correspond to the grayscale levels for which the amplifiers are halted.

Table 73 grayscale level amplifiers in operation

amplifier	COL[1:0]			GRAM data RGB	
	2'h0	2'h1	2'h2		
V0	*	*	*	6'h00	6'h3F
V1	*			6'h01	6'h3E
V2	*	*		6'h02	6'h3D
V3	*			6'h03	6'h3C
V4	*	*		6'h04	6'h3B
V5	*			6'h05	6'h3A
V6	*	*		6'h06	6'h39
V7	*			6'h07	6'h38
V8	*	*		6'h08	6'h37
V9	*			6'h09	6'h36
V10	*	*		6'h0A	6'h35
V11	*			6'h0B	6'h34
V12	*	*		6'h0C	6'h33
V13	*			6'h0D	6'h32
V14	*	*		6'h0E	6'h31
V15	*			6'h0F	6'h30
V16	*	*		6'h10	6'h2F
V17	*			6'h11	6'h2E
V18	*	*		6'h12	6'h2D
V19	*			6'h13	6'h2C
V20	*	*		6'h14	6'h2B
V21	*			6'h15	6'h2A
V22	*	*		6'h16	6'h29
V23	*			6'h17	6'h28
V24	*	*		6'h18	6'h27
V25	*			6'h19	6'h26
V26	*	*		6'h1A	6'h25
V27	*			6'h1B	6'h24
V28	*	*		6'h1C	6'h23
V29	*			6'h1D	6'h22
V30	*	*		6'h1E	6'h21
V31	*			6'h1F	6'h20

amplifier	COL[1:0]			GRAM data RGB	
	2'h0	2'h1	2'h2		
V32	*			6'h20	6'h1F
V33	*	*		6'h21	6'h1E
V34	*			6'h22	6'h1D
V35	*	*		6'h23	6'h1C
V36	*			6'h24	6'h1B
V37	*	*		6'h25	6'h1A
V38	*			6'h26	6'h19
V39	*	*		6'h27	6'h18
V40	*			6'h28	6'h17
V41	*	*		6'h29	6'h16
V42	*			6'h2A	6'h15
V43	*	*		6'h2B	6'h14
V44	*			6'h2C	6'h13
V45	*	*		6'h2D	6'h12
V46	*			6'h2E	6'h11
V47	*	*		6'h2F	6'h10
V48	*			6'h30	6'h0F
V49	*	*		6'h31	6'h0E
V50	*			6'h32	6'h0D
V51	*	*		6'h33	6'h0C
V52	*			6'h34	6'h0B
V53	*	*		6'h35	6'h0A
V54	*			6'h36	6'h09
V55	*	*		6'h37	6'h08
V56	*			6'h38	6'h07
V57	*	*		6'h39	6'h06
V58	*			6'h3A	6'h05
V59	*	*		6'h3B	6'h04
V60	*			6'h3C	6'h03
V61	*	*		6'h3D	6'h02
V62	*			6'h3E	6'h01
V63	*	*	*	6'h3F	6'h00

*: amplifier in operation

The following table shows the relationship between GRAM data and liquid crystal grayscale level.

Table 74 GRAM data and LCD grayscale level (REV = 0) in FRC mode

GRAM data RGB	Selected grayscale level	
	positive	negative
6'h00	V0	V63
6'h01	(V0+V2)/2	(V61+V63)/2
6'h02	V2	V61
6'h03	(V2+V4)/2	(V59+V61)/2
6'h04	V4	V59
6'h05	(V4+V6)/2	(V57+V59)/2
6'h06	V6	V57
6'h07	(V6+V8)/2	(V55+V57)/2
6'h08	V8	V55
6'h09	(V8+V10)/2	(V53+V55)/2
6'h0A	V10	V53
6'h0B	(V10+V12)/2	(V51+V53)/2
6'h0C	V12	V51
6'h0D	(V12+V14)/2	(V49+V51)/2
6'h0E	V14	V49
6'h0F	(V14+V16)/2	(V47+V49)/2
6'h10	V16	V47
6'h11	(V16+V18)/2	(V45+V47)/2
6'h12	V18	V45
6'h13	(V18+V20)/2	(V43+V45)/2
6'h14	V20	V43
6'h15	(V20+V22)/2	(V41+V43)/2
6'h16	V22	V41
6'h17	(V22+V24)/2	(V39+V41)/2
6'h18	V24	V39
6'h19	(V24+V26)/2	(V37+V39)/2
6'h1A	V26	V37
6'h1B	(V26+V28)/2	(V35+V37)/2
6'h1C	V28	V35
6'h1D	(V28+V30)/2	(V33+V35)/2
6'h1E	V30	V33
6'h1F	(V30+V33)/2	(V30+V33)/2

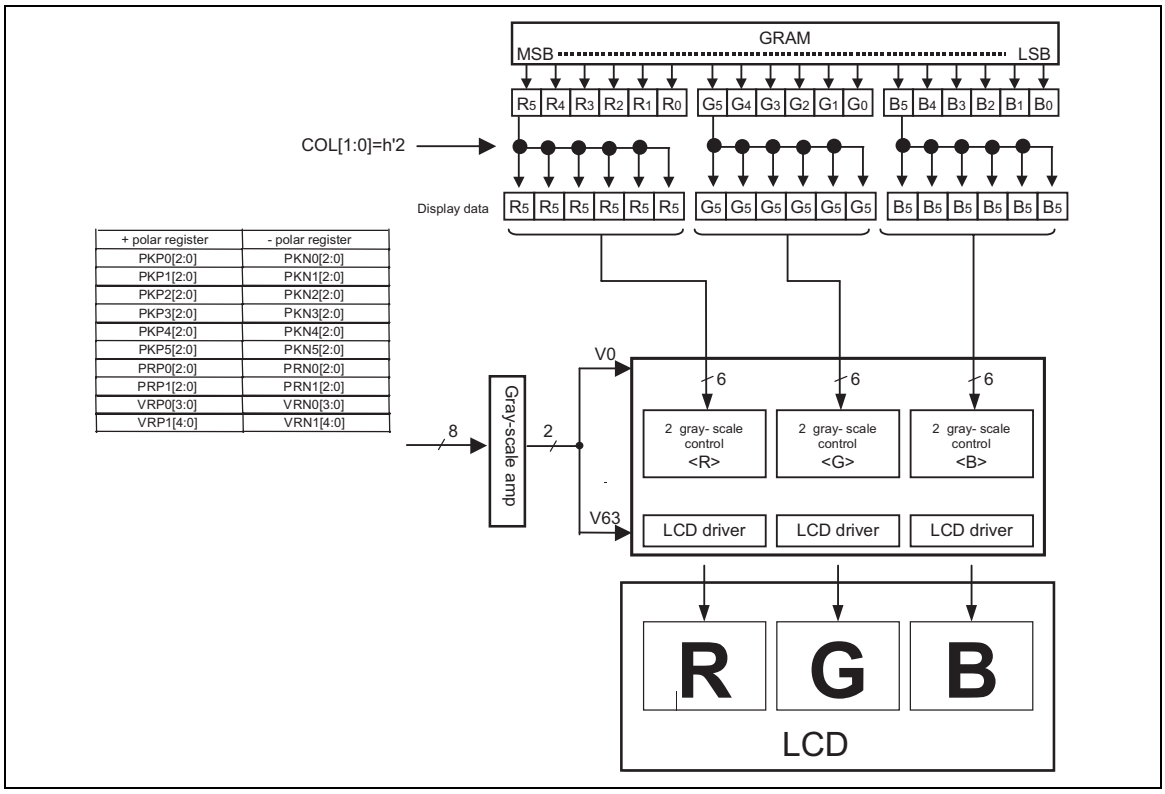
GRAM data RGB	Selected grayscale level	
	positive	negative
6'h20	(V30+V33)/2	(V30+V33)/2
6'h21	V33	V30
6'h22	(V33+V35)/2	(V28+V30)/2
6'h23	V35	V28
6'h24	(V35+V37)/2	(V26+V28)/2
6'h25	V37	V26
6'h26	(V37+V39)/2	(V24+V26)/2
6'h27	V39	V24
6'h28	(V39+V41)/2	(V22+V24)/2
6'h29	V41	V22
6'h2A	(V41+V43)/2	(V20+V22)/2
6'h2B	V43	V20
6'h2C	(V43+V45)/2	(V18+V20)/2
6'h2D	V45	V18
6'h2E	(V45+V47)/2	(V16+V18)/2
6'h2F	V47	V16
6'h30	(V47+V49)/2	(V14+V16)/2
6'h31	V49	V14
6'h32	(V49+V51)/2	(V12+V14)/2
6'h33	V51	V12
6'h34	(V51+V53)/2	(V10+V12)/2
6'h35	V53	V10
6'h36	(V53+V55)/2	(V8+V10)/2
6'h37	V55	V8
6'h38	(V55+V57)/2	(V6+V8)/2
6'h39	V57	V6
6'h3A	(V57+V59)/2	(V4+V6)/2
6'h3B	V59	V4
6'h3C	(V59+V61)/2	(V2+V4)/2
6'h3D	V61	V2
6'h3E	(V61+V63)/2	(V0+V2)/2
6'h3F	V63	V0

Note 1) This table shows effective grayscale levels by FRC grayscale.

8-color Display Mode

The HD66781 incorporates an 8-color display mode. The available grayscale levels are V0 and V63, and the voltages for the other levels (V1-V62) are halted to reduce power consumption.

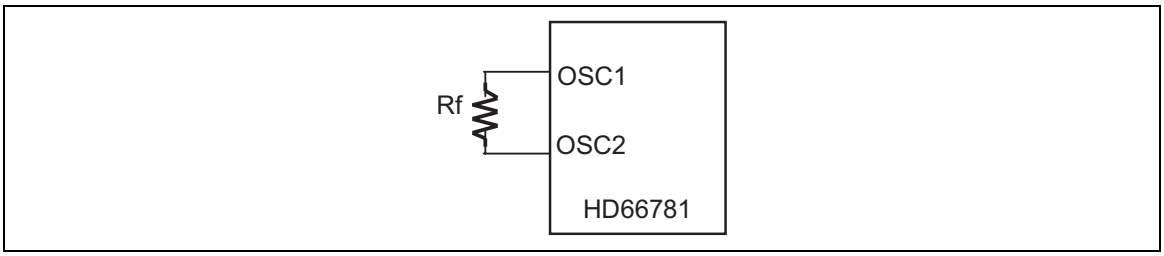
The γ-fine-adjustment registers, PKP0-PKP5 and PKN0-PKN5 are not available in the 8-color display mode. Since the power supplies for the levels V1-V62 are halted in the 8-color mode, data are converted to automatically select V0/V63 levels: the MSB of each R, G, B, pixel of GRAM data is allocated to the lower 5 bits of R, G, B of display data. The HD 66781 enables to switch between 8-color and normal display modes without rewriting GRAM data only with the COL setting.



+ polar register	- polar register
PKP0[2:0]	PKN0[2:0]
PKP1[2:0]	PKN1[2:0]
PKP2[2:0]	PKN2[2:0]
PKP3[2:0]	PKN3[2:0]
PKP4[2:0]	PKN4[2:0]
PKP5[2:0]	PKN5[2:0]
PRP0[2:0]	PRN0[2:0]
PRP1[2:0]	PRN1[2:0]
VRP0[3:0]	VRN0[3:0]
VRP1[4:0]	VRN1[4:0]

Oscillation Circuit

The HD66781 generates oscillation by an internal R-C oscillator with an external oscillation resistor placed between the OSC1 and OSC2 pins. The oscillation frequency varies depending on the value of external resistor, the distance of wiring, and the operational power supply voltage. For example, the oscillation frequency becomes low when increasing the value of Rf resistor, or lowering the power supply voltage. See the "Notes to Electric Characteristics" section for the relationship between the Rf resistor value and the oscillation frequency.



External Resistor Oscillation Mode

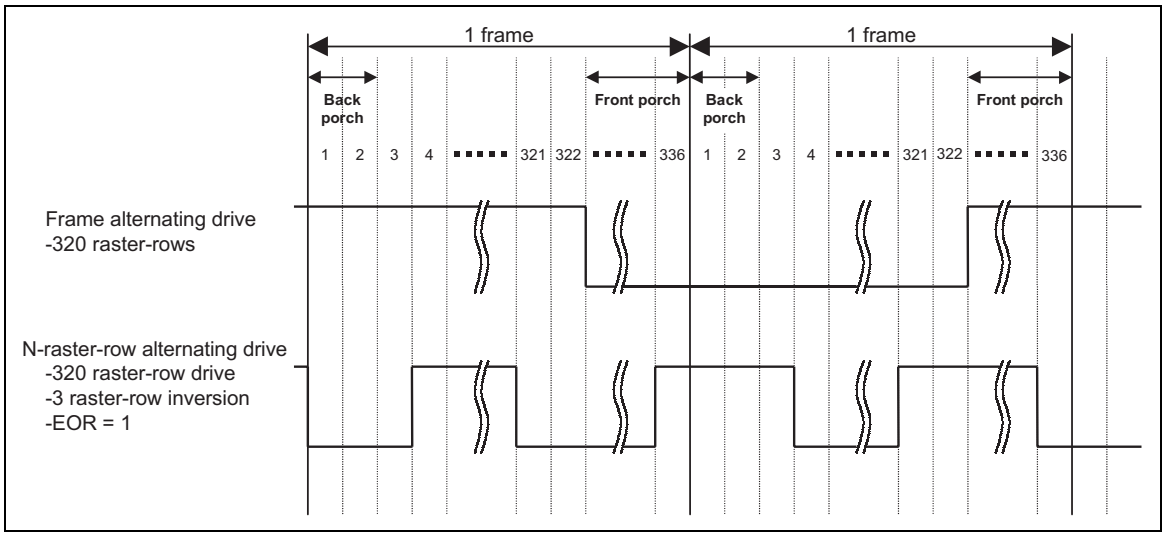
Note 1) Place the Rf resistor as close to the OSC1, OSC2 pins as possible.

Note 2) Make sure not to arrange other wiring close to or beneath OSC1-OSC2 wiring to avoid effects from coupling

n-raster-row Inversion alternating Drive

The HD66781, in addition to LCD inversion alternating drive by frame, supports n-raster-row inversion alternating drive where alternation occurs by n raster-rows, where n takes a number from 1 to 64. The n-raster-row inversion alternating drive enables to overcome the problems related to display quality.

In determining n (the value set by the NW bit +1), the number of raster-rows by which alternation occurs, check the display quality on the actual liquid crystal panel. Setting a small number of raster-rows will raise the alternating frequency of the liquid crystal and increase the charge/discharge current on the liquid crystal cells.



n-raster-row alternating drive

Note 1) Make sure to set EOR = 1 to avoid direct bias on liquid crystal during n-raster-row alternating drive.

Interlaced Drive

The HD66781 supports interlaced drive, which divides one frame into n fields and then drives to prevent flickers.

To determine the number of fields (n: value set by the FLD bits), check the display quality on the actual liquid crystal panel. The following table shows the gate selection for each number of fields, 1 to 3. The figure illustrates the output waveforms of the 3-field interlaced drive.

Table 75

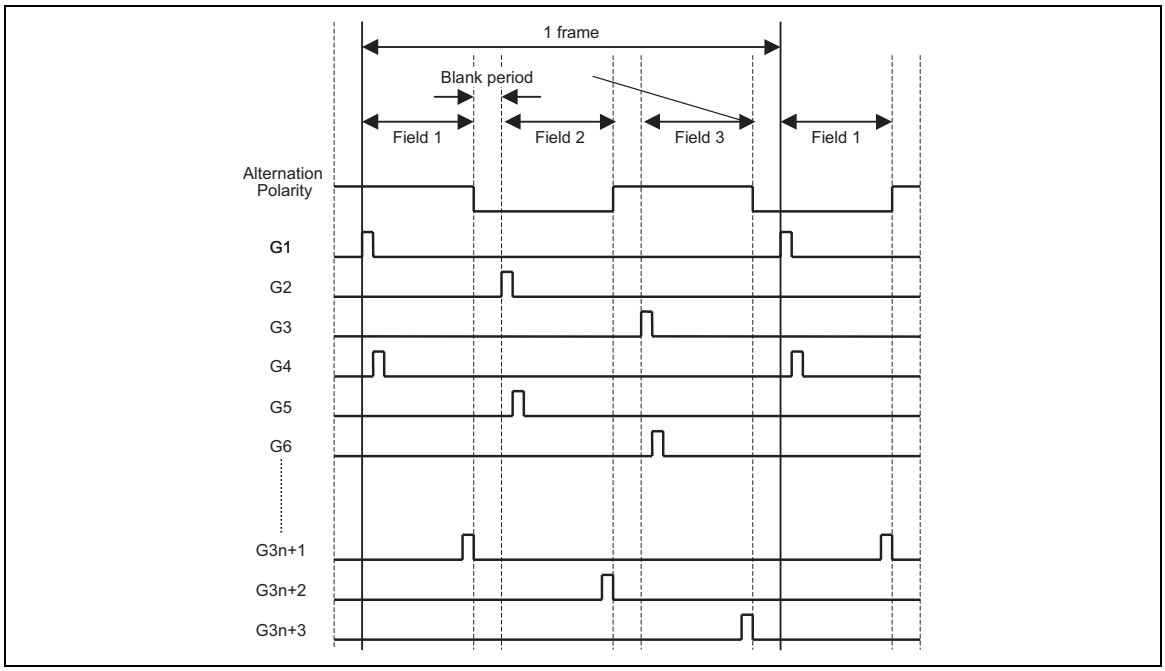
GA=0, SM=0, GS0=0, GS1=0				
FLD1-0	**2'h1**		**2'h3**	
Field / Gate	**-**	**1**	**2**	**3**
G1	O	O		
G2	O		O	
G3	O			O
G4	O	O		
G5	O		O	
G6	O			O
G7	O	O		
G8	O		O	
G9	O			O
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
G317	O		O	
G318	O			O
G319	O	O		
G320	O		O	

GA=1, SM=0, GS0=0, GS1=1				
FLD1-0	**2'h1**		**2'h3**	
Field / Gate	**-**	**1**	**2**	**3**
G328	O	O		
G327	O		O	
G326	O			O
G325	O	O		
G324	O		O	
G323	O			O
G322	O	O		
G321	O		O	
G320	O			O
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
G12	O		O	
G11	O			O
G10	O	O		
G9	O		O	

Note 1) Interlaced drive is not available in RGB interface mode.

Note 2) Middle porch must be set to BP = 3 (3 lines) for interlaced drive.

Note 3) OSD (α blending), scrolling, and resizing functions are not available with interlaced drive.

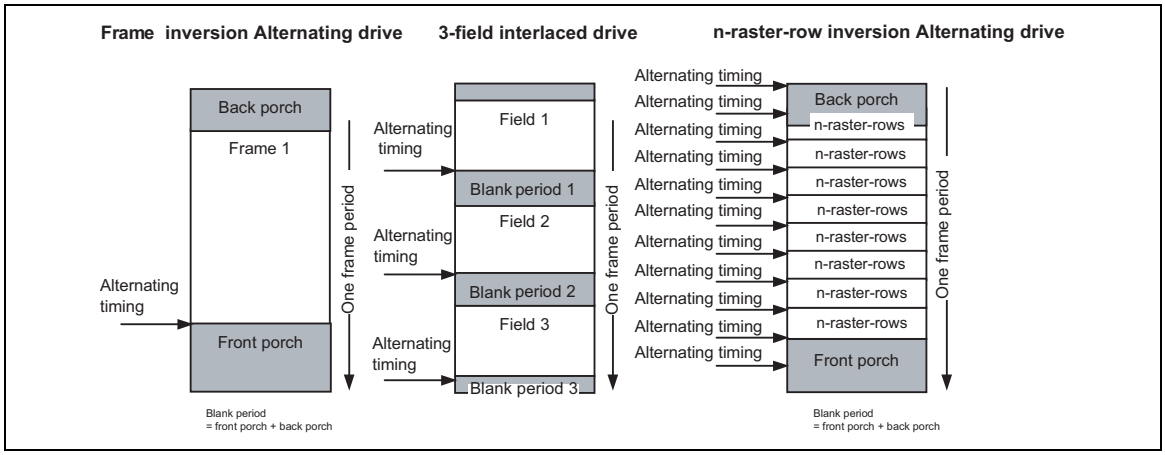


3-field interlaced drive: gate output timing

Alternating Timing

The following figure illustrates the alternating timing of each alternating drive formula. In case of frame inversion alternating drive, alternation occurs at the completion of one frame, followed by a blank that lasts for 16H periods. In case of interlaced drive, alternation occurs at the completion of one field, followed by a blank. The total period of the blanks in one frame adds up to 16H period. In case of n-raster-row, a blank lasting 16H period is inserted after all screens are drawn.

During interlaced drive, make the numbers of back, front porches more than the numbers of fields.



Alternating timing

Frame-Frequency Adjustment Function

The HD66781 incorporates frame frequency adjustment function. The frame frequency during the liquid crystal drive is adjusted by the instruction setting (DIVI, RTNI) while keeping the oscillation frequency fixed.

By setting the oscillation frequency high in advance, it becomes possible to switch the frame frequency in accordance to the kind of displayed picture (i.e. moving/still picture). When displaying a still picture, set the frame frequency low to save power consumption, while setting the frame frequency high when displaying a moving picture which requires high-speed screen switching.

Relationship between Liquid Crystal Drive Duty and Frame Frequency

The relationship between the liquid crystal drive duty and the frame frequency is calculated by the following formula. The frame frequency is adjusted by the instruction setting with the 1-H period adjustment bit (RTNI bit) and the operation clock division bit (DIVI bit).

(Formula for the frame frequency)

$$\text{Frame frequency} = \frac{\text{fosc}}{\text{Clock cycles per raster-row} \times \text{division ratio} \times (\text{Line+BP+ FP})} \quad [\text{Hz}]$$

fosc	: R-C oscillation frequency
Clock cycles per raster-row	: RTNI bits
Division ratio	: DIVI bit
Line	: number of drive raster-rows (NL)
Front Porch	: FP bits
Back Porch	: BP bits

Calculation Example The maximum frame frequency = 60 Hz

Number of drive raster-row	: 320
1-H period	: 16 clock cycles (RTNI[4:0] = 2'h10)
Operation clock division ratio	: 1 division

$$\text{fosc} = 60\ \text{Hz} \times 16\ \text{clocks} \times 1\ \text{division} \times (320+2+14)\ \text{lines} = 323\ (\text{kHz})$$

In this case, the R-C oscillation frequency becomes 323 kHz. Adjust the value of external resistor for R-C oscillator to set the frequency 323kHz.

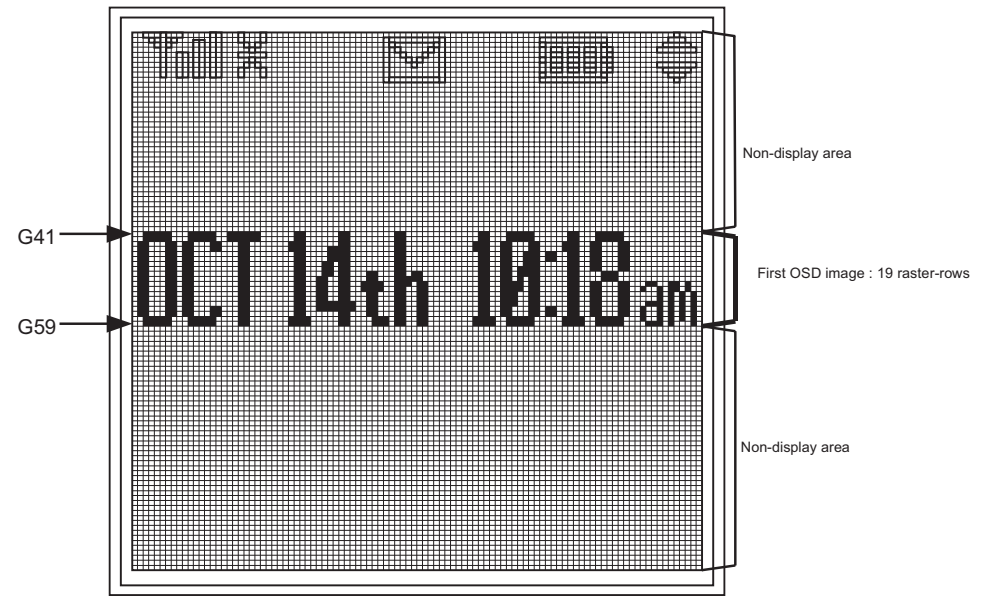
Partial Display Function

The HD66781 enables arbitrary settings for on-display picture RAM area and the display position on the screen with the use of OSD. When the display of base image is turned off (BASEE=0), OSD is displayed 100%.

By making settings for OSD RAM area (OSA, OEA) and OSD position (ODP), the HD66781 allows displaying an arbitrary set of data. Other than OSD area becomes no-display area to reduce power consumption.

The partial display area using OSD can be made up to 3 areas.

In combination with 8-color mode and off-scan settings (PTS, PTG, ISC), more power-saving display will be obtained. Make an appropriate setting taking power-saving effect and display quality into consideration.



Number of driving raster-row	: NL0 =6'h07 (64 raster-rows)
Base picture display ENABLE	: BASEE = 0
First OSD picture display RAM area	: (OSA0, OEA0) = (8'h000, 8'h013)
First OSD picture display position	: ODP0=8'h028
First OSD picture display ENABLE	: OSDE=1

Partial Display

Note 1) See the "RAM Address and Display Position on the Panel" for more details on the relationship between the display area and the setting of RAM area.

Power-saving drive settings

The HD66781 incorporates various settings for lower power consumption display. The low power consumption and the quality of display are in trade-off, and the power-saving effect may vary depending on the characteristics of a panel. Make an appropriate setting among the settings listed below taking the trade-off into consideration.

1. 8-color display mode (COL)

When this mode is selected (COL [1:0] = 2'h2), voltage generation for grayscale levels other than V0 and V63 levels is halted. In this mode, only 8 colors are available for display for saving power.

2. Low power consumption display mode (COL, FRC)

Setting COL[1:0] to 2'h1 halts 32 amplifiers among V0 ~ V63 grayscale amplifiers to display with low power consumption. In combination with the FRC mode setting, it is possible to realize display with low power consumption in abundant colors.

In this mode, 250,047 colors are available with 18-bit, 16-bit x2, 9-bit x2, 8-bit x3 (RGB 6 bits each) interfaces and 64,512 colors are available with 16-bit x1, 8-bit x2 interfaces and SPI (R, B: 5 bits, G: 6 bits). Using this mode with short screen refreshing cycle may affect the quality of display. Consider the trade-off between the display quality and power-saving effects before use. See the "Low power consumption display mode" (p.169) for details.

3. Partial display (OSD)

The partial display is made with OSD and base image display off setting (BASEE = 0). Display operation is limited to the partial display area to save power. Power saving effects will increase as the number of partial display lines decreases. Also, see "Partial Display Function"(p.139) for details.

4. Non-lit drive setting

The non-lit drive setting is available for partial display and allows specifying the kind of source outputs in the non-lit drive area with PTS bits. Also, in the non-lit drive area, grayscale generation amplifier is halted and step-up clock cycle is slowed down to half.

PTG bits can specify the scan mode of gate bus lines in the non-lit drive area. In the interval gate scan mode, gate bus lines are scanned by the frame cycle specified by ISC bits to hold power consumption required for scanning gate bus lines to minimum. The longer scan cycle may affect the quality of display. Make an appropriate setting by taking trade-off between power-saving effects and display quality.

Table 76 Source outputs in non-display area

PTS[2:0]	Source output in non-display area		Non-display area	Non-display area
	Positive polarity	Negative polarity	Grayscale amp operation	Step-up clock frequency
3'h0	V63	V0	V0 to V63	DC0,DC1Setting
3'h1	Setting disabled	Setting disabled	-	-
3'h2	GND	GND	V0 to V63	DC0,DC1Setting
3'h3	Hi-Z	Hi-Z	V0 to V63	DC0,DC1Setting
3'h4	V63	V0	V0,V63	DC0,DC1Setting x1/2
3'h5	Setting disabled	Setting disabled	-	-
3'h6	GND	GND	V0,V63	DC0,DC1Setting x1/2
3'h7	Hi-Z	Hi-Z	V0,V63	DC0,DC1Setting x1/2

Note 1) Gate outputs in non-lit drive area can be controlled by off-scan mode (with PTG bits).

Note 2) The operation halt of grayscale amplifier and the slowdown of step-up clock frequency are valid only to the non-display area.

Note 3) When DC[4:3]=2'h3, the frequency of step-up clocks in the non-display area are not slowed down half even if PTS[2:0] is set to 4, 6 or 7.

Table 77 Gate outputs in non-display area

PTG[1:0]	DISPTMG output	Gate output in non-display area	Source output in non-display area
2'h0	Normal drive	Normal scan	PTS setting
2'h1	GND	DISPTMG (Fixed)	PTS setting
2'h2	Internal drive	Interval scan	PTS setting
2'h3	Setting disabled	-	-

Note 1) When the interval scan is executed, make setting for the frame alternating drive.

Table 78 Interval gate scan frequency

ISC[3:0]	Scan frequency	When (fFLM) = 60Hz
4'h0	Setting disabled	–
4'h1	3 frames	50ms
4'h2	5 frames	84ms
4'h3	7 frames	117ms
4'h4	9 frames	150ms
4'h5	11 frames	184ms
4'h6	13 frames	217ms
4'h7	15 frames	251ms
4'h8	17 frames	284ms
4'h9	19 frames	317ms
4'hA	21 frames	351ms
4'hB	23 frames	384ms
4'hC	25 frames	418ms
4'hD	27 frames	451ms
4'hE	29 frames	484ms
4'hF	31 frames	518ms

5. Frame frequency setting

Frame frequency adjusting functions (with DIVI, RTNI bits) allows changing liquid crystal alternating frequency through instructions. Frame frequency can be reduced to achieve low power consumption while display method with low power consumption such as partial display mode is employed. See "Frame Frequency Adjustment Function"(p.178) section for details.

Generally, the lower frame frequency and the quality of display are in trade-off. The power-saving effects and the quality of display also vary depending on the characteristics of a panel. Check the quality of display on the panel before use.

6. Liquid crystal alternating drive

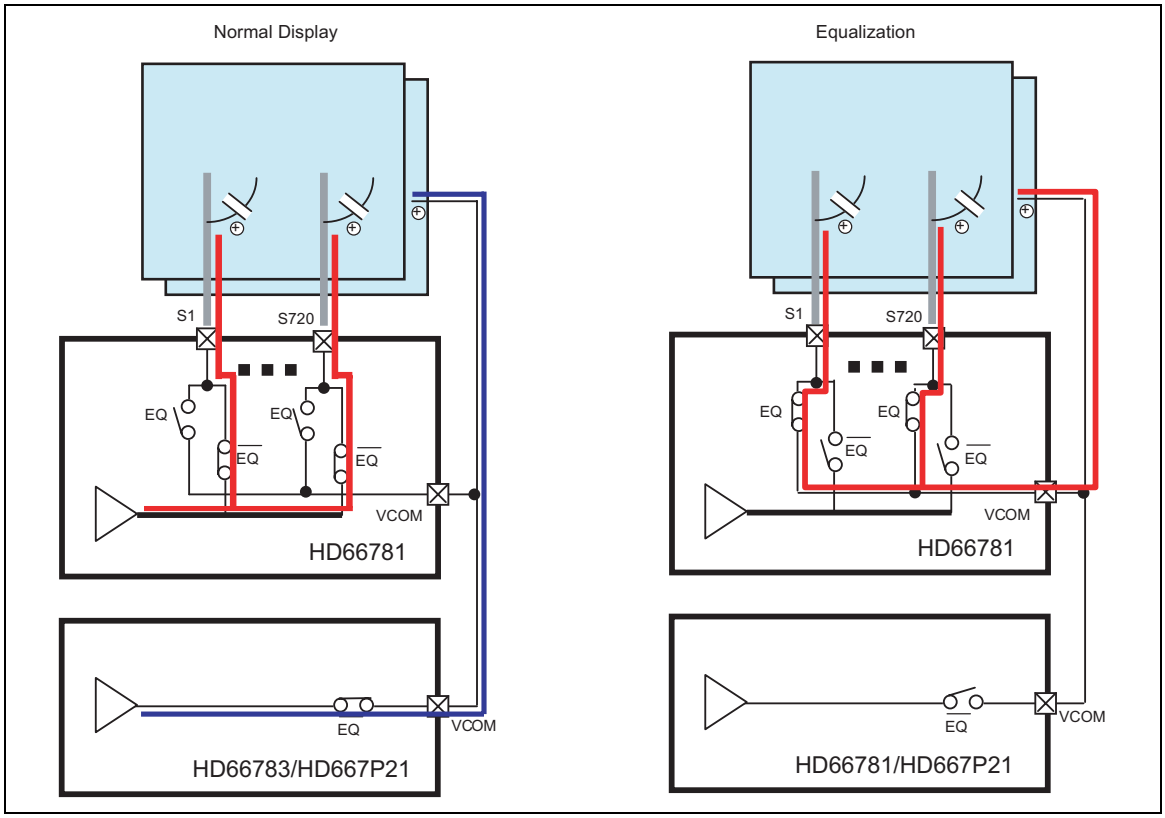
The HD66781 allows selecting among frame alternating drive, 3-field interlace drive, and line inversion alternating drive through instructions (B/C, EOR, NW, and FLD). Select an appropriate alternating drive method for the kind of display. See the "Alternating Timing"(p.177) section for details.

Generally, the lower frame frequency and the quality of display are in trade-off. The power-saving effects and the quality of display also vary depending on the characteristics of a panel. Check the quality of display on the panel before use.

Equalization function

The HD66781 incorporates source-Vcom equalization function, which short-circuits source outputs S1-S720 and Vcom at alternating points to equalize the electric potential of source capacities and Vcom capacities during “High” period of EQ signal.

By driving source and Vcom from the equalized electric potential, the electric charges accumulated in the source and Vcom capacities are reallocated, and power consumption is reduced.



Note 1) Equalization function is only available when Vcom Low level ≥ 0V
Note 2) Power-saving effects depend on display data.

Specifications of external element of HD66781

The specifications of external element connected to power supply circuit of HD66781 are as follows.

Table 79 Capacitor

Capacitor capacitance	Recommended capacitor voltage	Connection pin
1μF Characteristics B	3V	VDD

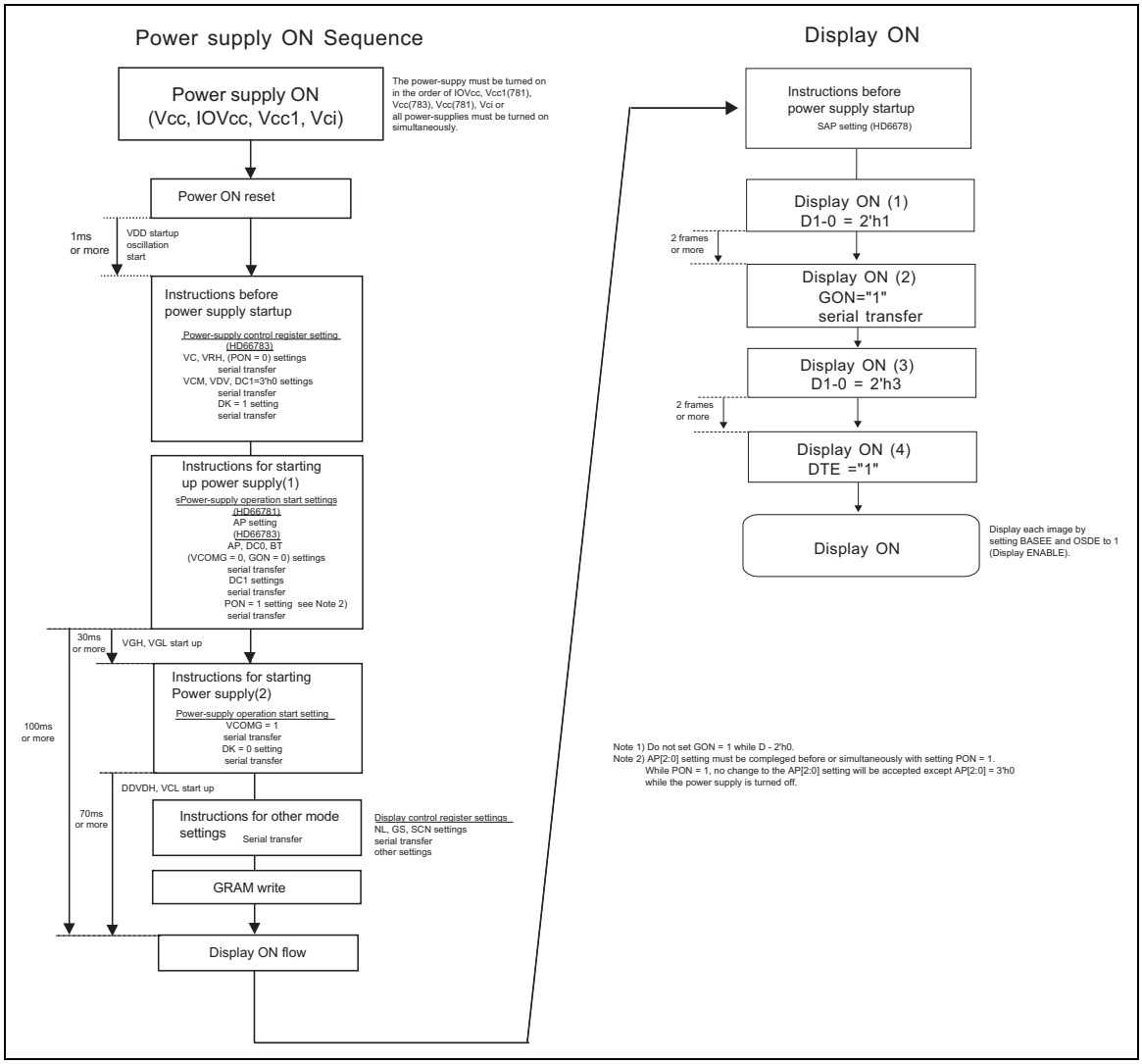
Instruction Setting

The following flowcharts show the sequences with respect to power on/off of the combined use of HD66781 and HD66783 or HD667P21, display on/off, standby set/release, and sleep set/release. Whenever turning on or off the power supply and so on, it must be done in accordance to the following procedures.

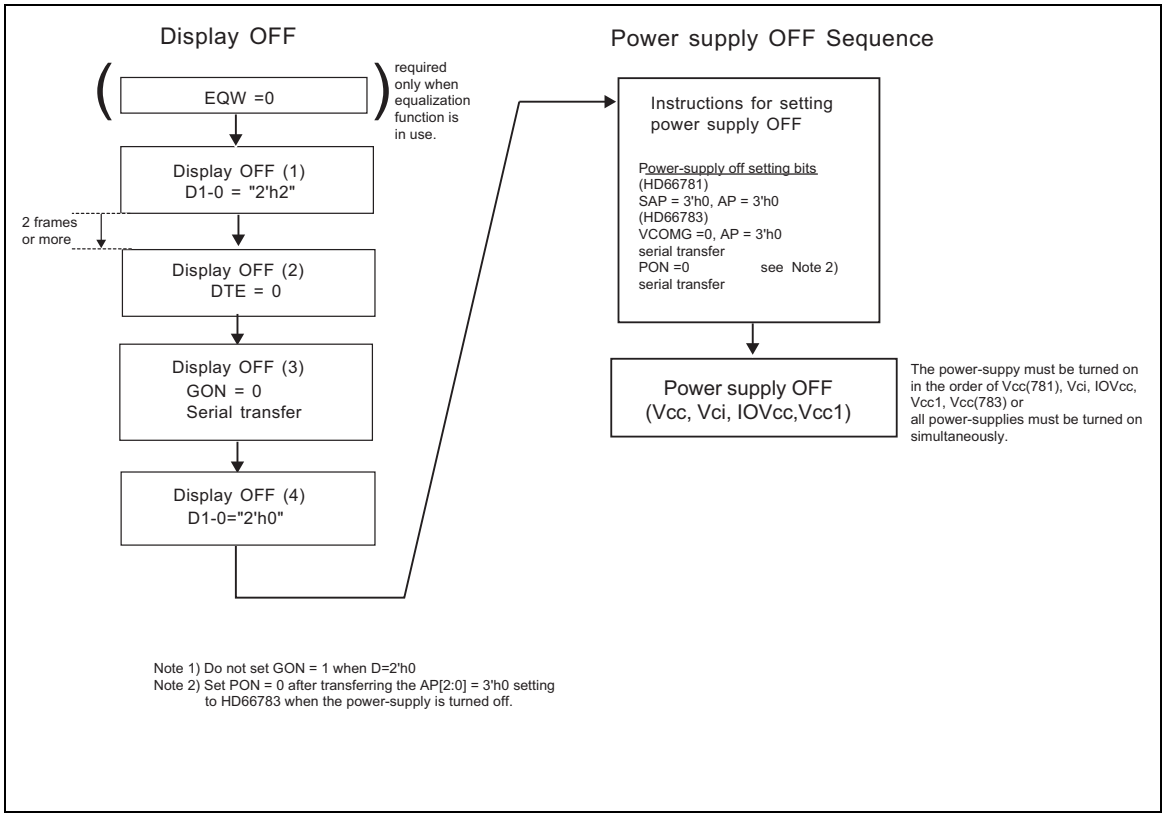
A serial interface is used to make instruction settings to the HD66783 and HD667P21, where a serial transfer is always required. The serial transfer must be made in accordance to the serial transfer sequence and right after the instructions are set.

Timing of the instruction setting is necessary to take into consideration the delay of 16-cycle internal clocks (OSC) from the start of serial transfer from the HD66781 through TE and IDX2-0 before each of the following mode settings becomes effective on the HD66783 and HD667P21.

Power-supply/display ON (LPTS = 0: a-Si TFT panel, with HD66783)

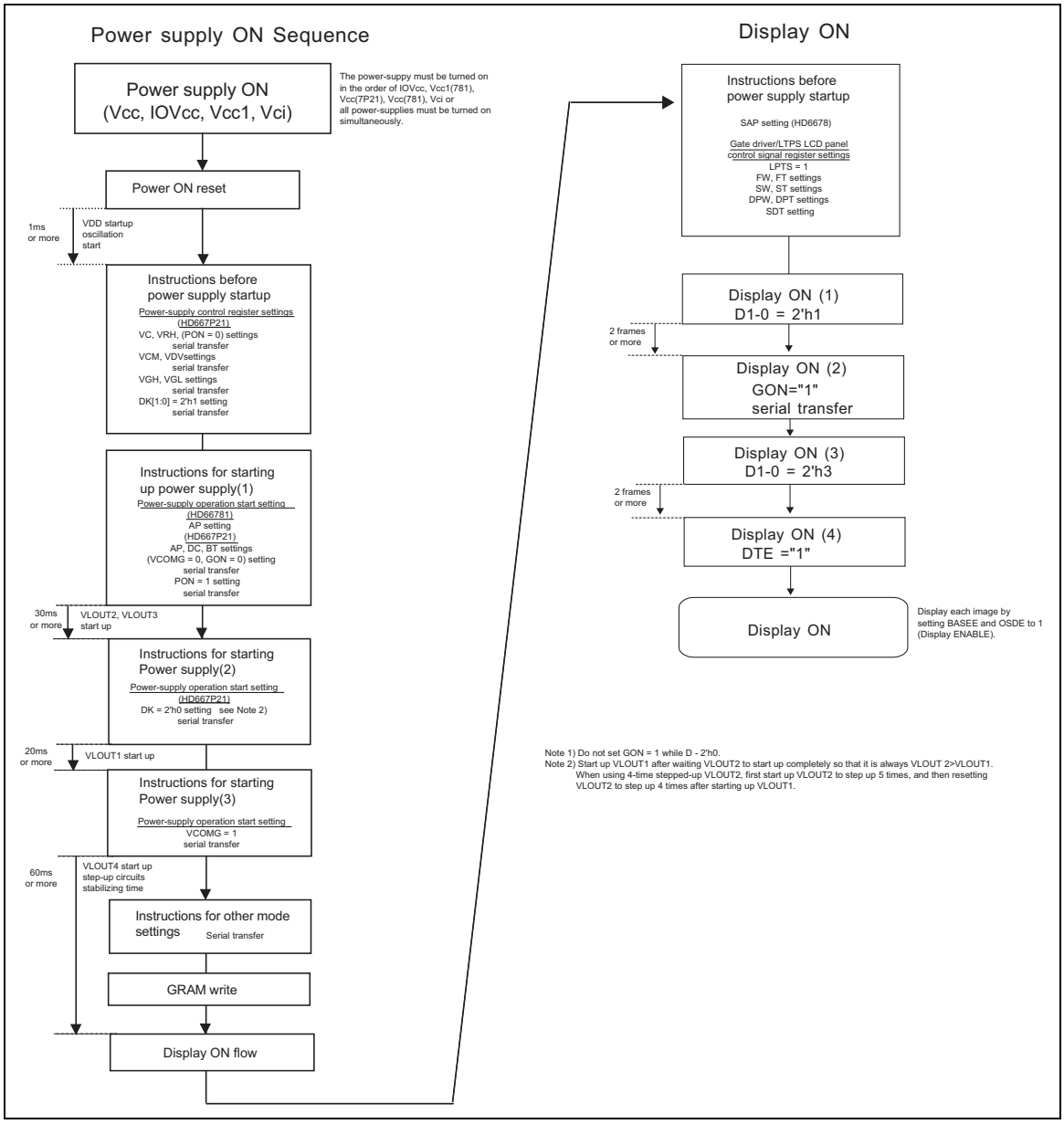


Power-supply/display OFF (LPTS = 0: a-Si TFT panel, with HD66783)

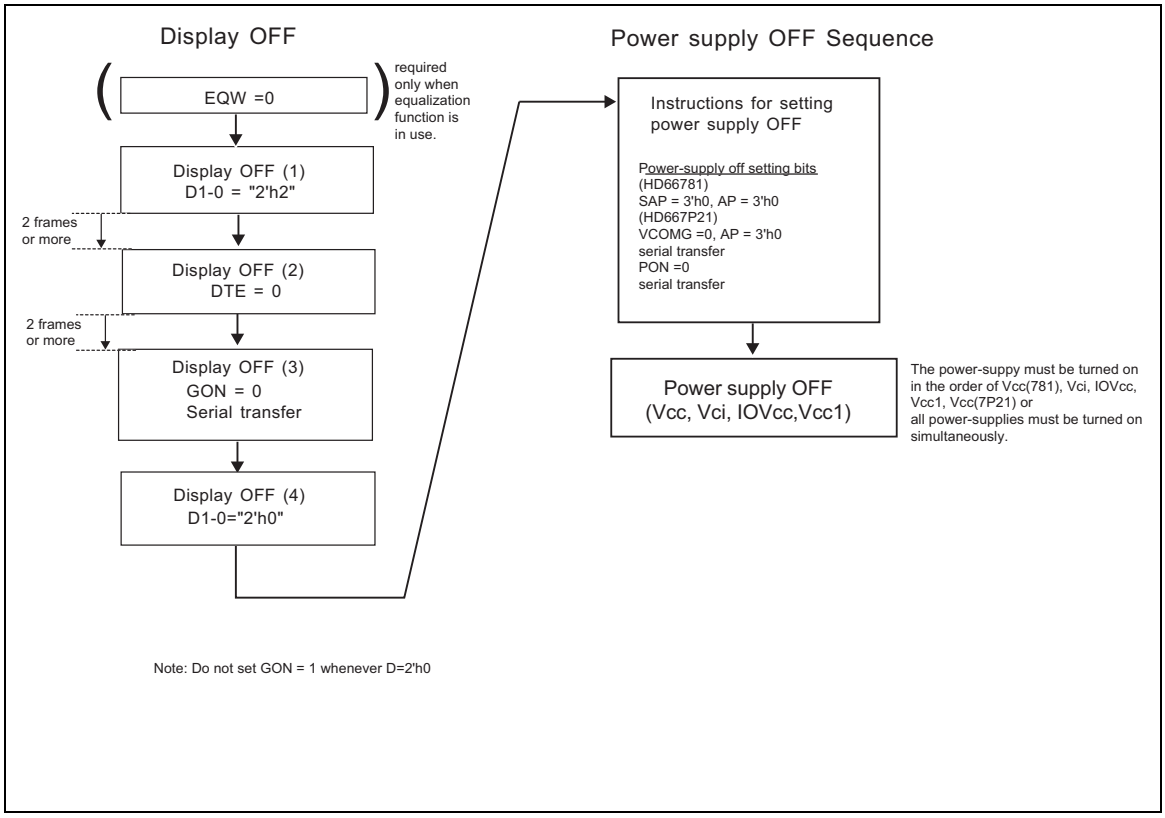


Note 1) Do not set GON = 1 when D=2'h0
Note 2) Set PON = 0 after transferring the AP[2:0] = 3'h0 setting to HD66783 when the power-supply is turned off.

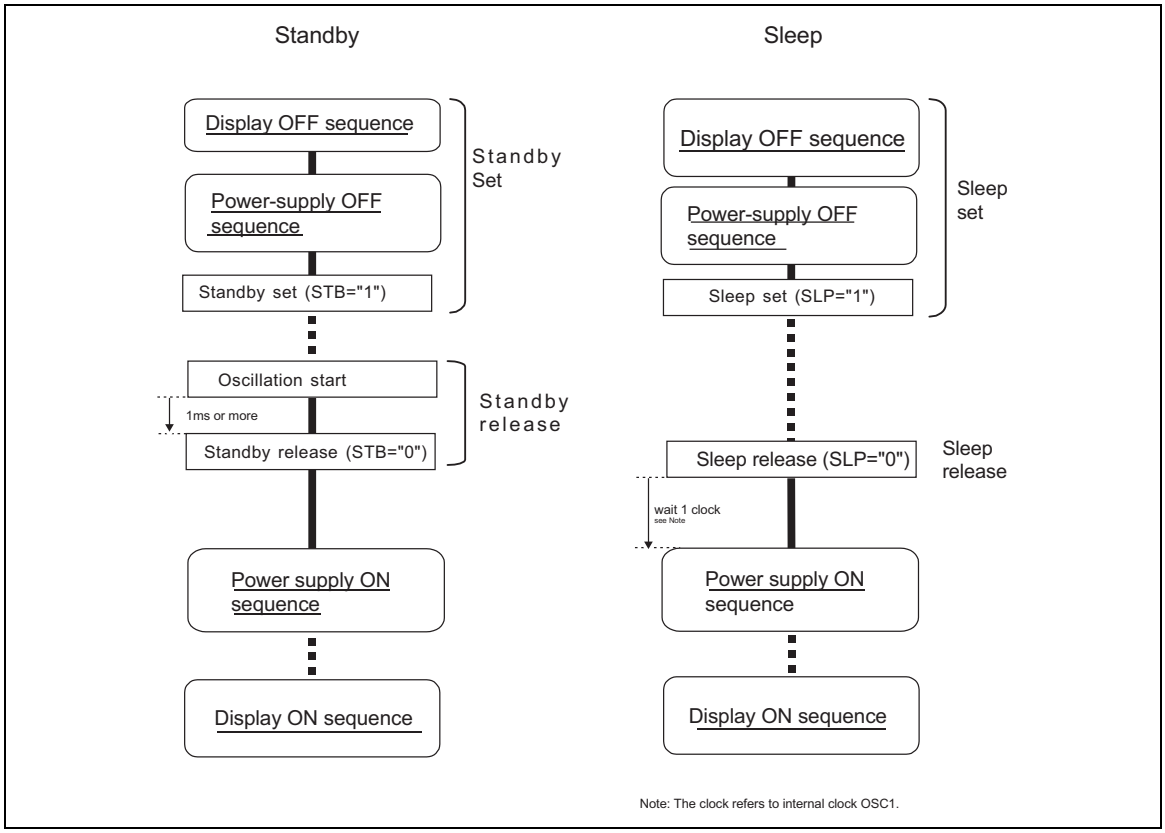
Power-supply/display ON (LPTS = 1: LTPS TFT panel, with HD667P21)



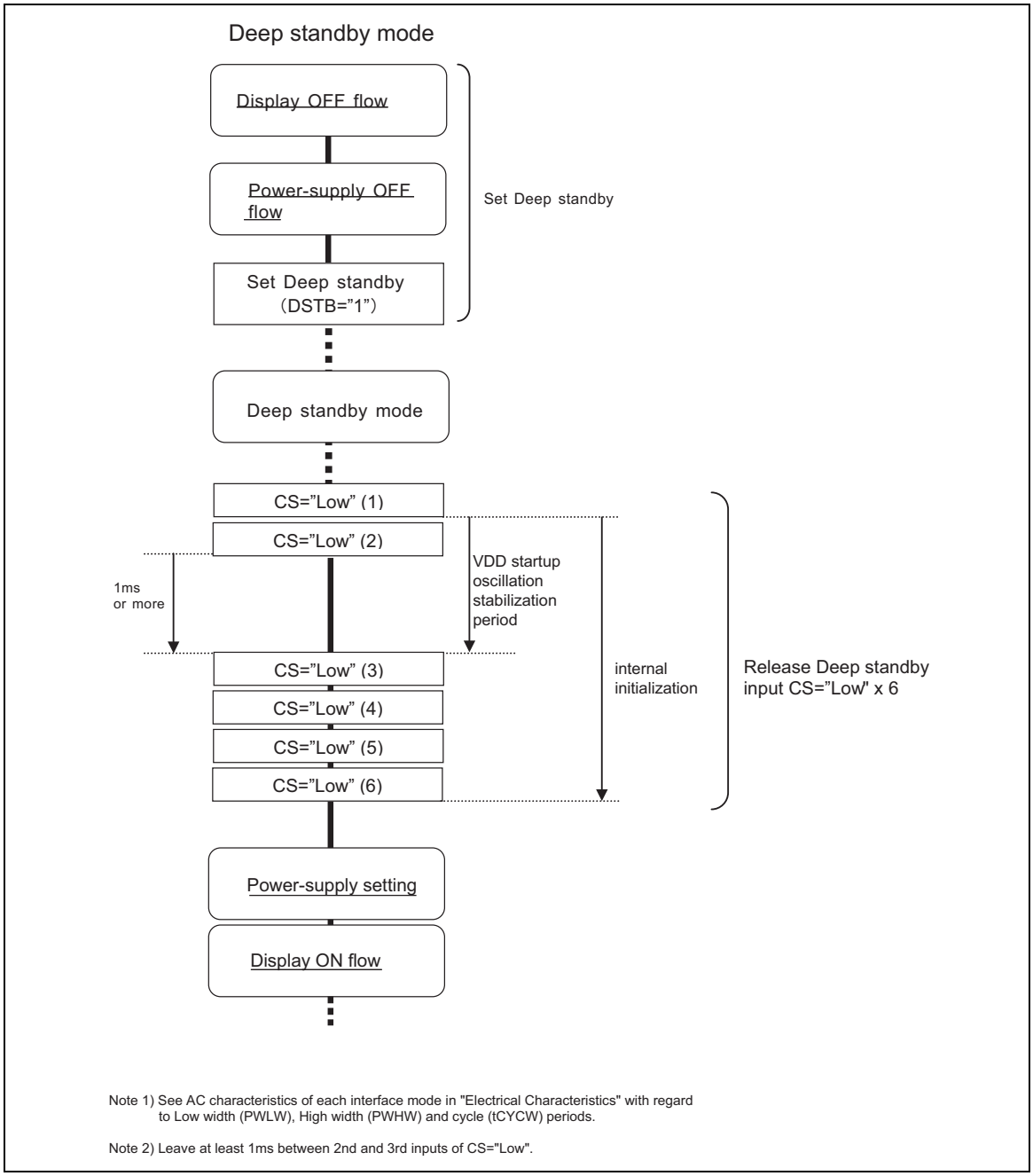
Power-supply/display OFF (LPTS = 1: LPTS TFT panel, with HD667P21)



Standby/Sleep mode



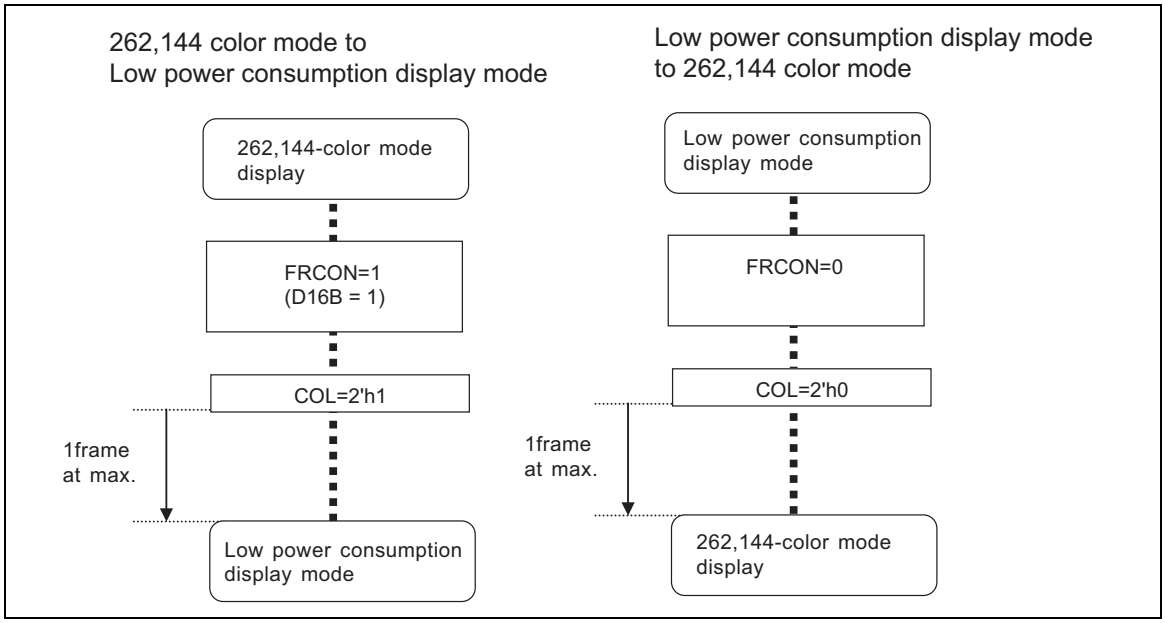
Deep standby mode



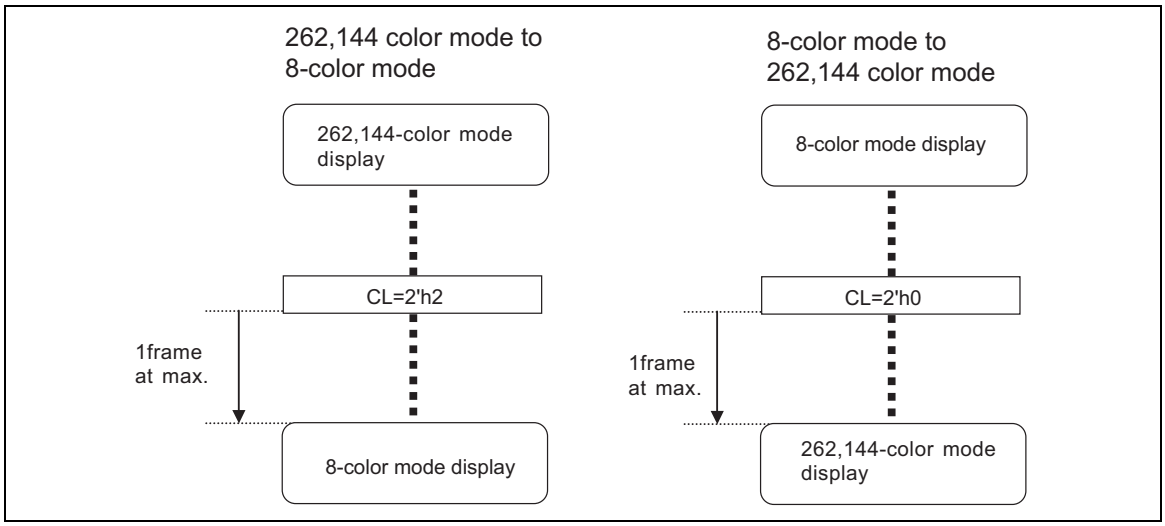
Note 1) See AC characteristics of each interface mode in "Electrical Characteristics" with regard to Low width (PWLW), High width (PWHW) and cycle (tCYCW) periods.

Note 2) Leave at least 1ms between 2nd and 3rd inputs of CS="Low".

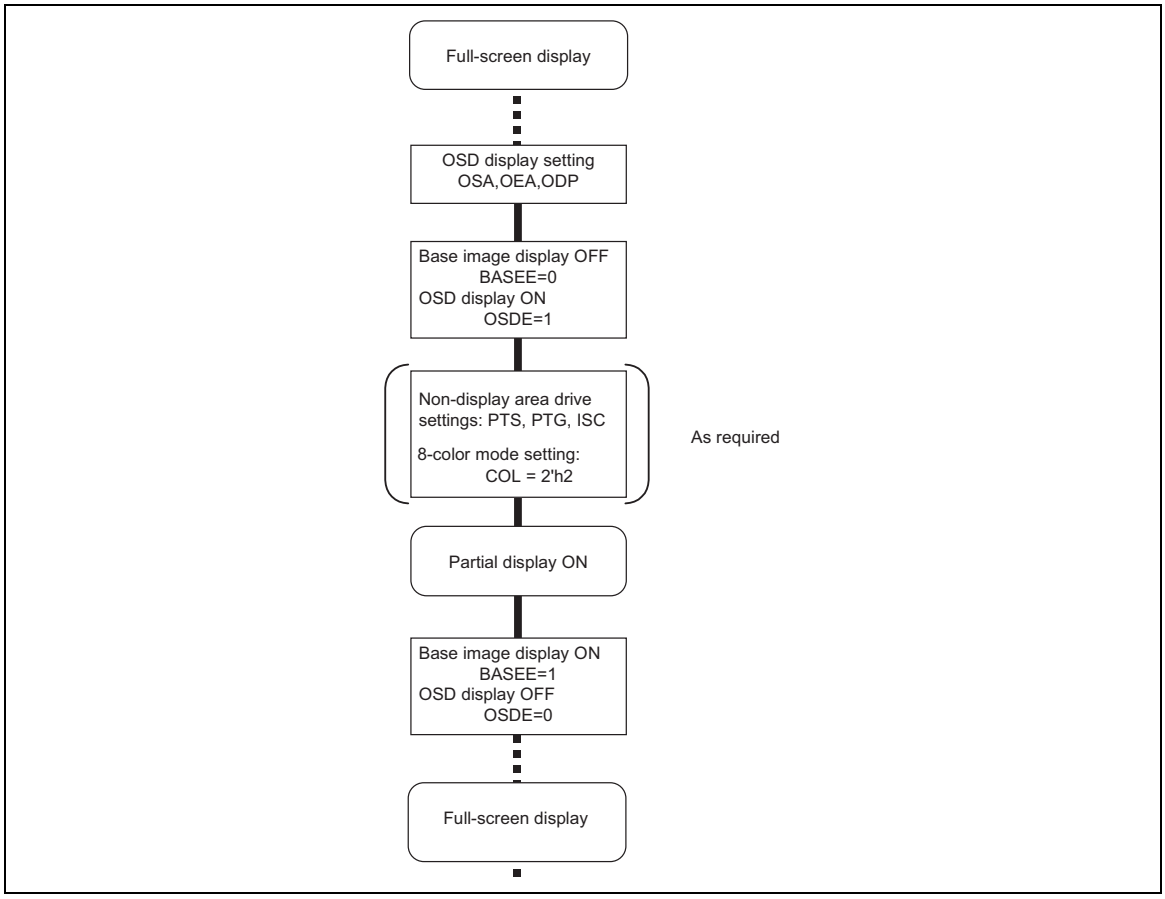
Low power consumption display mode



8-color mode



Partial display mode



Absolute Maximum Values

Item	Symbol	Unit	Value	Notes
Power supply voltage (1)	IOVcc, Vcc1	V	-0.3 ~ + 4.6	1, 2, 5
Power supply voltage (2)	Vcc - GND	V	-0.3 ~ + 4.6	1, 3, 5
Power supply voltage (3)	DDVDH - GND	V	-0.3 ~ + 6.5	1, 4
Input voltage	Vt	V	-0.3 ~ Vcc + 0.3	1
Operating temperature	Topr	°C	-40 ~ + 85	1, 6

Note 1) The LSI may be permanently damaged if it is used under the condition exceeding the above absolute maximum values. It is also recommended to use the LSI within the limit of its electric characteristics during normal operation. Exceeding the conditions may lead to malfunction of LSI and affect its credibility.

Note 2) IOVcc(High) ≥ GND(Low), Vcc1(High) ≥ GND(Low) must be observed.

Note 3) Vcc(High) ≥ GND(Low) must be observed.

Note 4) DDVDH(High) ≥ GND(Low) must be observed.

Note 5) Vcc(High) ≥ IOVcc(Low), Vcc(High) ≥ Vcc1(Low) must be observed.

Note 6) The DC and AC characteristics of chip and wafer products are guaranteed at 85 °C.

Note 7) The electric potential of this LSI's substrate is GND. The electrical connection of the other side of the chip must be at the electric potential of an insulated state or GND. The electrical and operational characteristics of the LSI will not be guaranteed otherwise.

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.5	2003, July 31	First issue		