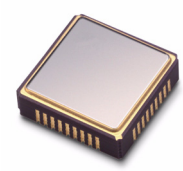
GENERAL DESCRIPTION

The M1020/21 is a VCSO (Voltage Controlled SAW Oscillator) based clock jitter attenuator PLL designed for clock jitter attenuation and frequency translation. The device is ideal for generating the transmit reference clock for optical network systems supporting up to 2.5Gb data rates. It can serve to jitter attenuate a stratum reference clock or a recovered clock in loop timing mode. The M1020/21 module includes a proprietary SAW (surface acoustic wave) delay line as part of the VCSO. This results in a high frequency, high-Q, low phase noise oscillator that assures low intrinsic output jitter.



FEATURES

- **Integrated SAW delay line; low phase jitter of < 0.5ps rms, typical (12kHz to 20MHz)**
- **Output frequencies of 62.5 to 175 MHz (Specify VCSO output frequency at time of order)**
- **LVPECL clock output (CML and LVDS options available)**
- **Reference clock inputs support differential LVDS, LVPECL, as well as single-ended LVCMOS, LVTTL**
- **Loss of Lock (LOL) output pin**
- **Narrow Bandwidth control input (NBW pin)**
- **Hitless Switching (HS) options with or without Phase Build-out (PBO) to enable SONET (GR-253) / SDH (G.813) MTIE and TDEV compliance during reselection**
- **Pin-selectable feedback and reference divider ratios**
- **Industrial temperature grade available**
- **Single 3.3V power supply**
- **Small 9 x 9 mm SMT (surface mount) package**

PIN ASSIGNMENT (9 x 9 mm SMT)

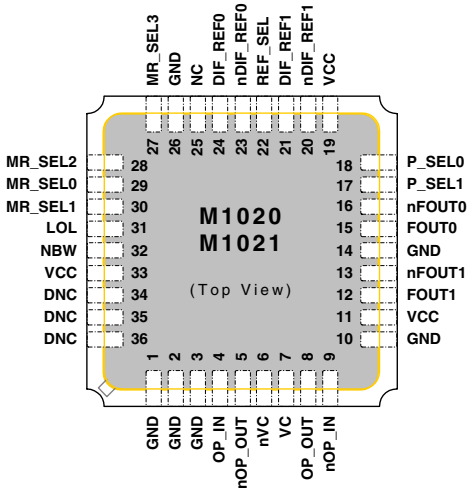


Figure 1: Pin Assignment

Example I/O Clock Frequency Combinations Using M1020-11-155.5200 or M1021-11-155.5200

Input Reference Clock (MHz)	PLL Ratio (Pin Selectable)	Output Clock (MHz) (Pin Selectable)
(M1020) (M1021)	(M1020) (M1021)	
19.44 or 38.88	8 or 4	155.52 or 77.76
77.76	2	
155.52	1	
622.08	0.25	

Table 1: Example I/O Clock Frequency Combinations

SIMPLIFIED BLOCK DIAGRAM

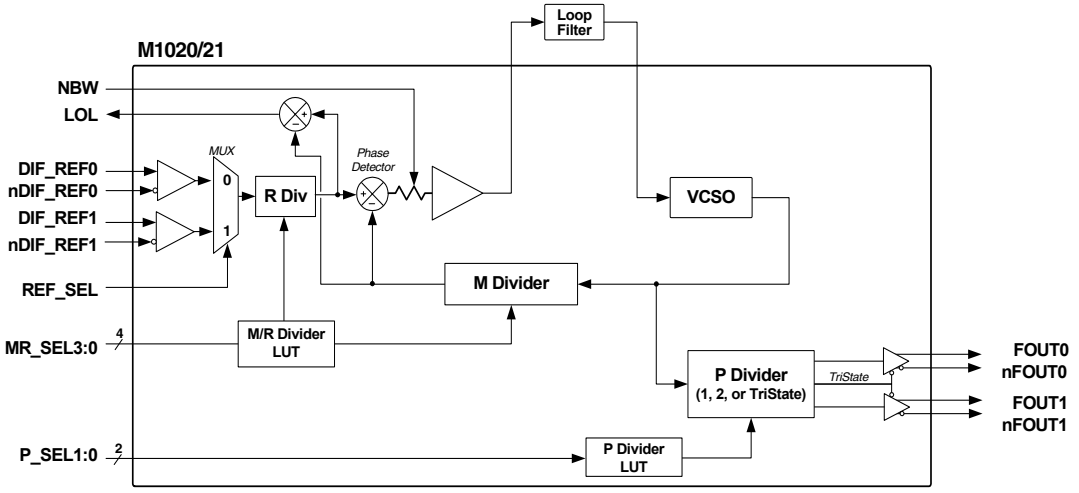


Figure 2: Simplified Block Diagram

PIN DESCRIPTIONS

Number	Name	I/O	Configuration	Description
1, 2, 3, 10, 14, 26	GND	Ground		Power supply ground connections.
4 9	OP_IN nOP_IN	Input		External loop filter connections. See Figure 5, External Loop Filter, on pg. 6.
5 8	nOP_OUT OP_OUT	Output		
6 7	nVC VC	Input		
11, 19, 33	VCC	Power		Power supply connection, connect to +3.3V.
12 13	FOUT1 nFOUT1	Output	No internal terminator	Clock output 1. Differential LVPECL (CML, LVDS available).
15 16	FOUT0 nFOUT0	Output	No internal terminator	Clock output 0. Differential LVPECL (CML, LVDS available).
17 18	P_SEL1 P_SEL0		Internal pull-down resistor[1]	Post-PLL , P divider selection. LVCMOS/LVTTL. See Table 5, P Divider Look-Up Table (LUT), on pg. 4.
20	nDIF_REF1	Input	Biased to Vcc/2 [2]	Reference clock input pair 1. Differential LVPECL or LVDS. Resistor bias on inverting terminal supports TTL or LVCMOS.
21	DIF_REF1		Internal pull-down resistor[1]	
22	REF_SEL	Input	Internal pull-down resistor[1]	Reference clock input selection. LVCMOS/LVTTL: Logic 1 selects DIF_REF1, nDIF_REF1. Logic 0 selects DIF_REF0, nDIF_REF0.
23	nDIF_REF0	Input	Biased to Vcc/2 [2]	Reference clock input pair 0. Differential LVPECL or LVDS. Resistor bias on inverting terminal supports TTL or LVCMOS.
24	DIF_REF0		Internal pull-down resistor [1]	
25	NC			No internal connection.
27 28 29 30	MR_SEL3 MR_SEL2 MR_SEL0 MR_SEL1	Input	Internal pull-down resistor[1]	M and R divider value selection. LVCMOS/ LVTTL. See Tables 3 and 4, M and R Divider Look-Up Tables (LUT) on pg. 3.
31	LOL	Output		Loss of Lock indicator output. Asserted when internal PLL is not tracking the input reference for frequency and phase. [3] Logic 1 indicates loss of lock. Logic 0 indicates locked condition.
32	NBW	Input	Internal pull-UP resistor[1]	Narrow Bandwidth enable. LVCMOS/LVTTL: Logic 1 - Narrow loop bandwidth, R_{IN} = 2100kΩ Logic 0 - Wide bandwidth, R_{IN} = 100kΩ
34, 35, 36	DNC		Do Not Connect.	Internal nodes. Connection to these pins can cause erratic device operation.

Table 2: Pin Descriptions

Note 1: For typical values of internal pull-down and pull-UP resistors, see **DC Characteristics** on pg. 8.
Note 2: Biased toVcc/2, with 50kΩ to Vcc and 50kΩ to ground. See **Differential Inputs Biased to VCC/2** on pg. 8.
Note 3: See **LVCMOS Output** in DC Characteristics on pg. 8.

DETAILED BLOCK DIAGRAM

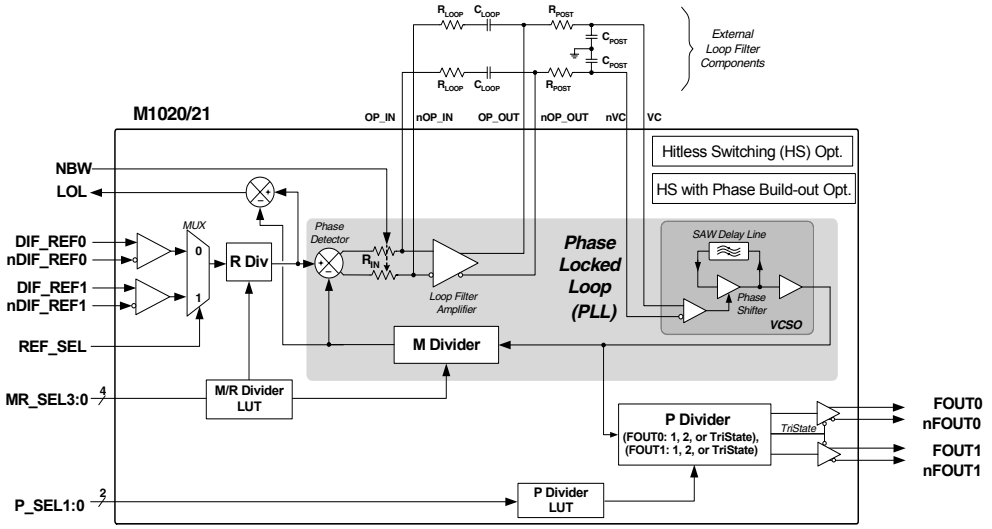


Figure 3: Detailed Block Diagram

DIVIDER SELECTION TABLES

M and R Divider Look-Up Tables (LUT)

The MR_SEL3:0 pins select the feedback and reference divider values M and R to enable adjustment of loop bandwidth and jitter tolerance. The look-up tables vary by device variant. M1020 and M1021 are defined in Tables 3 and 4 respectively.

Tables 3 and 4 provide example Fin and phase detector frequencies with 155.52MHz *VCSO devices (***M1020-11-155.5200** *and* **M1021-11-155.5200***).* *See "Ordering Information" on pg. 10.*

M1020 M/R Divider LUT

MR_SEL3:0	M Div	R Div	Total PLL Ratio	Fin for 155.52MHz VCSO (MHz)	Phase Det. Freq. for 155.52MHz VCSO (MHz)
0 0 0 0	8	1	8	19.44	19.44
0 0 0 1	32	4	8	19.44	4.86
0 0 1 0	128	16	8	19.44	1.215
0 0 1 1	512	64	8	19.44	0.30375
0 1 0 0	2	1	2	77.76	77.76
0 1 0 1	8	4	2	77.76	19.44
0 1 1 0	32	16	2	77.76	4.86
0 1 1 1	128	64	2	77.76	1.215
1 0 0 0	1	1	1	155.52	155.52
1 0 0 1	4	4	1	155.52	38.88
1 0 1 0	16	16	1	155.52	9.72
1 0 1 1	64	64	1	155.52	2.43
1 1 0 0	Test Mode[1]		N/A	N/A	N/A
1 1 0 1	1	4	0.25	622.08	155.52
1 1 1 0	4	16	0.25	622.08	38.88
1 1 1 1	16	64	0.25	622.08	9.72

Table 3: M1020 M/R Divider LUT

Note 1: Factory test mode; do not use.

M1021 M/R Divider LUT

MR_SEL3:0	M Div	R Div	Total PLL Ratio	Fin for 155.52MHz VCSO (MHz)	Phase Det. Freq. for 155.52MHz VCSO (MHz)
0 0 0 0	4	1	4	38.88	38.88
0 0 0 1	16	4	4	38.88	9.72
0 0 1 0	64	16	4	38.88	2.43
0 0 1 1	256	64	4	38.88	0.6075
0 1 0 0	2	1	2	77.76	77.76
0 1 0 1	8	4	2	77.76	19.44
0 1 1 0	32	16	2	77.76	4.86
0 1 1 1	128	64	2	77.76	1.215
1 0 0 0	1	1	1	155.52	155.52
1 0 0 1	4	4	1	155.52	38.88
1 0 1 0	16	16	1	155.52	9.72
1 0 1 1	64	64	1	155.52	2.43
1 1 0 0	Test Mode[1]		N/A	N/A	N/A
1 1 0 1	1	4	0.25	622.08	155.52
1 1 1 0	4	16	0.25	622.08	38.88
1 1 1 1	16	64	0.25	622.08	9.72

Table 4: M1021 M/R Divider LUT

Note 1: Factory test mode; do not use.

General Guidelines for M and R Divider Selection

General guidelines for M/R divider selection (see following pages for more detail):

- A lower phase detector frequency should be used for loop timing applications to assure PLL tracking, especially during GR-253 jitter tolerance testing. The recommended maximum phase detector frequency for loop timing mode is 19.44MHz. The LOL pin should not be used during loop timing mode.
- When LOL is to be used for system health monitoring, the phase detector frequency should be 5MHz or greater. Low phase detector frequencies make LOL overly sensitive, and higher phase detector frequencies make LOL less sensitive.

P Divider Look-Up Table (LUT)

The P_SEL1 and P_SEL0 pins select the post-PLL divider values P1 and P0. The output frequency of the SAW can be divided by 1 or 2, or the outputs can be TriStated. The outputs can be placed into the valid state combinations as listed in Table 5.

P_SEL1:0	P Values		M1020-155.5200 or M1021-155.5200 Output Frequency (MHz)	
	for FOUT0	for FOUT1	FOUT0	FOUT1
0 0	2	2	77.76	77.76
0 1	1	1	155.52	155.52
1 0	2	1	77.76	155.52
1 1	TriState	TriState	N/A	N/A

Table 5: P Divider Look-Up Table (LUT)

FUNCTIONAL DESCRIPTION

The M1020/21 is a PLL (Phase Locked Loop) based clock generator that generates output clocks synchronized to one of two selectable input reference clocks. An internal high "Q" SAW delay line provides low jitter signal performance.

A pin-selected look-up table is used to select the PLL feedback divider (M Div) and reference divider (R Div) as shown in Tables 3 and 4 on pg. 3. These look-up tables provide flexibility in both the overall frequency multiplication ratio (total PLL ratio) and phase detector frequency.

The M1020/21 includes a Loss of Lock (LOL) indicator, which provides status information to system management software. A Narrow Bandwidth (NBW) control pin is provided as an additional mechanism for adjusting PLL loop bandwidth without affecting the phase detector frequency.

Options are available for Hitless Switching (HS) with or without Phase Build-out (PBO). They provide SONET/SDH MTIE and TDEV compliance during a reference clock reselection.

Input Reference Clocks

Two clock reference inputs and a selection mux are provided. Either reference clock input can accept a differential clock signal (such as LVPECL or LVDS) or a single-ended clock input (LVCMOS or LVTTL on the non-inverting input).

A single-ended reference clock on the unselected reference input can cause an increase in output clock jitter. For this reason, differential reference inputs are preferred; interference from a differential input on the non-selected input is minimal.

Implementation of single-ended input has been facilitated by biasing nDIF_REF0 and nDEF_REF1 to Vcc/2, with 50kΩ to Vcc and 50kΩ to ground. The input clock structure, and how it is used with either LVCMOS/LVTTL inputs or a DC- coupled LVPECL clock, is shown in Figure 4.

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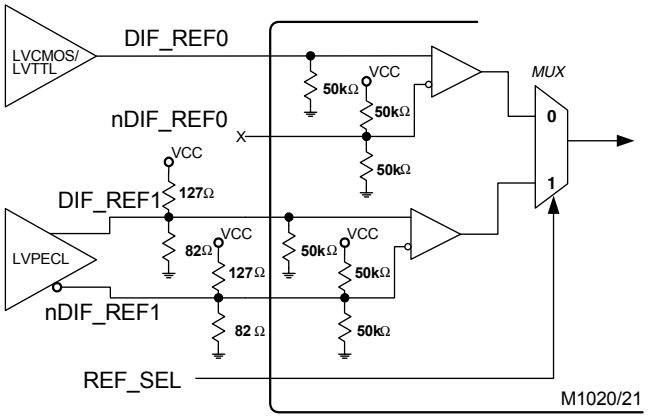


Figure 4: Input Reference Clocks

Differential LVPECL Inputs

Differential LVPECL inputs are connected to both reference input pins in the usual manner. The external load termination resistors shown in Figure 4 (the 127Ω and 82Ω resistors) will work for both AC and DC coupled LVPECL reference clock lines. These provide the 50Ω load termination and the VTT bias voltage.

Single-ended Inputs

Single-ended inputs (LVCMOS or LVTTL) are connected to the non-inverting reference input pin (DIF_REF0 or DIF_REF1). The inverting reference input pin (nDIF_REF0 or nDIF_REF1) must be left unconnected.

*In single-ended operation, when the unused inverting input pin (*nDIF_REF0 *or* nDEF_REF1*) is left floating (not connected), the input will self-bias at VCC/2.*

PLL Operation

The M1020/21 is a complete clock PLL. It uses a phase detector and configurable dividers to synchronize the output of the VCSO with the selected reference clock.

The “M” divider divides the VCSO output frequency, feeding the result into the plus input of the phase detector.

The output of the “R” divider is fed into the minus input of the phase detector. The phase detector compares its two inputs. The phase detector output, filtered externally, causes the VCSO to increase or decrease in speed as needed to phase- and frequency-lock the VCSO to the reference input.

The value of the M divider directly affects closed loop bandwidth.

The relationship between the nominal VCSO center frequency (Fvcso), the M divider, the R divider, and the input reference frequency (Fin) is:

$$Fvcso = Fin \times \frac{M}{R}$$

For the available M divider and R divider look-up table combinations, Tables 3 and 4 on pg. 3 list the Total PLL Ratio as well as Fin when using the **M1020-11-155.5200** or the **M1021-11-155.5200**. (See “Ordering Information” on pg. 10.)

Post-PLL Divider

The M1020/21 also features a post-PLL (P) divider.

By using the P Divider, the device’s output frequency (Fout) can be the VCSO center frequency (Fvcso) or 1/2 Fvcso, or 0.

The P_SEL0 and P_SEL1 pins select the value for the P divider. (See Table 5 on pg. 4.)

When the P divider is included, the complete relationship for the output frequency (Fout) is defined as:

$$Fout = \frac{Fvcso}{P} = Fin \times \frac{M}{R \times P}$$

Due to the narrow tuning range of the VCSO (±200ppm), appropriate selection of all of the following are required for the PLL be able to lock: VCSO center frequency, input frequency, and divider selections.

Loss of Lock Indicator (LOL) Output Pin

Under normal device operation, when the PLL is locked, the LOL Phase Detector drives LOL to logic 0. Under circumstances when the VCSO cannot lock to the input (as measured by a greater than 4 ns discrepancy between the feedback and reference clock rising edges at the LOL Phase Detector) the LOL output goes to logic 1. The LOL pin will return back to logic 0 when the phase detector error is less than 2 ns. The loss of lock indicator is a low current LVCMOS output.

Guidelines for Using LOL

In a given application, the magnitude of peak-to-peak jitter at the phase detector will usually increase as the R divider is increased. If the LOL pin will be used to detect an unusual clock condition, or a clock fault, the MR_SEL3:0 pins should be set to provide a phase detector frequency of 5MHz or greater. Otherwise, false LOL indications may result. A phase detector frequency of 10MHz or greater is desirable when reference jitter is over 500ps, or when the device is used within a noisy system environment. Refer to Tables 3 and 4 on pg. 3 for phase detector frequency when using the **M1020-11-155.5200** or the **M1021-11-155.5200**.

TriState

The TriState feature puts the LVPECL output driver into a high impedance state, effectively disconnecting the driver from the FOUT and nFOUT pins of the device. A logic 0 is then present on the clock net. The impedance of the clock net is then set to 50Ω by the external circuit resistors. (This is in distinction to a CMOS output in TriState, in which case the net goes to a high impedance and the logic value floats.) The 50Ω impedance level of the LVPECL TriState allows manufacturing In-circuit Test to drive the clock net with an external 50Ω generator to validate the integrity of clock net and the clock load.

Any unused output (single-ended or differential) should be left unconnected (floating) in system application. This minimizes output switching current and therefore minimizes noise modulation of VCSO.

Optional Hitless Switching and Phase Build-out

The M1020/21 is available with a Hitless Switching feature that is enabled during device manufacturing. In addition, a Phase Build-out feature is also offered. These features are offered as device options and are specified by device order code. Refer to "Ordering Information" on pg. 10.

The Hitless Switching feature (with or without Phase Build-out) is designed for applications where switching occurs between two stable system reference clocks. It should not be used in loop timing applications, or when reference clock jitter is greater than 1 ns pk-pk. Hitless Switching is triggered by the LOL circuit, which is activated by a 4 ns phase transient. This magnitude of phase transient can generated by the CDR (Clock & Data Recovery unit) in loop timing mode, especially during a system jitter tolerance test. It can also be generated by some types of Stratum clock DPLLs (digital PLL), especially those that do not include a post de-jitter APLL (analog PLL).

When the M1020/21 is operating in wide bandwidth mode (NBW=0), the optional Hitless Switching function puts the device into narrow bandwidth mode when activated. This allows the PLL to lock the new input clock phase gradually. With proper configuration of the external loop filter, the output clock complies with MTIE and TDEV specifications for GR-253 (SONET) and ITU G.813 (SDH) during input reference clock changes.

The optional proprietary Phase Build-out (PBO) function enables the PLL to absorb most of the phase change of the input clock. The PBO function selects a new VCSO clock edge for the PLL Phase Detector feedback clock, selecting the edge closest in phase to the new input clock phase. This reduces re-lock time, the generation of wander, and extra output clock cycles.

The Hitless Switching and Phase Build-out functions are triggered by the LOL circuit. For proper operation, a low phase detector frequency must be avoided. See "Guidelines for Using LOL" on pg. 5 for information regarding the phase detector frequency.

HS/PBO Triggers

The HS function (or the combined HS/PBO function) is armed after the device locks to the input clock reference. Once armed, HS is triggered by the occurance of a Loss of Lock condition. This would typically occur as a consequence of a clock reference failure, a clock failure upstream to the M1020/21, or a M1020/21 clock reference mux reselection.

HS/PBO Operation

Once triggered, the following HS/PBO sequence occurs:

1. The HS function disables the PLL Phase Detector and puts the device into NBW (narrow bandwidth) mode. The internal resistor Rin is changed to 2100kΩ. See the External Loop Filter on pg. 6.
2. If included, the PBO function adds to (builds out) the phase in the clock feedback path (in VCSO clock cycle increments) to align the feedback clock with the (new) reference clock input phase.
3. The PLL Phase Detector is enabled, allowing the PLL to re-lock.
4. Once the PLL Phase Detector feedback and input clocks are locked to within 2 ns for eight consecutive cycles, a timer (WBW timer) for resuming wide bandwidth (in 175 ns) is started.
5. When the WBW timer times out, the device reverts to wide loop bandwidth mode (*i.e.,* Rin is returned to 100kΩ) and the HS/PBO function is re-armed.

Narrow Bandwidth (NBW) Control Pin

A Narrow Loop Bandwidth control pin (NBW pin) is included to adjust the PLL loop bandwidth. In wide bandwidth mode (NBW=0), the internal resistor Rin is 100kΩ. With the NBW pin asserted, the internal resistor Rin is changed to 2100kΩ. This lowers the loop bandwidth by a factor of about 21 (approximately 2100 / 100) and lowers the damping factor by a factor of about 4.6 (the square root of 21), assuming the same loop filter components.

External Loop Filter

To provide stable PLL operation, the M1020/21 requires the use of an external loop filter. This is provided via the provided filter pins (see Figure 5).

Due to the differential signal path design, the implementation requires two identical complementary RC filters as shown here.

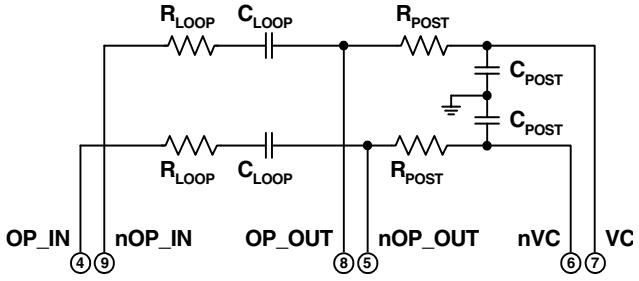


Figure 5: External Loop Filter

See Table 6, Example External Loop Filter Component Values on pg. 7.

PLL bandwidth is affected by loop filter component values, the "M" value, and the "PLL Loop Constants" listed in AC Characteristics on pg. 9.

The MR_SEL3:0 settings can be used to actively change PLL loop bandwidth in a given application. See "M and R Divider Look-Up Tables (LUT)" on pg. 3.

PLL Simulator Tool Available

A free PC software utility is available on the ICS website (www.icst.com). The M2000 Timing Modules PLL Simulator is a downloadable application that simulates PLL jitter and wander transfer characteristics. This enables the user to set appropriate external loop component values in a given application.

For guidance on device or loop filter implementation, contact CMBU (Commercial Business Unit) Product Applications at (508) 852-5400.

Example External Loop Filter Component Values[1] for M1020-yz-155.5200 and M1021-yz-155.5200

VCSO Parameters: K_{VCO} = 200kHz/V, R_{IN} = 100kΩ (pin NBW = 0), VCSO Bandwidth = 700kHz.

Device Configuration					Example External Loop Filter Comp. Values				Nominal Performance Using These Values		
F_{REF} (MHz)	F_{VCSO} (MHz)	MR_SEL3:0	MDiv	NBW	R_{LOOP}	C_{LOOP}	R_{POST}	C_{POST}	PLL Loop Bandwidth	Damping Factor	Passband Peaking (dB)
19.44 [2]	155.52	0 0 0 0	8	0	6.8kΩ	10µF	82kΩ	1000pF	315Hz	5.4	0.07
38.88 [3]	155.52	0 0 0 1	16	0	12kΩ	10µF	82kΩ	1000pF	270Hz	6.7	0.05
77.76 [4]	155.52	0 1 0 1	8	0	6.8kΩ	10µF	82kΩ	1000pF	315Hz	5.4	0.07
77.76 [5]	155.52	0 1 1 0	32	0	22kΩ	4.7µF	82kΩ	1000pF	250Hz	6.0	0.05
155.52 [4]	155.52	1 0 1 0	16	0	12kΩ	10µF	82kΩ	1000pF	270Hz	6.7	0.05
155.52 [5]	155.52	1 0 1 1	64	0	47kΩ	2.2µF	82kΩ	1000pF	266Hz	6.2	0.05

Table 6: Example External Loop Filter Component Values

Note 1: K_{VCO} , VCSO Bandwidth, M Divider Value, and External Loop Filter Component Values determine Loop Bandwidth, Damping Factor, and Passband Peaking. For PLL Simulator software, go to www.icst.com.
Note 2: This row is for the M1020 only.
Note 3: This row is for the M1021 only.
Note 4: Optimal for system clock filtering.
Note 5: Optimal for loop timing mode (LOL or Hitless Switching should not be used).

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Rating	Unit
V_I	Inputs	-0.5 to V_{CC} +0.5	V
V_O	Outputs	-0.5 to V_{CC} +0.5	V
V_{CC}	Power Supply Voltage	4.6	V
T_S	Storage Temperature	-45 to +100	°C

Table 7: Absolute Maximum Ratings

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in Recommended Conditions of Operation, DC Characteristics, or AC Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

RECOMMENDED CONDITIONS OF OPERATION

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
T_A	Ambient Operating Temperature	Commercial	0		+70	°C
		Industrial	-40		+85	°C

Table 8: Recommended Conditions of Operation

ELECTRICAL SPECIFICATIONS

DC Characteristics

Unless stated otherwise, V_{CC} = 3.3V ±5%, T_A = 0 °C to +70 °C (commercial), T_A = -40 °C to +85 °C (industrial), F_{VCSO} = F_{OUT} = 150-175MHz, LVPECL outputs terminated with 50Ω to V_{CC} - 2V

	Symbol	Parameter		Min	Typ	Max	Unit	Conditions
Power Supply	V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V	
	I_{CC}	Power Supply Current			175	225	mA	
All Differential Inputs	V_{P-P}	Peak to Peak Input Voltage	DIF_REF0, nDIF_REF0, DIF_REF1, nDIF_REF1	0.15			V	
	V_{CMR}	Common Mode Input		0.5		V_{CC} - .85	V	
	C_{IN}	Input Capacitance				4	pF	
Differential Inputs with Pull-down	I_{IH}	Input High Current (Pull-down)	DIF_REF0, DIF_REF1			150	µA	V_{CC} = V_{IN} = 3.456V
	I_{IL}	Input Low Current (Pull-down)		-5			µA	
	$R_{pulldown}$	Internal Pull-down Resistance			50		kΩ	
Differential Inputs Biased to VCC/2	I_{IH}	Input High Current (Biased)	nDIF_REF0, nDIF_REF1			150	µA	V_{IN} = 0 to 3.456V
	I_{IL}	Input Low Current (Biased)		-150			µA	
	R_{bias}	Biased to Vcc/2			See Figure 4			
All LVCMOS / LVTTL Inputs	V_{IH}	Input High Voltage	REF_SEL, MR_SEL3, MR_SEL2, MR_SEL1, MR_SEL0, P_SEL1, P_SEL0, NBW	2		V_{CC} + 0.3	V	
	V_{IL}	Input Low Voltage		-0.3		0.8	V	
	C_{IN}	Input Capacitance				4	pF	
LVCMOS / LVTTL Inputs with Pull-down	I_{IH}	Input High Current (Pull-down)	REF_SEL, MR_SEL3, MR_SEL2, MR_SEL1, MR_SEL0, P_SEL1, P_SEL0			150	µA	V_{CC} = V_{IN} = 3.456V
	I_{IL}	Input Low Current (Pull-down)		-5			µA	
	$R_{pulldown}$	Internal Pull-down Resistance			50		kΩ	
LVCMOS / LVTTL Inputs with Pull-UP	I_{IH}	Input High Current (Pull-UP)	NBW			5	µA	V_{CC} = 3.456V V_{IN} = 0 V
	I_{IL}	Input Low Current (Pull-UP)		-150			µA	
	R_{pullup}	Internal Pull-UP Resistance			50		kΩ	
Differential Outputs	V_{OH}	Output High Voltage	FOUT0, nFOUT0, FOUT1, nFOUT1	V_{CC} - 1.4		V_{CC} - 1.0	V	
	V_{OL}	Output Low Voltage		V_{CC} - 2.0		V_{CC} - 1.7	V	
	V_{P-P}	Peak to Peak Output Voltage [1]		0.4		0.85	V	
LVCMOS Output	V_{OH}	Output High Voltage	LOL	2.4		V_{CC}	V	I_{OH}= 1mA
	V_{OL}	Output Low Voltage		GND		0.4	V	I_{OL}= 1mA

Note 1: Single-ended measurement. See Figure 6, Output Rise and Fall Time, on pg. 9.

Table 9: DC Characteristics

ELECTRICAL SPECIFICATIONS (CONTINUED)

AC Characteristics

Unless stated otherwise, V_{CC} = 3.3V ±5%, T_A = 0 °C to +70 °C (commercial), T_A = -40 °C to +85 °C (industrial), F_{VCSO} = F_{OUT} = 150-175MHz, LVPECL outputs terminated with 50Ω to V_{CC} - 2V

	Symbol	Parameter		Min	Typ	Max	Unit	Conditions
	F_{IN}	Input Frequency	DIF_REF0, nDIF_REF0, DIF_REF1, nDIF_REF1	15		700	MHz	
	F_{OUT}	Output Frequency	FOUT0, nFOUT0, FOUT1, nFOUT1	62.5		175	MHz	
	APR	Absolute Pull-Range of VCSO	Commercial	±120	±200		ppm	
			Industrial	±50	±150		ppm	
PLL Loop Constants [1]	K_{VCO}	VCO Gain			200		kHz/V	
	R_{IN}	Internal Loop Resistor	Wide Bandwidth		100		kΩ	
			Narrow Bandwidth		2100		kΩ	
	BW_{VCSO}	VCSO Bandwidth			700		kHz	
Phase Noise and Jitter	Φn	Single Side Band Phase Noise @155.52MHz	1kHz Offset		-83		dBc/Hz	Fin=19.44 or 38.88_MHz Tot. PLL ratio = 8 or 4. See pg. 3
			10kHz Offset		-113		dBc/Hz	
			100kHz Offset		-136		dBc/Hz	
	J(t)	Jitter (rms) @155.52MHz	12kHz to 20MHz		0.4	0.6	ps	
	odc	Output Duty Cycle [2]		45	50	55	%	
	t_R	Output Rise Time [2] for FOUT0, nFOUT0, FOUT1, nFOUT1		350	450	550	ps	20% to 80%
	t_F	Output Fall Time [2] for FOUT0, nFOUT0, FOUT1, nFOUT1		350	450	550	ps	20% to 80%

Table 10: AC Characteristics

Note 1: Parameters needed for PLL Simulator software; see Table 6, Example External Loop Filter Component Values, on pg. 7.
Note 2: See Parameter Measurement Information on pg. 9.

PARAMETER MEASUREMENT INFORMATION

Output Rise and Fall Time

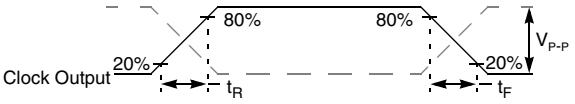


Figure 6: Output Rise and Fall Time

Output Duty Cycle

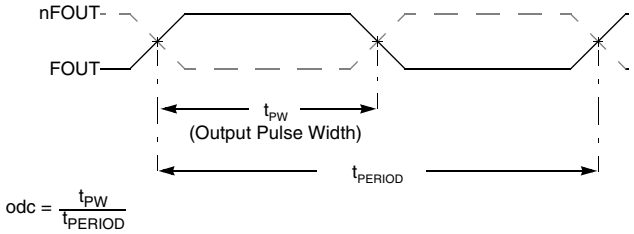
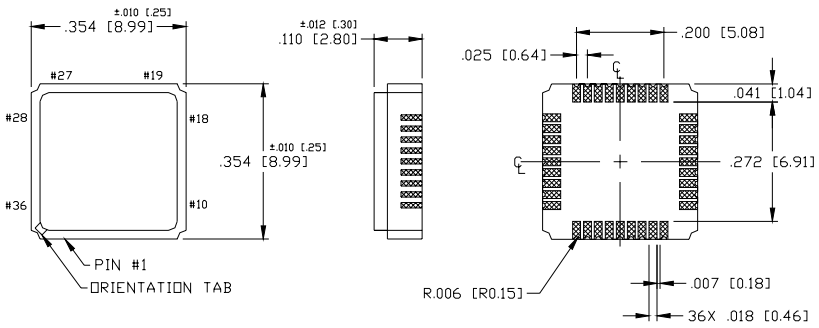


Figure 7: Output Duty Cycle

DEVICE PACKAGE - 9 x 9mm CERAMIC LEADLESS CHIP CARRIER

Mechanical Dimensions:



Refer to the SAW PLL application notes web page at www.icst.com/products/appnotes/SawPllAppNotes.htm for application notes, including recommended PCB footprint, solder mask, and furnace profile.

NOTES:
1. DIMENSIONS ARE IN INCHES, DIMENSIONS IN [ ] ARE MM.
2. UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE ±.005 [.13]

Figure 8: Device Package - 9 x 9mm Ceramic Leadless Chip Carrier

ORDERING INFORMATION

Part Numbering Scheme

Part Number: M102x-1z-xxx.xxxx

Frequency Input Divider Option
0 = Fin can equal Fvcso divided by: 8, 2, or 1
1 = Fin can equal Fvcso divided by: 4, 2, or 1

Output type
1 = LVPECL
(For CML or LVDS clock output, consult factory)

Hitless Switching / Phase Build-out Options
1 = none
2 = Hitless Switching
3 = Hitless Switching with Phase Build-out

Temperature
"-" = 0 to +70 °C (commercial)
I = - 40 to +85 °C (industrial)

VCSO Frequency (MHz)
See Table 11, right. Consult ICS for other frequencies.

Figure 9: Part Numbering Scheme

Standard VCSO Output Frequencies (MHz)*
Consult ICS for the availablity of other VCSO frequencies

125.0000	167.3280
155.5200	167.3316
156.2500	167.7097
156.8324	168.0400
161.1328	172.6423
166.6286	173.3708
167.2820	

Table 11: Standard VCSO Output Frequencies (MHz)

Note *: Fout can equal Fvcso divided by: 1 or 2

Consult ICS for the availability of other VCSO frequencies.

Example Part Numbers

VCSO Frequency (MHz)	Temperature	Order Part Number (Examples)
155.52	commercial	**M1020-11-155.5200** or **M1021-11-155.5200**
	industrial	**M1020-11I155.5200** or **M1021-11I155.5200**
156.25	commercial	**M1020-11-156.2500** or **M1021-11-156.2500**
	industrial	**M1020-11I156.2500** or **M1021-11I156.2500**

Table 12: Example Part Numbers