

**MAXIM**

# Single-Ended-to-Differential LVECL/LVPECL 2:1 Multiplexer

**MAX9380**

## General Description

The MAX9380 is a high-speed, low-jitter 2:1 multiplexer for clock and data distribution applications. The device selects one of the two single-ended inputs and converts it to a differential output.

The MAX9380 features low part-to-part skew of 33ps and propagation delay of 263ps.

The MAX9380 operates from a +3.0V to +3.8V supply for LVPECL applications or from a -3.0V to -3.8V supply for LVECL applications. The input is selected by a single select input. The select and data inputs feature internal pull-down resistors that ensure a low default state if left open.

These devices are specified for operation from -40°C to +85°C, and are available in space-saving 8-pin  $\mu$ MAX and SO packages.

## Features

- ◆ >300mV Differential Output at 3.5GHz
- ◆ Low 20mA Supply Current
- ◆ 33ps (typ) Part-to-Part Skew
- ◆ 263ps (typ) Propagation Delay
- ◆ <0.2psRMS Added Random Jitter
- ◆ High-Speed Select Input
- ◆ Output Low with Open Inputs
- ◆ Pin Compatible with MC10EP58

## Applications

Precision Clock Distribution  
DSLAM  
DLC  
Base Station  
ATE

## Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX9380EUA*	-40°C to +85°C	8 $\mu$ MAX
MAX9380ESA	-40°C to +85°C	8 SO-EP**

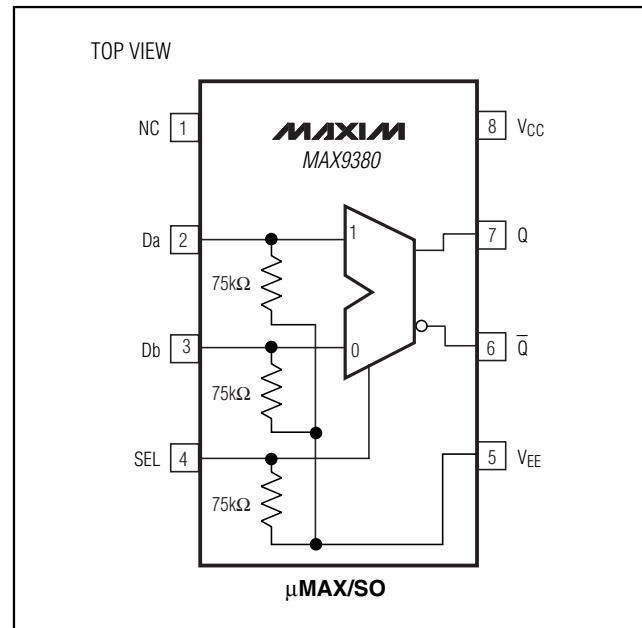
\*Future product—contact factory for availability.

\*\*EP = Exposed paddle.

## Input/Output Function Table

INPUTS	OUTPUTS	
Da (SEL = high) or Db (SEL = low)	Q	$\bar{Q}$
High	H	L
Low or open	L	H

## Pin Configuration

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Maxim Integrated Products 1

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# Single-Ended-to-Differential LVECL/LVPECL 2:1 Multiplexer

## ABSOLUTE MAXIMUM RATINGS

VCC - VEE	.....-0.3V to +4.1V
Inputs (Da, Db, SEL)	.....VEE - 0.3V to VCC + 0.3V
Output Current (Continuous)	.....50mA
Output Current (Surge)	.....100mA
Junction-to-Ambient Thermal Resistance in Still Air	
8-Pin $\mu$ MAX	.....+221°C/W
8-Pin SO*	.....+170°C/W
Junction-to-Ambient Thermal Resistance with 500LFPM Airflow	
8-Pin $\mu$ MAX	.....+155°C/W
8-Pin SO*	.....+99°C/W

Junction-to-Case Thermal Resistance	
8-Pin $\mu$ MAX	.....+39°C/W
8-Pin SO	.....+40°C/W
Operating Temperature Range	.....-40°C to +85°C
Junction Temperature	.....+150°C
Storage Temperature Range	.....-65°C to +150°C
ESD Protection	
Human Body Model (Inputs and Outputs)	.....2kV
Soldering Temperature (10s)	.....+300°C
* Rating is for exposed paddle not connected.	

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

(VCC - VEE = +3.0V to +3.8V, outputs terminated with 50 $\Omega$  to VCC - 2.0V, unless otherwise noted.) (Notes 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
<b>INPUTS (Da, Db, SEL)</b>												
Input High Voltage	V <sub>IH</sub>		V <sub>CC</sub> - 1.210	V <sub>CC</sub> - 0.885	V <sub>CC</sub> - 1.145	V <sub>CC</sub> - 0.820	V <sub>CC</sub> - 1.085	V <sub>CC</sub> - 0.760			V	
Input Low Voltage	V <sub>IL</sub>		V <sub>CC</sub> - 1.935	V <sub>CC</sub> - 1.610	V <sub>CC</sub> - 1.870	V <sub>CC</sub> - 1.545	V <sub>CC</sub> - 1.81	V <sub>CC</sub> - 1.485			V	
Input High Current	I <sub>IH</sub>	V <sub>IN</sub> = V <sub>IH</sub> (MAX)		150		150		150			$\mu$ A	
Input Low Current	I <sub>IL</sub>	V <sub>IN</sub> = V <sub>IL</sub> (MIN)	0.5		0.5		0.5				$\mu$ A	
<b>OUTPUTS (Q, <math>\bar{Q}</math>)</b>												
Single-Ended Output High Voltage	V <sub>OH</sub>	Figure 1	V <sub>CC</sub> - 1.135	V <sub>CC</sub> - 0.979	V <sub>CC</sub> - 1.07	V <sub>CC</sub> - 0.959	V <sub>CC</sub> - 0.82	V <sub>CC</sub> - 1.01	V <sub>CC</sub> - 0.947	V <sub>CC</sub> - 0.76	V	
Single-Ended Output Low Voltage	V <sub>OL</sub>	Figure 1	V <sub>CC</sub> - 1.935	V <sub>CC</sub> - 1.721	V <sub>CC</sub> - 1.87	V <sub>CC</sub> - 1.698	V <sub>CC</sub> - 1.62	V <sub>CC</sub> - 1.81	V <sub>CC</sub> - 1.681	V <sub>CC</sub> - 1.56	V	
Differential Output Voltage	V <sub>OH</sub> - V <sub>OL</sub>	Figure 1	550	748	550	741	550	734			mV	
<b>POWER SUPPLY</b>												
Supply Current	I <sub>EE</sub>	(Note 4)		18	26	20	26	22	30		mA	

# Single-Ended-to-Differential LVECL/LVPECL 2:1 Multiplexer

MAX9380

## AC ELECTRICAL CHARACTERISTICS

( $V_{CC} - V_{EE} = +3.0V$  to  $+3.8V$ , outputs loaded with  $50\Omega$  to  $V_{CC} - 2V$ ,  $V_{IH} = V_{CC} - 1.11V$ ,  $V_{IL} = V_{CC} - 1.53V$ , input frequency =  $2.0GHz$ , input transition time =  $125ps$  (20% to 80%). Typical values are at  $V_{CC} - V_{EE} = +3.3V$ , unless otherwise noted.) (Notes 1, 5)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Data Input-to-Output Delay	$t_{PLH1}$ , $t_{PHL1}$	Figure 1	176	258	298	192	263	316	222	277	385	ps
Select Input-to-Output Delay	$t_{PLH2}$ , $t_{PHL2}$	Figure 2	210	304	329	219	308	360	247	318	392	ps
Part-to-Part Skew	$t_{SKPP}$	Data input to output (Note 6)		27	122		33	124		14	163	ps
Added Random Jitter (Note 7)	$t_{RJ}$	$f_{IN} = 3.2GHz$ , clock pattern			1.2		0.2	1.2			1.2	ps (RMS)
Added Deterministic Jitter (Note 7)	$t_{DJ}$	2.0Gbps, $2^{23} - 1$ PRBS			51		36	51			51	ps (p-p)
		3.2Gbps, $2^{23} - 1$ PRBS			77		48	77			77	
Switching Frequency	$f_{MAX}$	Figure 1	$V_{OH} - V_{OL} \geq 300mV$	3.0	3.5		3.0	3.5		3.0	3.5	GHz
			$V_{OH} - V_{OL} \geq 550mV$	2.0			2.0			2.0		
Output Rise/Fall Time (20% to 80%)	$t_R$ , $t_F$	Figure 1	50		96	50		96	50		98	ps

**Note 1:** Measurements are made with the device in thermal equilibrium.

**Note 2:** Current into a pin is defined as positive. Current out of a pin is defined as negative.

**Note 3:** DC parameters are production tested at  $+25^\circ C$ . DC limits are guaranteed by design and characterization over the full operating temperature range.

**Note 4:** All pins are open except  $V_{CC}$  and  $V_{EE}$ .

**Note 5:** Guaranteed by design and characterization. Limits are set to  $\pm 6$  sigma.

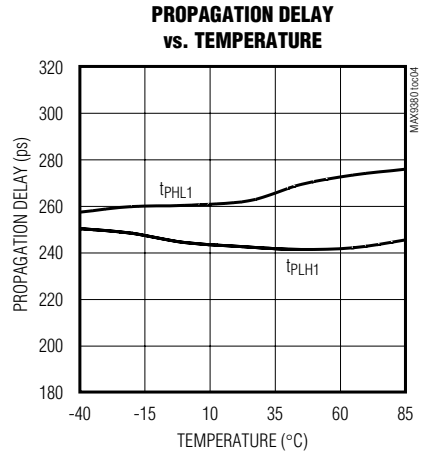
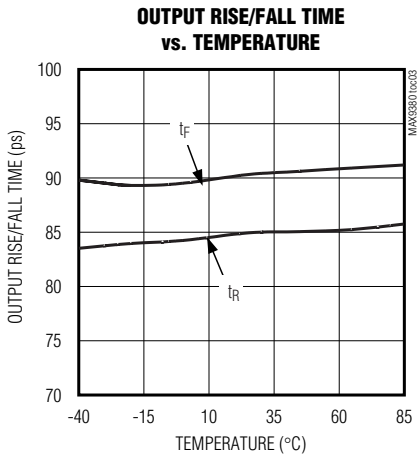
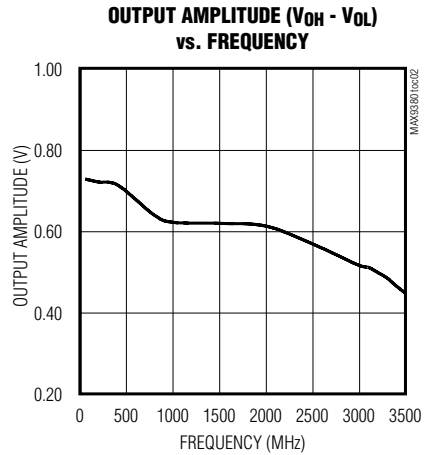
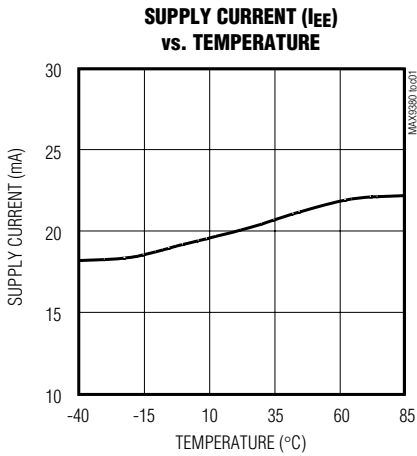
**Note 6:** Measured between outputs of different parts at the signal crossing points under identical conditions for a same-edge transition.

**Note 7:** Device jitter added to the input signal.

# Single-Ended-to-Differential LVECL/LVPECL 2:1 Multiplexer

## Typical Operating Characteristics

( $V_{CC} - V_{EE} = +3.3V$ ,  $V_{IH} = V_{CC} - 1.165V$ ,  $V_{IL} = V_{CC} - 1.475V$ , outputs loaded with  $50\Omega$  to  $V_{CC} - 2.0V$ , input frequency = 1GHz, input transition time = 125ps (20% to 80%), unless otherwise noted.)



# Single-Ended-to-Differential LVECL/LVPECL 2:1 Multiplexer

## Pin Description

MAX9380

PIN	NAME	FUNCTION
1	NC	No Connection. Not internally connected.
2	Da	Single-Ended LVECL/LVPECL Data Input. Da is low default through internal 75kΩ pulldown resistor.
3	Db	Single-Ended LVECL/LVPECL Data Input. Db is low default through internal 75kΩ pulldown resistor.
4	SEL	Single-Ended Control Input. SEL is low default through an internal 75kΩ pulldown resistor selecting Db. Setting SEL to high selects Da.
5	V <sub>EE</sub>	Negative Supply Voltage
6	$\bar{Q}$	Differential LVECL/LVPECL Output. Open Emitter. $\bar{Q}$ is default high when inputs are open.
7	Q	Differential LVECL/LVPECL Output. Open Emitter. Q is default low when inputs are open.
8	V <sub>CC</sub>	Positive Supply Voltage. Bypass V <sub>CC</sub> to V <sub>EE</sub> with 0.1μF and 0.01μF capacitors as close to the device as possible, with the smaller capacitor closest to the IC.
Exposed Paddle	EP	Exposed paddle (MAX9380ESA-EP only). Connect to V <sub>EE</sub> internally. See package dimension.

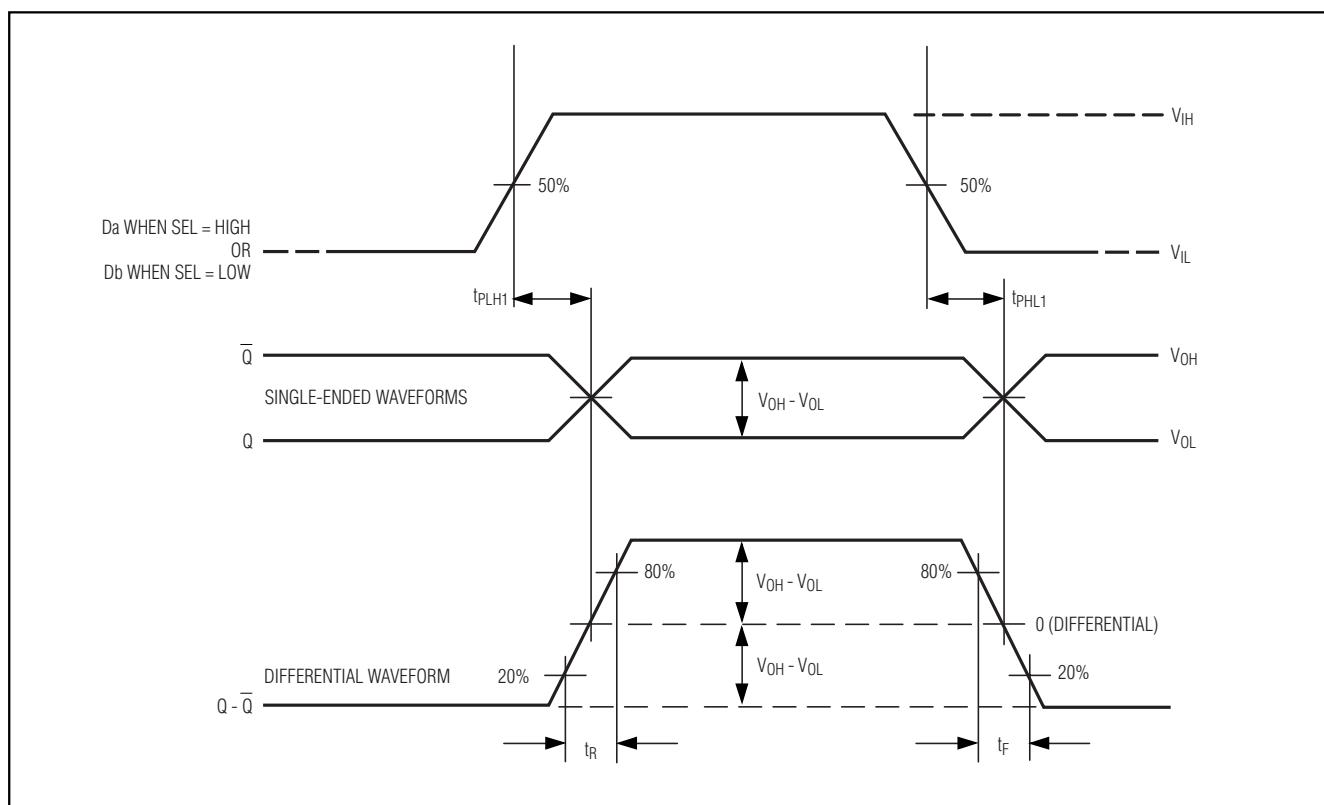


Figure 1. Data Input-to-Output Propagation Delay and Transition Timing Diagram

# Single-Ended-to-Differential LVECL/LVPECL 2:1 Multiplexer

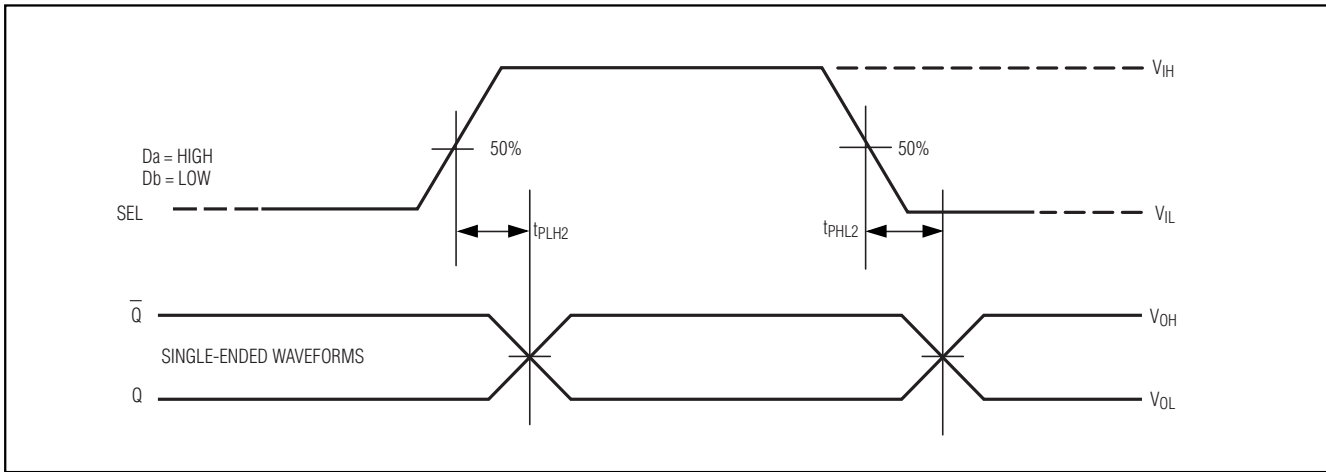


Figure 2. Select Input-to-Output Propagation Delay and Transition Timing Diagram

## Detailed Description

The MAX9380 is a high-speed, low-jitter 2:1 multiplexer designed for clock and data distribution. The device selects one of the two single-ended inputs.

The multiplexer function is controlled by the single-ended SEL input. A high level on the SEL input selects the single-ended data input Da. Similarly, a low level on the SEL input selects the single-ended data input Db. The selected input is converted to a differential signal at the Q and  $\bar{Q}$  outputs.

The inputs Da, Db, and SEL have a 75k $\Omega$  pulldown to V<sub>EE</sub>. This ensures that an open input has a low state. All inputs can be driven from a single-ended LVECL/LVPECL signal or to V<sub>EE</sub> and V<sub>CC</sub>.

## Applications Information

### LVECL/LVPECL

In LVECL systems, the positive supply voltage is conventionally chosen to be system ground. This arrangement produces the best noise immunity since ground is normally a system-wide reference voltage. Operate the MAX9380 with V<sub>CC</sub> = 0 (ground) and V<sub>EE</sub> = -3.3V for an LVECL system.

The MAX9380 operates in LVPECL systems by connecting V<sub>EE</sub> to ground and V<sub>CC</sub> to a positive supply voltage. Connect V<sub>CC</sub> = +3.3V and V<sub>EE</sub> = 0 for an LVPECL system.

## Power-Supply Bypassing

Adequate power-supply bypassing is necessary to maximize the performance and noise immunity. This is particularly true of use in an LVPECL system where the power-supply voltage is used as a reference. Bypass V<sub>CC</sub> to V<sub>EE</sub> with high-frequency surface-mount ceramic 0.1 $\mu$ F and 0.01 $\mu$ F capacitors in parallel as close to the device as possible, with the 0.01 $\mu$ F capacitor closest to the device pins. Use multiple parallel vias for ground plane connection to minimize inductance.

## Circuit Board Traces

Input and output trace characteristics affect the performance of ECL devices. Connect each of the MAX9380 inputs and outputs to a 50 $\Omega$  characteristic impedance trace. Avoid discontinuities in differential impedance and maximize common-mode noise immunity by maintaining the distance between differential traces and avoid sharp corners. Minimize the number of vias to prevent impedance discontinuities. Reduce reflections by maintaining the 50 $\Omega$  characteristic impedance through connectors and across cables. Minimize skew by matching the electrical length of the traces.

## Output Termination

Terminate outputs through 50 $\Omega$  to V<sub>CC</sub> - 2V or use an equivalent Thevenin termination. When a single-ended signal is taken from a differential output, terminate both outputs. For example, if the Q output of the MAX9380 is connected to a single-ended input, terminate both the Q and  $\bar{Q}$  outputs.

# Single-Ended-to-Differential LVECL/LVPECL 2:1 Multiplexer

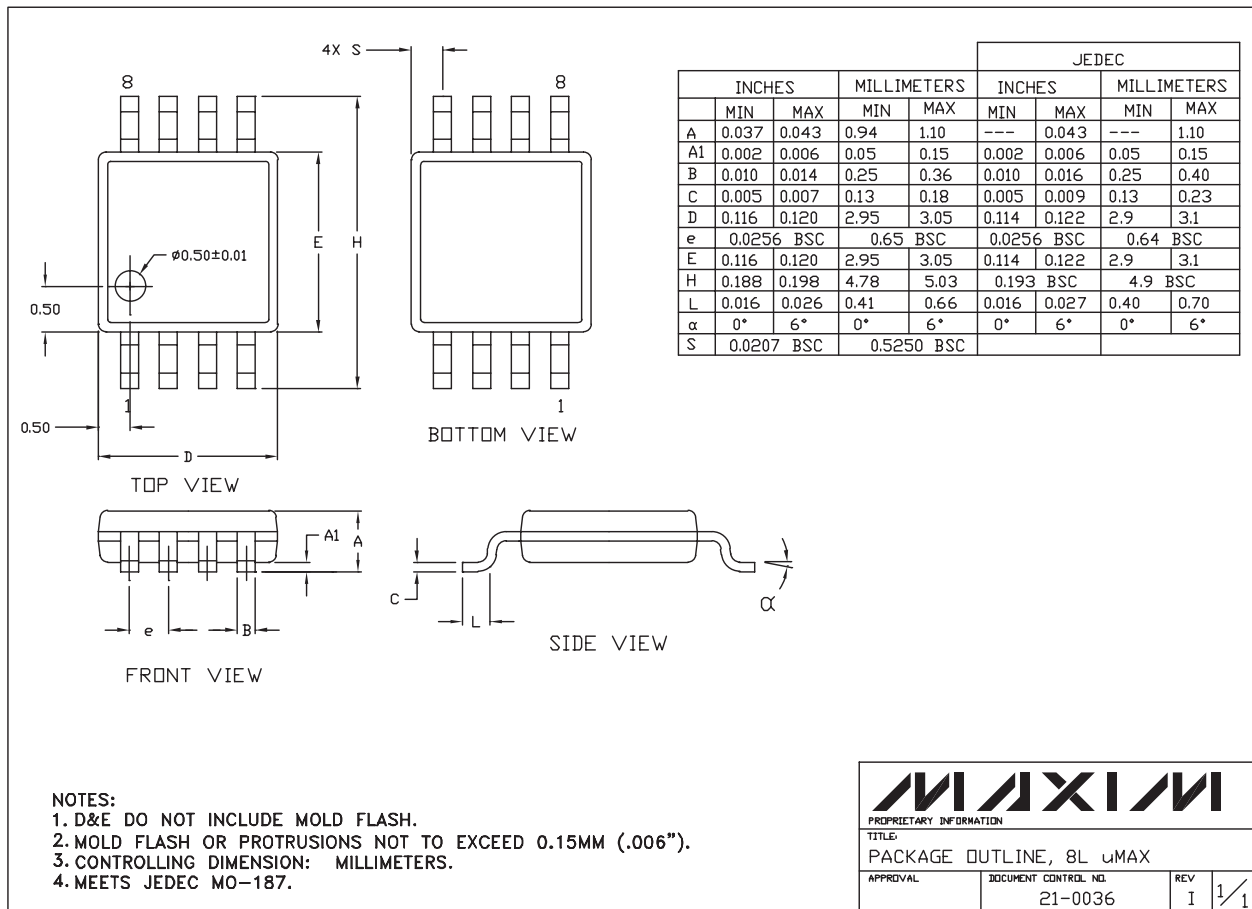
## Chip Information

TRANSISTOR COUNT: 242

PROCESS: Bipolar

## Package Information

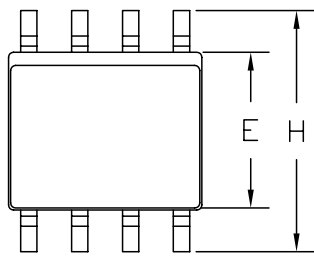
MAX9380



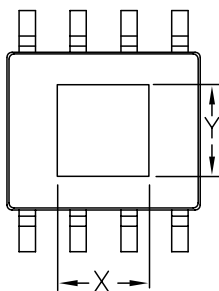
8LUMAXDEPS

# Single-Ended-to-Differential LVECL/LVPECL 2:1 Multiplexer

## Package Information (continued)

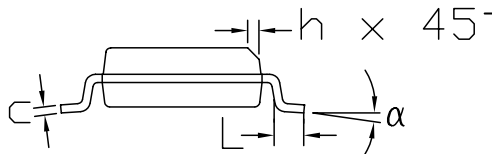
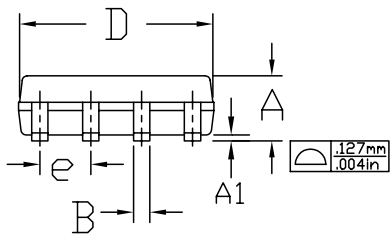


TOP VIEW



BOTTOM VIEW

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
D	0.189	0.197	4.80	5.00
e	0.050	BSC	1.27	BSC
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27
$\alpha$	0°	8°	0°	8°
X	.082	.098	2.08	2.49
Y	.082	.098	2.08	2.49



NOTES:

1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS-012 AA.
5. DIMENSIONS X AND Y DEFINE EXPOSED PAD METAL AREA.

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 PROPRIETARY INFORMATION  
 TITLE PACKAGE OUTLINE  
 8L SOIC, .150" EXPOSED PAD  
 APPROVAL \_\_\_\_\_ DWG 21-0111 REV A 1/1

8L SOIC EXP. PAD EFS

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