# SGS-THOMSON
## MICROELECTRONICS

# MK5027

## SS7 SIGNALLING
## LINK CONTROLLER

- CMOS
- FULLY COMPATIBLE WITH BOTH 8 OR 16 BIT SYSTEMS
- SYSTEM CLOCK RATE TO 10MHz. DATA RATE UP TO 2.5Mbps FOR SS7 PROTOCOL PROCESSING,7Mbps FOR TRANSPARENT HDLC MODE
- COMPLETE LEVEL 2 IMPLEMENTATION
- COMPATIBLE WITH 1988 CCITT, AT&T, ANSI, AND BELLCORE SIGNALLING SYSTEM NUMBER 7 LINK LEVEL PROTOCOLS
- 52 PIN PLCC AND 48-PIN DIP PIN-FOR-PIN COMPATIBLE WITH THE SGS-THOMSON X.25 CHIP (MK5025) AND NEARLY PIN-FOR-PIN COMPATIBLE WITH THE SGS-THOMSON VLANCE CHIP (MK5032)
- BUFFER MANAGEMENT INCLUDES:
  - Initialization Block
  - Separate Receive and Transmit Rings
  - Variable Descriptor Ring and Window Sizes.
- ON CHIP DMA CONTROL WITH PROGRAMMABLE BURST LENGTH
- SELECTABLE BEC OR PCR RETRANSMISSION METHODS, INCLUDING FORCED RETRANSMISSION FOR PCR
- HANDLES ALL 7 SS7 TIMERS
- HANDLES ALL SS7 FRAME FORMATTING:
  - Zero bit insert and delete
  - FCS generation and detection
  - Frame delimiting with flags
- PROGRAMMABLE MINIMUM SIGNAL UNIT SPACING (number of flags between SU's)
- HANDLES ALL SEQUENCING AND LINK CONTROL
- SELECTABLE FCS OF 16 OR 32 BITS.
- TESTING FACILITIES:
  - Internal Loopback
  - Silent Loopback
  - Optional Internal Data Clock Generation
  - Self Test
- ALL INPUTS AND OUTPUTS ARE TTL COMPATIBLE
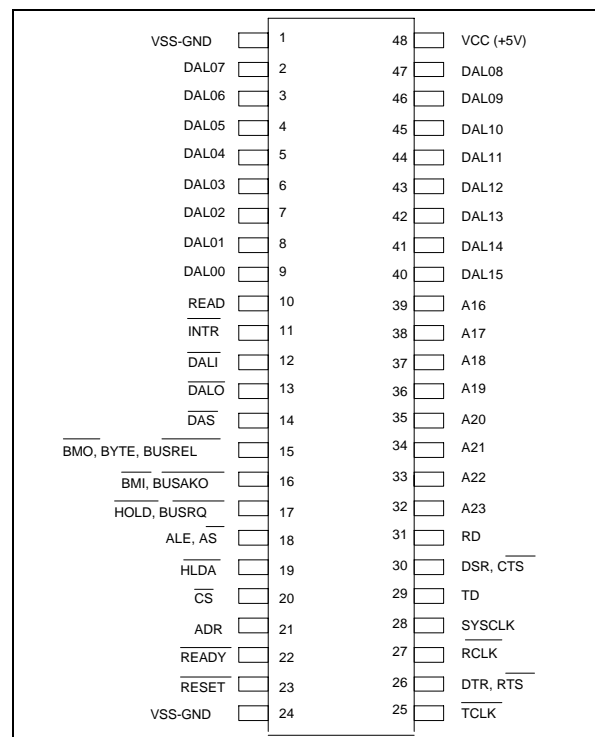- PROGRAMMABLE FOR FULL OR HALF DUPLEX OPERATION

## DESCRIPTION

The SGS-THOMSON Signalling System #7 Signalling Link Controller (MK5027) is a VLSI semi-



**DIP48**          **PLCC52**
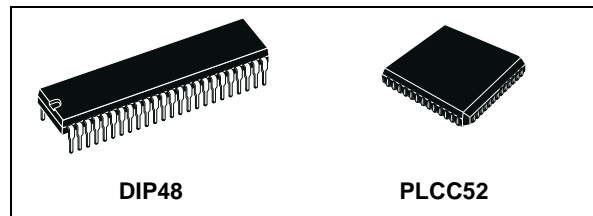
conductor device which provides a complete link control function conforming to the 1988 CCITT version of SS7. This includes frame formatting, transparency (so called "bit-stufling"), error recovery by two types of retransmission, error monitoring, sequence number control, link status control, and FISU generation. One of the outstanding features of the MK5027 is its buffer management which includes on-chip DMA. This feature allows users to handlq multiple packets of receive and transmit data at a time. (A conventional data link-control chip plus a separate DMA chip would handle data for only a single block at a time.) The MK5027 may be used with any of several popular 16 and 8 bit microprocessors, such as 68000, 6800, Z8000, Z80, LSI-11, 8086, 8088, 8080, etc.

**Figure 1:** Pin Connection.



| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | VSS-GND | 48 | VCC (+5V) |
| 2 | DAL07 | 47 | DAL08 |
| 3 | DAL06 | 46 | DAL09 |
| 4 | DAL05 | 45 | DAL10 |
| 5 | DAL04 | 44 | DAL11 |
| 6 | DAL03 | 43 | DAL12 |
| 7 | DAL02 | 42 | DAL13 |
| 8 | DAL01 | 41 | DAL14 |
| 9 | DAL00 | 40 | DAL15 |
| 10 | READ | 39 | A16 |
| 11 | INTR | 38 | A17 |
| 12 | DALI | 37 | A18 |
| 13 | DALO | 36 | A19 |
| 14 | DAS | 35 | A20 |
| 15 | BMO, BYTE, BUSREL | 34 | A21 |
| 16 | BMI, BUSAKO | 33 | A22 |
| 17 | HOLD, BUSRQ | 32 | A23 |
| 18 | ALE, AS | 31 | RD |
| 19 | HLDA | 30 | DSR, CTS |
| 20 | CS | 29 | TD |
| 21 | ADR | 28 | SYSCLK |
| 22 | READY | 27 | RCLK |
| 23 | RESET | 26 | DTR, RTS |
| 24 | VSS-GND | 25 | TCLK |

**Table 1:** Pin Description.
**LEGEND:**

| | | | |
|---|---|---|---|
| I | Input only | O | Output only |
| IO | Input/Output | 3S | 3-State |
| OD | Open Drain (no internal pull-up) | | |

| Signal Name | Pin(s) | Type | Description |
|---|---|---|---|
| DAL<15:00> | 2-9 40-47 | IO/3S | The time multiplexed Data Address bus. During the address portion of a memory transfer, DALe15:00 contains the lower 16 bits of the memory address. During the data portion of a memory transfer, DAL<15:00> contains the read or write data, depending on the type of transfer. |
| READ | 10 | IO/3S | READ indicates the type of operation that the bus controller is performing during a bus transaction. READ is driven by the MK5027 only while it is the BUS MASTER. READ is valid during the entire bus transaction and is tristated at all other times. MK5027 as a Bus Slave: READ = HIGH - Data is placed on the DAL lines by the chip. READ = LOW - Data is taken off the DAL lines by the chip. MK5027 as a Bus Master: READ = HIGH - Data is taken off the DAL lines by the chip. READ = LOW - Data is placed on the DAL lines by the chip. |
| $\overline{\text{INTR}}$ | 11 | O/OD | INTERRUPT is an attention interrupt line that indicates that one or more of the following CSR0 status flags is set: MISS, MERR, RINT, TINT or PINT. INTERRUPT is enabled by CSR0<0.9>, INEA = 1. |
| $\overline{\text{DALI}}$ | 12 | O/3S | DAL IN is an external bus transceiver control line. $\overline{\text{DALI}}$ is driven by the MK5027 only while it is the BUS MASTER. $\overline{\text{DALI}}$ is asserted by the MK5027 when ‌| ads from the DAL lines during the data portion of a READ transfer. $\overline{\text{DALI}}$ is not asserted during a WRITE transfer. |
| $\overline{\text{DALO}}$ | 13 | O/3S | DAL OUT is an external bus transceiver control line. $\overline{\text{DALO}}$ is driven by the MK5027 only while it is the BUS MASTER. $\overline{\text{DALO}}$ is asserted by the MK5027 when it drives the DAL lines during the address portion of a READ transfer or for the duration of a WRITE transfer. |
| $\overline{\text{DAS}}$ | 14 | IO/3S | DATA STROBE defines the data portio,n of a transaction. By definition, data is stable and valid at the low to high transition of $\overline{\text{DAS}}$. This signal is driven by the MK5027 while it is the BUS MASTER. During the BUS SLAVE operation, this pin is used as an input. At all other times the signal is tristated. |
| $\overline{\text{BMO}}$ $\overline{\text{BYTE}}$ $\overline{\text{BUSREL}}$ | 15 | IO/3S | I/O pins 15 and 16 are programmable through CSR4. If bit 06 of CSR4 is set to a one, pin 15 becomes input $\overline{\text{BUSREL}}$ and is used by the host to signal the MK5027 to terminate a DMA burst after the current bus transfer has completed. If bit 06 is clear the pin 15 is an output and behaves as described below for pin 16. |

**Note:** Pin out shown is for 48 pin dip.

**Table 1:** Pin Description (continued)

| Signal Name | Pin(s) | Type | Description |
|---|---|---|---|
| $\overline{BM1}$ $\overline{BUSAKO}$ | 16 | O/3S | Pins 15 and 16 are programmable though bit 00 of CSR4 (BCON). If CSR4<00> BCON = 0,   I/O PIN 15 = BMO (O/3S)   I/O PIN 16 = BM1 (O/3S) BYTE MASK<1:0> indicates the byte(s) on the DAL to be read or written during this bus transaction. MK5027 drives these lines only as a Bus Master. MK5027 ignores the BM lines when it is a Bus Slave. Byte selection is done as outlined in the following table. <br><br> $\overline{BM1}$    $\overline{BM0}$       TYPE OF TRANSFER <br><br> LOW      LOW       ENTIRE WORD <br> LOW      HIGH     UPPER BYTE (DAL<15:08>) <br> HIGH    LOW       LOWER BYTE (DAL<07:00>) <br> HIGH    HIGH     NONE <br> If CSR4<00>BCON = 1,   I/O PIN 15 = $\overline{BYTE}$ (O/3S)   I/O PIN 16 = $\overline{BUSAKO}$(O) Byte selection is done using the BYTE line and DAL<00> latched during the address portion of the bus transaction. MK5027 drives BYTE only a Bus Master and ignores it when a Bus Slave. Byte selection is done as outlined in the following table. <br><br> BYTE     DAL<00>    TYPE OF TRANSFER <br><br> LOW      LOW       ENTIRE WORD <br> LOW      HIGH      ILLEGAL CONDITION <br> HIGH    LOW       LOWER BYTE <br> HIGH    HIGH      UPPER BYTE <br><br> $\overline{BUSAKO}$ is a bus request daisy chain output. If MK5027 is not requesting the bus and it receives HLDA, $\overline{BUSAKO}$ will be driven low. If MK5027 is requesting the bus when it receives HLDA, $\overline{BUSAKO}$ will remain high. Note: All transfers are entire word unless the MK5027 is configured for 8 bit operation. |
| $\overline{HOLD}$ $\overline{BUSRQ}$ | 17 | IO/OD | Pins 17 is configured through bit 0 of CSR4. If CSR4<00> BCON = 0,   I/O PIN 17 = $\overline{HOLD}$ $\overline{HOLD}$ request is asserted by MK5027 when it requires a DMA cycle, if $\overline{HLDA}$ is inactive, regardless of the previous state of the HOLD pin. $\overline{HOLD}$ is held low for the entire ensuing bus transaction. If CSR4<00> BCON = 1,   I/O PIN 17 = $\overline{BUSRQ}$ $\overline{BUSRQ}$ is asserted by MK5027 when it requires a DMA cycle if the prior state of the $\overline{BUSRQ}$ pin was high and $\overline{HLDA}$ is inactive. $\overline{BUSRQ}$ is held low for the entire ensuing bus transaction. |
| $\underline{ALE}$ $\overline{AS}$ | 18 | O/3S | The active level of ADDRESS STROBE is programmable through CSR4. The address portion of a bus transfer occurs while this signal is at its asserted level. This signal is driven by MK5027 while it is the BUS MASTER. At all other times, the signal is tristated. If CSR4<01> ACON = 0,   I/O PIN 18 = ALE ADDRESS LATCH ENABLE is used to demultiplex the DAL lines and define the address portion of the transfer and remains low during the data portion. If CSR4<01> ACON = 1,   I/O PIN 18 = $\overline{AS}$ As $\overline{AS}$, the signal pulses low during the address portion of the bus transfer. The low to high transition of $\overline{AS}$ can be used by a slave device to strobe the address into a register. $\overline{AS}$ is effectively the inversion of ALE. |
| $\overline{HLDA}$ | 19 | I | HOLD AKNOWLEDGE is the response to $\overline{HOLD}$. When $\overline{HLDA}$ is low in response to MK5027's assertion of $\overline{HOLD}$, the MK5027 is the Bus Master. $\overline{HLDA}$ should be desasserted ONLY after $\overline{HOLD}$ has been released by the MK5027. |

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**Table 1:** Pin Description (continued)

| Signal Name | Pin(s) | Type | Description |
|---|---|---|---|
| $\overline{CS}$ | 20 | I | CHIP SELECT indicates, when low, that the MK5027 is the slave device for the data transfer.$\overline{CS}$ must be valid througout the enture transaction. |
| ADR | 21 | I | ADDRESS selects the Register Address Port or the Register Data Port. It must be valid throughout the data portion of the transfer and is only used by the chip when $\overline{CS}$ is low.<br><br>ADR        PORT<br>LOW       REGISTER DATA PORT<br>HIGH       REGISTER ADDRESS PORT |
| $\overline{READY}$ | 22 | IO/OD | When the MK5027 is a Bus Master, $\overline{READY}$ is an asynchronous acknowledgement from the bus memory that memory will accept data in a WRITE cycle or that memory has put data on the DAL lines in a READ cycle.<br>As a bus Slave, the MK5027 asserts $\overline{READY}$ when it has put data on the DAL lines during a READ cycle or is about to take data from the DAL lines during WRITE cycle. $\overline{READY}$ is a response to $\overline{DAS}$ and it will be released after $\overline{DAS}$ or $\overline{CS}$ is negated. |
| $\overline{RESET}$ | 23 | I | $\overline{RESET}$ is the Bus signal that will cause MK5027 to cease operation, clear its internal logic and enter an idle state with the Power Off bit of CSR0 set. |
| $\overline{TCLK}$ | 25 | I | TRANSMIT CLOCK. A 1x clock input for transmitter timing. TD changes on the falling edge of $\overline{TCLK}$. The frequency of $\overline{TCLK}$ may not be greater than the frequency of SYSCLK. |
| $\frac{DTR}{\overline{RTS}}$ | 26 | IO | DATA TERMINAL READY, REQUEST TO SEND. Modem control pin. Pin 26 is configurable through CSR5. This pin can be programmed to behave as output $\overline{RTS}$ or as programmable IO pin DTR. If configured as $\overline{RTS}$, the MK5027 will assert this pin if it has data to send and throughout the transmission of a signal unit. |
| $\overline{RCLK}$ | 27 | I | RECEIVE CLOCK. A 1x clock input for receiver timing. RD is sampled on the rising edge of $\overline{RCLK}$. The frequency of $\overline{RCLK}$ may not be greater than the frequency of SYSCLK. |
| SYSCLK | 28 | I | SYSTEM CLOCK. System clock used for internal timing of the MK5027. SYSCLK should be a square wave, of frequency up to 10MHz. |
| TD | 29 | O | TRANSMIT DATA. Transmit serial data output. |
| $\frac{DSR}{\overline{CTS}}$ | 30 | IO | DATA SET READY, CLEAR TO SEND. Modem Control Pin. Pin 30 is configurable through CSR5. This pin can be programmed to behave as input $\overline{CTS}$ or as programmable IO pin DSR. If configured as $\overline{CTS}$, the MK5027 will transmit all ones while $\overline{CTS}$ is high. |
| RD | 31 | I | RECEIVE DATA. Received serial data input. |
| A<23:16> | 32-39 | O/3S | Address bits <23:16> used in conjunction with DAL <15:00> to produce a 24 bit address. MK5027 drives these lines only as a Bus Master.<br>A23-A20 may be driven continuously as described in the CSR4<7> BAEN bit. |
| VSS-GND | 1, 24 | | Ground Pins |
| VCC | 48 | | Power Supply Pin<br>+5.0 VDC $\pm$ 5% |

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**Figure 2:** Possible System Configuration for the MK5027.
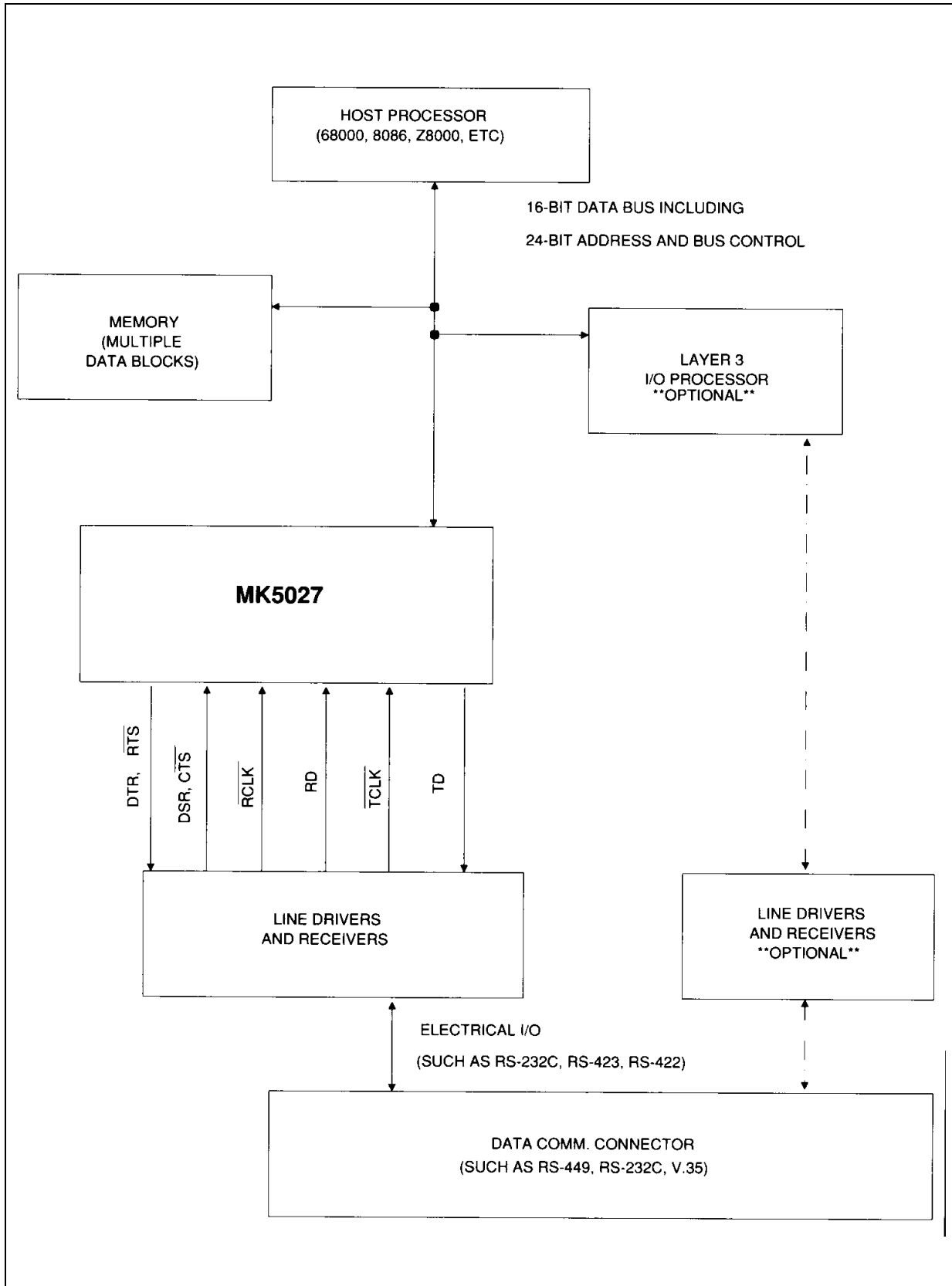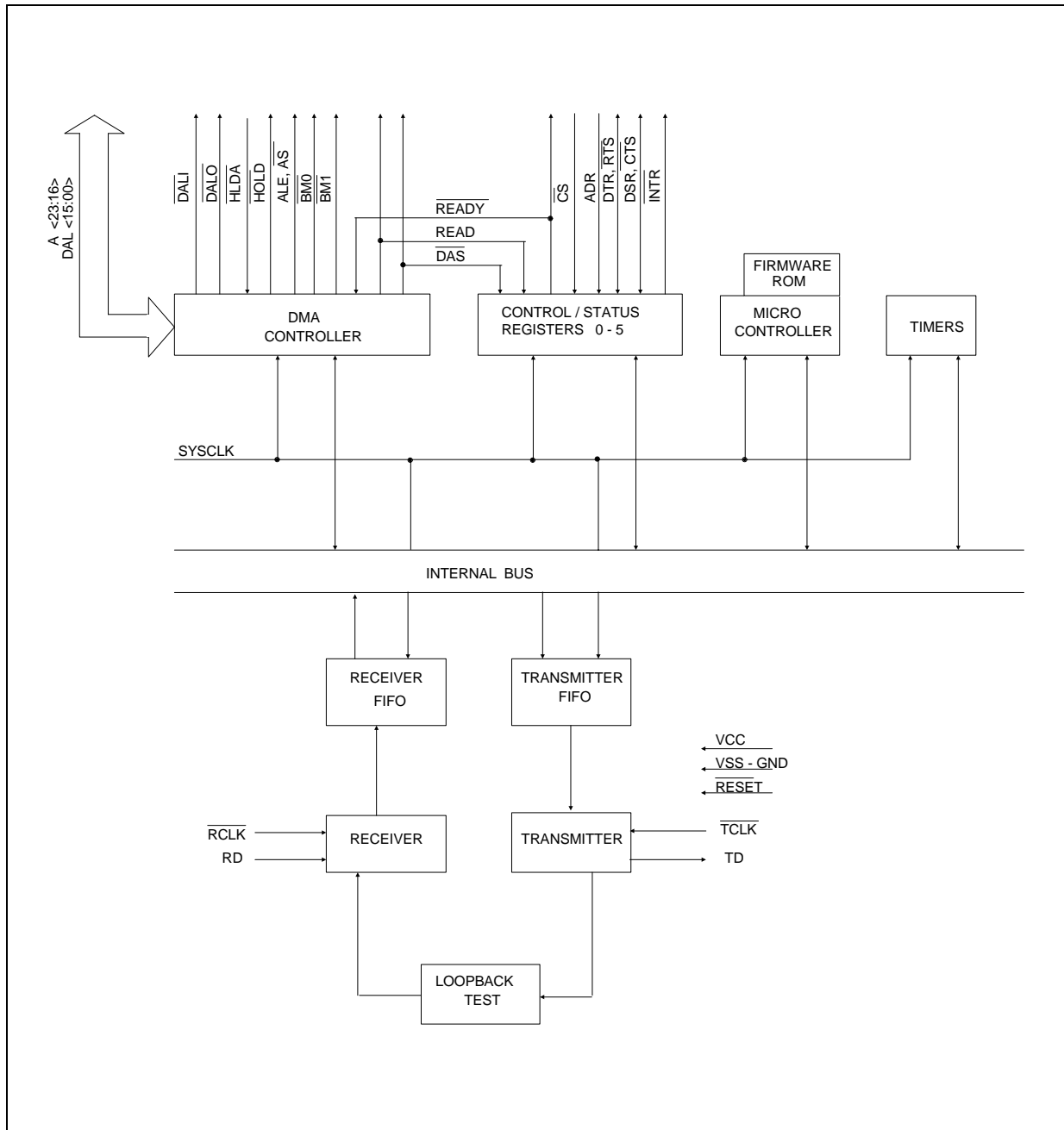
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**Figure 3:** MK5027 Simplified Block Diagram.



## OPERATIONAL DECRIPTION

The SGS-THOMSON Signalling System #7 Signalling Link Controller (MK5027) device is a VLSI product intended for data communication applications requiring SS7 link level control. The MK5027 will perform all frame formatting, such as: frame delimiting with flags, FCS generation and detection. It will also perform all error recovery and link control. The MK5027 also includes a buffer management mechanism that allow the user to transmit and/or receive multiple MSU's. Contained in the buffer management is an on-chip dual chan-nel DMA: one channel for receive and one chan-nel for transmit. The MK5027 handles error recovery and link status signalling.

The MK5027 is intended to be used with any popular 16 or 8 bit microprocessor. Possible system configuration for the MK5027 is shown in Figure 2. The MK5027 will move multiple blocks of receive and transmit data directly into and out of memory through the host's bus. An I/O acceleration processor in Figure 2 is recommended, but not required.

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All signal pins on the MK5027 are TTL compatible. This has the advantage of making the MK5027 in- dependent of the physical interface. As shown in Figure 2. line drivers and receivers are used for electrical- connection to the physical layer.

## SERIAL INTERFACE

The MK5027 provides two separate serial channels: one for received data and one for transmitted data. These serial channels are completely separate and may be run at different clock frequencies The receiver is responsible for recognizing frame boundries. removal of inserted zeroes (for transparency) and checking the incoming FCS. Signal units with in correct FCS values are discarded. The receiver also parallelizes the incoming data which is placed into the receive data buffers within the receive descriptor ring The transmitter is responsible for framing and serializing the data frames placed in the transmit descriptor ring. The transmitter calculates the FCS of the outgoing data and appends it to the data The transmitter generates flag sequences for inter-signal unit fill, at least two flags are transmitted between adjacent signal units. The FCS calculations for both directions of serial data optionally follow either the 16 bit CRC CCITT or the 32-bit CRC 32 algorithms FCS generation and checking can also be optionally disabled if necessary.

## MICROPROCESSOR INTERFACE

The MK5027 contains a dual channel DMA on chip to handle data transfers to and from the host mem- ory. All access to the initialization block and descriptor rings is handled in this way The address bus is 24 bits wide and does not use any segmentation or paging methods. Data transfers can optionally be 8 and 16 bit operations. this allows easy interfacing with both 8 and 16 bit processors DMA transfers can be up to 1. 8 or an unlimited number of words per transfer under program control During bus slave operation the

MK5027 allows access to its 6 control/status registers which are used to monitor and control the chip. These registers are used to control link procedures, configure interface options, control and monitor interrupt status. and more. Bus slave mode also allows both 8 and 16 bit accesses.

## BUFFER MANAGEMENT

The basic organization of the buffer management is a circular queue of tasks in memory called descriptor rings. There are separate rings to describe the transmit and receive operations. Up to 128 buffers may be queued-up on a descriptor ring awaiting execution by the MK5027 The descriptor ring has a segment assigned to each buffer. Each segment holds a pointer for the starting address of the buffer. and holds a value for the length of the buffer in bytes.

Each segment also contains two control bits called OWNA and OWNB, which denote whether the MK5027. the HOST. or the I/O ACCELERATION PROCESSOR (if present) "owns" the buffer. For transmit. when the MK5027 owns the buffer. the MK5027 is allowed and commanded to transmit the buffer When the MK5027 does not own the buffer, it will not transmit that buffer. For receive. when the MK5027 owns a buffer. it may place received data into that buffer. Conversely. when the MK5027 does not own a receive buffer, it will not place received data in that buffer.

The MK5027 buffer management mechanism will handly signal units which are longer than the length of an individual buffer. This is done by a chaining method which utilizes multiple buffers. The MK5027 tests the next segment in the descriptor ring in a "look ahead" manner. If the packet is too long for one buffer, the next buffer will be used after filling the first buffer: that is, "chained". The MK5027 will then "look ahead" to the next buffer, and chain that buffer if necessary, and so on The operational parameters for the buffer management are defined by the user in the initialization block The parameters defined include the basic mode of operation. the number of entries for the transmitter and receiver descriptor rings. etc.

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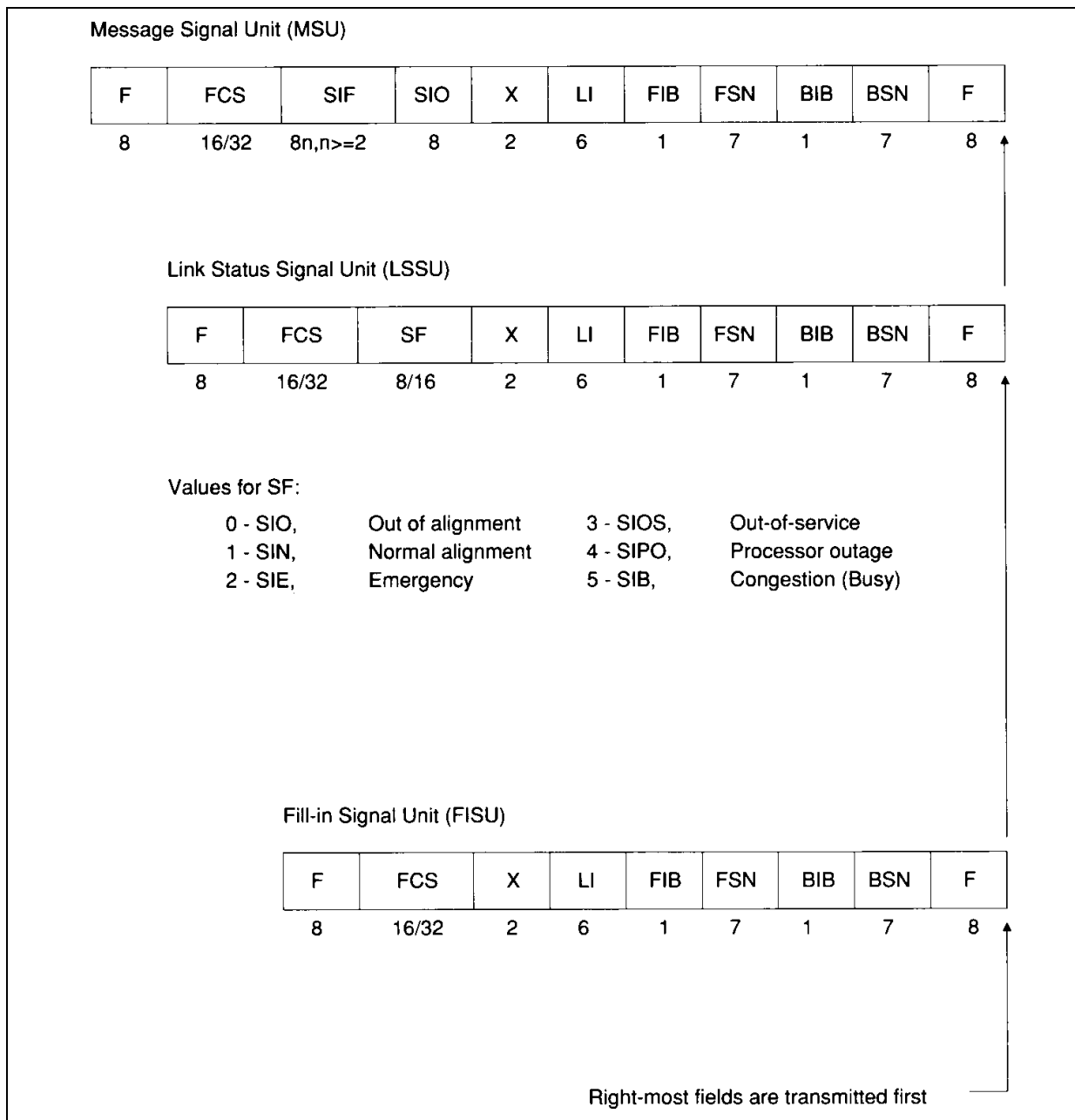**MICROELECTRONICS**

**Figure 4:** MK5027 Buffer Management.
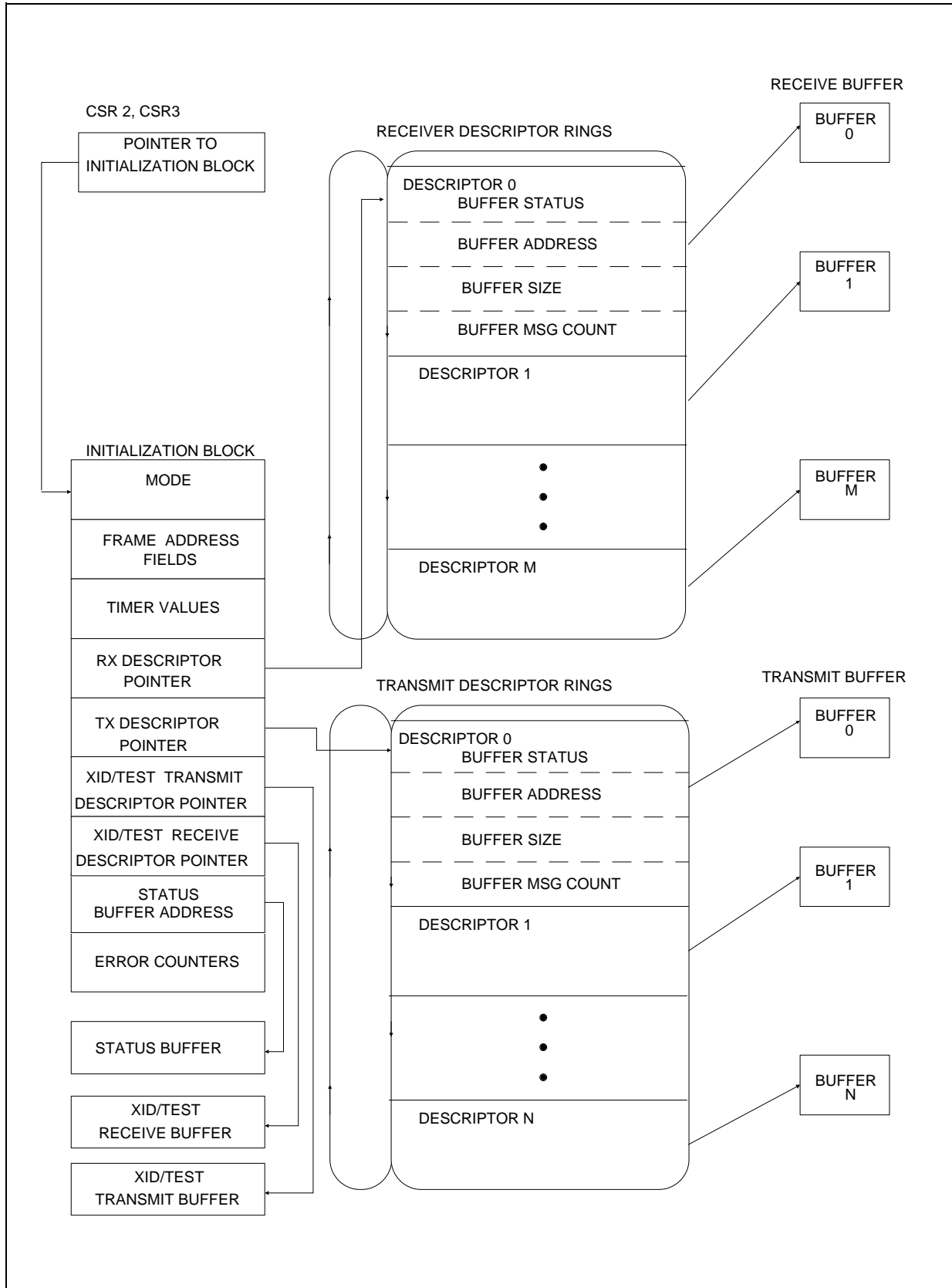
## SIGNALLING UNIT REPERTOIRE

The signal unit repertoire of the MK5027 is shown in Table 1. This set conforms to the 1988 CCITT specification for level 2 of Signalling System #7.

The definitions for the symbols for the frame types are:

| Name | Definition |
|------|------------|
| F | Flag Sequence |
| FSN | Forward Sequence Number |
| BSN | Backward Sequences Number |
| FIB | Forward Indicator Bit |
| BIB | Backward Indicator Bit |
| LI | Lenght Indicator |
| X | Programmed As Zeroes |
| SIO | Signalling Information Octet |
| SIF | Service Information Field |
| SF | Satus Field |
| FCS | Frame Check Sequence |

**Table 1:** MK5027 Signal Unit Repertoire.

Message Signal Unit (MSU)

| F | FCS | SIF | SIO | X | LI | FIB | FSN | BIB | BSN | F |
|---|-----|-----|-----|---|----|-----|-----|-----|-----|---|
| 8 | 16/32 | 8n,n>=2 | 8 | 2 | 6 | 1 | 7 | 1 | 7 | 8 |

Link Status Signal Unit (LSSU)

| F | FCS | SF | X | LI | FIB | FSN | BIB | BSN | F |
|---|-----|-----|---|----|-----|-----|-----|-----|---|
| 8 | 16/32 | 8/16 | 2 | 6 | 1 | 7 | 1 | 7 | 8 |

Values for SF:

| 0 - SIO, | Out of alignment | 3 - SIOS, | Out-of-service |
|----------|------------------|-----------|----------------|
| 1 - SIN, | Normal alignment | 4 - SIPO, | Processor outage |
| 2 - SIE, | Emergency | 5 - SIB, | Congestion (Busy) |

Fill-in Signal Unit (FISU)

| F | FCS | X | LI | FIB | FSN | BIB | BSN | F |
|---|-----|---|----|-----|-----|-----|-----|---|
| 8 | 16/32 | 2 | 6 | 1 | 7 | 1 | 7 | 8 |

Right-most fields are transmitted first

## MK5027 ELECTRICAL SPECIFICATIONS
## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Temperature under Bias | −25°C to +100°C |
| Storage Temperature | −65°C to +150°C |
| Voltage on Any Pin with Respect to Ground | −0.5V to VCC +0.5V |
| Power Dissipation | 0.50W |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the above device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affectdevice reliability.

## DC CHARACTERISTICS
$T_A$=0 °C to 70 °C, $V_{CC}$ = +5V ±5 percent unless otherwise specified.

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $V_{IL}$ | | -0.5 | | +0.8 | V |
| $V_{IH}$ | | +2.0 | | $V_{CC}$ +0.5 | V |
| $V_{OL}$ | @ IOL = 3.2 mA | | | +0.5 | V |
| $V_{OH}$ | @ IOH= -0.4 mA | +2.4 | | | V |
| $I_{IL}$ | @ VIN = 0.4 to $V_{CC}$ | | | +10 | mA |
| $I_{CC}$ | @ TSCT = 100 ns | | 50 | | µA |

## CAPACITANCE
f = 1MHz

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $C_{IN}$ | Capacitance on Input pins | | | 10 | pF |
| $C_{OUT}$ | Capacitance on Output Pins | | | 10 | pF |
| $C_{IO}$ | Capacitance on I/O pins | | | 20 | pF |

## AC TIMING SPECIFICATIONS
$T_A$ = 0 °C to 70 °C, $V_{CC}$ = +5V ±5 percent, unless otherwise specified.

| No | Signal | Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| 1 | SYSCLK | $T_{SCT}$ | SYSCLK period | | 100 | | 20000 | ns |
| 2 | SYSCLK | $T_{SCL}$ | SYSCLK low time | | 45 | | | ns |
| 3 | SYSCLK | $T_{SCH}$ | SYSCLK high time | | 45 | | | ns |
| 4 | SYSCLK | $T_{SCR}$ | Rise time of SYSCLK | | 0 | | 8 | ns |
| 5 | SYSCLK | $T_{SCF}$ | Fall time of SYSCLK | | 0 | | 8 | ns |
| 6 | $\overline{TCLK}$ | $T_{TCT}$ | $\overline{TCLK}$ period | | 140 | | | ns |
| 7 | $\overline{TCLK}$ | $T_{TCL}$ | $\overline{TCLK}$ low time | | 63 | | | ns |
| 8 | $\overline{TCLK}$ | $T_{TCH}$ | $\overline{TCLK}$ high time | | 63 | | | ns |
| 9 | $\overline{TCLK}$ | $T_{TCR}$ | Rise time of $\overline{TCLK}$ | CL = 50 pF | 0 | | 8 | ns |
| 10 | $\overline{TCLK}$ | $T_{TCF}$ | Fall time of $\overline{TCLK}$ | | 0 | | 8 | ns |
| 11 | TD | $T_{TDP}$ | TD data propagation delay after the falling edge of $\overline{TCLK}$ | CL = 50 pF | | | 40 | ns |
| 12 | TD | $T_{TDH}$ | TD data hold time after the falling edge of $\overline{TCLK}$ | | 5 | | | ns |

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**AC TIMING SPECIFICATIONS** (Continued)

$T_A = 0\ °C$ to $70\ °C$, $V_{CC} = +5V\ \pm 5$ percent, unless otherwise specified.

| No | Signal | Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Units |
|----|--------|--------|-----------|-----------------|------|------|------|-------|
| 13 | $\overline{RCLK}$ | $T_{RCT}$ | $\overline{RCLK}$ period | | 140 | | | ns |
| 14 | $\overline{RCLK}$ | $T_{RCH}$ | $\overline{RCLK}$ high time | | 63 | | | ns |
| 15 | $\overline{RCLK}$ | $T_{RCL}$ | $\overline{RCLK}$ low time | | 63 | | | ns |
| 16 | $\overline{RCLK}$ | $T_{RCR}$ | Rise time of $\overline{RCLK}$ | | 0 | | 8 | ns |
| 17 | $\overline{RCLK}$ | $T_{RCF}$ | Fall time of $\overline{RCLK}$ | | 0 | | 8 | ns |
| 18 | RD | $T_{RDR}$ | RD data rise time | | 0 | | 8 | ns |
| 19 | RD | $T_{RDF}$ | RD data fall time | | 0 | | 8 | ns |
| 20 | RD | $T_{RDH}$ | RD hold time after rising edge of $\overline{RCLK}$ | | 5 | | | ns |
| 21 | RD | $T_{RDS}$ | RD setup time prior to rising edge of $\overline{RCLK}$ | | 30 | | | ns |
| 22 | A/DAL | $T_{DOFF}$ | Bus Master driver disable after rising edge of $\overline{HOLD}$ | | 0 | | 50 | ns |
| 23 | A/DAL | $T_{DON}$ | Bus Master driver enable after falling edge of $\overline{HLDA}$ | TSCT = 100ns | 0 | | 200 | ns |
| 24 | $\overline{HLDA}$ | $T_{HHA}$ | Delay to falling edge of $\overline{HLDA}$ from falling edge of $\overline{HOLD}$ (Bus Master) | | 0 | | | ns |
| 25 | $\overline{RESET}$ | $T_{RW}$ | $\overline{RESET}$ pulse width | | 30 | | | ns |
| 26 | A/DAL | $T_{CYCLE}$ | Read/write, address/data Cycle Time | TSCT = 100ns | 600 | | | ns |
| 27 | A | $T_{XAS}$ | Address setup time to falling edge of ALE | | 100 | | | ns |
| 28 | A | $T_{XAH}$ | Address hold time after the rising edge of $\overline{DAS}$ | | 50 | | | ns |
| 29 | DAL | $T_{AS}$ | Address setup time to falling edge of ALE | | 75 | | | ns |
| 30 | DAL | $T_{AH}$ | Address hold time after the falling edge of ALE | | 20 | | | ns |
| 31 | DAL | $T_{RDAS}$ | Data setup time to the falling edge of $\overline{DAS}$ (Bus Master read) | | 55 | | | ns |
| 32 | DAL | $T_{RDAH}$ | Data hold time after the rising edge of $\overline{DAS}$ (bus master read) | | 0 | | | ns |
| 33 | DAL | $T_{DDAS}$ | Data setup time to the falling edge of $\overline{DAS}$ (bus master write) | | 0 | | | ns |
| 34 | DAL | $T_{WDS}$ | Data setup time to the rising edge of $\overline{DAS}$ (bus master write) | | 250 | | | ns |
| 35 | DAL | $T_{WDH}$ | Data hold time to the rising edge of $\overline{DAS}$ (bus slave write) | | 35 | | | ns |
| 36 | DAL | $T_{SRDH}$ | Data hold time after the rising edge of $\overline{DAS}$ (bus slave read) | TSCT = 100ns | 0 | | 35 | ns |
| 37 | DAL | $T_{SWDH}$ | Data hold time after the rising edge of DAS (bus slave write) | | 0 | | | ns |
| 38 | DAL | $T_{SWDS}$ | Data setup time to the falling edge of $\overline{DAS}$ (bus slave write) | | 0 | | | ns |
| 39 | ALE | $T_{ALEW}$ | ALE width high | | 110 | | | ns |
| 40 | ALE | $T_{DSW}$ | Delay from rising edge od $\overline{DAS}$ to the rising edge of ALE | | 70 | | | ns |
| 41 | DAS | $T_{DSW}$ | $\overline{DAS}$ width low | | 200 | | | ns |

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## AC TIMING SPECIFICATIONS (Continued)
$T_A = 0\ °C$ to $70\ °C$, $V_{CC} = +5V\ \pm 5$ percent, unless otherwise specified.

| No | Signal | Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| 42 | $\overline{DAS}$ | $T_{ADAS}$ | Delay from the falling edge of ALE to the falling edge of $\overline{DAS}$ | | 80 | | | ns |
| 43 | $\overline{DAS}$ | $T_{RIDF}$ | Delay from the rising edge of DALO to the falling edge of $\overline{DAS}$ (bus master read) | | 35 | | | ns |
| 44 | $\overline{DAS}$ | $T_{RDYS}$ | Delay from the falling edge of $\overline{READY}$ to the falling edge of $\overline{DAS}$ | $T_{ARYD} = 300ns$ $T_{SCT} = 100ns$ | 120 | | 200 | ns |
| 45 | $\overline{DALI}$ | $T_{ROIF}$ | Delay from the rising edge of $\overline{DALO}$ to the falling edge of $\overline{DALI}$ (bus master read) | | 70 | | | ns |
| 46 | $\overline{DALI}$ | $T_{RIS}$ | $\overline{DALI}$ setup time to the rising edge of $\overline{DAS}$ (bus master read) | | 150 | | | ns |
| 47 | $\overline{DALI}$ | $T_{RIH}$ | $\overline{DALI}$ hold time after the rising edge of $\overline{DAS}$ (bus master read) | | 0 | | | ns |
| 48 | $\overline{DALI}$ | $T_{RIOF}$ | Delay from the rising edge of $\overline{DALI}$ to the falling edge of $\overline{DALO}$ (bus master read) | | 70 | | | ns |
| 49 | $\overline{DALO}$ | $T_{OS}$ | $\overline{DALO}$ setup time to the falling edge of ALE (bus master read) | | 110 | | | ns |
| 50 | $\overline{DALO}$ | $T_{ROH}$ | $\overline{DALO}$ hold time after the falling edge of ALE (bus master read) | | 35 | | | ns |
| 51 | $\overline{DALO}$ | $T_{WDSI}$ | Delay from the rising edge of $\overline{DAS}$ to the rising edge of DALO (bus master write) | | 50 | | | ns |
| 52 | $\overline{CS}$ | $T_{CSH}$ | $\overline{CS}$ hold time after the rising edge of $\overline{DAS}$ (bus slave) | | 0 | | | ns |
| 53 | $\overline{CS}$ | $T_{CSS}$ | $\overline{CS}$ setup time to the falling edge of $\overline{DAS}$ (bus slave) | | 0 | | | ns |
| 54 | $\overline{ADR}$ | $T_{SAH}$ | $\overline{ADR}$ hold time after the rising edge of DAS (bus slave) | | 0 | | | ns |
| 55 | $\overline{ADR}$ | $T_{SAS}$ | $\overline{ADR}$ setup time to the falling edge of $\overline{DAS}$ (bus slave) | | 0 | | | ns |
| 56 | $\overline{READY}$ | $T_{ARYD}$ | Delay from the falling edge of ALE to the falling edge of $\overline{READY}$ to Insure a Minimum Bus Cycle Time (600ns) | $T_{SCT} = 100ns$ | | | 150 | ns |
| 57 | $\overline{READY}$ | $T_{SRDS}$ | Data setup time to the falling edge of $\overline{READY}$ (bus slave read) | | 75 | | | ns |
| 58 | $\overline{READY}$ | $T_{RDYH}$ | $\overline{READY}$ hold time after the rising edge of $\overline{DAS}$ (bus master) | | 0 | | | ns |
| 59 | $\overline{READY}$ | $T_{SRYH}$ | $\overline{READY}$ hold time after the rising edge of $\overline{DAS}$ (bus slave) | $T_{SCT} = 100ns$ | 0 | | 35 | ns |
| 60 | $\overline{READY}$ | $T_{RSH}$ | READ hold time after rhe rising edge of $\overline{DAS}$ (bus slave) | | 0 | | | ns |
| 61 | READ | $T_{SRS}$ | READ setup time after rhe rising edge of $\overline{DAS}$ (bus slave) | | 0 | | | ns |
| 62 | $\overline{READY}$ | $T_{RDYD}$ | Delay from falling edge of $\overline{DAS}$ to falling edge of $\overline{READY}$ (bus slave) | $T_{SCT} = 100ns$ | | 200 | | ns |

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**Figure 5A:** TTL Output Load Diagram.  **Figure 5B:** Open Drain Output Load Diagram.
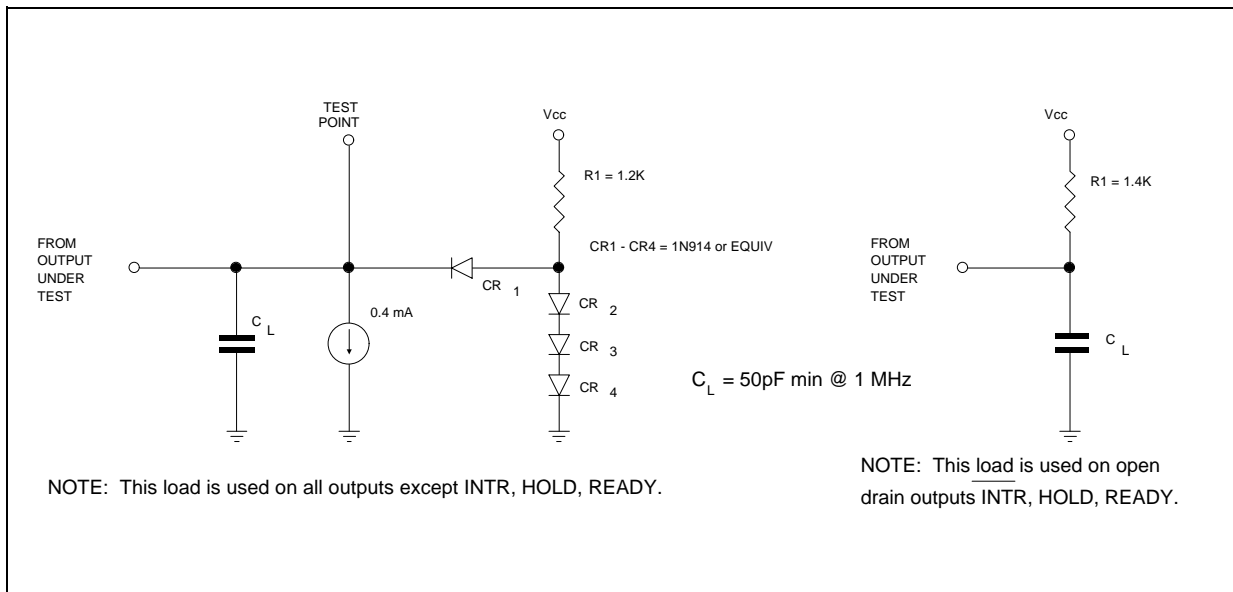


**Figure 6:** MK5027 Serial Link Timing Diagram

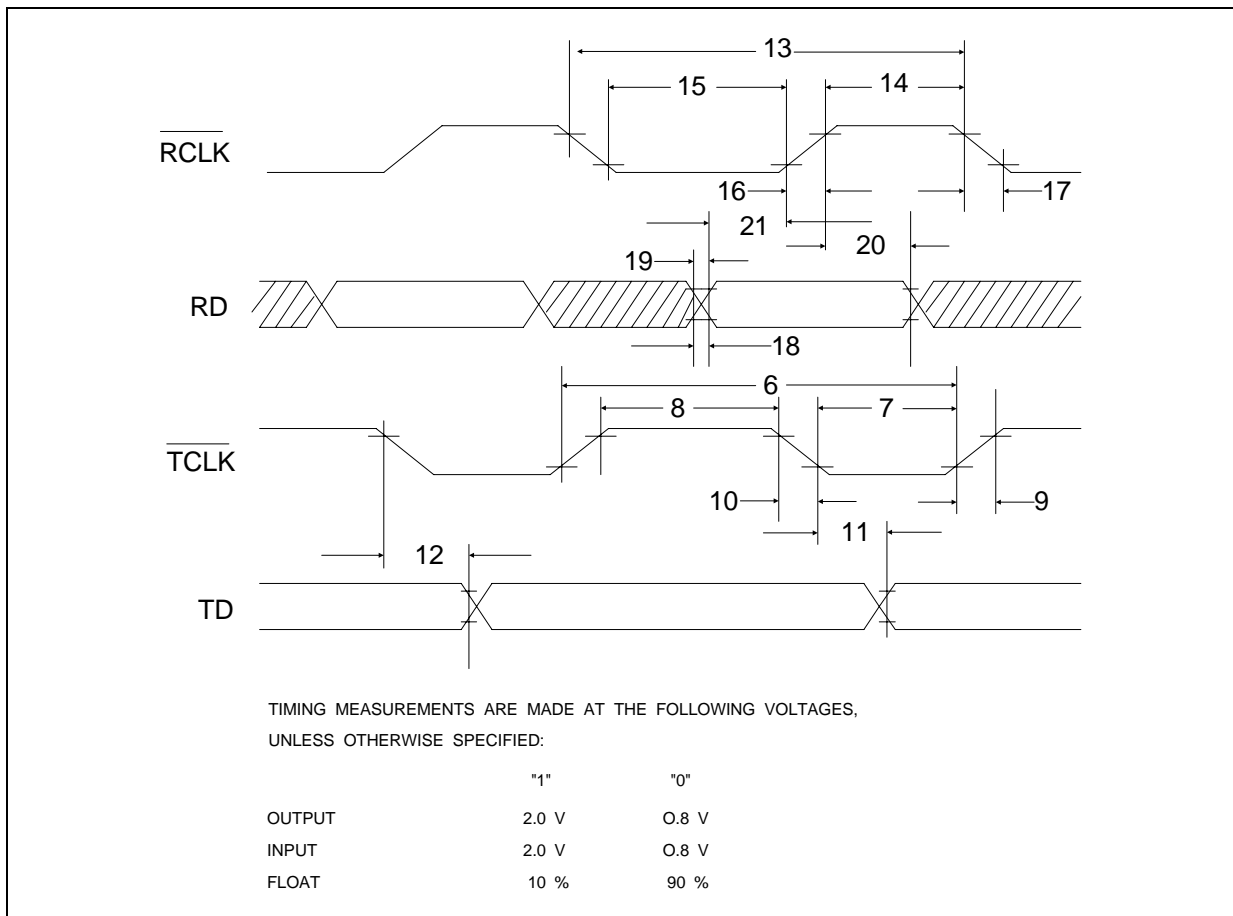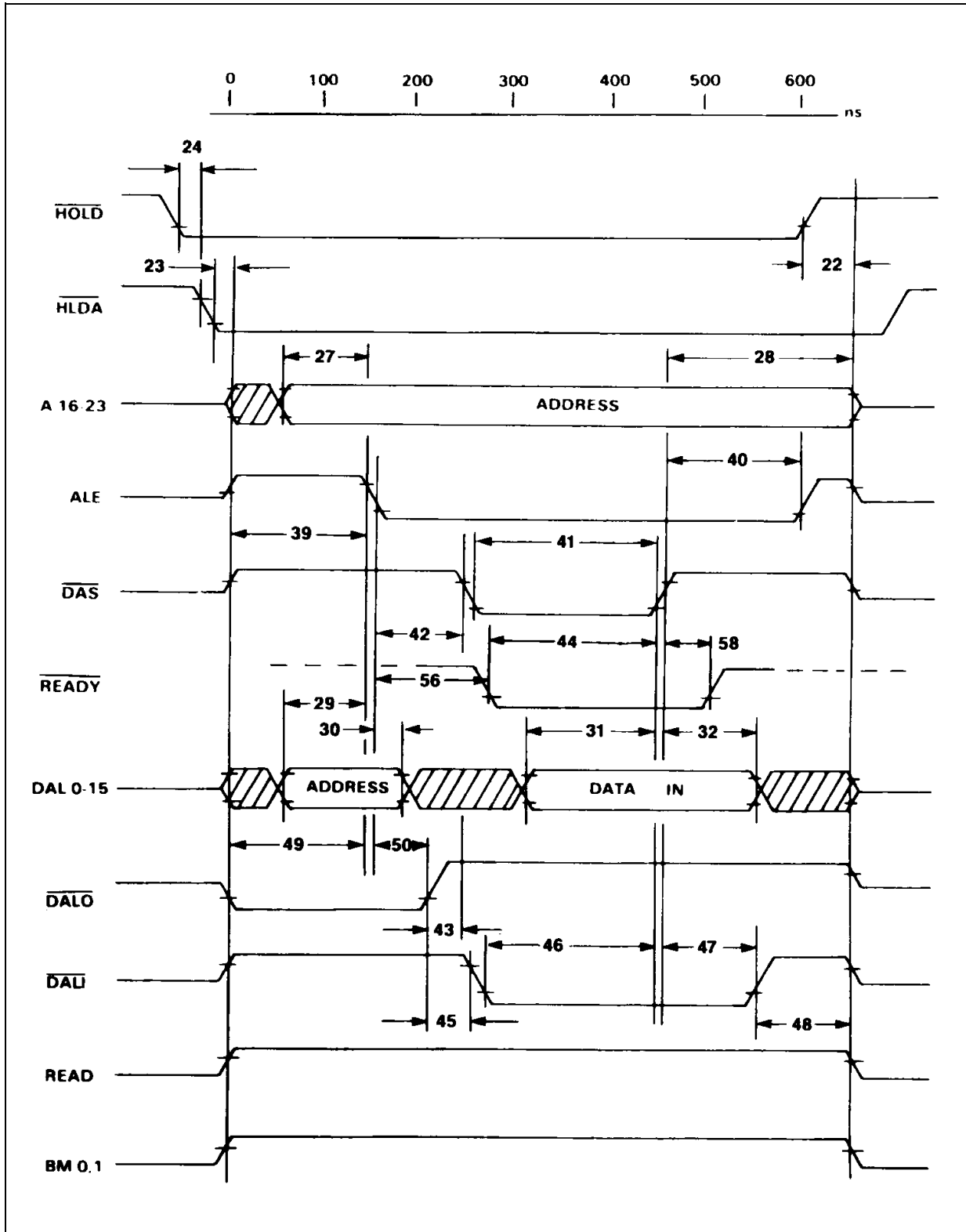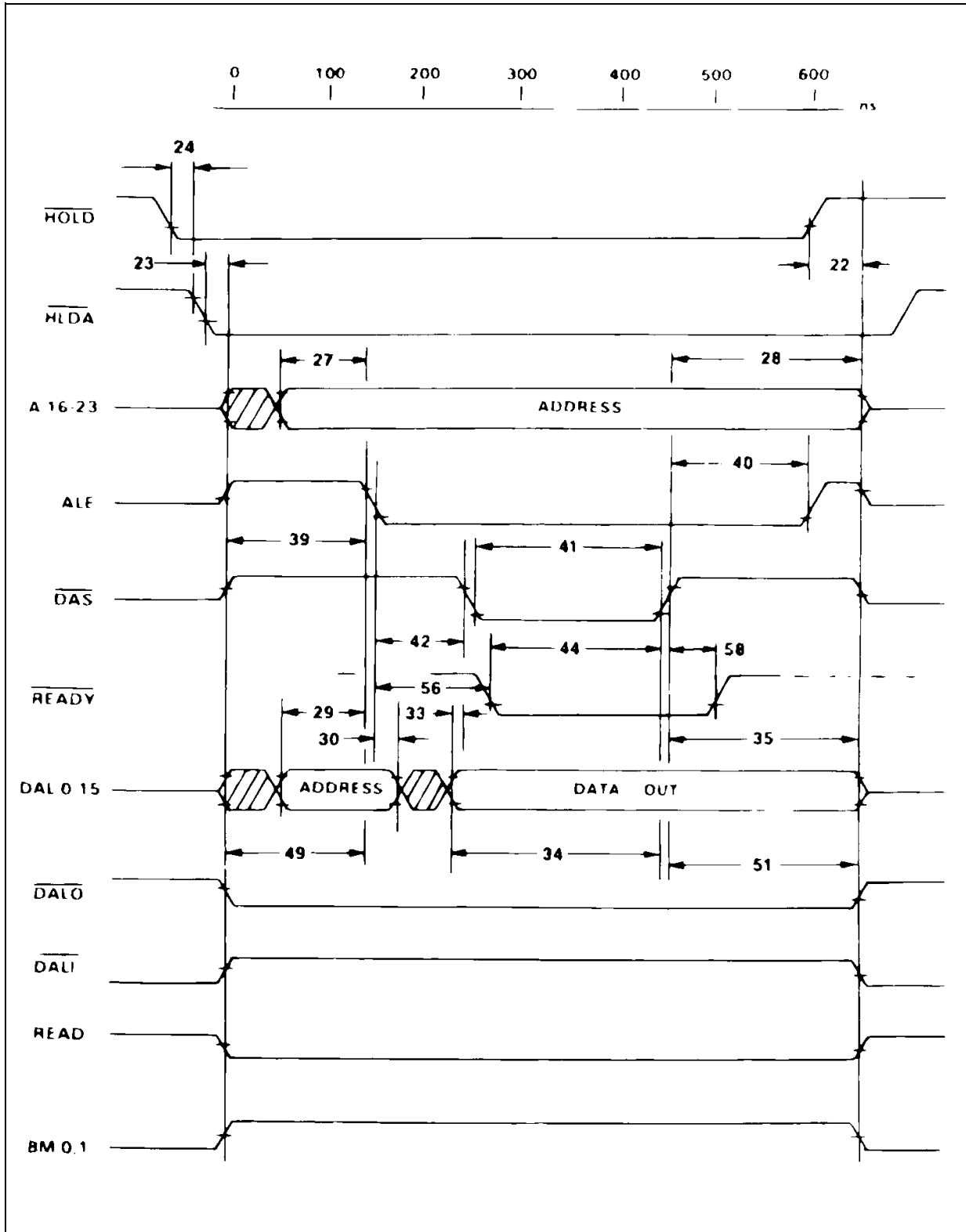**SGS-THOMSON**
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**Figure 7:** MK5027 Bus Master Timing Diagram (read).



**Note:** The Bus Master cycle time will increase from a minimum of 600ns in 100ns steps until the slave device return READY.

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**Figure 8:** MK5027 Bus Master Timing Diagram (write).



**Note:** The Bus Master cycle time will increase from a minimum of 600ns in 100ns steps until the slave device return READY.

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**Figure 9:** MK5027 Bus Slave Timing Diagram (read)
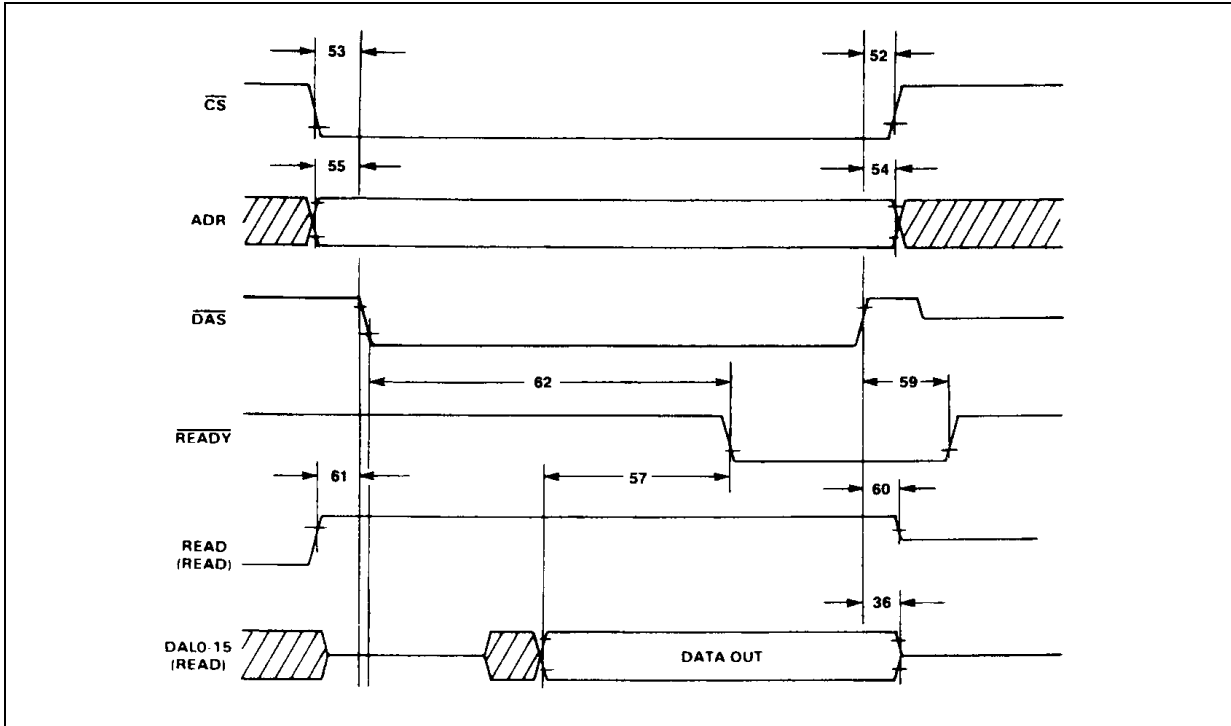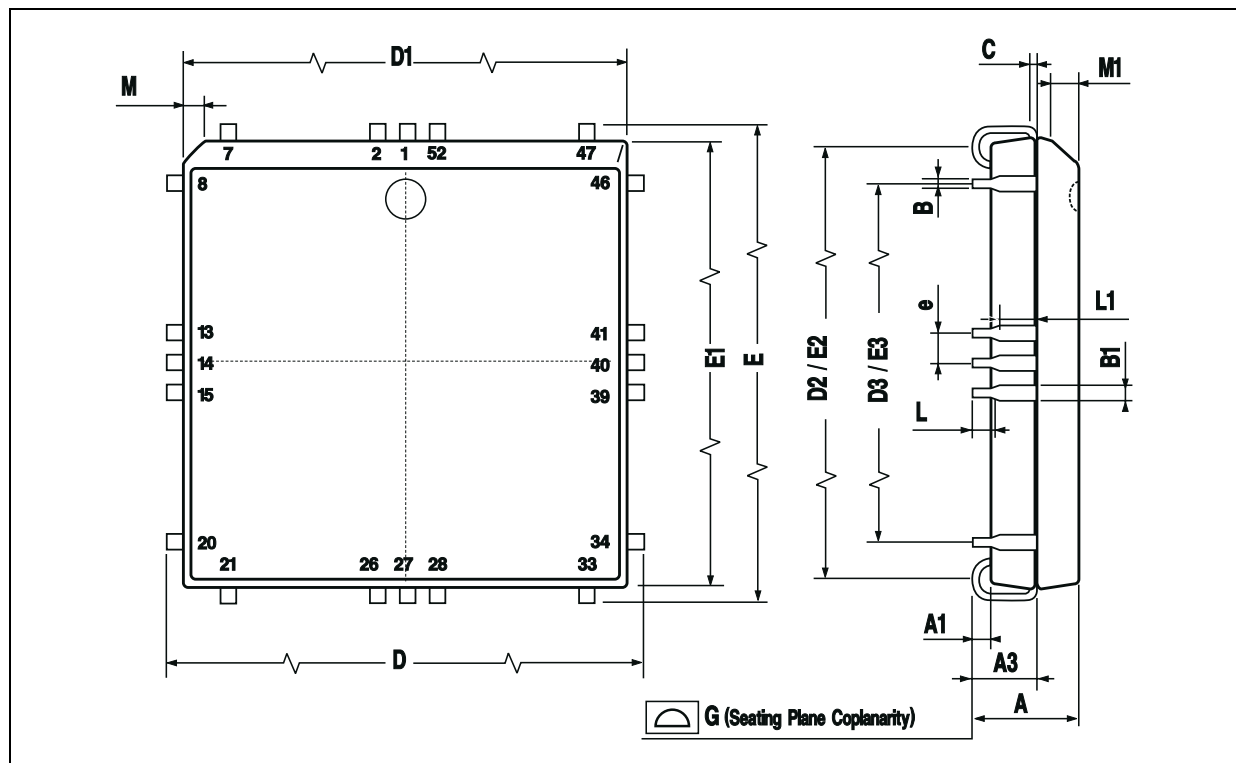


**Figure 10:** MK5027 Bus Slave Timing Diagram (write)

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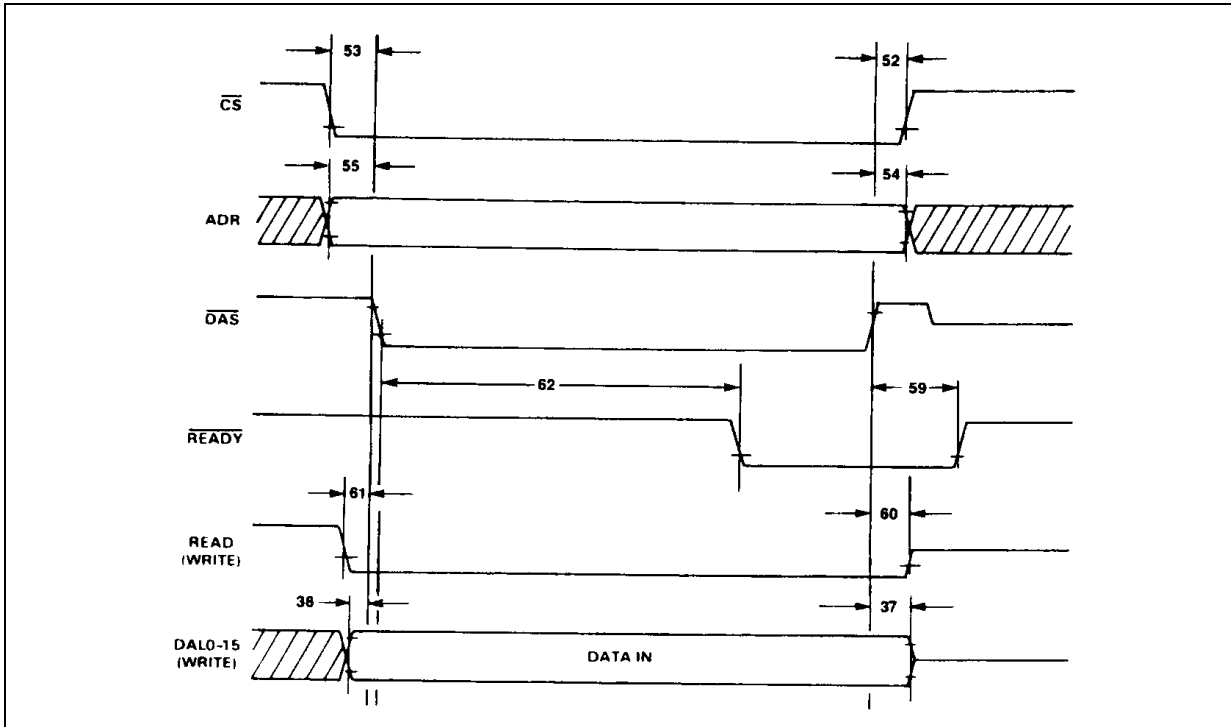
**DIP48 PACKAGE MECHANICAL DATA**

| DIM. | mm | | | inch | | |
|------|------|------|------|------|------|------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| a1 | | 0.63 | | | 0.025 | |
| b | | 0.45 | | | 0.018 | |
| b1 | 0.23 | | 0.31 | 0.009 | | 0.012 |
| b2 | | 1.27 | | | 0.050 | |
| D | | | 62.74 | | | 2.470 |
| E | 15.2 | | 16.68 | 0.598 | | 0.657 |
| e | | 2.54 | | | 0.100 | |
| e3 | | 58.42 | | | 2.300 | |
| F | | | 14.1 | | | 0.555 |
| I | | 4.445 | | | 0.175 | |
| L | | 3.3 | | | 0.130 | |

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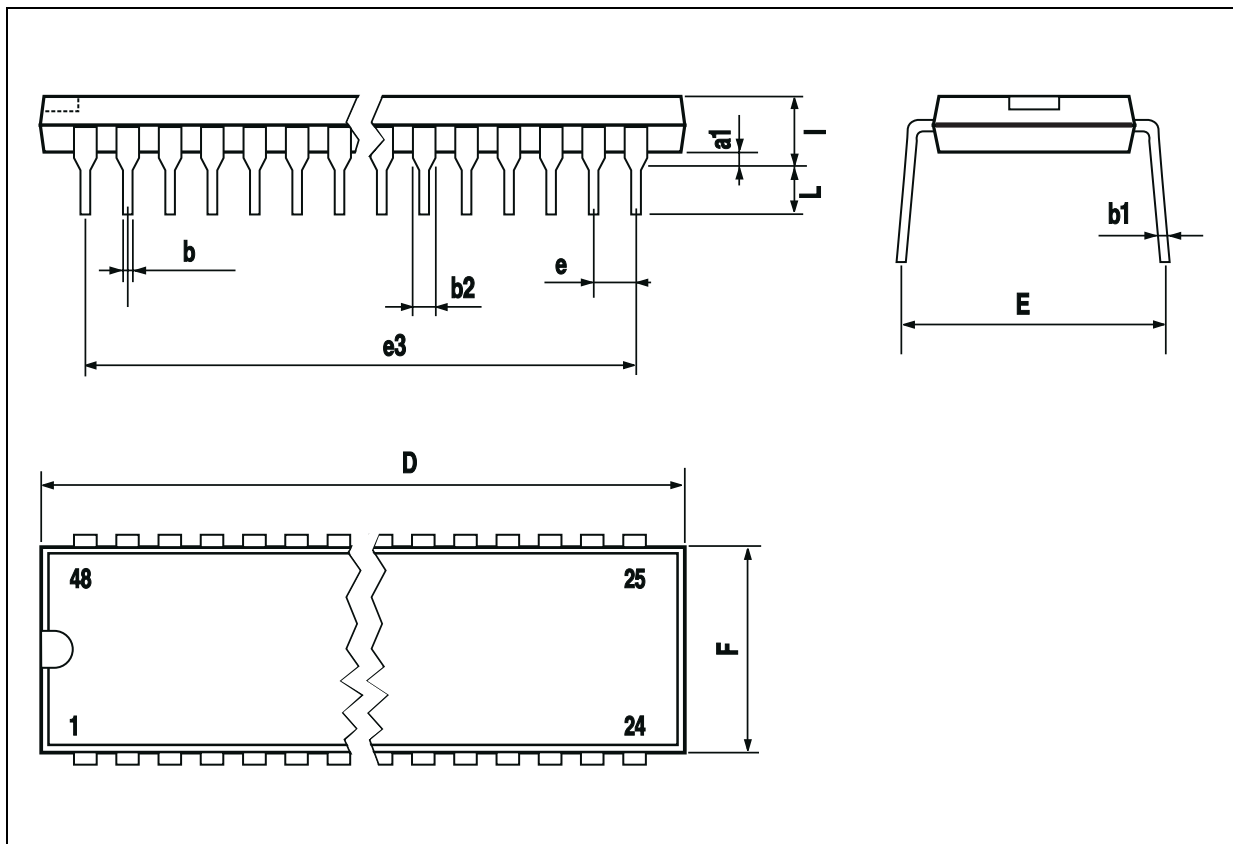
## PLCC52 PACKAGE MECHANICAL DATA

| DIM. | mm | | | inch | | |
|------|-----|-----|-----|-----|-----|-----|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | 4.20 | 5.08 | | 0.165 | 0.20 |
| A1 | | 0.51 | | | 0.020 | |
| A3 | | 2.29 | 3.30 | | 0.090 | 0.13 |
| B | | 0.33 | 0.53 | | 0.013 | 0.021 |
| B1 | | 0.66 | 0.81 | | 0.026 | 0.032 |
| C | 0.25 | | | 0.01 | | |
| D | | 19.94 | 20.19 | | 0.785 | 0.795 |
| D1 | | 19.05 | 19.20 | | 0.750 | 0.756 |
| D2 | | 17.53 | 18.54 | | 0.690 | 0.730 |
| D3 | 15.24 | | | 0.60 | | |
| E | | 19.94 | 20.19 | | 0.785 | 0.795 |
| E1 | | 19.05 | 19.20 | | 0.750 | 0.756 |
| E2 | | 17.53 | 18.54 | | 0.690 | 0.730 |
| E3 | 15.24 | | | 0.60 | | |
| e | 1.27 | | | 0.05 | | |
| L | | 0.64 | | | 0.025 | |
| L1 | | 1.53 | | | 0.060 | |
| M | | 1.07 | 1.22 | | 0.042 | 0.048 |
| M1 | | 1.07 | 1.42 | | 0.042 | 0.056 |

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