DDR2 Configurable Registered Buffer

Features:

- Compatible with JEDEC standard SSTU32864
- Differential Clock inputs
- SSTL_18 Clock and data input signaling
- Output circuitry minimizes effects of SSO and unterminated lines
- LVCMOS input levels on control and $\overline{\text{RESET}}$ pins
- 1.7V-1.9V Supply voltage range.
- Max Clock frequency > 300MHz

Applications:

- PC3200/4300 DDR2 memory modules
- 1:1 25-bit or 1:2 14-bit configurable registered buffer
- 1.8V data registers

General Description

The SLGSSTU32864 is a configurable registered buffer designed for 1.7V to 1.9V VDD operating range. When C1 input pin is low, the SLGSSTU32864 is 1:1 25-bit configuration. When C1 input pin is high, the SLGSSTU32864 is 1:2 14-bit configuration. Additionally, C0 input pin controls the 1:2 pinout as register-A configuration (if low) , and register-B configuration (if high). The C0,C1, and $\overline{\text{RESET}}$ pins are LVCMOS input levels.The C0,C1 input pins are not intended to be switched dynamically during normal operation. They should be tied to logic high or low levels to configure the register.

Data propagation from D to Q is controlled by the differential clock (CLK/$\overline{\text{CLK}}$) and a control signals. The rising edge of CLK (crossing with $\overline{\text{CLK}}$ falling) is used to register the Data. All inputs are SSTL_18 except C0,C1, and $\overline{\text{RESET}}$ pins.

The SLGSSTU32864 supports low-power standby operation. Setting $\overline{\text{RESET}}$ pin to a logic “low” disables (CLK/$\overline{\text{CLK}}$) receivers, and allows floating inputs to all other receivers as well (D, V_{REF} , CLK/$\overline{\text{CLK}}$). Additionally, all internal registers are reset, and outputs (Q) are set “low”. $\overline{\text{RESET}}$ input pin must always be driven to a valid logic state “high” or “low”.

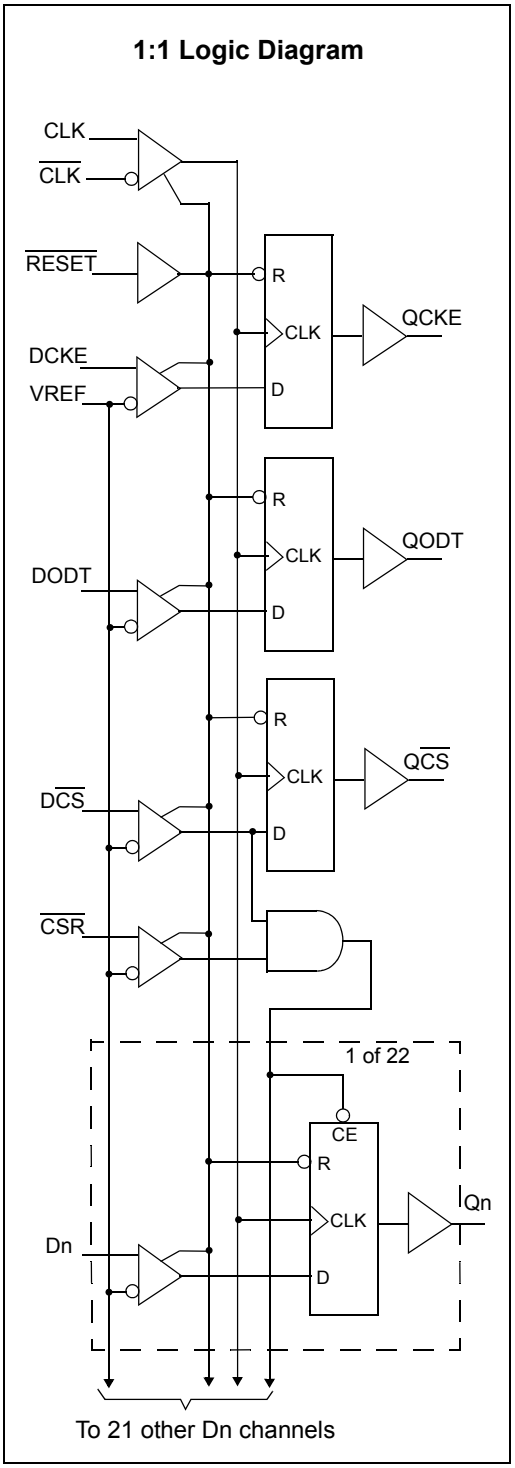
$\overline{\text{RESET}}$, an LVCMOS asynchronous signal, is also intended for use at the time of power-up. $\overline{\text{RESET}}$ must be held at a logic “low” level during power up. This ensures defined outputs before a stable CLK/$\overline{\text{CLK}}$ is supplied.

The SLGSSTU32864 supports low-power active operation as it monitors $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ inputs. The Qn outputs will be prevented from changing states when both $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ inputs are high. The Qn outputs will be allowed to change state if either one of $\overline{\text{DCS}}$ or $\overline{\text{CSR}}$ inputs is low. If $\overline{\text{DCS}}$ control is not desired, then $\overline{\text{CSR}}$ input should be held low. In that case, the setup and hold times of $\overline{\text{DCS}}$ is the same as the other D inputs.

Ordering Information:

Package type	Package suffix	Topside marking	Ordering code
LFBGA-96ball 13.5 X 5.5 mm body	X	SLGSSTU32864EX	SLGSSTU32864EX-TR (2,000 pcs/tape and reel)
LFBGA-96ball 13.5 X 5.5 mm body	X	SLGSSTU32864EX	SLGSSTU32864EX (2,000 pcs/tray)

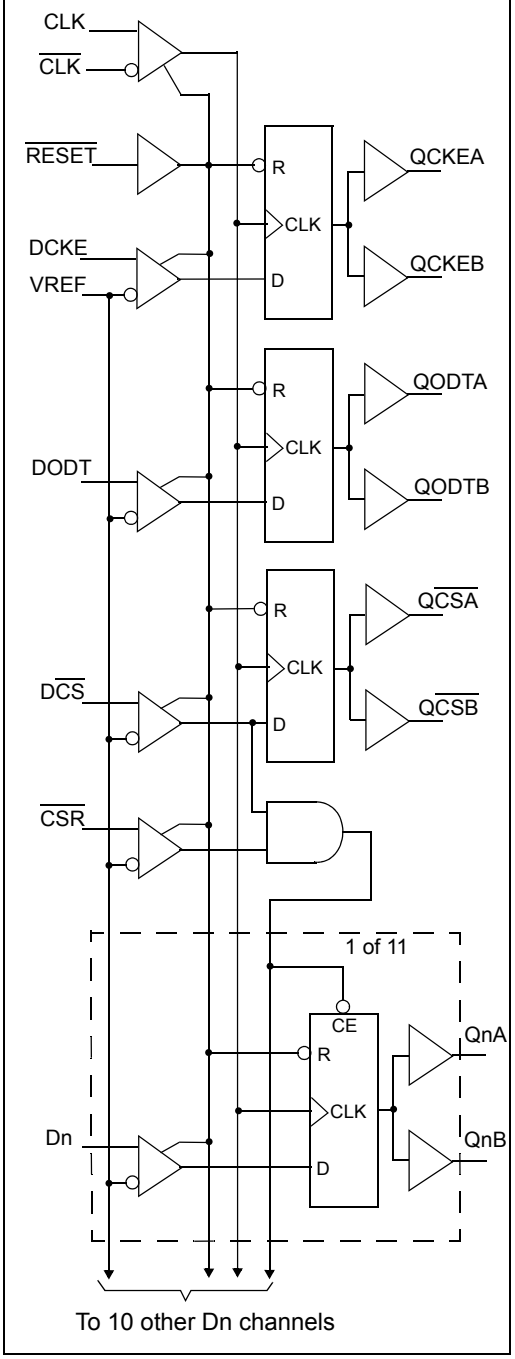
1:1 Logic Diagram



SLGSSTU32864 top view pinout, 1:1 (C0=0,C1=0)

	1	2	3	4	5	6
A	DCKE	NC	VREF	VDD	QCKE	DNU
B	D2	D15	GND	GND	Q2	Q15
C	D3	D16	VDD	VDD	Q3	Q16
D	DODT	NC	GND	GND	QODT	DNU
E	D5	D17	VDD	VDD	Q5	Q17
F	D6	D18	GND	GND	Q6	Q18
G	NC	$\overline{\text{RESET}}$	VDD	VDD	C1	C0
H	CLK	$\overline{\text{DCS}}$	GND	GND	$\overline{\text{QCS}}$	DNU
J	$\overline{\text{CLK}}$	$\overline{\text{CSR}}$	VDD	VDD	ZOH	ZOL
K	D8	D19	GND	GND	Q8	Q19
L	D9	D20	VDD	VDD	Q9	Q20
M	D10	D21	GND	GND	Q10	Q21
N	D11	D22	VDD	VDD	Q11	Q22
P	D12	D23	GND	GND	Q12	Q23
R	D13	D24	VDD	VDD	Q13	Q24
T	D14	D25	VREF	VDD	Q14	Q25

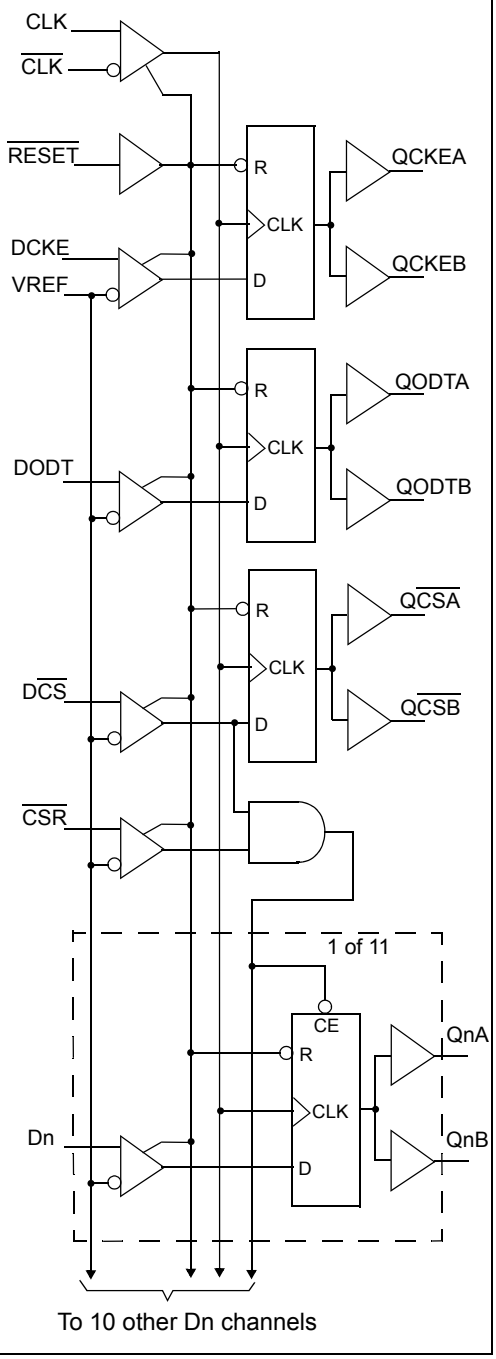
1:2 "A"- configuration Logic Diagram



SLGSSTU32864 top view pinout, 1:2 "A"(C0=0,C1=1)

	1	2	3	4	5	6
A	DCKE	NC	VREF	VDD	QCKEA	QCKEB
B	D2	DNU	GND	GND	Q2A	Q2B
C	D3	DNU	VDD	VDD	Q3A	Q3B
D	DODT	NC	GND	GND	QODTA	QODTB
E	D5	DNU	VDD	VDD	Q5A	Q5B
F	D6	DNU	GND	GND	Q6A	Q6B
G	NC	$\overline{\text{RESET}}$	VDD	VDD	C1	C0
H	CLK	$\overline{\text{DCS}}$	GND	GND	$\overline{\text{QCSA}}$	$\overline{\text{QCSB}}$
J	$\overline{\text{CLK}}$	$\overline{\text{CSR}}$	VDD	VDD	ZOH	ZOL
K	D8	DNU	GND	GND	Q8A	Q8B
L	D9	DNU	VDD	VDD	Q9A	Q9B
M	D10	DNU	GND	GND	Q10A	Q10B
N	D11	DNU	VDD	VDD	Q11A	Q11B
P	D12	DNU	GND	GND	Q12A	Q12B
R	D13	DNU	VDD	VDD	Q13A	Q13B
T	D14	DNU	VREF	VDD	Q14A	Q14B

1:2 "B"- configuration Logic Diagram



SLGSSTU32864 top view pinout, 1:2 "B"(C0=1,C1=1)

	1	2	3	4	5	6
A	D1	NC	VREF	VDD	Q1A	Q1B
B	D2	DNU	GND	GND	Q2A	Q2B
C	D3	DNU	VDD	VDD	Q3A	Q3B
D	D4	NC	GND	GND	Q4A	Q4B
E	D5	DNU	VDD	VDD	Q5A	Q5B
F	D6	DNU	GND	GND	Q6A	Q6B
G	NC	$\overline{\text{RESET}}$	VDD	VDD	C1	C0
H	CLK	$\overline{\text{DCS}}$	GND	GND	$\overline{\text{QCSA}}$	$\overline{\text{QCSB}}$
J	$\overline{\text{CLK}}$	$\overline{\text{CSR}}$	VDD	VDD	ZOH	ZOL
K	D8	DNU	GND	GND	Q8A	Q8B
L	D9	DNU	VDD	VDD	Q9A	Q9B
M	D10	DNU	GND	GND	Q10A	Q10B
N	DODT	DNU	VDD	VDD	QODTA	QODTB
P	D12	DNU	GND	GND	Q12A	Q12B
R	D13	DNU	VDD	VDD	Q13A	Q13B
T	DCKE	DNU	VREF	VDD	QCKEA	QCKEB

SLGSSTU32864 Terminal Description:

TERMINAL NAME	TYPE	DESCRIPTION
Q (1:25)	OUTPUT	Q-Outputs that are stopped by $\overline{CSR}$ & $\overline{DCS}$ control.
GND	GROUND	Ground
VDD	POWER	Supply voltage
D (1:25)	INPUT	D-Inputs latched in on the rising edge of CLK crossing falling edge of $\overline{CLK}$
CLK	INPUT	Positive clock input
$\overline{CLK}$	INPUT	Negative clock input
C0,C1	INPUT	Control inputs for register configurations: 1:1 , 1:2 A , 1:2 B
$\overline{RESET}$	INPUT	Asynchronous reset (active low)
VREF	INPUT	Input reference voltage. Both inputs are internally connected together by 200Ω
$\overline{CSR}$, $\overline{DCS}$	INPUT	Chip select control pins. Q1-Q25 outputs stopped when $\overline{CSR}$ & $\overline{DCS}$=high
DODT	INPUT	D-input. This register not stopped by $\overline{CSR}$ & $\overline{DCS}$ control.
DCKE	INPUT	D-input. This register not stopped by $\overline{CSR}$ & $\overline{DCS}$ control.
$Q\overline{CS}$	OUTPUT	Q-Output. Not stopped by $\overline{CSR}$ & $\overline{DCS}$ control.
QODT	OUTPUT	Q-Output. Not stopped by $\overline{CSR}$ & $\overline{DCS}$ control.
QCKE	OUTPUT	Q-Output. Not stopped by $\overline{CSR}$ & $\overline{DCS}$ control.
NC	NC	No-connect. Ball present, but no internal connection to the die.
DNU	DNU	Do-not-use. Ball internally connected to the die and should be left open-circuit.
ZOL,ZOH	NC	Reserved for future use. Ball present, not electrically connected to the die.

Function Table

Inputs						Outputs		
$\overline{RESET}$	$\overline{DCS}$	$\overline{CSR}$	CLK	$\overline{CLK}$	Dn,DODT, DCKE	Qn	$Q\overline{CS}$	QODT, QCKE
H	L	L	↑	↓	L	L	L	L
H	L	L	↑	↓	H	H	L	H
H	L	L	L or H	L or H	X	Q_0	Q_0	Q_0
H	L	H	↑	↓	L	L	L	L
H	L	H	↑	↓	H	H	L	H
H	L	H	L or H	L or H	X	Q_0	Q_0	Q_0
H	H	L	↑	↓	L	L	H	L
H	H	L	↑	↓	H	H	H	H
H	H	L	L or H	L or H	X	Q_0	Q_0	Q_0
H	H	H	↑	↓	L	Q_0	H	L
H	H	H	↑	↓	H	Q_0	H	H
H	H	H	L or H	L or H	X	Q_0	Q_0	Q_0
L	X, or Floating	X, or Floating	X, or Floating	X, or Floating	X, or Floating	L	L	L

Absolute Maximum Ratings

Storage Temperature. . . . . -65°C to +150°C
Supply Voltage. . . . . -0.5 to 2.5V
Input Voltage[1,2]. . . . . -0.5 to 2.5V
Output Voltage[1,2] . . . . . -0.5 to V_{DD} +0.5
Input Clamp Current. . . . . -50 mA
Output Clamp Current . . . . . ±50 mA
Continuous V_{DD} or GND Current/Pin. . . . . ±100 mA
BGA Package Thermal Impedance[3] . . . . . 37°C/W

Notes:
1. The input and output negative voltage ratings may be exceded if the input and output clamp currents are within limits.
2. Limited to 2.5V Max.
3. The package thermal impedance is calculated according to JESD 51-7

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to this device. These
ratings are stress specifications only and functional operation of the device at these or other conditions above
those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Recommended Operating Conditions:

PARAMETER			MIN	TYP	MAX	UNITS
V_{DD}	Supply Voltage		1.7		1.9	V
V_{REF}	Reference Voltage		0.49 X V_{DD}	.5 X V_{DD}	0.51 X V_{DD}	
V_{TT}	Termination Voltage		V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04	
V_I	Input Voltage		0		V_{DD}	
$V_{IH\ (DC)}$	DC Input High Voltage	Data Inputs	V_{REF} +0.125			
$V_{IH\ (AC)}$	AC Input High Voltage		V_{REF} + 0.25			
$V_{IL\ (DC)}$	DC Input Low Voltage				V_{REF} -0.125	
$V_{IL\ (AC)}$	AC Input Low Voltage				V_{REF} - 0.25	
V_{IH}	Input High Voltage Level	$\overline{RESET}$, Cn	0.65 X V_{DD}			
V_{IL}	Input Low Voltage Level				0.35 X V_{DD}	
V_{ICR}	Common mode Input Range	CLK, $\overline{CLK}$	0.675		1.125	
V_{ID}	Differential Input Voltage		0.6			
I_{OH}	High-Level Output Current				-8	mA
I_{OL}	Low-Level Output Current				8	
T_A	Operating Free-Air Temperature		0		70	°C

SLGSSTU32864 DC Electrical Characteristics

V_{DD} = 1.8 +/-0.1V (unless otherwise stated)

PARAMETER		CONDITIONS		V_{DD}	MIN	TYP	MAX	UNITS
V_{OH}		I_{OH} = -100μA		1.7V -1.9V	V_{DD} - 0.2			V
		I_{OH} = -6mA		1.7V	1.2			
V_{OL}		I_{OL} = 100μA		1.7V -1.9V			0.2	
		I_{OL} = 6mA		1.7V			0.5	
I_I	All Inputs	$V_I = V_{DD}$ or GND	I_O = 0	1.9V			±5	μA
I_{DD}	Standby (Static)	$\overline{RESET}$ = GND		1.9V			100	μA
	Operating (Static)	$V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, $\overline{RESET} = V_{DD}$					40	mA
I_{DDD}	Dynamic operating (clock only)	$\overline{RESET} = V_{DD}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK & $\overline{CLK}$ switching 50% duty cycle		1.8V		28		μA/ MHz
	Dynamic Operating 1:1 (each data input)	$\overline{RESET} = V_{DD}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK & $\overline{CLK}$ switching 50% duty cycle. One data input switching at half clock frequency, 50%duty cycle				18		μA/ clock MHZ/ data
	Dynamic Operating 1:2 (each data input)					36		μA/ clock MHZ/ data
C_i	Data Inputs	$V_I = V_{REF}$ ± 250 mV		1.8V	2.5	3.8	5	pF
	CLK and $\overline{CLK}$	V_{ICR}=0.9V, $V_{I(PP)}$ = 600mV			4.4	4.8	5.2	
	$\overline{RESET}$	$V_I = V_{DD}$ or GND			4.2	4.6	5	

Timing Requirements:

(over operating free-air temperature range, unless otherwise noted) Input slew rates are 1V/ns ± 20%.

PARAMETER			MIN	MAX	UNITS
f_{clock}	Clock frequency			300	MHz
t_W	Pulse duration. CLK,$\overline{CLK}$ high or low		1		ns
t_{ACT}	Differential active time[4]			10	ns
t_{INACT}	Differential inactive time[5]			15	ns
t_S	Setup time	$\overline{DCS}$ before CLK↑, $\overline{CLK}$↓, $\overline{CSR}$ high	0.7		ns
		$\overline{DCS}$ before CLK↑, $\overline{CLK}$↓, $\overline{CSR}$ low	0.5		ns
t_H	Hold time	$\overline{CSR}$, ODT, CKE, and Data before CLK↑, $\overline{CLK}$↓	0.5		ns
		$\overline{DCS}$, $\overline{CSR}$, ODT, CKE, Data before CLK↑, $\overline{CLK}$↓	0.5		ns

Notes: 4. Data and VREF inputs must be held low for a minimum time (t_{ACT} max) after $\overline{RESET}$ driven high

5. Data, VREF, and CLK,$\overline{CLK}$ inputs must be held at valid logic (high or low) levels for a minimum time (t_{INACT} max) after $\overline{RESET}$ driven low

AC Specifications

Switching Characteristics:

(over recommended operating free-air temperature range, unless otherwise noted)

SYMBOL	From (Input)	To (Output)	V_{DD} = 1.8V ± 0.1V			UNITS
			MIN	TYP	MAX	
f_{MAX}			300			MHz
t_{PDM}[6,7]	CLK, $\overline{CLK}$	Q	1.41		2.5	ns
t_{RPHL}	$\overline{RESET}$	Q			3	ns

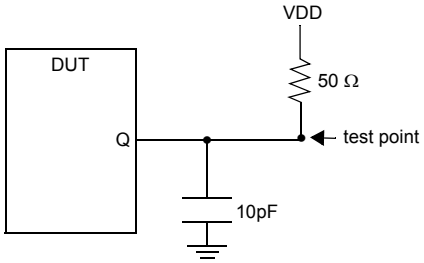
Notes: 6. Includes 350pS trace delay of the test load
7. Guaranteed by design and may not be 100% production tested.

Output Buffer Characteristics:

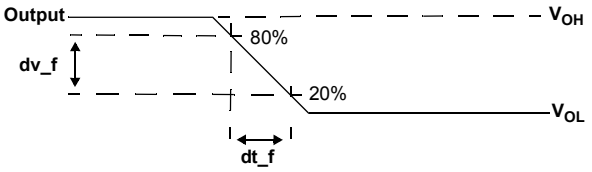
(over recommended operating free-air temperature range, unless otherwise noted)

SYMBOL	From	To	V_{DD} = 1.8V ± 0.1V			UNITS
			MIN	TYP	MAX	
dV/dt_r	20%	80%	1		4	V/ns
dV/dt_f	80%	20%	1		4	V/ns
dV/dt_Δ[8]					1	V/ns

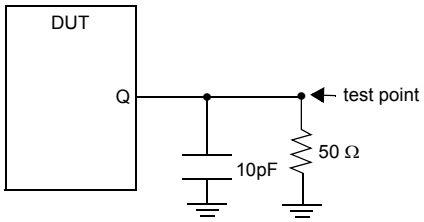
Notes: 8. Difference between rising and falling edge rates.



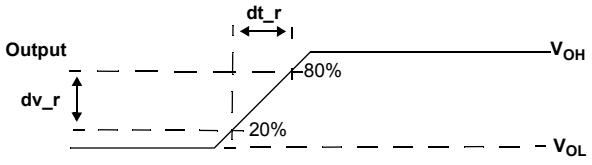
Output load test circuit:
high to low slew rate



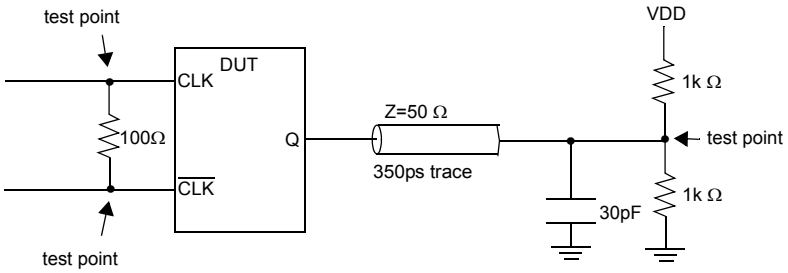
Voltage waveform: high to low slew rate



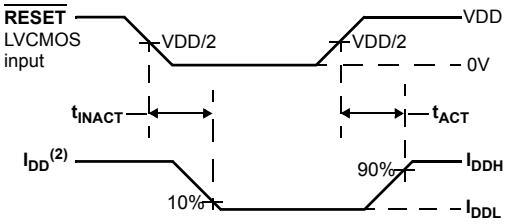
Output load test circuit:
low to high slew rate



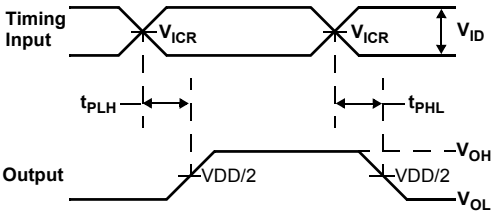
Voltage waveform: low to high slew rate



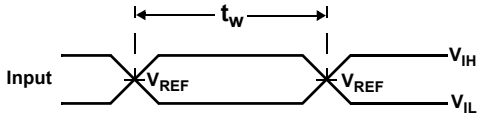
Output load test circuit



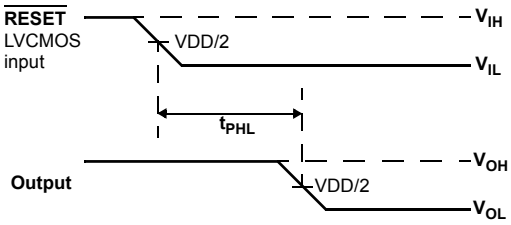
Voltage and Current Waveforms
Inputs Active and Inactive Times



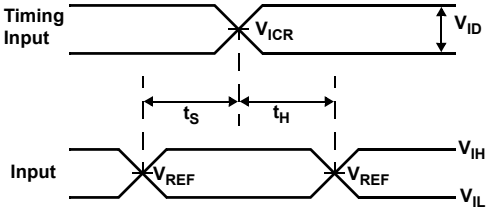
Voltage Waveforms - Propagation Delay Times



Voltage Waveforms - Pulse Duration



Voltage Waveforms - Propagation Delay Times

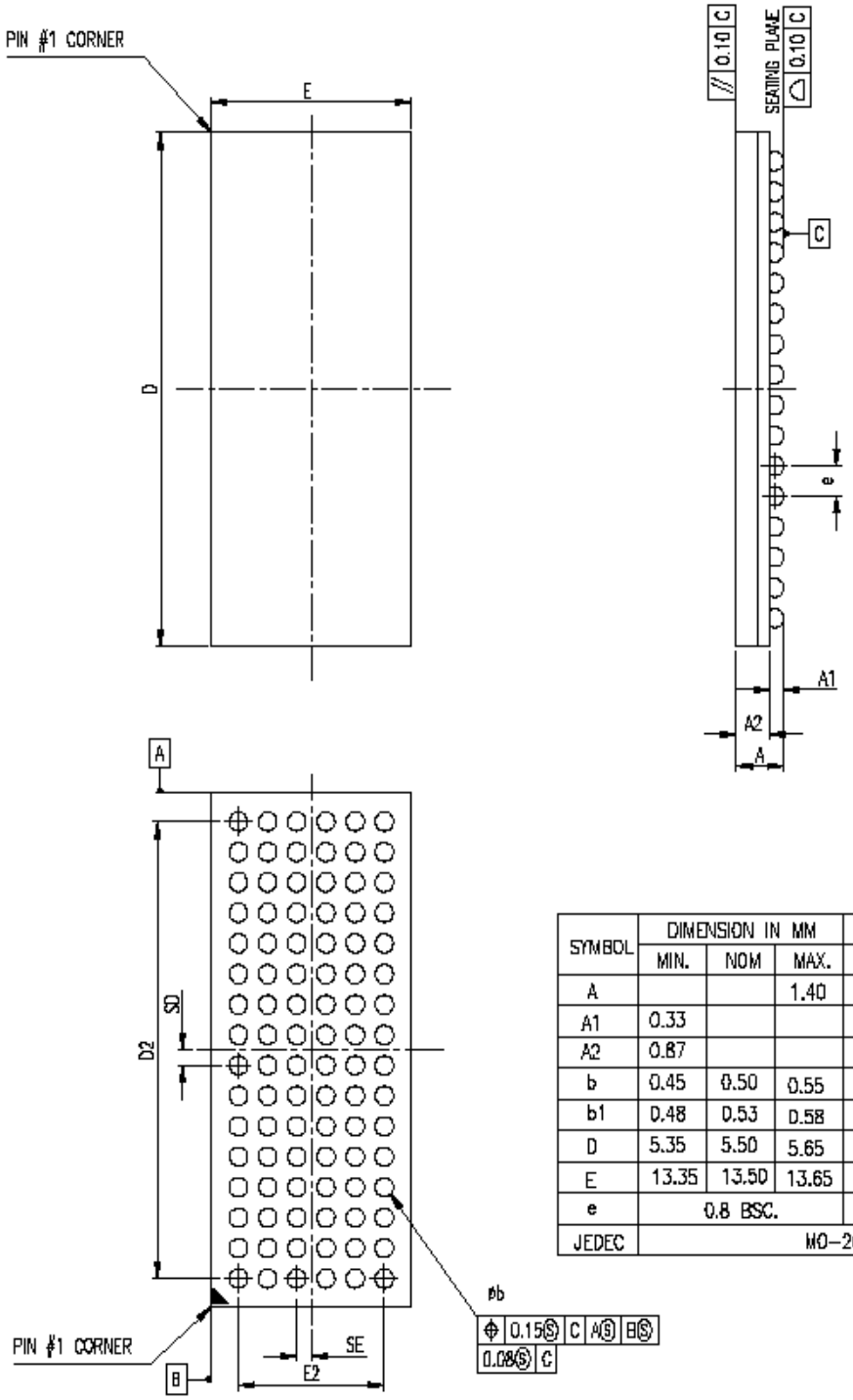


Voltage Waveforms - Setup and Hold Times

Notes:

1. C_L includes measurement probe and jig capacitance.
2. Conditions for I_{DD} testing are with clock and data inputs at V_{DD} or GND, and I_O = 0mA
3. All input pulses are supplied by generators having: Zo=50Ω,
   input slew rate = 1 V/ns ± 20% (unless otherwise specified).
4. The outputs are measured individually with one transition per measurement.
5. $V_{IH} = V_{REF}$ + 250mV (AC levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS input.
6. $V_{IL} = V_{REF}$ - 250mV (AC levels) for differential inputs. V_{IL} = GND for LVCMOS input.
7. $t_{PLH} = t_{PHL} = t_{PD}$

Package dimensions: SLGSSTU32864EX 96-LFBGA



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.40			0.055
A1	0.33			0.013		
A2	0.87			0.034		
b	0.45	0.50	0.55	0.018	0.020	0.022
b1	0.48	0.53	0.58	0.019	0.021	0.023
D	5.35	5.50	5.65	0.210	0.217	0.222
E	13.35	13.50	13.65	0.526	0.531	0.537
e	0.8 BSC.			0.031 BSC.		
JEDEC	MO-205(REF)					

N	SE (mm)	SD (mm)	E2 (mm)	D2 (mm)	JEDEC(REF)
96	0.40 BSC.	0.40 BSC.	4.00 BSC.	12.00 BSC.	MO-205GC