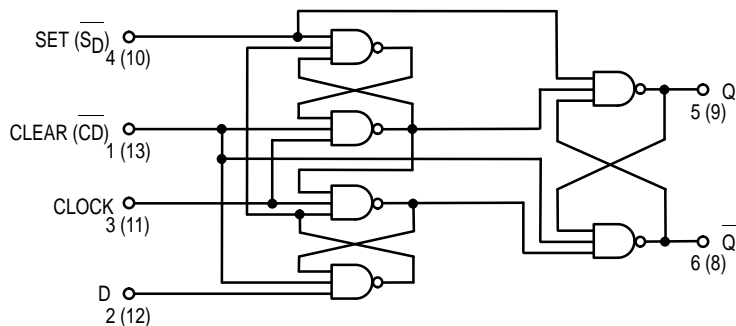# MOTOROLA

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP

The SN54/74LS74A dual edge-triggered flip-flop utilizes Schottky TTL circuitry to produce high speed D-type flip-flops. Each flip-flop has individual clear and set inputs, and also complementary Q and Q outputs.

Information at input D is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the HIGH or the LOW level, the D input signal has no effect.

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP

LOW POWER SCHOTTKY

LOGIC DIAGRAM (Each Flip-Flop)

SET ($\overline{S_D}$) 4 (10)

CLEAR ($\overline{C_D}$) 1 (13)

CLOCK 3 (11)

D 2 (12)

Q 5 (9)

$\overline{Q}$ 6 (8)

J SUFFIX
CERAMIC
CASE 632-08

N SUFFIX
PLASTIC
CASE 646-06
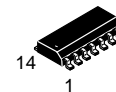
D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ   Ceramic
SN74LSXXN   Plastic
SN74LSXXD   SOIC

MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{S_D}$	$\overline{S_D}$	D	Q	$\overline{Q}$
Set	L	H	X	H	L
Reset (Clear)	H	L	X	L	H
*Undetermined	L	L	X	H	H
Load "1" (Set)	H	H	h	H	L
Load "0" (Reset)	H	H	I	L	H

* Both outputs will be HIGH while both S_D and C_D are LOW, but the output states are unpredictable if S_D and C_D go HIGH simultaneously. If the levels at the set and clear are near V_{IL} maximum then we cannot guarantee to meet the minimum level for V_{OH}.
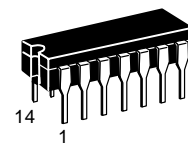
H, h = HIGH Voltage Level
L, I = LOW Voltage Level
X = Don't Care
i, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.
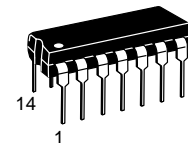
LOGIC SYMBOL

V_{CC} = PIN 14
GND = PIN 7

SN54/74LS74A

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input High Current Data, Clock Set, Clear				20 40	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
	Data, Clock Set, Clear				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current Data, Clock Set, Clear				−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 1)		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				8.0	mA	V_{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
f_{MAX}	Maximum Clock Frequency	25	33		MHz	Figure 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Clock, Clear, Set to Output		13	25	ns	Figure 1	
			25	40	ns		

AC SETUP REQUIREMENTS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
$t_{W(H)}$	Clock	25			ns	Figure 1	V_{CC} = 5.0 V
$t_{W(L)}$	Clear, Set	25			ns	Figure 2	
t_s	Data Setup Time — HIGH	20			ns	Figure 1	
	LOW	20			ns		
t_h	Hold Time	5.0			ns	Figure 1	

SN54/74LS74A

AC WAVEFORMS
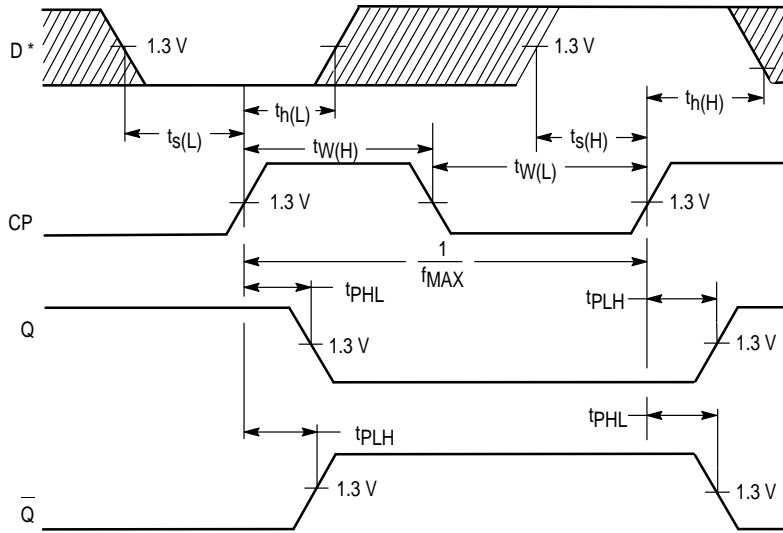
*The shaded areas indicate when the input is permitted to change for predictable output performance.

**Figure 1. Clock to Output Delays, Data
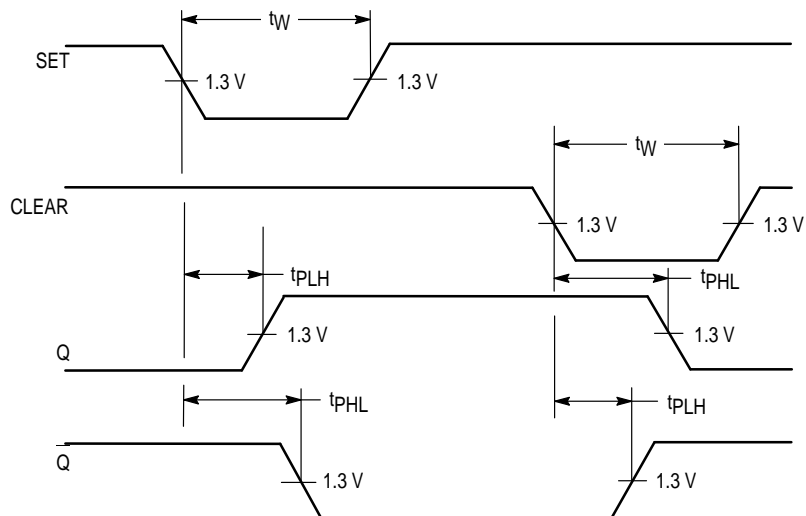Set-Up and Hold Times, Clock Pulse Width**

**Figure 2. Set and Clear to Output Delays,
Set and Clear Pulse Widths**