

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC7MZ245FK

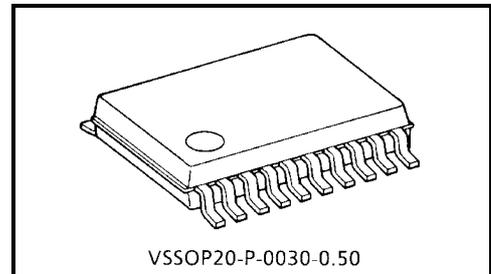
Low Voltage Octal Bus Transceiver with 5 V Tolerant Inputs and Outputs

The TC7MZ245FK is a high performance cmos octal bus transceiver. Designed for use in 3.3 V systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

The device is designed for low-voltage (3.3 V) VCC applications, but it could be used to interface to 5 V supply environment for both inputs and outputs.

The direction of data transmission is determined by the level of the DIR input. The enable input (\overline{OE}) can be used to disable the device so that the busses are effectively isolated.

All inputs are equipped with protection circuits against static discharge.



Weight: 0.03 g (typ.)

Features

- Low voltage operation: $V_{CC} = 2.0\sim 3.6$ V
- High speed operation: $t_{pd} = 7.0$ ns (max) ($V_{CC} = 3.0\sim 3.6$ V)
- Output current: $|I_{OH}|/I_{OL} = 24$ mA (min) ($V_{CC} = 3.0$ V)
- Latch-up performance: ± 500 mA
- Package: VSSOP (US20)
- Bidirectional interface between 3.3 V and 5.0 V signals.
- Power down protection is provided on all inputs and outputs.
- Pin and function compatible with the 74 series (74AC/VHC/HC/F/ALS/LS etc.) 245 type.

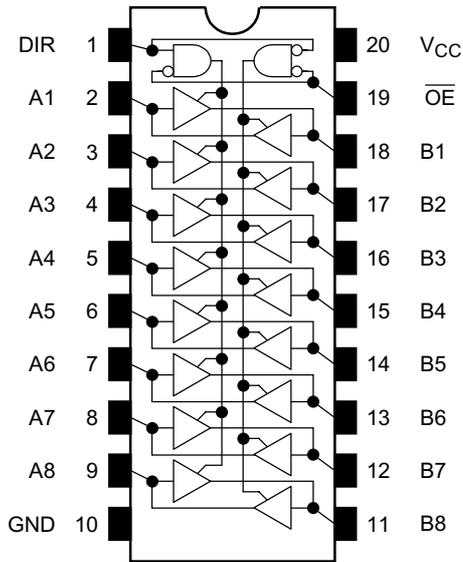
Note: Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.

All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors.

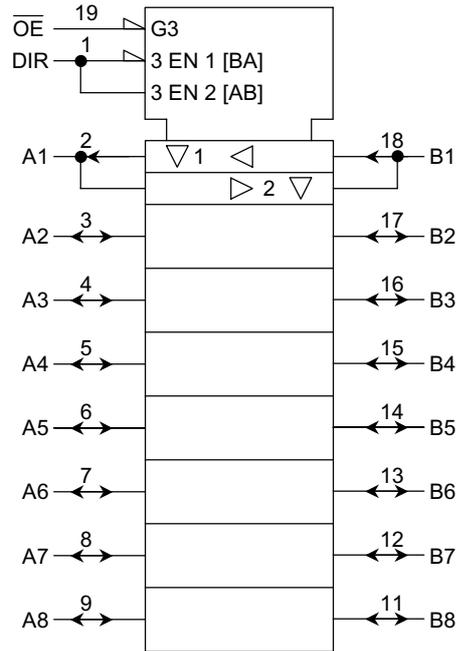
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Pin Assignment (top view)



IEC Logic Symbol



Truth Table

Inputs		Outputs	Function	
\overline{OE}	DIR		A-Bus	B-Bus
L	L	A = B	Output	Input
L	H	B = A	Input	Output
H	X	Z	High Impedance	

X: Don't care

Z: High impedance

Maximum Ratings

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5~7.0	V
DC input voltage (DIR, \overline{OE})	V_{IN}	-0.5~7.0	V
DC bus I/O voltage	$V_{I/O}$	-0.5~7.0 (Note1)	V
		-0.5~ $V_{CC} + 0.5$ (Note2)	
Input diode current	I_{IK}	-50	mA
Output diode current	I_{OK}	± 50 (Note3)	mA
DC output current	I_{OUT}	± 50	mA
Power dissipation	P_D	180	mW
DC V_{CC} /ground current	I_{CC}/I_{GND}	± 100	mA
Storage temperature	T_{stg}	-65~150	°C

Note1: Output in off-state

Note2: High or low state. I_{OUT} absolute maximum rating must be observed.

Note3: $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

Recommended Operating Conditions

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0~3.6	V
		1.5~3.6 (Note4)	
Input voltage (DIR, \overline{OE})	V_{IN}	0~5.5	V
Bus I/O voltage	$V_{I/O}$	0~5.5 (Note5)	V
		0~ V_{CC} (Note6)	
Output current	I_{OH}/I_{OL}	± 24 (Note7)	mA
		± 12 (Note8)	
Operating temperature	T_{opr}	-40~85	°C
Input rise and fall time	dt/dv	0~10 (Note9)	ns/V

Note4: Data retention only

Note5: Output in off-state

Note6: High or low state

Note7: $V_{CC} = 3.0\sim 3.6$ V

Note8: $V_{CC} = 2.7\sim 3.0$ V

Note9: $V_{IN} = 0.8\sim 2.0$ V, $V_{CC} = 3.0$ V

Electrical Characteristics

DC Characteristics (Ta = -40~85°C)

Characteristics		Symbol	Test Condition		V _{CC} (V)	Min	Max	Unit
Input voltage	High level	V _{IH}	—		2.7~3.6	2.0	—	V
	Low level	V _{IL}	—		2.7~3.6	—	0.8	
Output voltage	High level	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -100 μA	2.7~3.6	V _{CC} - 0.2	—	V
				I _{OH} = -12 mA	2.7	2.2	—	
				I _{OH} = -18 mA	3.0	2.4	—	
				I _{OH} = -24 mA	3.0	2.2	—	
	Low level	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 100 μA	2.7~3.6	—	0.2	
				I _{OL} = 12 mA	2.7	—	0.4	
				I _{OL} = 16 mA	3.0	—	0.4	
				I _{OL} = 24 mA	3.0	—	0.55	
Input leakage current		I _{IN}	V _{IN} = 0~5.5 V		2.7~3.6	—	±5.0	μA
3-state output off-state current		I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0~5.5 V		2.7~3.6	—	±5.0	μA
Power off leakage current		I _{OFF}	V _{IN} /V _{OUT} = 5.5 V		0	—	10.0	μA
Quiescent supply current		I _{CC}	V _{IN} = V _{CC} or GND		2.7~3.6	—	10.0	μA
			V _{IN} /V _{OUT} = 3.6~5.5 V		2.7~3.6	—	±10.0	
Increase in I _{CC} per input		ΔI _{CC}	V _{IH} = V _{CC} - 0.6 V		2.7~3.6	—	500	

AC Characteristics (Ta = -40~85°C)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Min	Max	Unit
Propagation delay time	t _{pLH}	Figure 1, Figure 2	2.7	—	8.0	ns
	t _{pHL}		3.3 ± 0.3	1.5	7.0	
Output enable time	t _{pZL}	Figure 1, Figure 3	2.7	—	9.5	ns
	t _{pZH}		3.3 ± 0.3	1.5	8.5	
Output disable time	t _{pLZ}	Figure 1, Figure 3	2.7	—	8.5	ns
	t _{pHZ}		3.3 ± 0.3	1.5	7.5	
Output to output skew	t _{osLH}	(Note10)	2.7	—	—	ns
	t _{osHL}		3.3 ± 0.3	—	1.0	

Note10: This parameter is guaranteed by design.

$$(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$$

Dynamic Switching Characteristics

(Ta = 25°C, Input: t_r = t_f = 2.5 ns, C_L = 50 pF, R_L = 500 Ω)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Typ.	Unit	
Quiet output maximum dynamic	V _{OL}	V _{OLP}	V _{IH} = 3.3 V, V _{IL} = 0 V	3.3	0.8	V
Quiet output minimum dynamic	V _{OL}	V _{OLV}	V _{IH} = 3.3 V, V _{IL} = 0 V	3.3	0.8	V

Capacitive Characteristics (Ta = 25°C)

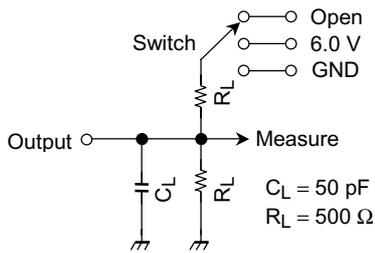
Characteristics	Symbol	Test Condition	V _{CC} (V)	Typ.	Unit
Input capacitance	C _{IN}	DIR, \overline{OE}	3.3	7	pF
Bus input capacitance	C _{I/O}	A _n , B _n	3.3	8	pF
Power dissipation capacitance	C _{PD}	f _{IN} = 10 MHz	(Note11) 3.3	25	pF

Note11: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation:

$$I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$$

AC Test Circuit



Parameter	Switch
t_{pLH}, t_{pHL}	Open
t_{pLZ}, t_{pZL}	6.0 V
t_{pHZ}, t_{pZH}	GND

Figure 1

AC Waveform

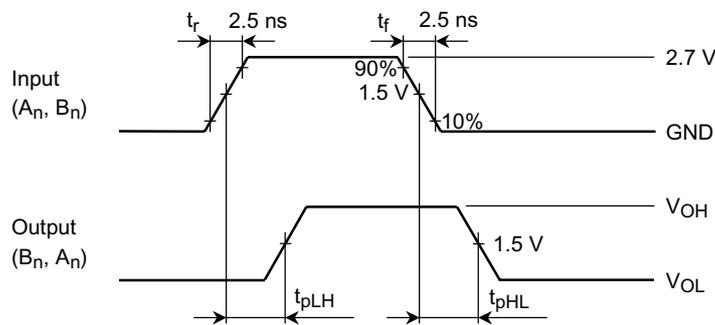


Figure 2 t_{pLH}, t_{pHL}

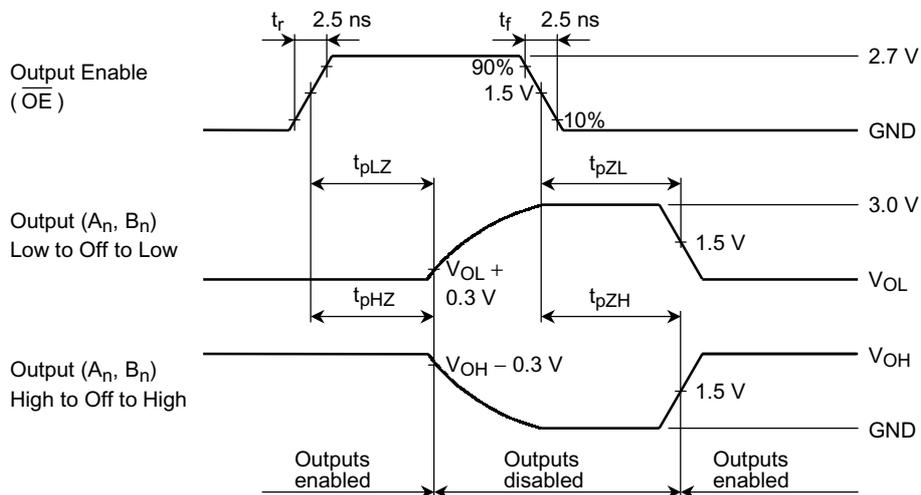
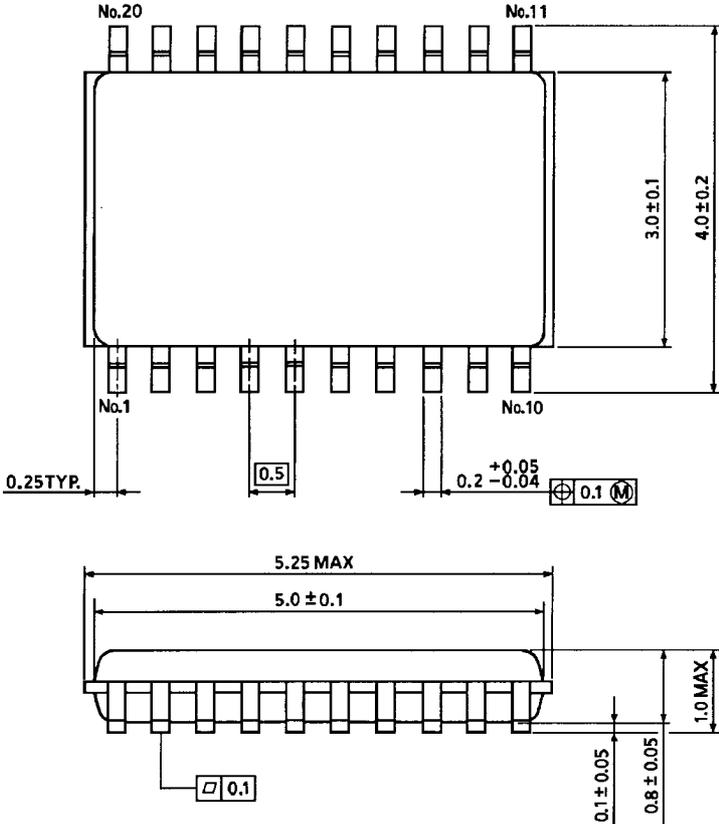


Figure 3 $t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}$

Package Dimensions

VSSOP20-P-0030-0.50

Unit : mm



Weight: 0.03 g (typ.)