DATA SHEET



MOS FIELD EFFECT TRANSISTOR $\mu PA1790$

SWITCHING N-AND P-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

This product is N-and P-Channel MOS Field Effect Transistor designed for motor driver applications.

FEATURES

- Dual chip type
- Low on-resistance

N-Channel $R_{DS(on)1} = 0.12 \Omega$ TYP. (VGs = 10 V, ID = 0.5 A) $R_{DS(on)2} = 0.19 \Omega$ TYP. (VGs = 4 V, ID = 0.5 A)

P-Channel R_{DS(on)1} = 0.45 Ω TYP. (V_{GS} = -10 V, I_D = -0.35 A) R_{DS(on)2} = 0.74 Ω TYP. (V_{GS} = -4 V, I_D = -0.35 A)

PACKAGE

Power SOP8

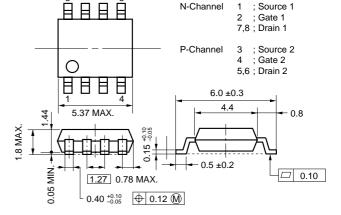
- Low input capacitance
 N-Channel C_{iss} = 180 pF TYP.
 P-Channel C_{iss} = 230 pF TYP.
- Built-in G-S protection diode

ORDERING INFORMATION

PART NUMBER

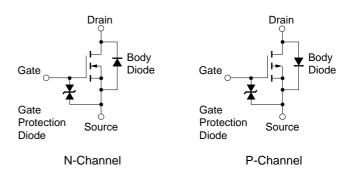
μPA1790G

• Small and surface mount package (Power SOP8)



PACKAGE DRAWING (Unit : mm)

EQUIVARENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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PARAMETER	SYMBOL	N-CHANNEL	P-CHANNEL	UNIT
Drain to Source Voltage (Vos = 0 V)	VDSS	60	-60	V
Gate to Source Voltage (VDS = 0 V)	Vgss	±20	∓20	V
Drain Current (DC)	D(DC)	±1.0	∓0.7	А
Drain Current (pulse) Note1	D(pulse)	±4.0	∓2.8	А
Total Power Dissipation (1 unit) Note2	Р⊤	1.7		W
Total Power Dissipation (2 unit) Note2	Р⊤	2.0		W
Channel Temperature	Tch	150		°C
Storage Temperature	Tstg	–55 to	°C	

ABSOLUTE MAXIMUM RATINGS (TA = 25°C, All terminals are connected.)

Notes 1. $PW \le 10 \ \mu s$, Duty Cycle $\le 1 \ \%$

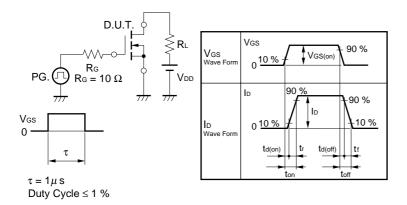
2. Mounted on ceramic substrate of 2000 mm² x 2.25 mm

ELECTRICAL CHARACTERISTICS (TA = 25 °C, All terminals are connected.)

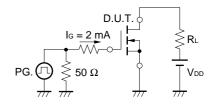
N-CHANNEL

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	RDS(on)1	Vgs = 10 V, Id = 0.5 A		0.12	0.26	Ω
	RDS(on)2	Vgs = 4 V, Id = 0.5 A		0.19	0.34	Ω
Gate to Source Cut-off Voltage	V _{GS(off)}	Vds = 10 V, Id = 1 mA	1.0	1.7	2.5	V
Forward Transfer Admittance	y _{fs}	Vds = 10 V, Id = 0.5 A	1.0	1.7		S
Drain Leakage Current	IDSS	Vds = 60 V, Vgs = 0 V			10	μA
Gate to Source Leakage Current	lgss	$V_{GS} = \pm 16 \text{ V}, \text{ V}_{DS} = 0 \text{ V}$			±10	μA
Input Capacitance	Ciss	V _{DS} = 10 V		180		pF
Output Capacitance	Coss	V _{GS} = 0 V		100		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		35		pF
Turn-on Delay Time	td(on)	ID = 0.5 A		1		ns
Rise Time	tr	VGS(on) = 10 V		1.4		ns
Turn-off Delay Time	$t_{d(off)}$	$V_{DD} = 30 V$		23		ns
Fall Time	tr	R _G = 10 Ω		17		ns
Total Gate Charge	QG	ID = 1.0 A		8		nC
Gate to Source Charge	QGS	Vdd = 48 V		1		nC
Gate to Drain Charge	Qgd	Vgs = 10 V		3.5		nC
Body Diode Forward Voltage	VF(S-D)	IF = 1.0 A, VGS = 0 V		0.75		V
Reverse Recovery Time	trr	IF = 1.0 A, VGS = 0 V		30		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A / μs		33		nC

TEST CIRCUIT 1 SWITCHING TIME



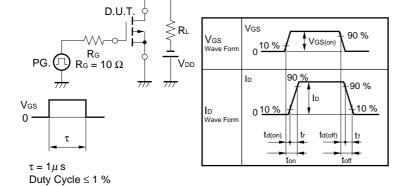
TEST CIRCUIT 2 GATE CHARGE



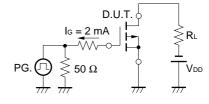
P-CHANNEL

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	RDS(on)1	V _{GS} = −10 V, I _D = −0.35 A		0.45	0.6	Ω
	RDS(on)2	Vgs = −4 V, Id = −0.35 A		0.74	1.1	Ω
Gate to Source Cut-off Voltage	VGS(off)	$V_{DS} = -10 \text{ V}, \text{ ID} = -1 \text{ mA}$	-1.0	-1.7	-2.5	V
Forward Transfer Admittance	y _{fs}	V⊳s = −10 V, I⊳ = −0.35 A	5.0			S
Drain Leakage Current	loss	$V_{DS} = -60 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$			-10	μA
Gate to Source Leakage Current	lgss	$V_{GS} = \mp 16 \text{ V}, \text{ Vds} = 0 \text{ V}$			∓ 10	μA
Input Capacitance	Ciss	V _{DS} = -10 V		230		pF
Output Capacitance	Coss	Vgs = 0 V		100		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		25		pF
Turn-on Delay Time	td(on)	I⊳ = −0.35 A		1.9		ns
Rise Time	tr	$V_{GS(on)} = -10 V$		1.7		ns
Turn-off Delay Time	td(off)	$V_{DD} = -30 V$		30		ns
Fall Time	tr	R _G = 10 Ω		15		ns
Total Gate Charge	QG	ID = -0.7 A		7.6		nC
Gate to Source Charge	Q _{GS}	Vdd = -48 V		1		nC
Gate to Drain Charge	Qgd	Vgs = -10 V		2		nC
Body Diode Forward Voltage	VF(S-D)	IF = 0.7 A, VGS = 0 V		0.85		V
Reverse Recovery Time	trr	IF = 0.7 A, VGS = 0 V		58		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A / μs		130		nC

TEST CIRCUIT 1 SWITCHING TIME



TEST CIRCUIT 2 GATE CHARGE



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