TOPAZ SEMICONDUCTOR

VP0808, VP1008

P-CHANNEL ENHANCEMENT-MODE D-MOS POWER FETs

ORDERING INFORMATION

Sorted Chips in Waffle Pack	VP0808CHP	VP1008CHP
TO-226AA (TO-92) Plastic Package	VP0808L	VP1008L
TO-237 Plastic Package	VP0808M	VP1008M
Description	-80V, 5.0 ohm	-100V, 5.0 ohm

FEATURES

- Gate Stand-off Voltage, ±40V min.
- Low Output and Transfer Capacitances
- N-Channel Complements Available

APPLICATIONS

- Motor Controls
- Logic Interfaces
- Pulse Amplifiers

ABSOLUTE MAXIMUM RATINGS (T_C = +25°C unless otherwise noted)

Drain-Source Voltage
- VP1008 ..... -100V
- VP0808 ..... -80V

Drain-Gate Voltage (R_{GS} = 1MΩ)
- VP1008 ..... -100V
- VP0808 ..... -80V

Gate-Source Voltage ..... ±40V

Continuous Drain Current

	T_C = +100°C	T_C = +25°C
TO-92 Pkg.	-.13A	-.21A
TO-237 Pkg.	-.21A	-.33A

Peak Pulsed Drain Current ..... -3.0A

Maximum Power Dissipation

	T_C = +100°C	T_C = +25°C
TO-92 Pkg.	0.4W	3.0W
TO-237 Pkg.	0.6W	4.3W

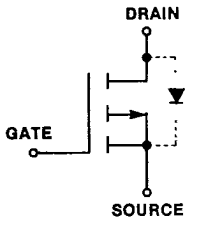
Linear Derating Factor

	Junction to Ambient (mW/°C)	Junction to Case (mW/°C)
TO-92 Pkg.	5.33	24
TO-237 Pkg.	8.0	34

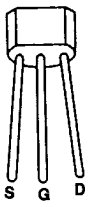
Operating Junction and Storage Temperature Range ..... -55 to +150°C

Lead Temperature (1/16" from mounting surface for 10 Sec) ..... +300°C

PIN CONFIGURATIONS

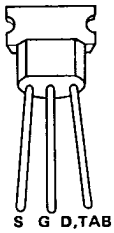


TO-226AA (TO-92)



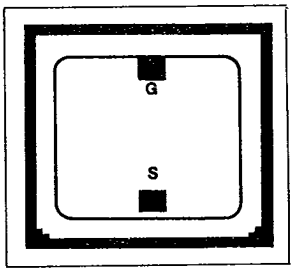
See Package 5

TO-237



See Package 7

CHIP CONFIGURATION



Dimensions: .054 × .051 × .020 in.
Drain is backside contact.

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ELECTRICAL CHARACTERISTICS (T_C = +25°C unless otherwise noted)

#		CHARACTERISTIC		VP0808 MIN	VP0808 TYP	VP0808 MAX	VP1008 MIN	VP1008 TYP	VP1008 MAX	UNIT	TEST CONDITIONS	
1	STATIC	BV_{DSS}	Drain-Source Breakdown Voltage	-80			-100			V	I_D = -10μA, V_{GS} = 0	
2		$V_{GS(th)}$	Gate-Source Threshold Voltage	-2.0		-4.5	-2.0		-4.5	V	V_{DS} = V_{GS} I_D = -1.0mA	
3		I_{GSS}	Gate-Body Leakage Current			-100			-100	nA	V_{GS} = -30V, V_{DS} = 0	
4						100			100		V_{GS} = +30V, V_{DS} = 0	
5		I_{DSS}	Drain-Source OFF Leakage Current			-10				μA	V_{DS} = -80V	
6						-500					V_{GS} = 0	T_C = +125°C
7									-10		V_{DS} = -100V	
8									-500		V_{GS} = 0	T_C = +125°C
9		$I_{D(on)}$	ON Drain Current[1]	-1.1			-1.1			A	V_{DS} = -25V, V_{GS} = -10V	
10		$V_{DS(on)}$	Drain-Source[1] ON Voltage		-4.5	-5.0		-4.5	-5.0	V	V_{GS} = -10V, I_D = -1.0A	
11		$r_{DS(on)}$	Drain-Source[1] ON Resistance		4.5	5.0		4.5	5.0	ohms	V_{GS} = -10V	
12						8.0			8.0		I_D = -1.0A	T_C = +125°C
13	DYNAMIC	g_{fs}	Common-Source[1] Forward Transcond.	200	270		200	270		mS	V_{DS} = -25V, I_D = -0.5A, f = 1KHz	
14		C_{iss}	Common-Source Input Capacitance		60	150		60	150	pF	V_{DS} = -25V, V_{GS} = 0 f = 1MHz	
15		C_{rss}	Common-Source Reverse Transfer Capacitance		8.0	25		8.0	25			
16		C_{oss}	Common-Source Output Capacitance		11	60		11	60			
17		$t_{d(on)}$	Turn-ON Delay Time			10			10	nsec	V_{DD} = -25V R_L = 45 ohms R_G = 25 ohms $V_{G(on)}$ = -10V	
18		t_r	Rise Time			15			15			
19		$t_{d(off)}$	Turn-OFF Delay Time			10			10			
20		t_f	Fall Time			15			15			
21	DIODE	I_S	Continuous Source Current	-.21			-.21			A	TO-92 Pkg.	
22				-.33			-.33				TO-237 Pkg.	
23		I_{SM}	Peak Source Current[1]			-3.0			-3.0			
24		V_{SD}	Source-Drain[1] Forward Voltage		1.2			1.2		V	V_{GS} = 0	I = .21A, TO-92 Pkg.
25					1.2			1.2				I = .33A, TO-237 Pkg.

Note 1: Pulse Test 80μSec, 1% Duty Cycle

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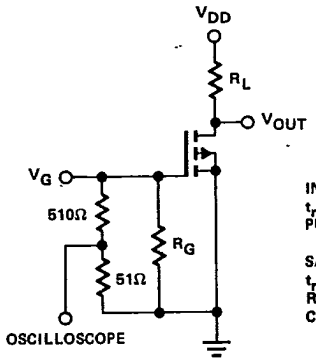
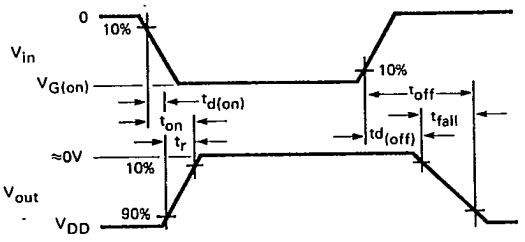
SWITCHING TIME TEST CIRCUIT



INPUT PULSE
t_r < 0.5 nSEC
PULSE WIDTH – 100 nSEC

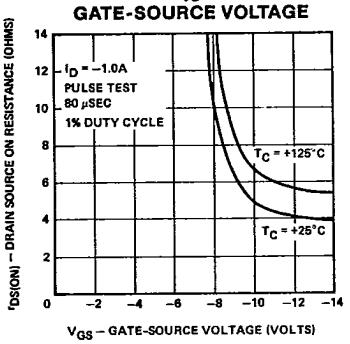
SAMPLING OSCILLOSCOPE
t_r < 0.36 nSEC
R_{in} > 1 MΩ
C_{in} < 2.0 pF

TEST WAVEFORMS

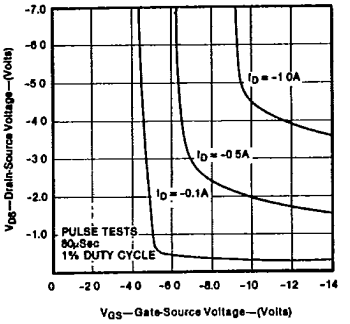


TYPICAL PERFORMANCE CHARACTERISTICS (T_C = +25°C unless otherwise specified)

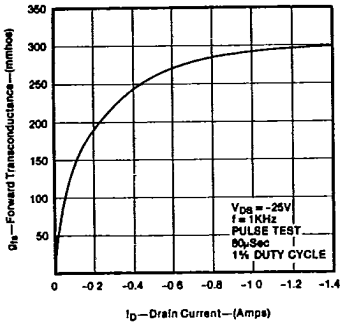
DRAIN-SOURCE ON RESISTANCE —vs— GATE-SOURCE VOLTAGE



ON VOLTAGE CHARACTERISTICS



FORWARD TRANSCONDUCTANCE —vs— ON DRAIN CURRENT



CAPACITANCES —vs— DRAIN-SOURCE VOLTAGE